Fraunhofer´s Initial and Ongoing Contributions in 3D IC Integration

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***Abstract*— Pioneering contributions of Fraunhofer in the field of 3D IC integration are presented, as well as recent 3D design and technology developments with a dedicated focus on the application of heterogeneous systems.**

***Keywords*— 3D IC, TSV, 3D Systems Design, Wafer Bonding, Vertical Interconnections, Heterogeneous Integration**

I. INTRODUCTION

Fraunhofer has been working on 3D integration since the late 1980´s, starting with a consortium of Siemens, AEG, Philips and the Fraunhofer IFT (now EMFT). Already in 1988 they successfully fabricated 3D CMOS devices based on recrystallization of Poly-Si. In a cooperative project between Siemens and Fraunhofer Munich we were the first to demonstrate a complete industrial 3DIC stacking process (1993-1996) based on wafer bonding and vertical integration of IC devices using inter-chip vias (later called TSV) [1, 2]. Very early, we pointed out thermal issues and presented thermal analysis of vertically integrated circuits [3], proposed memory on logic as key application for 3D technology and investigated the performance improvement of the memory hierarchy of RISC systems [4].

End of the 1990´s Prof. Mitsumasa Koyanagi´s team at the Tohoku University, for the first time in the world succeeded in fabricating 3D ICs using TSV, explicitly 3D stacked image sensor and 3D stacked memory test chips [5, 6] representing *the* pioneering contributions of today´s two main applications. From this time on, we were advantageously exchanging technology and its application knowhow between our research groups in Sendai and Munich.

Already end of the 1990´s we focused on 3D technologies for the use of known good dies by chip-to-wafer stacking (against at the time´s main stream of wafer-to-wafer-stacking) in a large German project with Infineon. Understanding the necessity for combining research on both, 3D technology and simulation & design at an early stage, we established a fruitful cooperation between the two Fraunhofer institutes in Munich and IIS in Dresden [7]. Realization of 3D chips needs specific design methodology. Essential driving forces for 3D are performance (speed), power consumption, costs, and form factor. In order to use the potential of 3D technologies for the economical realization of highly complex and intelligent systems it is necessary to develop not only the manufacturing technology but also the design technology, normally tailored on requirements concerning high system performance and reliability.

There are some physical effects with a growing influence on the circuit behavior. That means some physical effects will play an increasing rule relating to the device function, such as signal integrity, cross talk, interconnect delays and irradiation, power & thermal behavioral, heat dissipation depending on transistor density, clock frequency and other more.

The influence of technology features to circuit behavior has to be minimized within the design process. This requires new design rules, models, methodologies, and tools for CAD of electronic systems implemented using 3D technologies. New methods will ensure the design ability, higher design efficiency and better design quality and lead to a higher system performance, robustness and reliability. Challenges are fail safe design, extreme low power, uniform distribution of power loss on the chip area and volume respectively (heat sources), testability, robustness regarding parasitics, operating conditions, and faults.

In the Design Automation division of the Fraunhofer Institute IIS have been worked on some named problems in several R&D projects together with partners from other institutes and development departments of companies, first and mainly with Fraunhofer Institute EMFT. The analysis and modeling of the influences of technology parameters (material, geometries, processes) and operating conditions on the device behavior (for an given technology) and on the circuit behavior carried out at the Fraunhofer Institute IIS leads to parameter dependent relationships, that are parameter dependent models. With these models and suitable optimization tools are essential design improvements possible, such as extensions of the acceptable parameter range, tolerance optimization, and minimization of parasitic influences on behavior. More results of R&D are methods for extreme low power design, thermal managements in 3D stacks, design for testability and test strategies, and floorplanning in consideration of and controlled by thermal and mechanical behavior [8, 12].

For special 3D chips such as memories, processors, FPGAs, and others specific tailored methodologies for manufacturing and design are developed. In addition to the named methods new system architectures and new circuitry which are ‘inherent’ robust regarding parasitic effects and parameter variation on electrical behavior are subject of R&D. Such fault tolerant circuits and architectures will be probably a base for

manufacturing of application specific 3D chips using existing standard technologies.

Starting 1999, we investigated 3D TSV technologies with particular focus on die-to-substrate stacking and initiated the European Integrating Projects e-CUBES®, as a first European 3D technology platform [9], and e-BRAINS with a.o., Infineon, Siemens, EPFL, IMEC and Tyndall, where we evaluated the application of 3D heterogeneous integration [10], including demonstration of high-performance communications [11]. In these projects, we worked also on approaches for systematic hierarchical modelling in order to carry out simulations in different physical domains, based on a unified description of the 3D system [12].

II. 3D IC TECHNOLOGY

Fraunhofer Munich pioneered 3D stacking in Europe by fabricating devices with TSVs and wafer bonding. In Fig. 1 (left) a cross section corresponding to an early TSV fabrication is shown. The process flow for TSV fabrication included high aspect ratio plasma etching processes of both dielectric layers and single crystal silicon (c-Si). The sequence started with CVD of SiO_2 onto the intermetal dielectrics (IMD) of a 3-layer metallization scheme serving later in the process flow as mask for the plasma etching process into the silicon substrate wafer.Next, a thick resist layer (3µm) was spun on this CVD-SiO_2 mask layer, lithographically pattered, and used as organic mask for plasma etching through all dielectric layers. When exposing the Si substrate the etch chemistry used provided highly selective etch stop on c-Si. After ashing of the remaining resist mask a highly conformal O_3-TEOS-CVD process followed by a spacer etching process left O_3-TEOS-SiO_2 only on the sidewalls of the hole in the dielectric layer stack. This sidewall liner was mandatory to protect the BPSG layer in the dielectric layer stack from lateral etch attack during wet chemical TSV cleaning later in the process flow after c-Si etching. In wet chemical SiO_2 etchants BPSG displays higher etch rates than all non-doped silicon oxides in the dielectric layer stack which would have resulted in voids in the TSV metallization sequence and in turn to reliability issues.

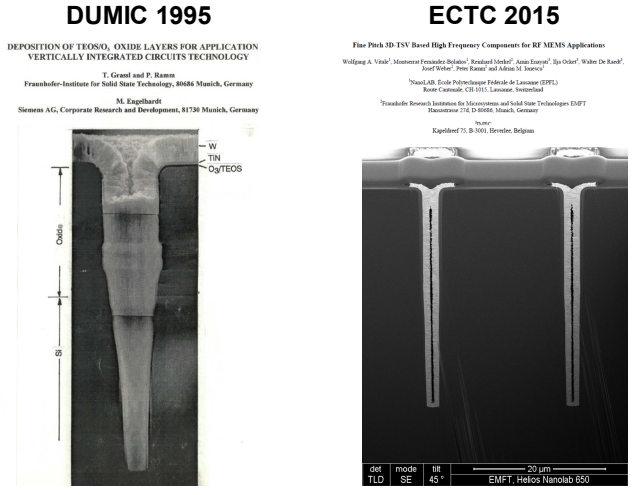

Figure 1: TSV fabrication at Fraunhofer Munich over two decades [1], [11]

Deep silicon trench etching into the substrate starting at the bottom of the hole in the dielectric stack and wet chemical trench cleaning (BOE) followed.

For lateral electrical isolation of the TSV a second O_3-TEOS-CVD spacer was fabricated leaving again c-Si exposed on the TSV bottom. A slight positive taper (~89°) of the TSV was mandatory for void-free subsequent TSV metallization.

The TSVs were metallized by MOCVD of TiN as thin barrier layer prior to the W-CVD process for compete TSV filling (followed by a metal etch-back process, not shown in Fig. 1). Electrical measurements demonstrated electrical resistances of such TSV close to the theoretically expected values.

The whole TSV fabrication sequence took full advantage of integrated processing by use of two multi-chamber cluster tools. One mainframe was equipped with the process modules for the dielectric deposition and etch sequence, including modules for resist ashing and for deep silicon trench etching. The second mainframe had all the process modules for the metal deposition and etch sequence.

Due to integrated processing, exposure to ambient occurred only for lithography, the wet chemical TSV clean and for the transfer of the wafers between the two multi-chamber cluster tools.

A major contribution, on the way to 3D IC fabrication, was the use of inter-metallic compound (IMC) bonding for both mechanical and electrical interconnections [7]. Such robust 3D IC process technology, based on IMC interconnects with a higher melting temperature than the bonding temperature, can be advantageously used e.g. in 3D stacked DRAM production.

Based on Solid-Liquid-Interdiffusion (SLID) bonding, a modular 3D-TSV technology was developed, targeting on multiple 3D device stacks with high-performance and small form factor requirements. Corresponding to this said TSV-SLID technology the TSVs are fabricated on partly or completely processed bare device wafers. TSVs are etched through dielectric layers and further into the silicon substrate of the devices, subsequently isolated and metallized (e.g. by deposition of copper or tungsten). After complete pre-processing of the TSVs the device, wafers are then temporarily bonded to a handling substrate. Subsequently the temporarily bonded wafers are thinned until the metal-filled TSVs are exposed from the rear side. The thinned devices are then connected to a second device wafer by SLID. At typical wafer bonding temperatures of 240 - 270°C the deposited tin is completely transformed into Cu_3Sn intermetallic compound. This ε-phase is thermodynamically stable with a melting point above 600°C. A key advantage of the TSV-SLID technology is that both the mechanical and the electrical interconnects are formed simultaneously – and the 3D integration process is completed with the SLID bonding.

After removal of the handling substrate, the TSVs are interconnected to the device metallization. With the TSV-SLID technology, the 3D integration can be executed subsequently for a next device layer to be stacked. This key ability of modularity is a consequence of the fact that the melting

temperature of the intermetallic compound is considerably higher than the wafer bonding temperature.

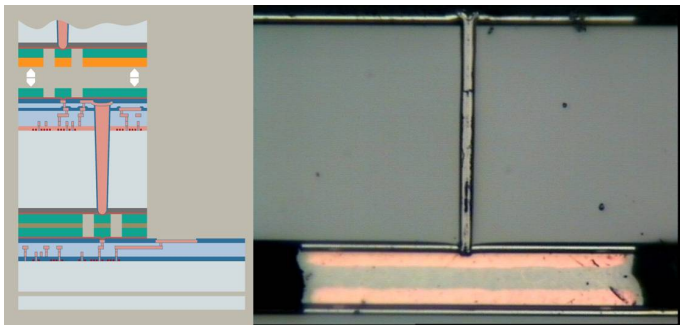

Figure 2: Application of wafer bonding for 3D IC integration: TSV-SLID technology based on metal bonding by Solid-Liquid-Interdiffusion (SLID) [9]

In Fig. 2, a comparison between concept and realization is shown. The SLID interconnect shows the characteristic appearance of pure copper as interconnect to the top and bottom device, mechanically and electrically joined by the grey intermetallic compound. Compared to the lateral and vertical dimensions of the SLID-contact pad, the TSV is very slim and offers a high aspect ratio. The dimensional relations as shown in Fig. 2 are owed the technological boundaries as minimum wafer thickness of freestanding handling (typically 50 µm) and an alignment accuracy of 50 µm.

III. Heterogeneous System Integration

A simplified 3D IC production roadmap is shown in Fig. 3. 3D integration technologies have become well-accepted approaches for fabrication of high-performance memory-enhanced products, explicitly stacked DRAMs, which are currently in high-volume production at Samsung, Hynix and Micron. Samsung started the production of 3D stacked DDR4 with via-middle technology in August 2015. So finally, after more than three decades of R&D, 3D IC integration has arrived in the electronic industry. The other application that has gone into high volume production is CMOS image sensors (CIS). Since 2017, Sony is producing stacked CIS for smart phone cameras: a 90 nm generation back-illuminated CIS top chip, 30 nm generation DRAM middle chip, and 40 nm generation image signal processor bottom chip. On the other hand, there have also been drawbacks. Most significantly, 3D memory-on-logic applications, widely predicted by many sources, have been postponed several times. The major issue is the high cost of 3D IC manufacturing. In fact, until 2019 CMOS image sensors and stacked DRAM were the only 3D ICs in high volume production. In addition, there is a new application track in development, based on 3D heterogeneous integration. One of the future main drivers is certainly sensor integration. The heterogeneous systems consisting of sensors with ICs, passive components and even energy harvesting systems are becoming more and more important especially for the high growth market area of distributed wireless sensor systems – which will constitute a key connected hardware infrastructure of the Internet-of-Things and Artificial Intelligence [13]. In consequence, our ongoing work has a dedicated focus on 3D-TSV technologies for heterogeneous sensor/IC systems in key application areas, as mobile communication, medical and health care devices [14].

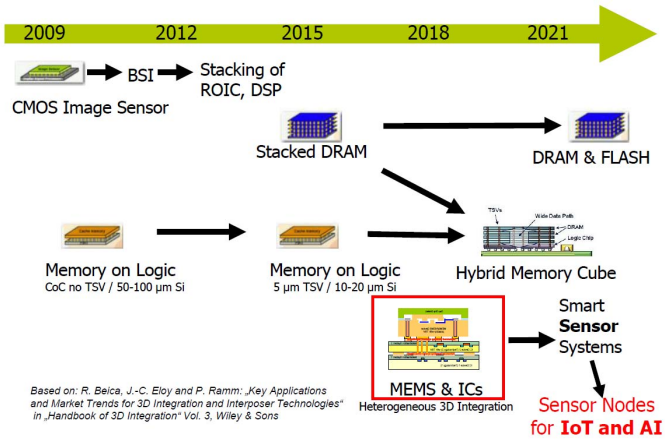

Figure 3: Roadmap for 3D IC application development

We evaluated the application of 3D heterogeneous system integration. An IC/MEMS heterogeneous system typically consist of a sensor, a transceiver unit and a logic unit. A demonstrator system for a compact tire-pressure-monitor system was build up by connecting a microprocessor unit and a transceiver ASIC by SLID-technology. At the transceiver-chip W-filled TSVs have been applied for routing the logic signals to the sensor-unit. The pressure sensor together with a bulk-acoustic (BAW) resonator were mounted by Au-stud bumps on top of the IC-Stack.

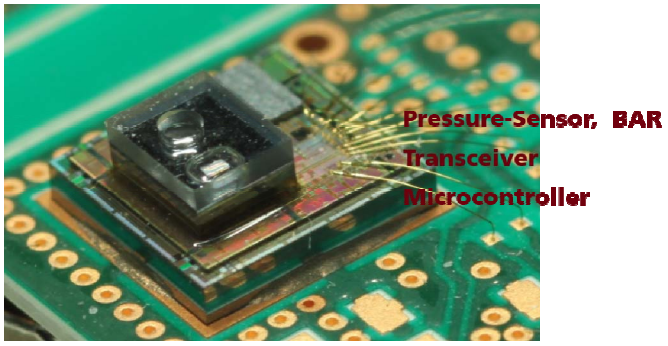

Figure 4: 3D heterogeneous system for tire pressure monitoring (Infineon, Fraunhofer, SINTEF)

For usage within the amazing field of particle physics a detector/IC system integration with direct SLID connections between the pixels of the sensor and the appropriate read-out logic was demonstrated.

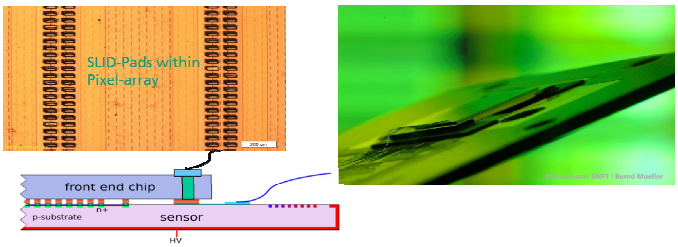

Figure 5: Heterogeneous integration of detector and readout circuit (Fraunhofer EMFT in co-operation with Max-Planck)

Recently our advanced TSV technology was also evaluated for mobile communication application. The development of interconnections suitable for radio-frequency (RF) and millimeter-wave (mm-wave) applications is of foremost importance for the feasibility of high-quality substrate-integrated devices. For this purpose, we introduce and validate the technology to implement fine-pitch high-aspect ratio tungsten-filled through-silicon vias (W-TSVs) adapted for high-frequency applications. We designed and characterized RF test structures to assess the quality of the W-TSVs and their suitability for radio-frequency integrated circuits (RFIC) applications, showing low insertion loss for TSV in coplanar waveguides (CPW) and high-performance wideband mm-wave antennas. Fig. 1 (right) shows a SEM cross-section view of W-filled TSVs prior to deposition of the top metal layer. Before the deposition of a SiO_2 layer providing electrical isolation between the TSVs and the substrate, we deposit a layer of amorphous silicon (a-Si) on top of the substrate and within the TSVs for improving the RF properties.

High aspect ratio W-filled TSV's have been applied for building up ultra-compact antenna structures for frequency ranges up to 60 GHz (see Fig. 6) [11].

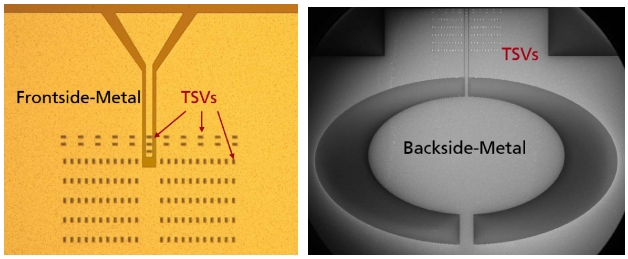

Figure 6: Micrograph (left side) and SEM-picture (right side) of 3D-TSV integrated antenna structure for 60 GHz.

3D heterogeneous integration enables a wide variety of system concepts. Therefore, early estimations of performance, cost and reliability are crucial. Hierarchical models which cover e.g. thermal effects, crosstalk and IR drop as well as thermal induced stress are essential. They provide valuable support of the functional design in different design phases [15]. Such a modular modeling is one important first step towards to modular and verified building blocks for efficient design of 3D systems.

Similar to the 2D case, a 3D design flow can be divided into a construction phase and a corresponding verification phase as depicted in Figure 7. On the left side the construction or design phase is shown, whereas the verification phase is shown on the right side. System-level design exploration should take place at a very early design stage. Most of the required interaction should be done within the 3D design space. On the other hand, to get a detailed evaluation of a chosen design option, the 2D tools can be involved as well. But this kind of interaction should be limited to a minimum as it is often time consuming. For verification, we separate into 2D and 3D as well.

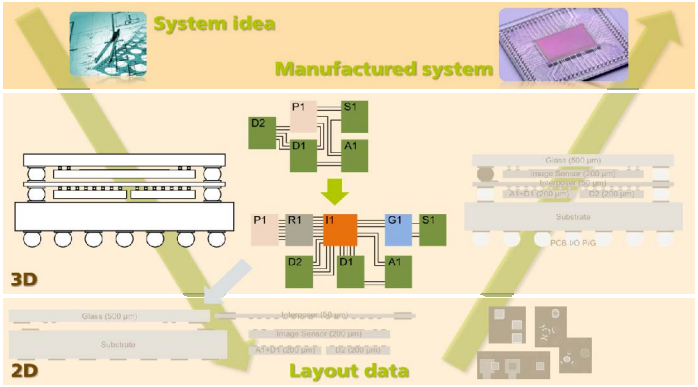

Figure 7. 3D design flow enabled by assembly design kit

To enable design and verification across integration levels the introduction of Assembly Design Kits (ADK) is mandatory. This covers technology and assembly information within an common database. With that a comprehensive design process is provided with the capability of optimizing across integration levels. This covers designing, simulation and verification with the usage of different technologies and the interaction across technologies.

However, advanced package technologies often introduce additional materials or material mixes into the system. This typically implies differences with regard to the material properties (e.g., coefficient of thermal expansion (CTE) or thermal resistivity). Differences between the materials' properties can cause mechanical and electrical issues. A prominent example is a crack induced by different CTEs between different materials of different components.

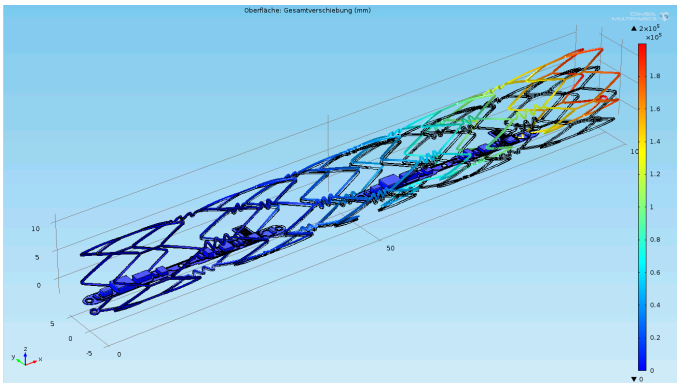

Figure 8. Thermal and mechanical analysis required

Furthermore, during system development, the designers face new (co-design) challenges, of finding an optimal packaging setup and technology combination considering performance, cost, supply chain, and reliability. In addition to these economical and technical aspects, physical effects have to be considered during the design of modern electronic systems involving electrical, mechanical, and thermal domain and the interaction between those domains. Analysis of relations like depicted in Figure 8 is essential for design success.

IV. SUMMARY

Three-dimensional integrated circuit (3D IC) integration is the most promising alternative to overcome the scaling limits of Moore's law allowing to reduce the interconnect lengths and power consumption while increasing the speed and the integration time.

In a large cooperative project with Siemens and Fraunhofer, they were the first to demonstrate a complete industrial 3D IC stacking process based on wafer bonding and vertical integration of IC devices using TSV. Almost two decades ago, Fraunhofer developed a robust 3D-TSV technology based on intermetallic compound (IMC) bonding by solid-liquid interdiffusion (SLID). The use of such IMC interconnections with a higher melting temperature than the applied bonding temperature, turned out a as a major contribution on the way to 3D stacked memory production. As late as 2015, after decades of R&D efforts, the first 3D IC high volume products were finally stacked DRAMs. As a drawback, 3D memory-on-logic applications, widely predicted, have been postponed several times. On the other hand, there is an additional 3D application track in development: advanced sensor/IC systems fabricated by 3D heterogeneous integration – for key application fields as mobile communication, automotive, medical and health care devices.

Our focus is on evaluating and optimizing the corresponding 3D technologies mainly regarding the product reliability and robustness of the processes, which are the key requirements for many applications. Our established cooperation between the Fraunhofer institutes EMFT in Munich and IIS in Dresden is focusing on 3D heterogeneous integration – in fact regarding both, technology *and* design. Targeted results are design methods for extreme low power design, thermal managements in 3D stacks, design for testability and test strategies, and floorplanning in consideration of and controlled by thermal and mechanical behavior.

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