SILICON-BASED MONOLITHIC TRIPLE-JUNCTION SOLAR CELLS WITH CONVERSION EFFICIENCY >34%

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ABSTRACT: Triple-junction solar cells with top cells made from III-V compound semiconductors on a silicon bottom cell show conversion efficiencies beyond the theoretical limit of single-junction devices, so this is one of the promising technologies for terrestrial photovoltaics. In this work, a III-V//Si tandem device with 34.5% efficiency is presented and further developments are discussed. A detailed investigation of the silicon bottom cell revealed, that with optimum wafer resistivity (~1 Ω cm) and low-temperature passivation of the cell perimeter, the perimeter losses can be reduced to ~0.2%$_{abs}$. This corresponds to an efficiency gain of up to 0.8%$_{abs}$ for the current devices.
Keywords: III-V Semiconductors, Silicon, Tandem, Multijunction Solar Cell, High-Efficiency

1 INTRODUCTION

To overcome the fundamental Shockley-Queisser limit of 33% conversion efficiency for single-junction solar cells [1], multi-junction devices have been developed in the last decades. III-V compound semiconductors have been used successfully for space applications with highest conversion efficiency and proven long-term stability, but at very high costs compared to terrestrial applications. The first step to reduce costs is to stack III-V top cells on a silicon bottom cell, which, at the same time, serves as a low-cost substrate. This concept was investigated at least since the 1980s, predicting a conversion efficiency >30% for AlGaAs/Si dual junctions [2] and respectable efficiencies above 20% were already demonstrated in the 1990s [3]. In this work, the stacking of III-V cells and silicon is implemented by direct wafer bonding, to obtain a very good mechanical, optical and electrical connection between high-quality sub cells [4]. This technology enables conversion efficiencies beyond the Shockley-Queisser limit [4], so it is well suited to optimize all the components of III-V//Si tandem devices and investigate fundamental and technological limitations.

This work presents the current developments in the field of III-V//Si triple-junction solar cells and discusses further potential, i.e. the avoidance of perimeter losses in the silicon bottom cell.

2 EXPERIMENTAL

A cross section of the final cell structure is shown in Fig. 1.

2.1 III-V Epitaxy of top cells

The top cells were grown by MOVPE in an AIX2800G4-TM reactor. Arsine and phosphine precursors were used for group V species and trimethyl-gallium, trimethylindium, and trimethylaluminium for the group III species. Further details on the MOVPE processes can be found in [4]. The GaInP/GaInAsP tandem cell structure was grown in an upright fashion on a GaAs wafer. To transfer the layer stack onto the silicon bottom cell, it was temporarily bonded to a sapphire wafer using HT-10.10 from Brewer Science and the GaAs substrate was chemically etched. To prepare the surface for direct wafer bonding to the silicon bottom cell, it was chemically-mechanically polished (CMP) to remove particles and smoothen the surface (RMS < 1 nm).

2.2 Silicon bottom cells

280 µm thick float-zone silicon wafers (p-type, 4 Ohm cm, double side polished) were used for the fabrication of the silicon bottom cells. Tunnel-oxide passivating contacts (TOPCon) [5] were formed on the front (n-type) and back side (p-type). A thin oxide was grown in HNO_3. 100 nm intrinsic amorphous silicon was deposited by LPCVD (both sides), doped by ion implantation of phosphorus (front side) and boron monofluoride (back side), and annealed to polysilicon at 850°C. Finally, the samples were exposed to a remote hydrogen plasma at 425°C. The front side was polished (CMP) to remove particles and remove approximately half of the poly-Si layer.

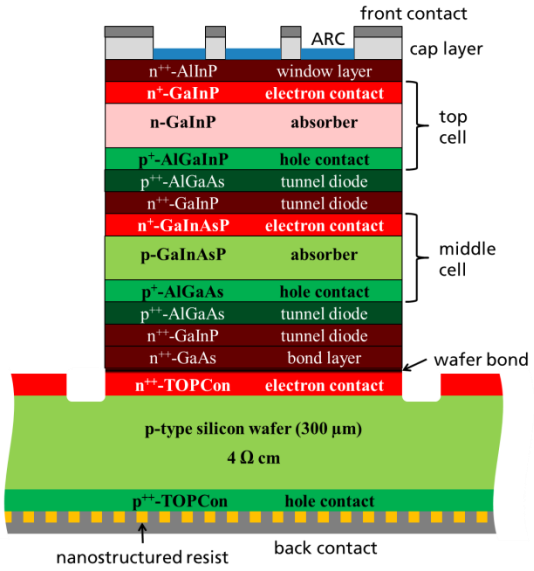

Figure 1: Cross section of the triple-junction solar cell (schematic).

2.2 Tandem cell fabrication

Direct wafer bonding of the top tandem cells and the silicon bottom cell was performed with a force of 2.4 kN at room temperature in an Ayumi SAB-100 bonder under high vacuum with preceding surface activation by Ar

ions (0.3 to 0.4 keV). Afterwards, the temporary bond of the top cells to the sapphire wafer was released by thermal slide (190°C) and protection layers were chemically etched.

The front metal contacts and anti-reflection coatings were deposited by evaporation and structured by photolithography. The active cell area was defined by wet-chemical mesa etching through the top cells and some micrometers into the silicon bottom cell.

Before evaporation of the metal contact on the back side (1 µm Ag), a photoresist was deposited and structured by nanoimprint lithography to obtain a diffraction grating [6].

3 RESULTS AND DISCUSSION

Highlights of the current triple-junction solar cells shown in Fig. 1 are:

- GaInP top cell with rear-hetero design [7]
- GaInAsP middle cell with band gap of 1.48 eV
- Silicon bottom cell with full-area passivating contacts on the front and back side
- Metal grating on the back side for path length enhancement of infrared light

The features of the silicon bottom cell were already introduced in 2018 leading to a conversion efficiency of 33.3% [4]. With the improved top cell and an AlGaAs middle cell (1.51 eV), the efficiency was raised even further to 34.1% (X610-06) [8]. The latest development step is a middle cell made of a quaternary material (GaInAsP) with superior quality compared to AlGaAs [9]. Implemented in the triple cell stack (X635-11), the GaInAsP middle cell leads to a new record efficiency of 34.5% (see Table I). The gain in open-circuit voltage (V_{OC}) was more than 50 mV. Furthermore, the quantum efficiency of the middle cell was boosted (see Fig. 2) causing approximately +1 mA/cm^2 in the total current density (calculated from EQE sum for AM1.5g spectrum). Unfortunately, the electrical contact on the back side showed a high series resistance. This technological issue caused a fill factor (FF) loss of about 2%$_{abs}$.

Table I: Parameters of the best triple-junction solar cells with an area of 4 cm^2 under AM1.5g standard testing conditions (calibrated measurements from Fraunhofer ISE CalLab).

cell	V_{OC} [V]	J_{SC} [mA/cm^2]	*FF* [%]	η [%]
X610-06	3.177	12.4	86.4	34.1
X635-11	3.230	12.8	83.2	34.5

There is still progress in several components and fabrication steps of the triple-junction solar cell, indicating further potential for the next cell generations. For example, a GaInAsP middle cell with rear hetero junction is currently investigated. The design of the silicon bottom cell is already very close to optimum, except for the cell perimeter which is unpassivated due to trench etching of the III-V cells and emitter separation. A strong charge carrier recombination with negative influence on the bottom cell performance is expected that requires detailed investigation.

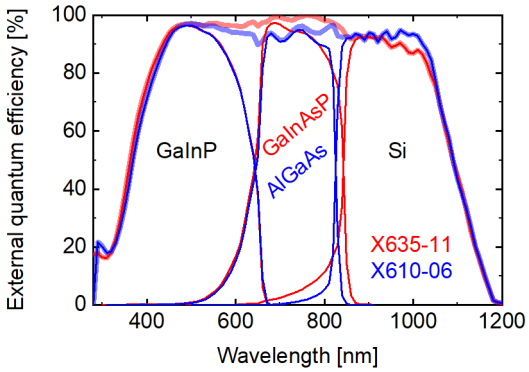

Figure 2: External quantum efficiency of the sub cells and the triple-cell sum (calibrated measurements from Fraunhofer ISE CalLab).

3.1 Perimeter loss in the silicon bottom cell

An elaborate simulation model for the silicon bottom cell was established with the device simulator Quokka3 [10]. The whole 4 cm^2 cell and perimeter was modeled in 3 dimensions, including detailed optics of the whole triple-junction cell (see Fig. 3). The spectral absorption of all III-V layers (stack of X610-06) were modeled by a combination of transfer-matrix calculations and OPTOS [11]. The effect of the metal grating on the back side was considered in Quokka3 by the Text-Z model with an appropriate parametrization. All input parameters were independently determined without any fitting to the investigated solar cells.

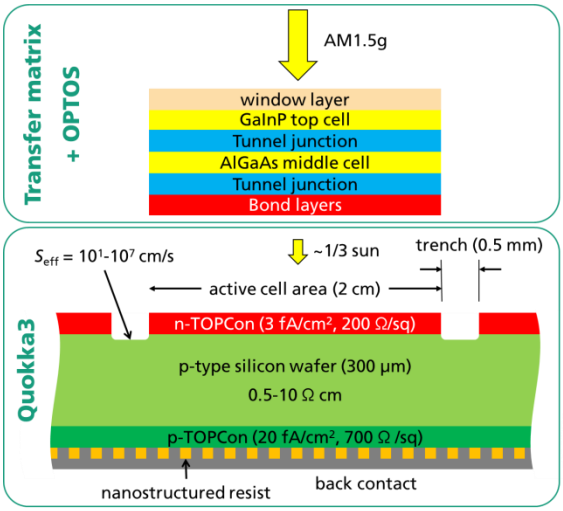

Figure 3: Cross section of the simulation model to investigate perimeter loss in the silicon bottom cell. The simulation was performed in 3D with Quokka on the full cell area including a detailed optical model with absorption of all III-V layers and the effect of the metal grating on the back side. The surface recombination velocity (S_{eff}) in the trenches and the bulk resistivity of the silicon absorber was varied.

In order to investigate the influence of a trench passivation, the effective surface recombination velocity (S_{eff}) in the trenches was varied from 10^1 (good passivation) to 10^7 cm/s (no passivation). Additionally, the resistivity of the silicon wafer was varied from 0.5 to 10 Ohm cm, because it is expected to have an influence on the perimeter losses [12–14].

Figure 4 shows the simulation results, i.e. the solar cell parameters of the silicon bottom cell in the triple-junction configuration. The maximum power (P_{MPP}) in mW/cm^2 is equivalent to the conversion efficiency in % of the silicon bottom cell. The simulations show that the efficiency continuously drops with increasing S_{eff} in the trenches due to increasing charge carrier recombination in the cell perimeter. This effect is rather weak for a silicon substrate with a bulk resistivity of 0.5 Ω cm, but becomes stronger with higher bulk resistivity (i.e. lower doping). The fundamental reason for this behavior is a higher minority carrier density at the same voltage for a material with higher resistivity, leading to a higher current loss in a region with fixed surface recombination velocity [14]. In contrast, the material with higher resistivity (4 to 10 Ω cm) shows a higher efficiency (7.5%) in the simulation of a unit cell without perimeter losses (see set of points to the very left in Fig. 4) due to lower Auger recombination.

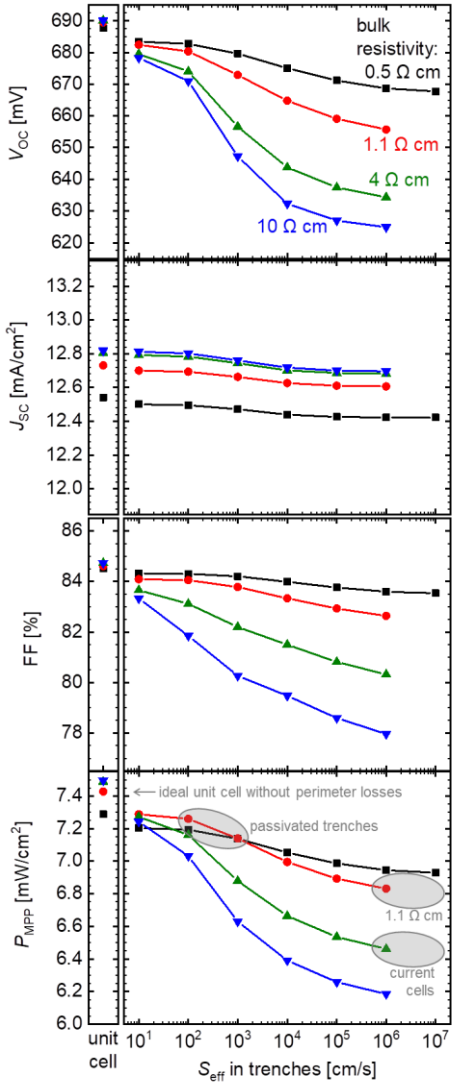

Figure 4: Results of the silicon bottom cell simulation, i.e. open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor (FF), and maximum power (P_{MPP}) which equals the conversion efficiency in percent. The isolated set of points to the very left corresponds to a unit cell simulation without perimeter loss.

The latest silicon bottom cells were all made on 4 Ω cm material – a good choice for cells with only minor lifetime limitations (i.e. low perimeter losses). But in the triple-junction device with unpassivated trenches, an effective surface recombination velocity (S_{eff}) of 10^6 to 10^7 cm/s has to be assumed. According to the simulation results, the efficiency of the current silicon bottom cells is about 6.5%. The perimeter losses are currently ~50 mV in V_{OC}, ~0.1 mA/cm^2 in J_{SC}, and ~4%$_{abs}$ in FF, which add up to ~1%$_{abs}$ loss in efficiency.
An efficiency gain of ~0.4%$_{abs}$ should be obtained by changing the bulk resistivity from 4 to ~1 Ω cm (c.f. grey spheres in Fig. 4). Adding a good trench passivation with S_{eff} = 10^2 cm/s would additionally boost the efficiency by ~0.4%$_{abs}$. For a current-matched multi-junction device, the power of the sub cells can be added up, so the optimized wafer doping and trench passivation imply an efficiency gain of ~0.8%$_{abs}$ for the triple-junction device.

3.2 Trench passivation

The passivation of the trenches was investigated experimentally. A silicon bottom cell precursor with full-area passivating contacts on both sides with etched trenches on the front side (n-TOPCon) was inspected with photoluminescence imaging (see Fig. 5 left). The luminescence signal is quite high in the center of the cells, but drops strongly towards the trenches between the cells due to the perimeter loss. In the trenches, the signal is very low due to charge carrier recombination at the unpassivated surface. After stripping the trench mask, Al_2O_3 was deposited on the whole front side with thermal atomic layer deposition at 95°C and activated at 250°C for 25 min. With this low-temperature trench passivation, the luminescence signal in the trenches was substantially increased (see Fig. 5 right). Consequently, the signal in the cells was higher and more homogeneous over the cell area.

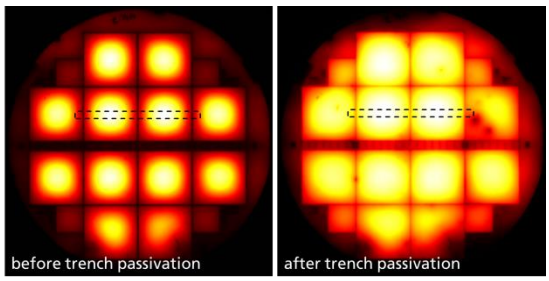

Figure 5: Photoluminescence images at 0.05 sun illumination of the same silicon bottom cell before trench passivation (left) and after passivation of trenches with Al_2O_3 annealed at 250°C for 25 min (right).

In order to estimate the surface recombination velocity in the trenches ($S_{eff,trench}$) after passivation, the photoluminescence signal was simulated with the 3D Quokka model of the silicon bottom cell. Figure 6 shows the luminescence across two cells with a trench in between before and after passivation. The comparison of measured and simulated data indicates a good match with $S_{eff,trench}$ > 10^5 cm/s before and $S_{eff,trench}$ < 10^3 cm/s after trench passivation. At an illumination intensity of 1 sun, the passivation performs even better with $S_{eff,trench}$ close to 10^2 cm/s (not shown here). Please note that Al_2O_3 could provide a much better passivation if the surface would be prepared by an HF-Dip and the Al_2O_3 would be activated at > 400°C, but these conditions are not compatible with

the triple-junction cell fabrication. According to the simulations, $S_{eff,trench}$ = 10^2 cm/s is sufficient to achieve almost optimum performance on 1.1 Ω cm silicon wafers (c.f. Fig. 4).

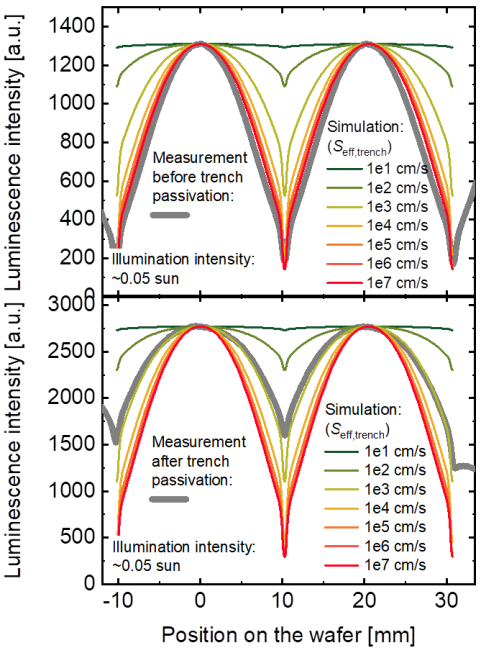

Figure 6: Measured photoluminescence intensity across a wafer (two cells including the trench, c.f. dashed lines in Fig. 5) before trench passivation (top) and after trench passivation (bottom) together with a simulation set (variation of the surface recombination velocity in the trenches $S_{eff,trench}$). Note that the simulated data is normalized to the maximum of the measured intensity.

5 SUMMARY

Triple-junction solar cells with top cells made from III-V compound semiconductors on a silicon bottom cell show conversion efficiencies beyond the Shockley-Queisser limit. There is still potential to raise the current record efficiency of 34.5% to 36% or even higher, due to improvements of the individual sub cells.

In this work, the perimeter losses in the silicon bottom cell were quantified to 1%$_{abs}$ in efficiency by simulations and experimental investigations. It was found, that with an adapted bulk resistivity (~1 Ω cm) and low-temperature passivation of the cell perimeter with Al_2O_3, the perimeter losses can be reduced to ~0.2%$_{abs}$. This corresponds to an efficiency gain of up to 0.8%$_{abs}$ for the current devices.

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