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MOVPE GROWTH OF III-V SOLAR CELLS ON SILICON IN 300MM CLOSED COUPLED SHOWERHEAD REACTOR

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ABSTRACT: III-V multi-junction solar cells grown on Ge substrates have achieved the highest solar cell conversion efficiency of 41.6 %. However, this device manufacturing is still costly and a major share of the cost can be attributed to the cost of the Ge substrate. Therefore, a replacement of Ge by Si would be beneficial. However, elaborate challenges arise from the 4.1% difference in lattice constant for Si and GaAs and due to the non-polar to polar interface leading to threading dislocations and anti-phase domains, respectively. To meet the required high crystalline quality for III-V multi-junction solar cells this paper presents approaches for the Si-to-GaAs transition evaluated on an industrial 300 mm CRIUS Closed Coupled Showerhead MOVPE reactor. Anti-phase domain free GaP nucleation layers with only 0.36% lattice mismatch at room temperature were grown on Si substrate. On top of these layers step-graded $Ga_{1-x}In_xP$ buffer structures mediate the lattice constant to GaAs although present process parameters have not yet enabled confinement of threading dislocations inside the buffer structure. A promising alternative route is the growth of an all Ge buffer layer directly on Si. Here we report on the results of the used two-step growth process.
Keywords: III-V on Si, Epitaxy, Gallium Arsenide Based Cells.

1 INTRODUCTION

1.1 Motivation

III-V multi-junction solar cells are the state-of-the-art approach for achieving high efficiencies in photovoltaic energy conversion for terrestrial concentrator and space applications. The devices combine multiple pn-junctions of different band gap energies to absorb the spectrum of the sun more efficiently. Highest conversion efficiencies of up to 41.6 % have been achieved by GaInP/GaInAs/Ge lattice-matched triple-junction solar cells grown on Ge substrate [1]. To develop the multi-junction concept further, an interesting option is to substitute Ge by Si. Using Si can increase the cell efficiency [2] and further advantages are the lower mass density and cost, higher crystal hardness and thermal conductivity, the existence of larger wafer diameter and the abundant availability. Therefore, the concept of combining III-V materials, such as GaAs, and Si has been investigated by researches for more than two decades, see for example [3,4,5].

Research on III-V solar cells on Si is strongly driven by their application as affordable commercial devices for renewable power generation and therefore the implementation in industrial high volume production is imperative. Acknowledging this intention, the investigations in this paper were entirely carried out by growth on an industrial feasible AIXTRON 300 mm CRIUS Closed Coupled Showerhead (CCS) MOVPE reactor with showerhead technology (figure 2).

1.2 Concepts for integration of III-V solar cells on Si

The integration of III-V materials on Si involves inherent challenges related to their rather different material properties. Amongst others, the growth of the polar on non-polar semiconductor may cause unintended formation of anti-phase domains (APDs) as well as anti-phase boundaries (APBs). Furthermore, one has to overcome the difference in lattice constant which depends on the used III-V material. This difference is the major cause for the generation of threading dislocations which can propagate into the active region of the solar cell device and degrade the solar cell performance.

In order to circumnavigate the task of changing lattice constant one can perform lattice matched III-V growth on Si in the diluted nitride (GaIn)(NAsP) material system. Although the growth can be lattice matched to Si and band gaps can be chosen in a range between 1-2 eV the drawback of this route is a short minority carrier diffusion length which significantly reduces the solar cell efficiency [6,7,8,9,10,11].

In contrast to this lattice matched approach the focus of this paper is the growth of III-V multi-junction solar cell structures along the lattice constant of GaAs and thus lattice mismatched to Si. Yet, the challenging 4.1 % difference in lattice constant between Si and GaAs has to be mastered by metamorphic buffer growth (figure 1).

The straightforward approach of direct GaAs growth on Si has been studied intensively in the past, e.g. in [3,4,5]. However, threading dislocation densities (TDDs) around 10^7 cm^{-2} in GaAs were observed [12,13] although TDDs well below 10^6 cm^{-2} are required for high-efficiency III-V solar cells [3,14]. Moreover, it is advisable to entirely avoid As during the initial growth phase of III-Vs on Si. As forms surface defects such as trenches, ridges or steps acting as defect nuclei. Simultaneously it reduces surface energy [15] and inhibits the rearrangement of Si surface atoms which is essential for the formation of one-domain Si surfaces which are considered to be a prerequisite for APD free III-V growth on Si [5]. Instead of direct transition from Si to GaAs and averting As-related defect nucleation at the same time we consider the nucleation of GaP on Si with a difference in lattice constant of only 0.36 % at room temperature as more favorable. The major challenge here is an APD-free GaP nucleation layer. This requires the preparation of a single-domain Si surface before the MOVPE growth process starts.

If an adequate GaP nucleation layer has been achieved a gradual increase of lattice constant to GaAs is

attainable by metamorphic $Ga_{1-x}In_xP$ or $GaAs_xP_{1-x}$ buffer structures (figure 1) [16].

Alternatively to III-V graded buffers it is an option to establish a Ge surface on Si which can be followed by (basically) lattice matched growth of GaAs solar cells on Ge. The Ge surface can be accomplished by grading layers in the $Si_{1-x}Ge_x$ system (figure 1). Though some results show low threading dislocation densities, RMS surface roughness of $Si_{1-x}Ge_x$ buffer structures is still quite high [17] so that a further polishing step is required. Other groups investigated, instead of grading layers, a direct low temperature growth of Ge on Si and reported TDDs as low as 10^5 cm^{-2} and RMS surface roughness of 0.33 nm [18]. In combination with a two-step strain-relaxation procedure [19] and subsequent high temperature Ge growth a relaxed Ge layer can be established which can be followed by GaAs solar cell growth.

In this paper attention is given to GaP nucleation on Si followed by metamorphic $Ga_{1-x}In_xP$ buffer growth as well as a direct deposition of Ge on Si followed by the growth of a single junction GaAs solar cell.

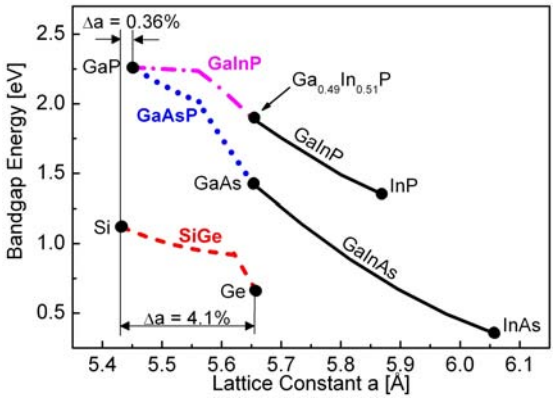

Figure 1: For growth of GaAs based solar cells on Si a difference in lattice constant of 4.1 % can be overcome by $Ga_{1-x}In_xP$ or $GaAs_xP_{1-x}$ buffer growth after initial GaP nucleation or by a transition (gradually or directly) from Si to Ge which is (basically) lattice matched to GaAs.

2 EXPERIMENTAL METHODS

GaP, GaInP and Ge layers were grown on highly n-doped Si (100) with 2° and 6° offcut towards the [111] direction. The growth took place in an AIXTRON 300 mm CRIUS Closed Coupled Showerhead MOVPE reactor for industrial volume production with showerhead technology and 7x4 inch configuration (conversion to 1x12 inch readily available). The reactor was specially designed for simultaneous Si, Ge and III-V growth. Temperatures were measured by in-situ process monitoring with a LayTec EpiCurveTwinTT© system consisting of two detector heads for pyrometrical temperature measurement and one additional head for wafer curvature measurement. Metal organic precursors TEGa, TMGa, TMIn and TBP were used for GaP/GaInP growth, GeH_4 for Ge growth and SiH_4 for Si growth (figure 2).

A GaP layer was grown (580 °C, 100 mbar, V/III = 10) on Si (figure 3(a)). The process starts with an initial in-situ oxygen desorption of the Si substrate by high temperature H_2 annealing. Afterwards a Si buffer was grown, which was annealed at high temperature for proper surface preparation. Then a GaP seed layer was established using the low temperature pulsed nucleation method. More details on the used process can be found in [20, 21].

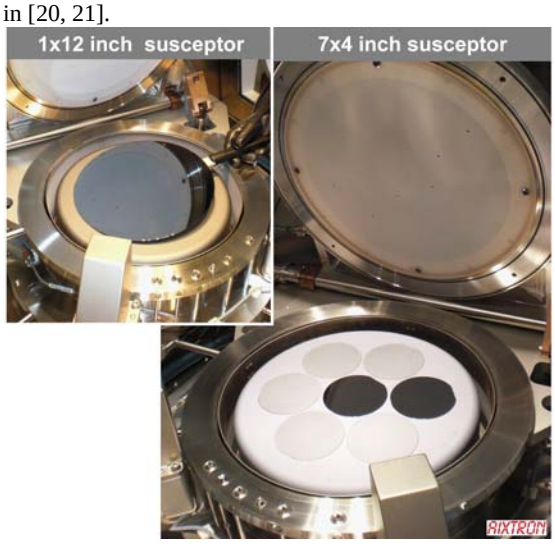

Figure 2: A 300mm CRIUS CCS with 7x4inch configuration (1x12" susceptor readily available) is used for III-V solar cell implementation on Si substrate.

On the basis of this GaP nucleation procedure a Si doped step-graded $Ga_{1-x}In_xP$ buffer structure was grown on top of a 150 nm thick GaP layer with a V/III ratio of 7.3, 620 °C surface temperature, 100 mbar reactor pressure and 9 buffer layers with 5.6 % increasing In content per step each 200 nm thick (figure 3(c)).

The direct growth of around 50 nm Ge on Si was performed at 420 °C, 50 mbar with GeH_4 after in-situ oxygen desorption by high temperature H_2 annealing and Si buffer growth. This low temperature Ge layer was annealed at 640 °C for 5 min before a 180 nm Ge layer was grown at 580 °C (figure 3(b)).

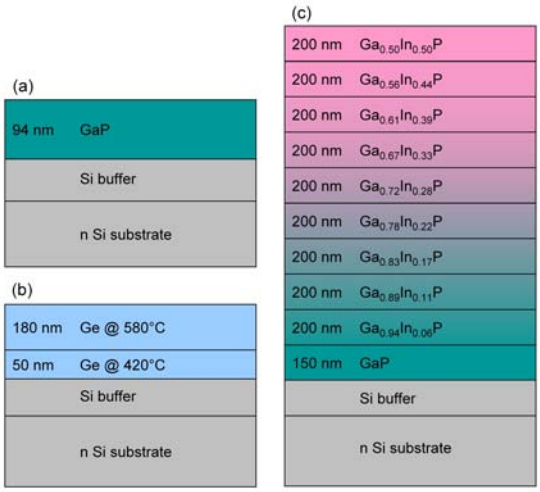

Figure 3: Three different structures grown in a 300 mm CRIUS CCS MOVPE reactor: **(a)** GaP nucleation layer. **(b)** Si/Ge virtual substrate obtained by two-step Ge growth. **(c)** Step-graded $Ga_{1-x}In_xP$ buffer structure grown on GaP nucleation layer (a).

The MOVPE grown structures were examined by x-ray diffraction (XRD), cross-sectional transmission

electron microscopy (TEM) and atomic force microscopy (AFM). Particularly the GaP nucleation layers were checked for APDs by TEM with special measurement conditions [21] and by AFM after annealing the samples at 700°C for 5min to uncover APDs [23]. In addition, directly after growth, ex-situ reflectance anisotropy spectroscopy (RAS) was applied to GaP surfaces in N_2 atmosphere to protect the GaP surface from degradation by reaction with oxygen.

3 RESULTS

3.1 GaP nucleation layer

According to XRD (004) rocking curve measurements the GaP layer thickness is 94 nm for both 2° and 6° offcut wafers. The separation of Si substrate and GaP layer peak and full width half maximum is 989/187 arcs and 987/187 arcs for 2° and 6° offcut wafers, respectively. This result implies similar high crystalline quality for both wafer offcuts.

For the analysis of the RAS measurements we also used a GaP layer homoepitaxially deposited on GaP substrate. The RAS signal of this layer served as an APD-free reference sample and allows a comparison with the RAS measurements on GaP grown on Si substrate (figure 4) [24,25]. The RAS signal intensity depends on the amount of APDs penetrating to the GaP surface. A qualitative indication for the amount of APDs is the difference in RAS intensity between the minimum around 2.5 eV and the maximum around 3.6 eV, hence denoted as min-to-max intensity. The better the RA spectra of the GaP-on-Si samples match with the GaP reference spectrum, i.e. large min-to-max intensity, the less APDs are on the GaP-on-Si surface. A zero line corresponds to an equal distribution of both anti-phases on the examined surface area.

Reflection anisotropy spectra of GaP-on-Si with 2° offcut mostly match homoepitaxial GaP with quite the same min-to-max intensity of around $20 \cdot 10^{-3}$. This result corresponds very well to the cross-sectional TEM image in figure 4. There are no stacking faults or microtwins and all APDs annihilate below the GaP surface so that the GaP surface is single-domain. GaP on 6° offcut Si shows less agreement with the reference with only around $15 \cdot 10^{-3}$ min-to-max intensity and therefore remaining APDs on the surface.

The run of the curve between minimum and maximum of the GaP-on-Si samples differs significantly from the GaP reference sample. This deviation is due to the presence of the additional Si-to-GaP interface [25].

The RAS results are consistent with AFM measurements of the same GaP-on-Si samples (figure 5). By sample annealing at 700 °C for 5 min APBs are made visible in the form of trenches and holes [23]. GaP on 2° offcut Si shows almost no remains of APBs in contrast to a roughly higher APD density on the 6° offcut Si wafer which can be held responsible for the reduced RAS min-to-max intensity.

Investigations on the first few monolayers of GaP revealed a three-dimensional growth mode turning into a two-dimensional surface with continuous growth. This problem – connected to the nucleation conditions – results in still visible APDs on the GaP surface as well as reduced RAS min-to-max intensity and has to be further optimized.

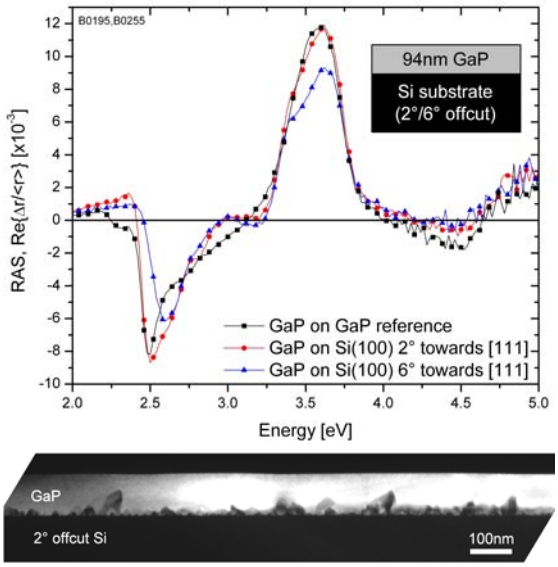

Figure 4: Top: Refelction anisotropy spectra of GaP nucleation layers on 2° and 6° offcut Si with the same nucleation condition in comparison with a homoepitaxial GaP-on-GaP reference. Bottom: Cross-sectional TEM image of the same GaP nucleation layer on 2° offcut Si. APDs annihilate each other below the GaP surface.

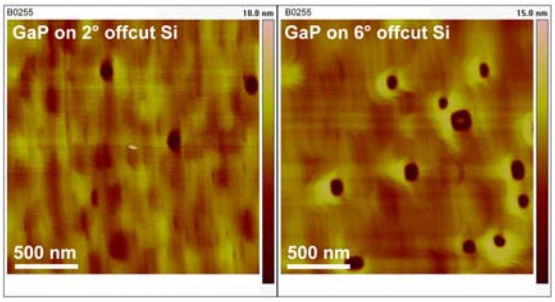

Figure 5: Exemplary AFM images of GaP surfaces on 2° and 6° offcut Si wafers (same samples as investigated by RAS).

3.2 $Ga_{1-x}In_xP$ buffer structure

On top of the GaP nucleation layers presented above, a $Ga_{1-x}In_xP$ buffer structure with 9 steps of 200 nm thickness each and increasing In content of 5.6 % per step was grown on 6° offcut Si substrate. Though many different growth conditions such as temperature, pressure, thickness and quantity of buffer layers, Ga precursor, etc. were tested $Ga_{1-x}In_xP$ buffer growth still turned out to be quite challenging.

In agreement with decreasing reflection in in-situ reflection measurement and decreasing layer peak full width half maximum in reciprocal space maps (both not shown here) TEM images show an increase in misfit dislocation and stacking fault quantity with each buffer layer originating from the buffer layer interfaces. As consequence the surface morphology becomes rough. Figure 6 depicts an overview of the common $Ga_{1-x}In_xP$ buffer structure on Si as well as a focus on the initial GaP and GaInP layers on 6° offcut Si substrate. The magnification shows a representative nucleation of a stacking fault at the GaP/GaInP interface penetrating through the entire buffer structure. In contrast to GaInAs – which has been successfully handled for metamorphic

triple-junction solar cells [26,27] – misfit dislocations are not bend at the buffer layer interfaces but multiply during growth and reach the sample surface. These threading dislocations are not confined inside the buffer structure as desired, impair high GaAs quality and therefore lead to poor solar cell performance.

Thus, we presently consider these $Ga_{1-x}In_xP$ buffer structures unsuitable for transition from Si to GaAs lattice constant. In contrast to $Ga_{1-x}In_xP$, $GaAs_xP_{1-x}$ buffers are more promising as has been demonstrated in [16], for instance. Still one has to be extra careful about the As-related problems during Si surface preparation mentioned above.

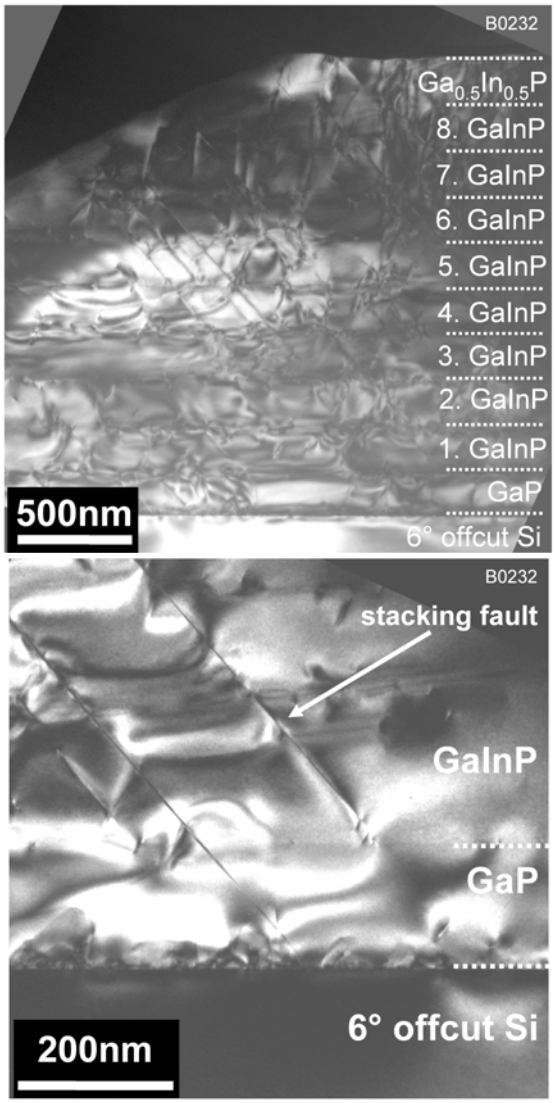

Figure 6: Top: $Ga_{1-x}In_xP$ step-graded buffer structure grown on GaP nucleation layer on 6° offcut Si substrate. With each buffer layer the amount of threading dislocations and stacking faults increases. Bottom: Stacking faults are created at the GaP/GaInP surface and penetrate unhindered through the following buffer layers, thus impairing required material quality.

3.4 Ge on Si by means of two-step growth process

Low temperature Ge layers of around 50 nm Ge were grown at 420 °C followed by an annealing at 640 °C and additional growth of 180 nm Ge at 580 °C. These Ge buffers retained only 4 % residual strain (according to XRD reciprocal space maps). Thus, the Ge layer is effectively relaxed and stress free lattice matched GaAs growth should be feasible. A lattice matched growth of high quality GaAs on Ge substrates (without APDs) is already carried out very successfully in lattice matched III-V multi-junction solar cells [1]. Anyhow, due to the applied MOVPE growth process which uses a growth temperature of 420 °C for the initial low temperature Ge layer we observed a three-dimensional growth mode and thus a fairly high surface roughness of the Ge buffer layer of about 2.0±0.4 nm. This needs to be improved before high-efficiency solar cell structures can be grown on this type of nucleation layers. To avoid three-dimensional growth and therefore reduce surface roughness growth temperatures for low temperature Ge below 300 °C can be a method of resolution [18].

4 SUMMARY AND CONCLUSION

This paper investigated various approaches to grow III-V-layers on Si substrate for the purpose of integrating III-V multi-junction solar cells on Si substrate. An industrial feasible 300 mm CRIUS Closed Coupled Showerhead MOVPE reactor was used. The challenge of APD-free III-V growth on Si can be mastered by initial GaP growth on Si with only 0.36 % lattice mismatch. The subsequent bridging of the 4.1 % difference in lattice constant between Si and GaAs with $Ga_{1-x}In_xP$ metamorphic buffer layers has not yet been successful in a wide range of process parameters. This is due to high dislocation nucleation during buffer growth and stacking faults formed at the buffer layer interfaces. It is expected that $GaAs_xP_{1-x}$ metamorphic buffers provide a more effective confinement of misfit dislocations within the buffer structure and therefore may be more suitable for high quality solar cell growth.

The alternative approach to compensate for APD formation and lattice mismatch by direct growth of an all Ge buffer layer in a two-step process is promising. Ge layers below 300 nm thickness on Si with only 4 % residual stress were deposited on Si. The MOVPE environment and low temperature Ge growth at 420 °C still induce initial three-dimensional Ge growth. This results in fairly high Ge surface roughness around 2 nm and may be coped by lower Ge deposition temperatures below 300 °C, as suggested in [18].

5 ACKNOWLEDGEMENTS

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