Simulation and Experimental Investigation of Slew Rate Related ESD Failures of CDM and CC-TLP

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Zusammenfassung – Dieses Paper untersucht kritische Belastungsfaktoren für die Korrelation zwischen CDM und Capacitively Coupled Transmission Line Pulsing (CC-TLP). Ausgehend von unzureichend reproduzierbaren Testergebnissen von drei verschiedenen CDM-Testsystemen wurde untersucht, ob dies mit Hilfe der kontaktbasierten Methode CC-TLP erklärt werden kann. Dabei wurde insbesondere der Einfluss der Anstiegsgeschwindigkeit des Stroms auf den Ausfallschwellwert analysiert. Neben der expliziten Untersuchung der CDM/CC-TLP-Korrelation an diesem Beispiel, wird eine verallgemeinerte Parametersimulationsstudie diskutiert.

Abstract – This paper investigates critical stress factors concerning the correlation between CDM and Capacitively Coupled Transmission Line Pulsing (CC-TLP). Starting from poorly reproducible test results of three different CDM testers, we examined the question if this can be resolved by the contact-mode test method CC-TLP and thereby analyzed in particular the impact of the current slew rate on the failure threshold. In addition to this explicit analysis of the CDM and CC-TLP correlation, a generalized parameter simulation study is presented.

1 Introduction

The Charged Device Model (CDM) is the main test method of IC component ESD testing. However, it suffers from the lack of reproducibility due to the air discharge. The demand for improved CDM control arising e.g. from, the technology scaling effect reveals more and more the limitations of CDM. The paper discusses some of these key issues and how they can be resolved by the contact-mode test method Capacitively Coupled Transmission Line Pulsing (CC-TLP). We thereby highlight the impact of the current slew rate on the failure threshold based on the results of three different CDM testers and the CC-TLP on a very small IC designed in a 0.25 µm BCD technology.

In this context, we demonstrate first results of a parameter simulation study. Subject of this study is the difference between the stress voltages on an ESD-protected element, e.g., a gate oxide, induced by CDM and CC-TLP. This enables us to investigate the correlation between CDM and CC-TLP in a more general way and to reveal critical stress factors. We thereby analyze in particular the impact of the current slew rate on the ESD stress voltage across a gate oxide.

2 Miscorrelation between three different CDM testers

The starting point of our investigations were the poorly correlating results of three CDM tester depicted in Table 1. The device-under-test (DUT) was an IC manufactured in a 0.25 µm BCD technology and assembled in a small package with a footprint of only 7.5 mm². The corresponding correlation study between CDM and CC-TLP was already discussed in detail in [1][2]. Therefore, it is summarized under the perspective of critical stress factors in this paper. In the three CDM tests, stress levels between 250 V and 1.5 kV were used. While first device failures were found at 500 V for tester A, tester B and C started to generate failures only at 750 V. For tester A and B at least half of the tested devices passed the test, even for 1.5 kV. Even when each CDM test is considered individually, the threshold voltage was not reproducible. Obviously, pin 3 only failed for tester A. To be able to understand this miscorrelation, we performed a deeper failure threshold analysis by means of CC-TLP, which raises the question: Can CC-TLP resolve the correlation issues between the three different CDM testers?

	CDM (testers and failing pins)					
Tester	A		B		C	
Pulses	1 (per pol.)		3 (per pol.)		1 (per pol.)	
< 500 V	27/0		12/0		6/0	
500 V	18/4	(1,2)	6/0		3/0	
625 V	9/5	(1,2)	6/0		3/0	
750 V	18/5	(1,2,3)	6/3	(2)	3/3	(1,2)
875 V	-	-	6/3	(1,2)	-	
1000 V	18/8	(1,2,3)	6/2	(1,2)	3/3	(1,2)
1500 V	18/8	(1,2,3)	-		3/2	(1,2)

Table 1: CDM test results reporting the ratio of the total sample size (left number) and the number of failing samples (right number). The number of the failing pins is denoted in brackets.

3 Correlation between CC-TLP and CDM testing

3.1 The CC-TLP system

In contrast to CDM, CC-TLP [3][4] is a contact-mode test method. While the contact needle of the CC-TLP probe is connected to a single pin of the floating DUT, a highly reproducible fast rising rectangular voltage pulse is send through a coaxial cable and the contact needle of the probe to the DUT (Figure 1). The gold-plated brass plane called Ground Plane (GP) is connected to the outer conductor of the coaxial cable and positioned above the DUT to form a background capacitance C_{Bg}. During a CC-TLP pulse, the background capacitance C_{Bg} starts to charge up with the rising edge of the pulse and to discharge with the falling edge of the pulse. Identical to VF-TLP, the stress current is obtained by the time domain reflectometer principle. A detailed description of the stress current calculation regarding the time shift as well as its alignment to CDM stress levels can be found in [1].

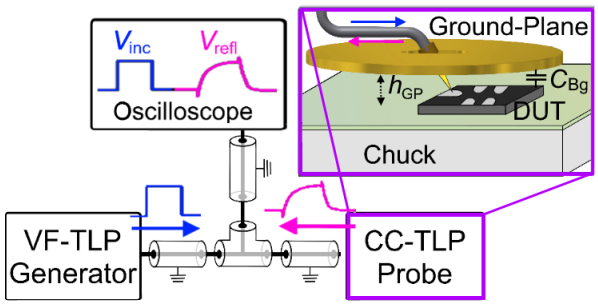

Figure 1: Probe set-up for CC-TLP testing on package level.

3.2 The CDM testers

All CDM tests were performed according to JESD22-C101F [5]. This standard requires an oscilloscope with single shot bandwidth of 1 GHz for calibration. The stress currents are recorded, however, there is no upper limitation on the bandwidth (Table 2), which makes the comparison of the different CDM tests difficult. The qualification test itself requires at least one positive and one negative stress pulse per pin. The number of zaps per voltage level as a critical stress factor is discussed in chapter 4.1.

		CDM			CC-TLP
		A	B	C	
Scope Bandwidth (GHz)		6	4	8	33
Number of Pulses (pos. and neg.)		1	3	1	multiple
Stress current	Rise time t_r (ps)	72	128	55	49
	Bandwidth (GHz)	5.9	3.3	7.7	8.7
	Slew rate (A/ns)	26	10	44	60

Table 2: Used test and measurement equipment as well as the number of pulses per pin and stress polarity.

The lower part of Table 2 characterizes the waveforms of the four test systems by stressing the ground pin of the DUT (Figure 2). Because of the small footprint of the package (7.5 mm²), the duration of the measured current waveforms is fairly small.

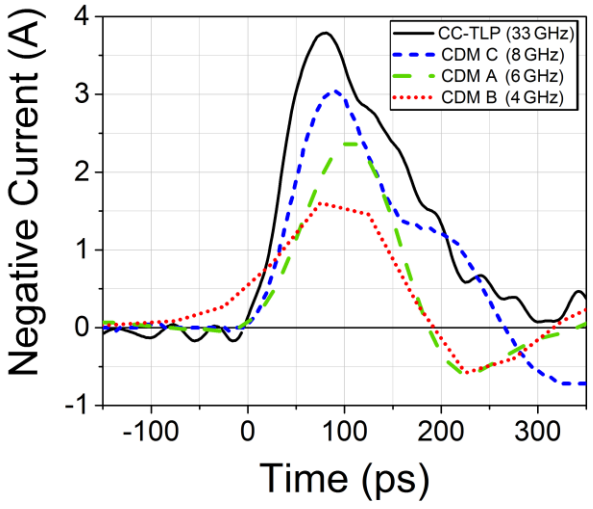

Figure 2: Current waveforms of CDM testers for +500 V CDM stress of the ground pin and CC-TLP with a higher current level.

The difference in amplitudes of the CDM curves is due to the variation arising from the air discharge and to the difference in the bandwidths of the oscilloscopes used (Table 2). The current transients of CDM and CC-TLP show comparable waveforms. This is required to induce the same failures. With 49 ps, the stress current waveform of CC-TLP has the shortest 10% - 90% rise time t_r (highest slew rate: 60 A/ns). As the signal bandwidths reconstructed from the rise times of the CDM waveforms (Figure 2) match the bandwidths of the used oscilloscopes very well (Table 2), these bandwidths seem to represent the limiting factor of the given CDM systems. A detailed description of the rise time, slew rate and the limiting bandwidth factor of the CC-TLP can be found in [1].

3.3 CC-TLP failure threshold analysis

For CC-TLP, the failure threshold was determined by an increasing step stress, the leakage current of which was monitored after each stress pulse. The evolution of the leakage currents is shown in Figure 3.

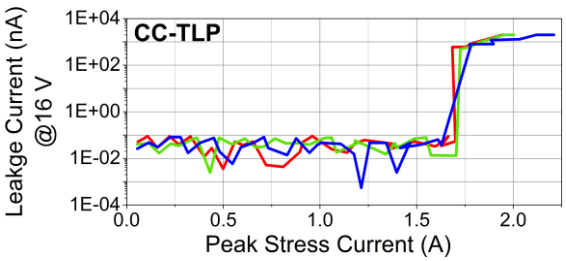

Figure 3: DC leakage current evolution at pin 2 of three different DUTs as function of the CC-TLP stress current.

For CC-TLP, all pins that were stressed above the failure threshold showed a clear leakage current. The failure signature was found to match the electrical failure signature of the failing units after CDM stress perfectly well. In contrast to CDM, the failure thresholds determined by CC-TLP were very reproducible (Figure 3). Single CC-TLP stress pulses as well as multiple CDM discharges gave the same test results, which shows that step stressing has no impact on the failure current. Overall, the failure thresholds determined with CC-TLP match those of the CDM testers. The reason why pin 3 showed no fail when stressed with tester B may be owning to the large failure threshold of pin 3 (~50% larger than pin 1), the corresponding 1.125 kV stress level of which was not covered by tester B. Tester C shows a <100% failure rate at 1.5 kV. This may be caused by partial discharges as shown in [6] which also may have prevented a failure of pin 3.

3.4 Correlation of failure signatures and failure locations

The failure location was narrowed down by backside photon emission microscopy. As can be seen in Figure 4, both images show emission spots at the same location.

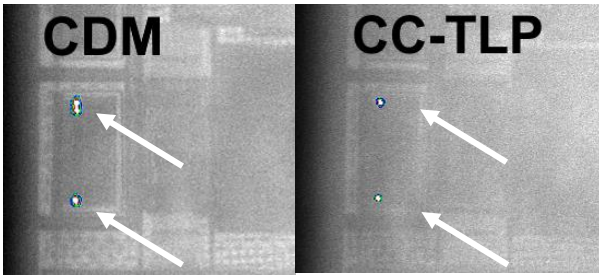

Figure 4: Backside photon emission microscopy images of DUTs with pin 2 failures. The spots indicate the failure locations after CDM stress (left) and CC-TLP stress (right).

Finally, the devices were deprocessed in order to investigate the detailed failure location and microscopic failure signature. After polysilicon etching scanning electron microscope (SEM), images were taken of a CDM and of a corresponding CC-TLP stressed device. They show the damaged gate oxide of a transistor connected to the stressed pin. Obviously, the CC-TLP measurement has caused the same failure signatures at the same location as the CDM stress. As a secondary effect, even a damaged drain-to-source junction suffering from a melt filament was found in a deeper analysis. An SEM image and the detailed description of this second effect failure mechanism can be found in [1].

Overall, there is an excellent correlation between CDM and CC-TLP stress.

4 Critical stress factors - reproducibility issues of CDM failure thresholds

The results of the CDM tests in Table 1 show a poor reproducibility of the threshold voltages between 500 V and 700 V with no hard limit (i.e. 100% failure rate) for the CDM robustness. In contrast, the failure threshold determined by CC-TLP is highly reproducible and lies within this range. It was verified by means of pre/post CDM stress drift analyses that no passing unit suffered from any degradation or wear-out effect after the stress. However, the soft transition from PASS to FAIL of testers A and B and the <100% failure rates of all CDM testers show that the reproducibility of the CDM testers is limited.

4.1 Number of CDM stress pulses per voltage level

As stated in Table 2, tester B used three stress pulses, whereas tester A and C used only one stress pulse per voltage level. However, the failure thresholds of testers B and C are in good agreement. This indicates that a failure dependency on the number of pulses per pin can be ruled out for the tested devices. However, since the number of pulses is a critical CDM stress factor that could lead to a miscorrelation [10], it is highlighted in the following section.

Many debates were held in the history of CDM testing about the number of CDM stress pulses per voltage level. Mainly, a statistical benefit conflicts with the time saving reduction of the stress pulses. In order to better weigh the pros and cons, this section offers a purely mathematical analysis of the advantage when using more than one zap per voltage level.

The qualification test according to JESD22-C101F [5] requires at least one positive and one negative stress pulse per pin. While the ESD standard ANSI/ESD S5.3.1 [7] states three zaps per polarity, their joint standard ANSI/ESDA/JEDEC JS-002-2014 [8] requires to apply at least one discharge per polarity to each pin and to test a minimum of three units. For tester B, three stress pulses are used in order to be less sensitive to outlines that do not reach the nominal peak current level and thus to increase the possibility to reach a failure rate of 100%. In this case (assuming a hard limit for the CDM robustness), the highest peak current I_p in each set of three stress pulses should be considered. Because in the case of no DUT failure, this was the highest stress current of the set below the current failure threshold and in the case of a DUT failure, it was definitively above the current failure threshold.

As a first approximation, we can assume that the single CDM peak currents follow a continuous normal distribution [9] (superimposed with an unknown distribution due to field emissions). In Figure 5, a normal distribution $f(I_p) = N(\mu, \sigma^2)$ (green curve) with a standard deviation of σ around a mean value μ represents a possible distribution of CDM peak currents I_p of one voltage level. Its cumulative distribution function $F(I_p) = \int_{-\infty}^{I_p} f(x)dx$ (green dashed line) gives the area under the probability density function and describes the probability that a stress pulse will take a peak current less than or equal to I_p.

We want to compare this distribution with the distribution that is obtained when the maximum of three pulses is considered $f_{\max(3)}(I_p)$. In that case, the probability to take a peak current less than or equal to I_p is that all three peak current values are less or equal to I_p. This means that its cumulative distribution function $F_{\max(3)}(I_p)$ (blue dashed line) is equivalent to $F(I_p)^3$. After that, we obtained $f_{\max(3)}(I_p)$ (blue line) by deviation of $F_{\max(3)}(I_p)$. It is remarkable that the probability density function $f_{\max(3)}(I_p)$ (blue curve) is also normally distributed around a higher mean value:

$$\mu_{\max(3)} = \int_{-\infty}^{\infty} I_p \, f_{\max(3)}(I_p) \, dI_p = \boldsymbol{\mu + 0.85\,\sigma}$$

Having N sets of three stress pulses, the standard deviation of the sampled mean $\mu_{\max(3)}$ is $\sigma_{\max(3)} N^{-1/2}$, where $\sigma_{\max(3)}$ stands for the standard deviation of the peak currents when using the "maximum-of-three-pulses" method. The benefit of using this method instead of all single pulses is that the standard deviation of its distribution $\sigma_{\max(3)}$ reduces by **25%** against σ:

$$\sigma_{\max(3)} = \sqrt{\int_{-\infty}^{\infty} \left(I_p - \mu_{\max(3)}\right)^2 f_{\max(3)}(I_p)\, dI_p} \approx \boldsymbol{0.75\,\sigma}$$

This relationship applies irrespective of the standard deviation σ of the CDM pulses. Using the maximum of **two**, **five** or **ten** pulses would decrease the peak current variation by **17%**, **33%** and **41%**. Hence, the "maximum-of-three-pulses" method improves the reproducibility of CDM tests. Furthermore, unless the waveform of each single zap is monitored and runt pulses are repeated, multiple zaps reduce the impact of accidental runt pulses.

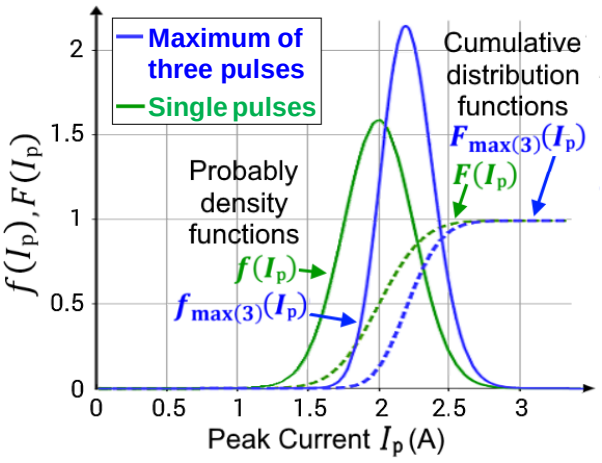

*Figure 5: Example of a peak current distribution of one CDM voltage level showing that the standard deviation by using only maximum of three pulses (blue) is around **25%** less than for using every single pulse (green).*

However, the benefit of reducing the peak current variation conflicts with the time saving reduction of the stress pulses to "at least one" in the standards [5],[8]. If the failure mechanism is subject to cumulative effects, the maximum-of-three-pulses method might have an influence on the degradation and ultimately on the failure threshold, as some pn-junctions show [10]. Thus, a consistent classification and a reliable correlation between the testers requires a clear specification of the number of stress pulses per voltage level.

4.2 Rise time (slew rate)

The following section deals with a second critical stress criterion, the rise time (slew rate). In this investigation, the most sensitive pin (pin 2) was stressed. Rise time filters that were inserted into the stress path varied the rise time of the CC-TLP setup. The stress currents and corresponding slew rates are plotted in Figure 6 for the different rise time configurations. As can be seen, by employing a 200 ps rise time filter, the failure threshold current increased. This indicates that both a threshold current and a threshold slew rate have to be exceeded in order to cause a failure, which is absolutely plausible given the naturally limited triggering speed of any ESD protection structure. For a detailed analysis, see [1].

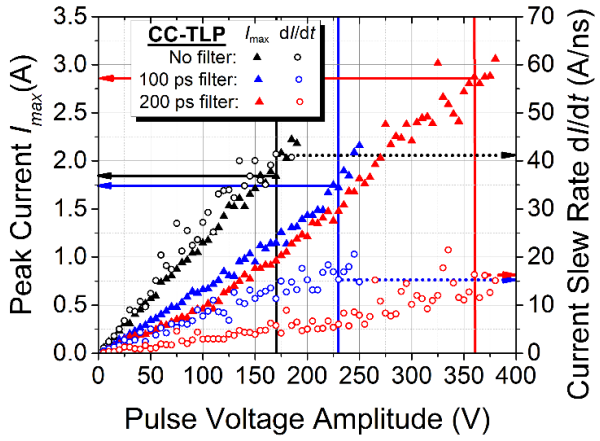

Figure 6: Peak currents (▲) and corresponding slew rates (o) for a CC-TLP step stress of pin 2 without (black), with 100 ps (blue) and with 200 ps (red) rise time filter in the stress path. The vertical lines mark the respective failure thresholds.

With the CC-TLP test and the usage of different rise time filters, we were able to identify the slew rate to be a critical stress factor for the tested devices. A corresponding diagram (Figure 7) visualizes these three data pairs as well as the corresponding data pairs of the CDM testers.

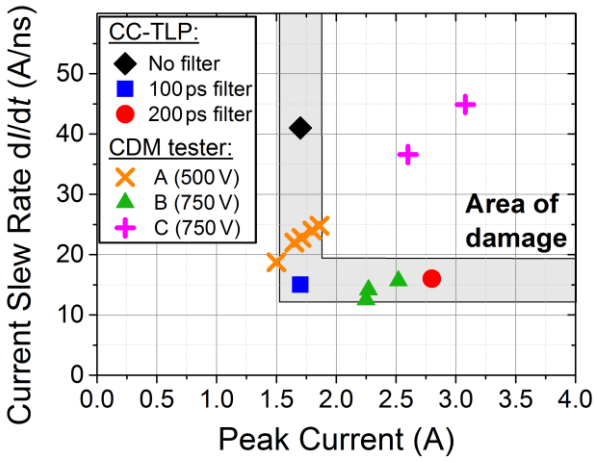

Figure 7: Threshold currents and threshold slew rates derived from CC-TLP step stress of pin 2 with different rise time filters (black, blue and red symbol) and corresponding data measured at the three CDM testers (orange, green and pink symbols)

The evaluation of the current slew rate of pin 2 stressed by tester B (Figure 7, green symbols) resulted in a somewhat threshold slew rate (based on the lower bandwidth of the scope) as for CC-TLP (Figure 7, blue and red symbol). The CDM slew rate variation caused by the air discharge (Figure 8) may explain the low failure rates above 625 V for tester B in Table 1. However, the threshold slew rate is clearly exceeded by testers A and C, even if a typical CDM slew rate spread of ± 25% as indicated in Figure 8 is assumed. Since the data of tester A is distributed around the peak current threshold in Figure 7, its peak current variation might be the limiting factor for its low failure rate at 500 V.

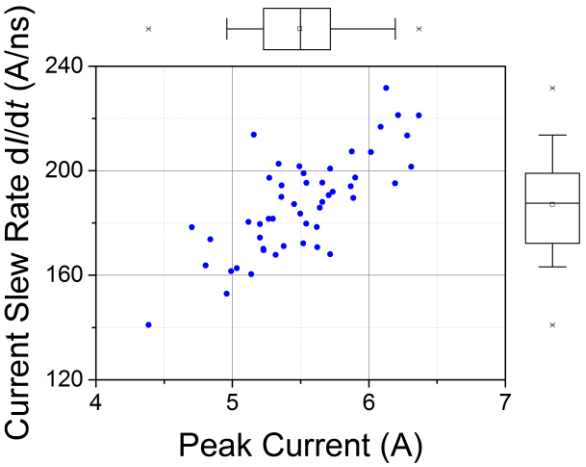

Figure 8: Peak current - slew rate distribution of 50 positive stress pulses obtained with tester B on pin 2 under test condition TC 750 of JS-002-2014 [8], measured with a 33 GHz oscilloscope. The distribution is illustrated by means of boxplots (25th and 75th percentiles) with whiskers (5th and 95th percentiles).

However, this variation cannot explain the low failure rates of tester A and tester C at higher stress levels. This leaves parasitic effects as a possible explanation. As explained in [6], the passing devices at 1.5 kV could be explained by partial discharges while operating tester A and C in the non-reproducible discharge regime.

Unfortunately, the root cause of the 500 V failure threshold obtained with tester A is still unknown. However, it should be noted that the 500 V and 625 V fails of tester A could not be repeated with the same tester in subsequent CDM tests of the same DUT, which opens the door for speculations on a temporarily miscalibrated or defective tester. More information about the reasons of the CDM miscorrelation can be found in [1].

5 Parameter simulation study

Inspired by the experimental results of the discussed correlation study, the following simulation study investigates the difference of the peak voltages on an ESD-protected element (e.g., a gate oxide), induced by CDM and CC-TLP in theory. One motivation is to understand the correlation between CDM and CC-TLP in a more general way and to identify the limits of each method.

5.1 Simulation model

5.1.1 The Device Under Test (DUT)

The object of investigation is the maximum voltage drop V_{IC} across an (internal) structure, which is represented by a capacitor C_{IC} (e.g., the capacitance of a gate oxide) and an optional series impedance $Z = R_{IC}$. It is protected by an ESD structure D_{ESD} in parallel (in a first approximation this is a simple ohmic resistor R_{ESD}) and enclosed by a background capacitor C_{Bg}, as can be seen in Figure 9. At the Port (or I/O pad respectively), the stress pulse is injected.

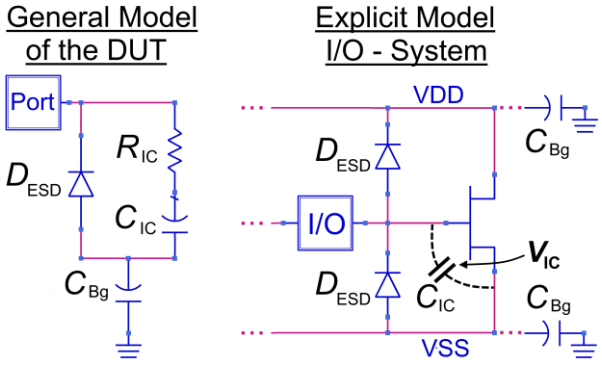

Figure 9: General (left) and specific (right) schematic of the system to be investigated in the simulations.

5.1.2 Simulation model of the testers

For the CC-TLP simulation, a stress voltage pulse (amplitude V_0, rise time t_r, pulse width w) is injected from a voltage source with output impedance $R_{S,CC\text{-}TLP} = 50\ \Omega$. To enhance comparability, the CDM discharge is treated as a long voltage step ($w_{CDM} \geq 30$ ns) through an equivalent RLC model [11] (Figure 10).

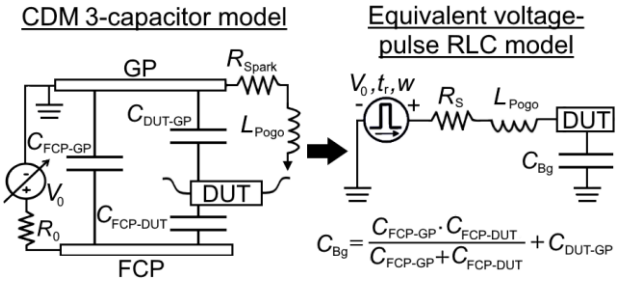

Figure 10: The discharge of the CDM 3-capacitor model (left side) is replaced by a voltage pulse into the equivalent RLC-circuit (right side) in the simulations.

The output impedance $R_{S,CDM}$ of the CDM voltage source is mainly given by the spark resistance R_{spark}. For an air discharge in a nitrogen atmosphere, its average was chosen to be $R_{S,CDM} = 28\ \Omega$ [12]. The inductance of the pogo pin L_{Pogo} is not represented through a lumped element in the simulation, since its corresponding effect can be set indirectly by the rise time t_r and the peak voltage V_0 of the pulse.

5.1.3 The complete simulation model

The entire schematics of CDM and CC-TLP test method simulations are illustrated in Figure 11.

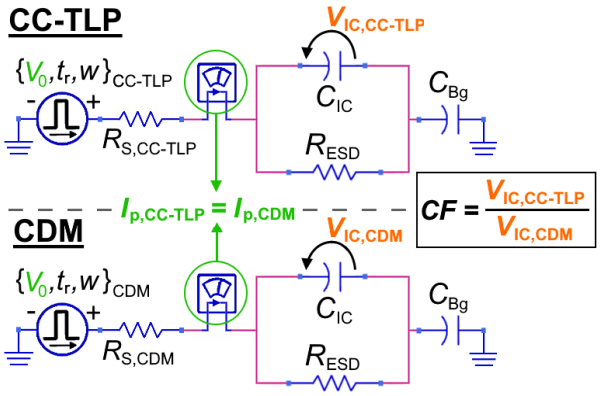

Figure 11: Schematics of the CC-TLP (top) and CDM test (bottom) in the simulation. The figure includes all the parameters that are used in the simulation.

Table 3 summarizes the parameters used for the simulation models of CDM and CC-TLP. The numbers in brackets denote the potential range of the parameter variation, a single bold number indicates the used default value in the simulation.

		(FI)CDM	CC-TLP
Discharge pulse-specific	R_S	(5 Ω - 80 Ω) **28 Ω**	**50 Ω**
	w	(≙ DC) **≳ 30 ns**	x-Axis of contour plots
	t_r	(10 ps-200 ps) **100 ps**	
	V_0	arbitrary value	voltage that creates a peak current equal to CDM
		→ $I_{p,CC\text{-}TLP} \stackrel{!}{=} I_{p,CDM}$	
DUT-specific	C_{Bg}	(0.5 pF - 5000.0 pF) **20 pF**	
	R_{IC}	**0 Ω**	
	C_{IC}	(1.0 fF - 5.0 pF) **1.0 pF**	
	R_{ESD}	y-Axis of contour plots	

Table 3: Parameters used in the simulation.

The necessary prerequisite for the comparison of the stress voltages induced across the gate-oxide is the same peak current I_p (Figure 11). This is the criterion in order to calibrate the CC-TLP pulse voltage with respect to the CDM stress [1]. The CDM and CC-TLP equivalent circuits differ according to their system impedances R_S, pulse lengths w and rise times t_r of their voltage pulses. Hence, with respect to a given CDM voltage $V_{0,CDM}$, a different pulse voltage $V_{0,CC\text{-}TLP}$ has to be set for CC-TLP to fulfill this calibration requirement. In the simulation, this is done by means of an optimization routine that minimizes their peak current difference for the given set of parameters before each measurement. In the case of a linear system (i.e. usage of resistances instead of protection diodes), also a post correction of their voltages is possible. Once equal peak currents are providing, we receive the resulting maximum voltage drop V_{IC} across the capacitance C_{IC}. As a factor of correlation, the quotient of the CC-TLP and CDM peak voltage drop is defined as:

$$\boldsymbol{CF := V_{IC,CC-TLP}/V_{IC,CDM}}$$

A correlation of both methods is given, if CF lies within a range of ±3% around 1. Consequently, a voltage understress of CC-TLP is denoted by $CF < 0.97$, a voltage overstress by $CF > 1.03$.

5.2 Results of the parameter study

The simulations were performed by means of the Keysight (Agilent) ADS circuit simulation tool and mathematically verified by Wolfram Mathematica.

5.2.1 Influence of the capacitance C_{IC}

One recurring speculation concerns a possible CC-TLP overvoltage across a gate-oxide, because of the longer stress duration of its pulse, which is caused by its source impedance of 50 Ω [15]. To resolve this matter, the correlation factors CF for two different capacitances of C_{IC} (e.g. gate-oxide capacitances) are plotted in Figure 12.

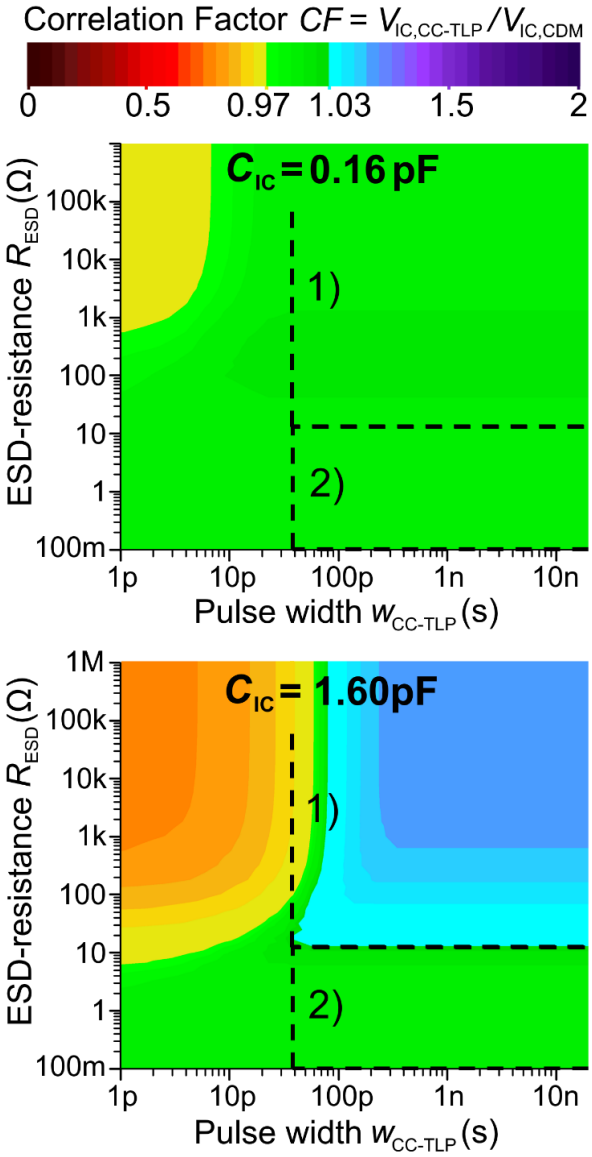

Figure 12: Correlation factor CF (color-coded) for two different capacities C_{IC} (all the other variables are set to their default values given in Table 3). The dashed lines specify region 1 and 2.

The dashed lines define the physical relevant regions for a functional ESD-protection (region 2: $R_{ESD} < 10\,\Omega$) and for a high resistant/no ESD-protection (region 1: $R_{ESD} > 10\,\Omega$). The area on the left side of region 1 and 2 has no practical meaning since it contains unrealistically small CC-TLP pulse widths below some tens of picoseconds. However, since the areas of understress and

overstress are moving, shrinking or expanding with the variation of parameters, this additional area serves to estimate the behavior of *CF*. By means of the *CF* color plot (Figure 12), we are able to find an appropriate answer to the previous question. If the variables are set to their default values given in Table 3, the following applies:
The maximum voltage drops of CDM testing and CC-TLP across the capacitor C_{IC} (e.g. gate-oxide capacitance) will only miscorrelate ($CF > 1.03$, voltage overstress), if the capacitance of the stressed structure is very high ($C_{IC} > 1$ pF) **AND** there is no a useful protection element (region 1: $R_{ESD} > 10\,\Omega$). This confirms what had been shown experimentally in several correlation studies over the last decade [10],[13]-[16]: Even though CC-TLP is based on a 50 Ω impedance, it correlates with CDM except for very special cases. In the following, we will discuss the influence of a variation of other variables within the ranges that are listed in brackets in Table 3.

5.2.2 Influence of the CDM spark resistance the background capacitance C_{BG} and R_{IC}

Taking into account the air discharge, the CDM spark resistance and in turn the CDM source impedance $R_{S,CDM}$ may vary for each pulse. A smaller resistance than the chosen default value of 28 Ω would increase an existing overvoltage of CC-TLP with respect to CDM stress in region 1. For larger spark resistances, up to 50 Ω, this overvoltage decreases and even become an undervoltage for values larger than 50 Ω.
For very small background capacitances C_{BG} of only a few picofarad, the overvoltage in region 1 disappears. Besides, the background capacitance C_{BG} shows nearly no influence on the simulation results, even when choosing different values for CDM stress and CC-TLP due to their different capacitive coupling of the chip.
The resistor R_{IC} that is connected in series with capacitor C_{IC} was set to 0 Ω, since the variation of its resistance shows only a slight increase or decrease of the correlation factor *CF*.

5.2.3 Influence of the rise time t_r

The most interesting quantity is the rise time t_r or slew rate respectively of the CDM and CC-TLP stress pulses. As shown in the experimental correlation study above, this may have an impact on the failure threshold (cf. 4.2). Apart from the interaction with the ESD protection structure regarding its triggering speed, the rise time has a direct influence on the peak voltage V_{IC} as depicted in Figure 14. Shorter CC-TLP rise times $t_{r,CC\text{-}TLP}$ in comparison to a default CDM rise time of $t_{r,CDM}$ = 100 ps lead to a decreased voltage drop of CC-TLP in region 1. This corresponds to an understress ($CF < 1$) for CC-TLP. Accordingly, longer CC-TLP rise times $t_{r,CC\text{-}TLP}$ lead to a CC-TLP overstress ($CF > 1$). In general, if CDM stress and CC-TLP are calibrated to the same peak current, the method with shorter rise times tends to result in a smaller peak voltage across the capacitor C_{IC} when there is no useful protection element (region 1: $R_{ESD} > 10\,\Omega$). This, of course, only applies if the rise times do not fall below the triggering time of the ESD protection structure. For a functional ESD-protection (region 2: $R_{ESD} < 10\,\Omega$), a miscorrelation depending on the rise time is not to be expected. In the linear case (with a resistance R_{ESD} as protection element), this simulated rise time relation can be derived on a purely mathematical basis by calculating the system response using the Laplace transformation. A logically comprehensible explanation could be the following:
As the capacitor C_{IC} charges, the charging current decreases exponentially with the RC time constant (based on $I = C\,\mathrm{d}U/\mathrm{d}t$). The shorter the CC-TLP rise time $t_{r,CC\text{-}TLP}$ of the voltage pulse, the earlier the voltage $V_{IC,CC\text{-}TLP}$ builds up across the capacitor C_{IC}. As Figure 13 shows, this results in a higher peak current $I_{p,CC\text{-}TLP}$ into the discharged capacitor. To receive an equal peak current value compared to a given CDM pulse, the higher CC-TLP peak value $I_{p,CC\text{-}TLP}$ has to be compensated by a smaller CC-TLP pulse voltage $V_{0,CC\text{-}TLP}$. However, this translates into a lower voltage drop of CC-TLP at the capacitor C_{IC}. Consequently, a miscorrelation in terms of a CC-TLP understress ($CF<1$) occurs.

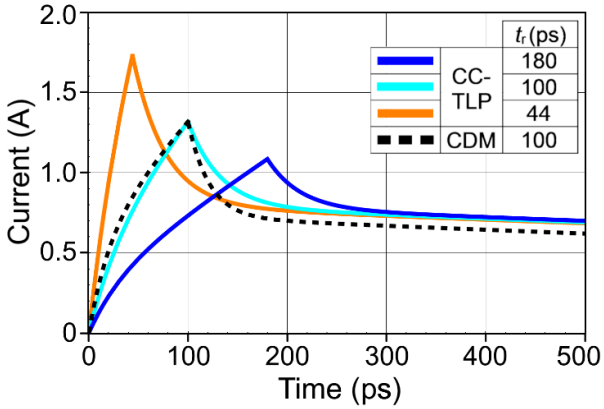

Figure 13: Stress current transients of the simulation model for different pulse rise times t_r and an unrealistic ESD-resistance of R_{ESD} = 100 Ω. The CDM pulse voltage was chosen to be 100 V. All the CC-TLP pulses have the same pulse voltage $V_{0,CC\text{-}TLP}$, which was selected in such a way that CC-TLP and CDM stress have the same peak current for a rise time of 100 ps.

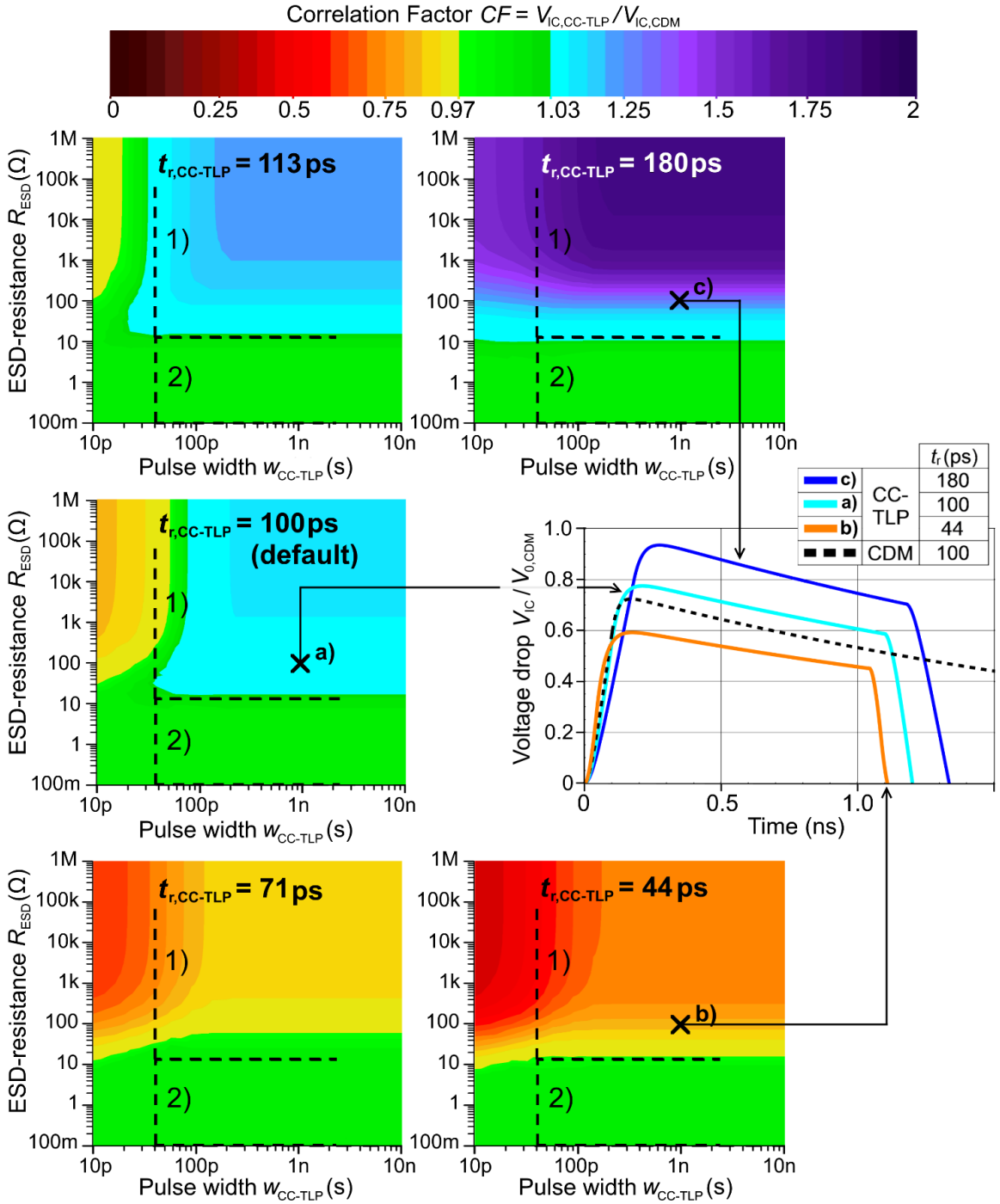

Figure 14: Color-coded diagrams showing the correlation factor CF for five different CC-TLP rise times $t_{r,CC\text{-}TLP}$ = {44, 71, 100, 113, 180} ps in comparison to a default CDM rise time of $t_{r,CDM}$ =100 ps. All the other variables are set to their default values given in Table 3. For an ESD-resistance of R_{ESD} = 100 Ω and a pulse width of $w_{CC\text{-}TLP}$ = 1 ns (✕), the centered plot exemplifies the transient voltage drop $V_{IC,CC\text{-}TLP}$ across the capacitor C_{IC} for three of these CC-TLP rise times. The black dashed line plots the corresponding CDM voltage transient $V_{IC,CDM}$ for a rise time of $t_{r,CDM}$ =100 ps.

5.3 Outlook for the simulation model

Although the simulated structure might seem to be fairly simple, the simulation provides a new general insight into the correlation issues between CDM stress and CC-TLP. One part of the future work on these simulations will be to make it more realistic, e.g., the implementation of non-linear ESD protection elements. It could be also beneficial to investigate the correlation between more alternative contact methods, e.g. CCDM and low-impedance CDM, and the correlation regarding different failure criteria, for instance energy related damages of a pn-junction. Furthermore, a verification of the simulation data by performing CDM and CC-TLP tests on corresponding structures implemented on a chip is intended.

6 Summary and conclusions

The correlation study between the poorly reproducible results of three different CDM testers and CC-TLP [1] was summarized under the perspective of critical stress factors in the paper. By means of a special investigation with CC-TLP, it was found that both a threshold current and a threshold slew rate have to be exceeded in order to cause a failure. Thus, we revealed the current slew rate to be an important factor for the non-reproducible CDM threshold and showed that CC-TLP was able to resolve main correlation issues between the three different CDM testers. Furthermore, we proved that the usage of three CDM stress pulses instead of only one pulse per voltage level results in a 25% reduced standard deviation of the peak current spread, which improves the repeatability of CDM test results.

Inspired by the experimental results of the investigated correlation study, we examined the general influence of different test parameters by means of a simulation study. In this context, we discussed differences of the CDM and CC-TLP induced peak voltages on an ESD protected element (e.g. a gate oxide). Even though CC-TLP is based on an impedance of 50 Ω, the simulation results confirm a general correlation between CDM and CC-TLP. This complies with the results, which have been gathered experimentally in several correlation studies over the last decade [10],[13]-[16]. If the CC-TLP voltage is calibrated with respect to the CDM stress and if the rise times are not shorter than the triggering time of the ESD protection element, the method with shorter rise times tends to cause a smaller peak voltage across the stressed gate oxide capacitor. The simulation model is subject to continuous improvement and is planned to examine the correlation of other alternative contact methods, e.g. CCDM and low-impedance CDM testers. Furthermore, an experimental verification of the simulation results is intended.
The findings of the given paper as well as previous correlation studies justify the establishment of the CC-TLP stress test method in the industrial environment.

Acknowledgements

The work was performed in close cooperation with Texas Instruments Deutschland GmbH. The authors would like to express their thanks to Professor Dr. Christoph Kutter for his EMFT PhD grant and the ESDA together with the co-sponsors CISCO and IBM for the ERC2016 Research Grant co-funding this work.

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