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Kerfless wafering approach with Si and Ge templates for Si, Ge and III-V epitaxy

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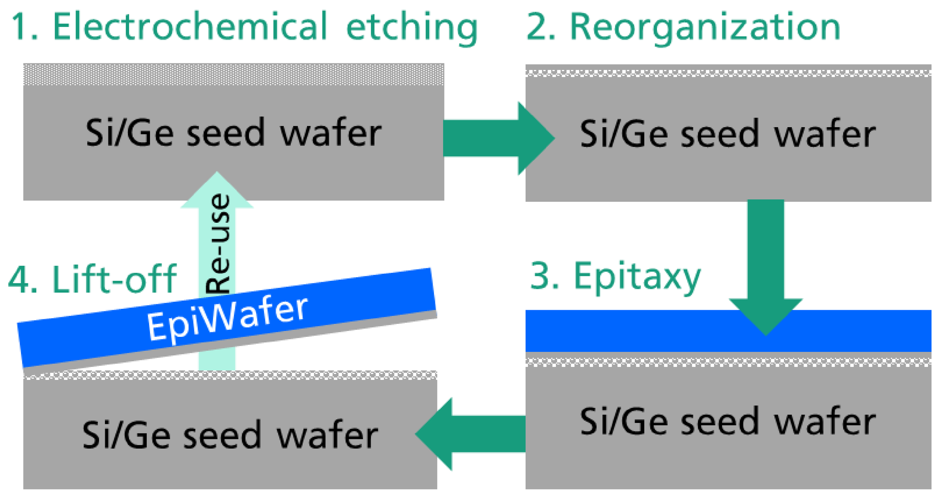
INTRODUCTION

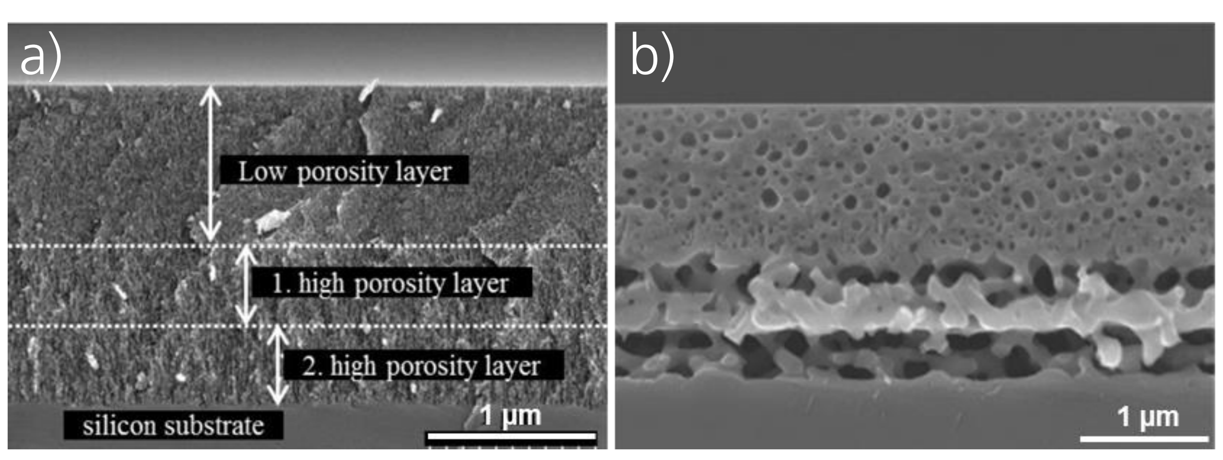
- "**Kerfless wafering**" of Si and Ge is an attractive approach to reduce material and energy consumption
- Kerfless wafering implies **epitaxially grown Si and Ge** wafers on reusable substrates with **porous detachment layer**



Schematic diagram of kerfless wafering

- For **Si**, we report on **high Si epitaxy quality** due to **new CVD tool**
- For **Ge**, we report on porous layer stack leading to **4" lift-off Ge templates** for future Ge or III-V epitaxial growth

POROUS SILICON + TEMPLATE FORMATION



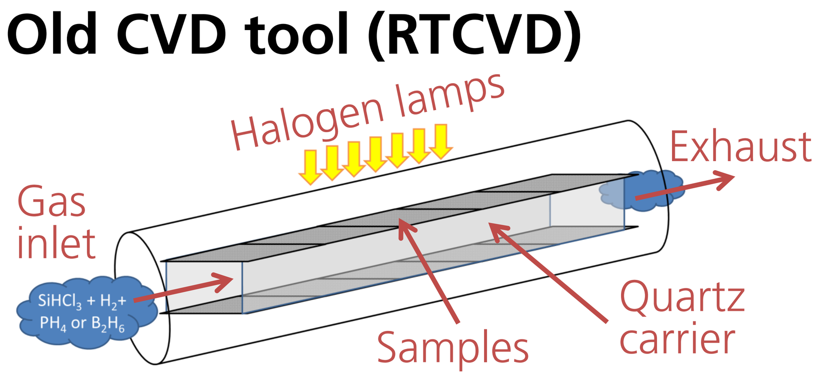
SEM image of porous Si a) before and b) after reorganization at 1120°C. A low-porosity layer on top of two high-porosity layers is visible

M. Drießen *et al.*, in *36th European Photovoltaic Solar Energy Conference. Proceedings* (2019), p. 135.

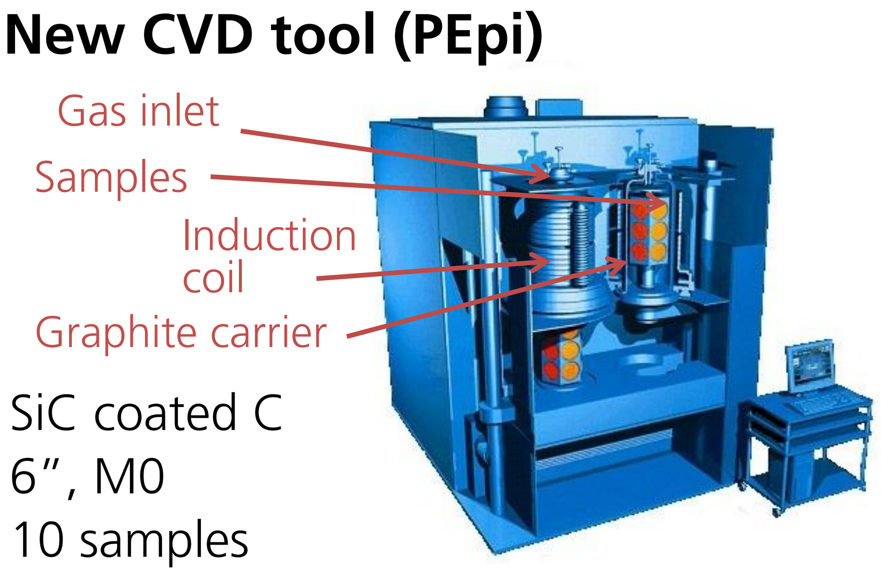
- For Si ($\rho \approx 20$ mΩcm, 6"), a well known porous layer is used, which leads to **closed, smooth Si template** with efficient detachment layer in old CVD tool
- Process is adopted in new CVD tool without optimization

SILICON EPITAXIE

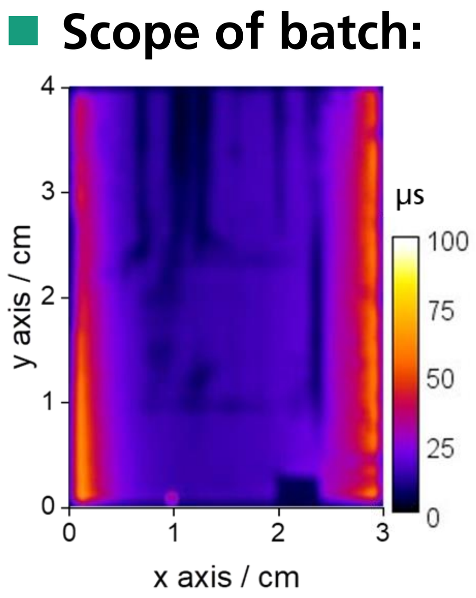
Old CVD tool (RTCVD)



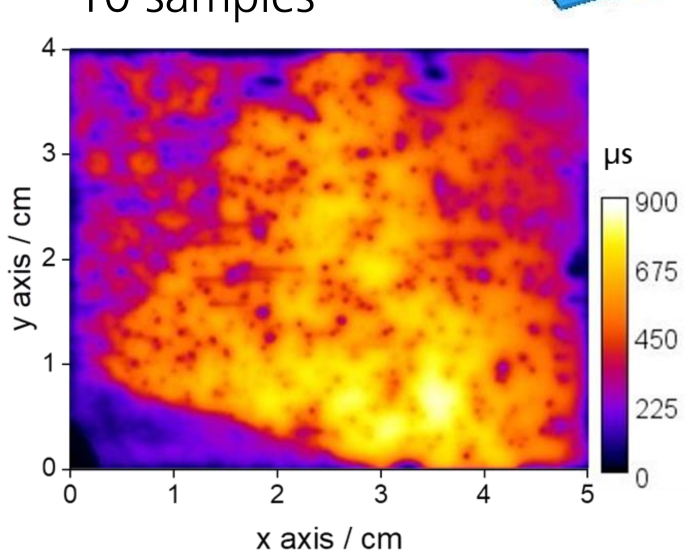
New CVD tool (PEpi)



	Old CVD tool (RTCVD)	New CVD tool (PEpi)
Carrier:	Quartz	SiC coated C
Sample size:	max. 4"	6", M0
Scope of batch:	2 samples	10 samples

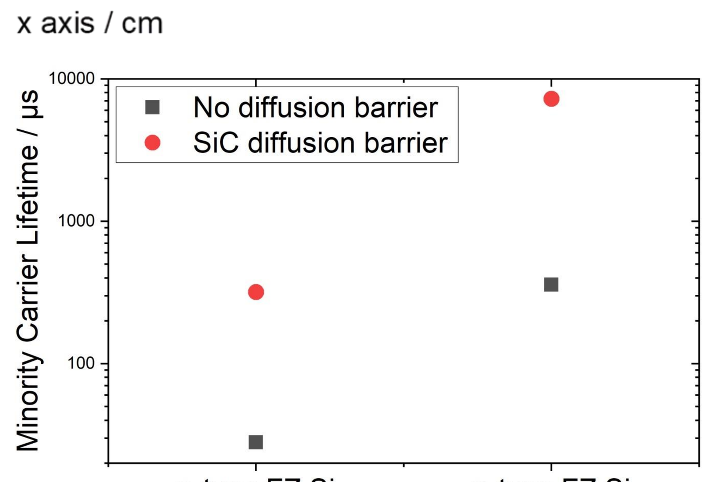


As-grown PL lifetime image of SiEpiWafer from **old CVD tool** (RTCVD) τ_{mean} **= 20 µs**



As-grown PL lifetime image of SiEpiWafer from **new CVD tool** (PEpi) τ_{mean} **= 430 µs**

- First **SiEpiWafers** grown in new CVD tool:
  - Layer thickness: **150 µm**
  - Total thickness variation: **~10%**
  - Doping level (adjustable): **1 Ωcm**
  - Minority carrier lifetimes τ_{eff} **> 800 µs**
- Strong lifetime increase in new CVD tool due to **low contamination** and **high thermal homogeneity**
- Lower contamination due to **SiC coated** carrier (new) instead of **quartz** carrier (old)



Effect of diffusion barrier on lifetime reference FZ samples annealed in old CVD tool for 30 min at 900°C

CONCLUSION

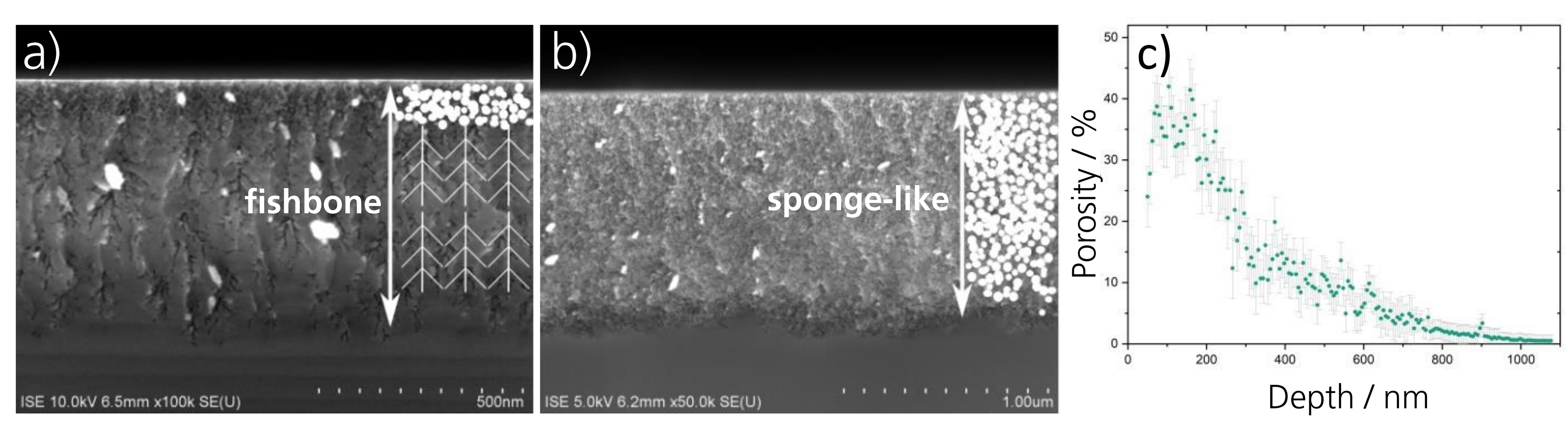
Silicon

- Our **new, microelectronic CVD tool** allows for EpiWafer growth on full area 6" and M0 wafers (M6 wafers in near future)
- High as-grown minority carrier lifetimes τ_{eff} **> 800 µs** could already be reached (non optimized templates)
- Lifetime increase is due to **low background contamination** and **high thermal homogeneity** in new CVD tool
- Next step: Understanding of correlation between template and crystal quality

Germanium

- Bipolar, electrochemical etching allows for formation of **porous Ge** with different structures (fishbone and sponge like)
- Annealing at 700°C leads to **closed, smooth Ge template** for III-V epitaxy
- Next step: First III-V growth on Ge template

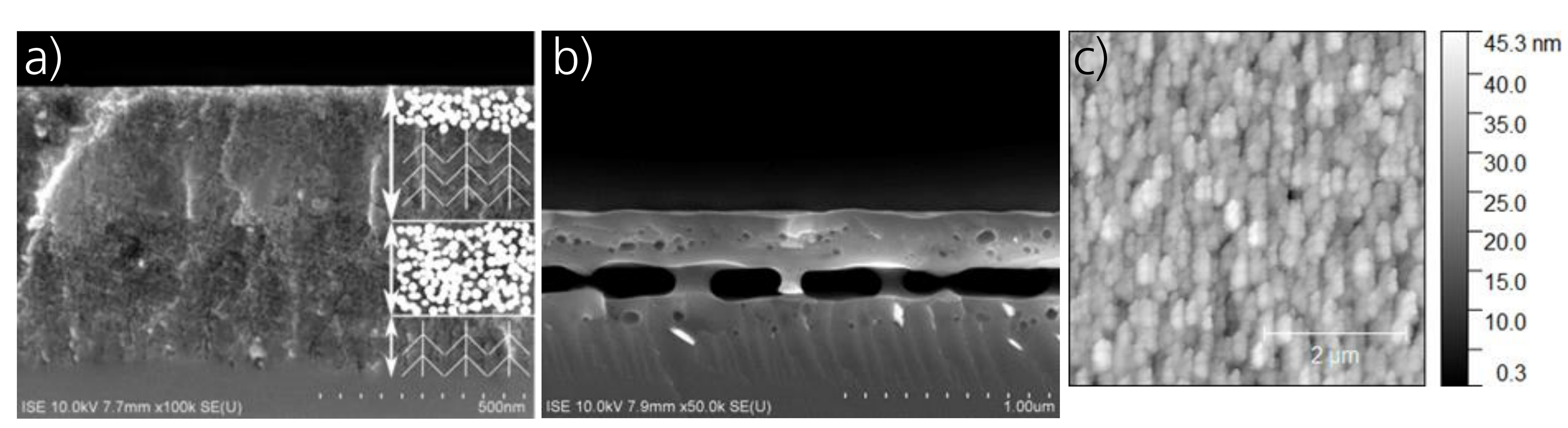
POROUS GERMANIUM



SEM cross section of a) Bipolar electrochemically etched fishbone layer. b) Bipolar electrochemically etched sponge-like layer. c) Porosity in dependence of depth of b)

- Ge substrate: Highly Ga-doped ($\rho \approx 20$ mΩcm) 4" Ge [100] wafers with 6° miscut towards the [111] plane, provided by UMICORE
- Porous Ge layers were **bipolar electrochemically etched** in batch tool provided by AMMT in HF electrolyte
- Porous Ge structures differ significantly from porous Si structures (e.g. **fishbone** and **sponge-like**)
- Constant etching parameters lead to **decreasing porosity**

GERMANIUM TEMPLATE FORMATION



SEM cross section of a) Porous layer generated by combination of different fishbone-like & sponge- like porous layers. b) Annealed structure from a) with clearly closed top layer followed by a separation layer consisting of voids and connection points between Ge bulk and top layer. c) AFM image of surface showed in b) with a RMS value of ≈ 5 nm

- Annealing experiments done under H_2 atmosphere in RTCVD tool
- Samples were annealed for 30 min at 700°C
- Combination of sponge like layer and fishbone layer leads to generation of separation layer and closed, smooth surface
- First III-V growth on Ge template is ongoing

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