Process and design optimization of SiC MOSFET for low on-state resistance

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Fraunhofer Society and Fraunhofer IISB

Fraunhofer Society

- Europe's largest application-oriented research organization
- Research according to the needs of the market

Fraunhofer IISB

- Leading SiC and power electronics institute
- Founded in 1985
- Located in Erlangen, Bavaria, Germany's hot spot for SiC and power electronics
- Close cooperation with FAU Erlangen-Nuremberg

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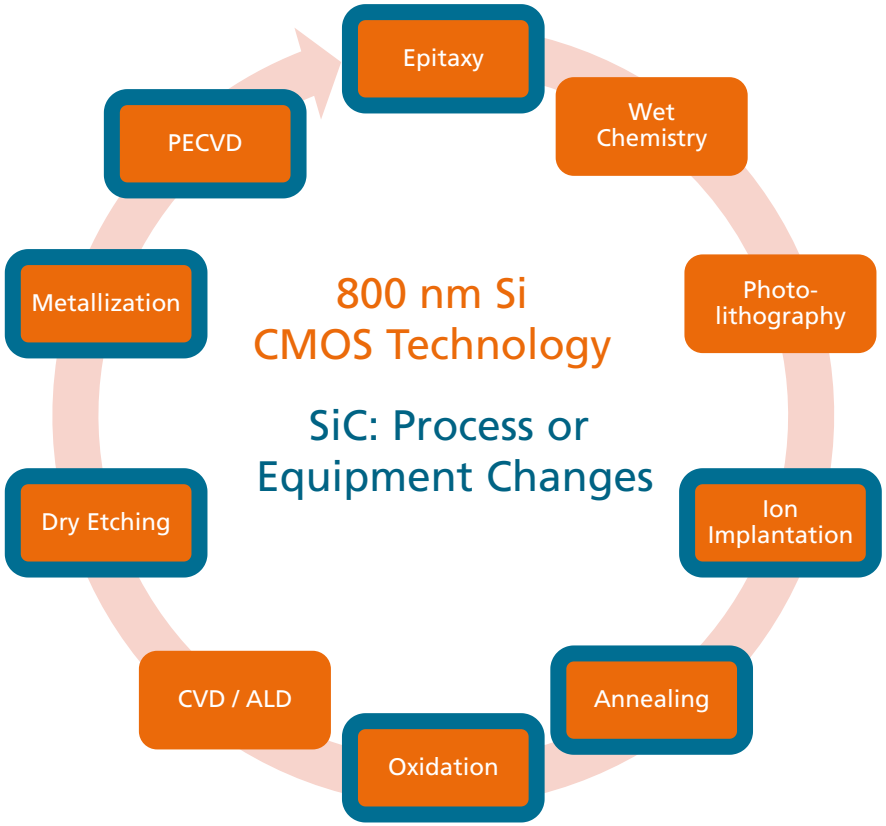
SiC prototypes and solutions

- Materials
- Devices
- Packaging and reliability
- Modules and systems



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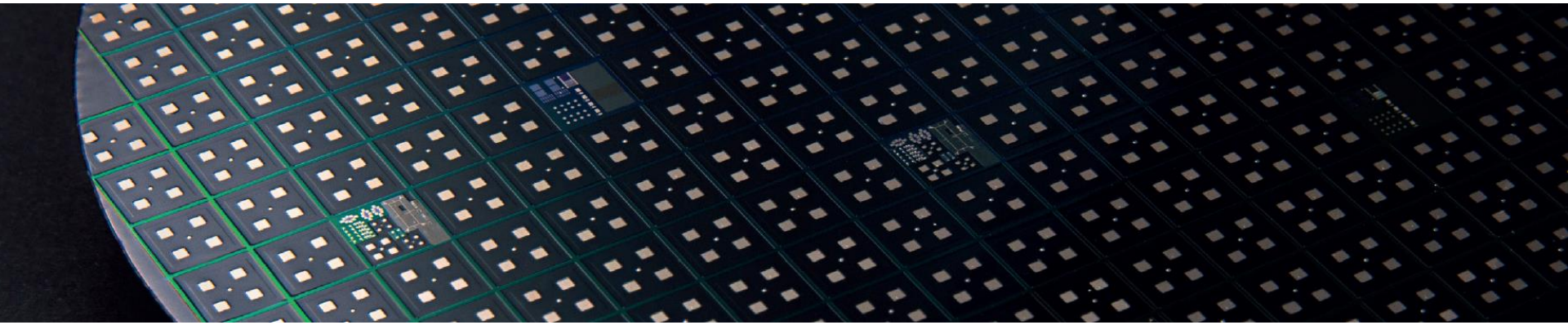
Properties of silicon carbide

- Why SiC for power semiconductor devices?

Parameter	Si	4H-SiC	Benefit from SiC
E_g (eV)	1.12	3.26	high-temperature operation
E_{crit} (MV/cm)	0.3	3	low on-state resistance
κ (W/cm/°C)	1.5	4.9	excellent heat dissipation
ν_{sat} (cm/s)	1×10^7	2.7×10^7	high switching frequency



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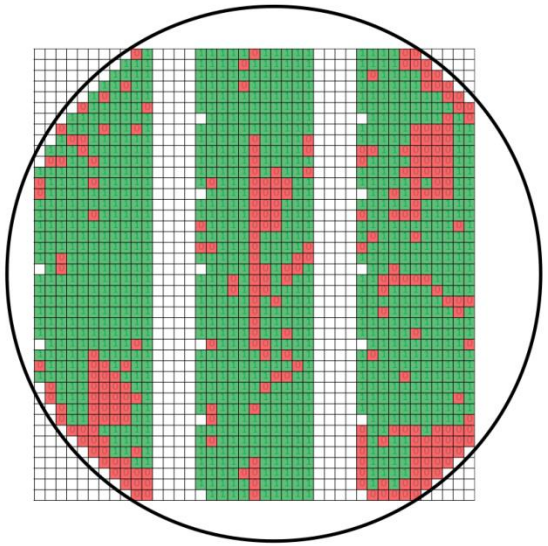
SiC Power MOSFET at Fraunhofer IISB

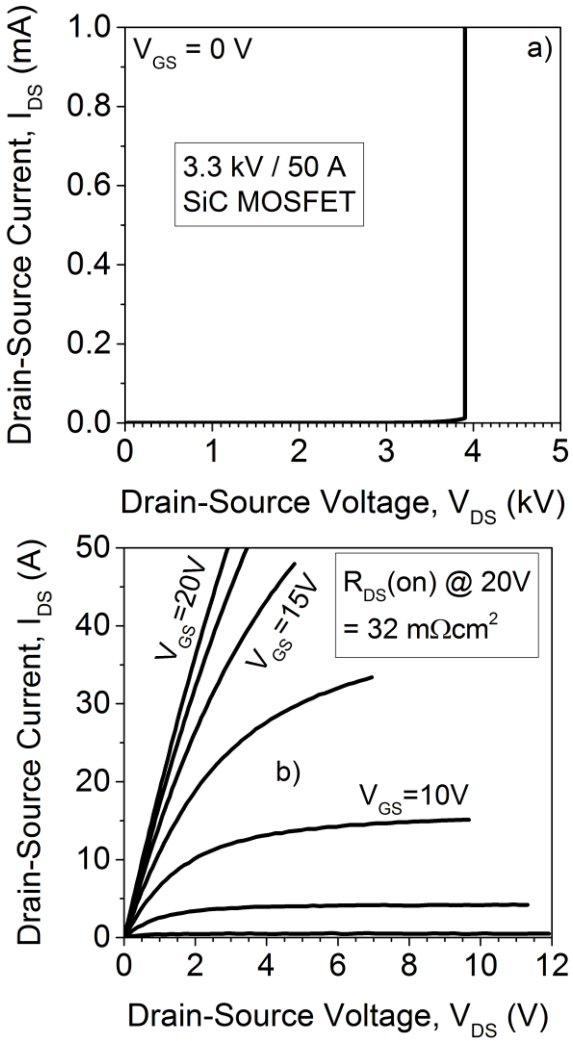
- Blocking voltage: 600 V – 3300 V
- Threshold voltage: 2 V – 3 V
- On-state resistance:
  - 10 mΩ cm² for 1.2 kV devices
  - 32 mΩ cm² for 3.3 kV devices
- Yield: 80% for 4 mm² chips



working chip

failure

Yield map for 1.2 kV SiC Power MOSFET, chip size = 4 mm²



Blocking and forward characteristics for 3.3 kV SiC Power MOSFET fabricated at Fraunhofer IISB

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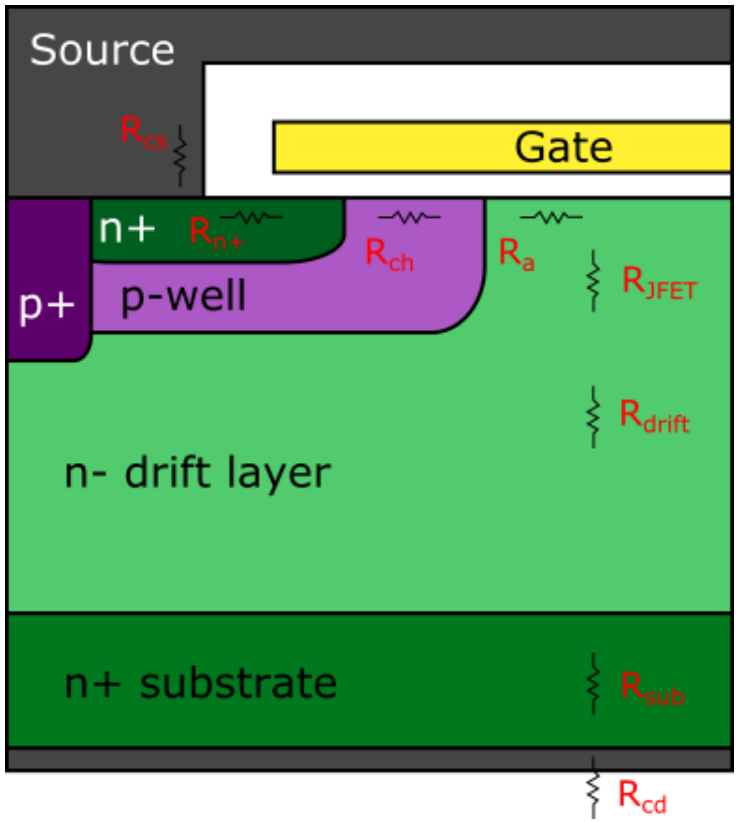
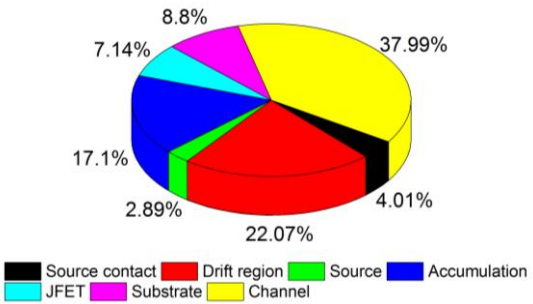
SiC Power MOSFET resistance

- Different components of on-state resistance

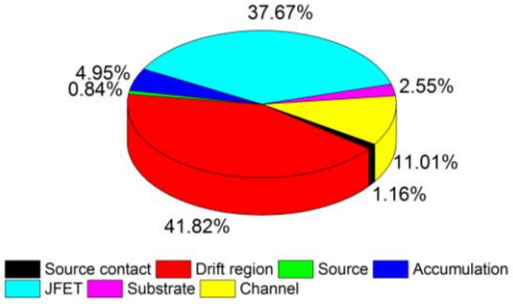


- Contribution of different components to total R_{DS}(on) depends on cell design and blocking voltage

1.2 kV SiC MOSFET



3.3 kV SiC MOSFET



Analytical simulation of resistance of SiC Power MOSFET with 3 µm JFET, 1 µm channel, 13 µm cell pitch

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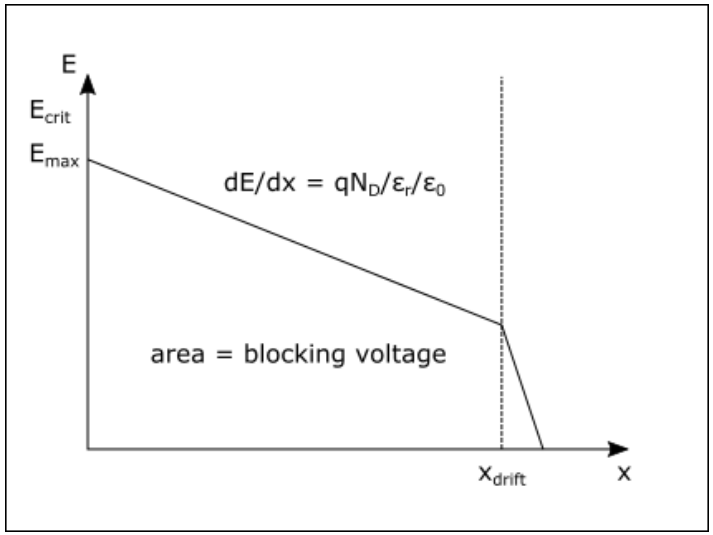
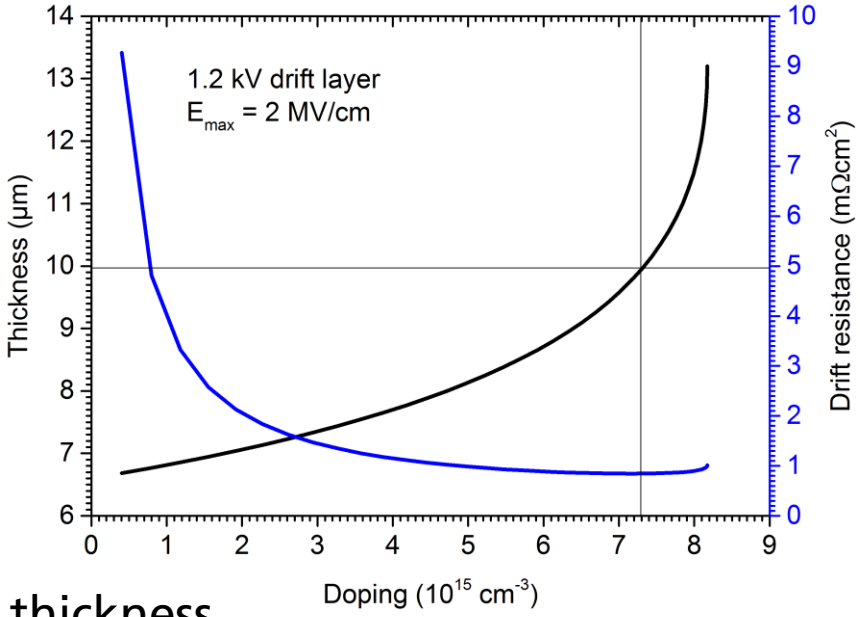
Resistance: drift layer

Voltage	650 V	1200 V	1700 V	3300 V
Contribution to R_{DS}(on)	10.8%	22.1%	31.9%	41.8%

- Optimization task: find drift layer doping and thickness at minimum resistance





- Too high doping and / or too small thickness

→ increase of electric field

→ increase of drain-source leakage current

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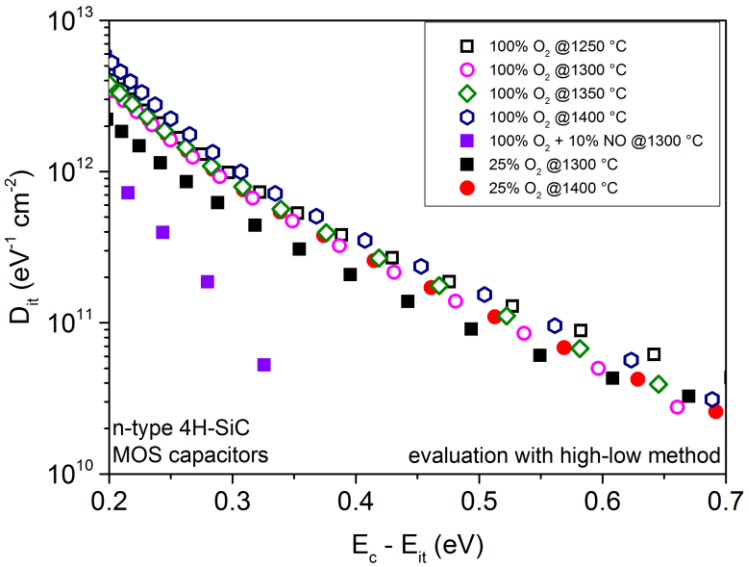
Resistance: channel

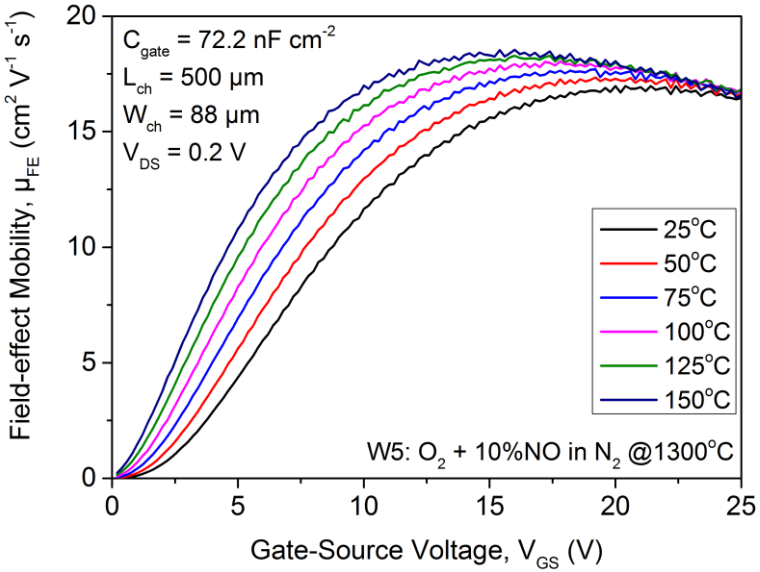
Voltage	650 V	1200 V	1700 V	3300 V
Contribution to R_{DS}(on)	45.9%	38.0%	30.9%	11.0%

- High density of states at SiO_2 / SiC interface → low mobility → high channel resistance
- Sophisticated gate oxides (NO annealing)

→ passivation of interface states and increase of electron mobility

→ shift of flatband (threshold) voltage





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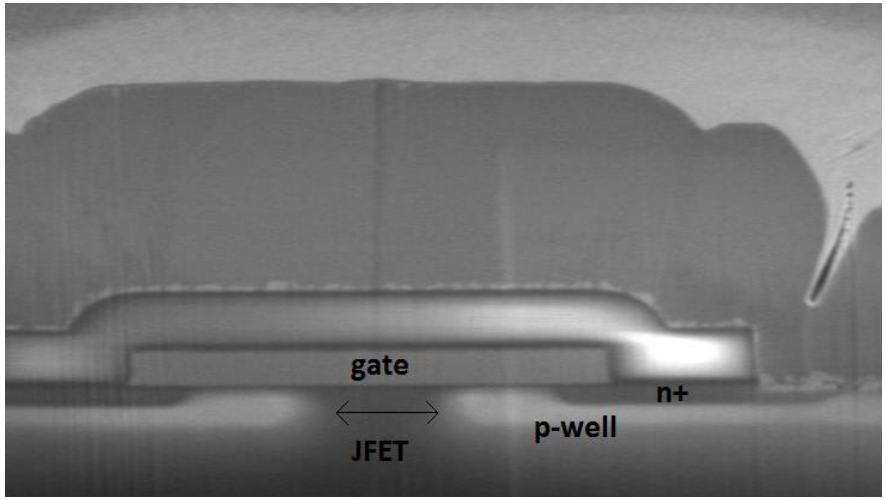
Resistance: JFET

Voltage	650 V	1200 V	1700 V	3300 V
Contribution to R_{DS}(on)	3.8%	7.1%	10.6%	37.7%

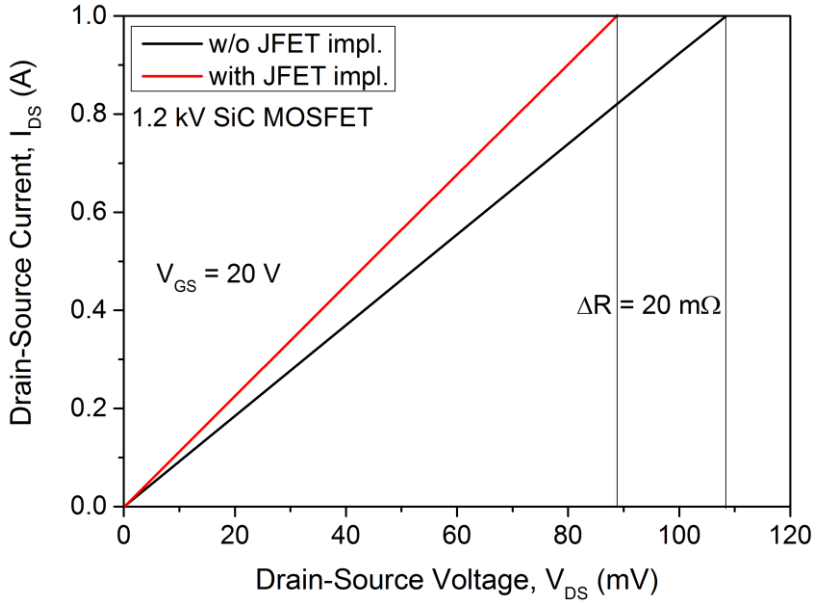
- JFET implantation used to reduce extension of the space charge region in the JFET region

→ decrease of JFET resistance

→ possible increase of electric field in gate oxide



FIB cross-section of 3.3 kV SiC MOSFET. Implanted regions are visible. Designed JFET width = 2.5 µm, but real JFET width = 1.4 µm.



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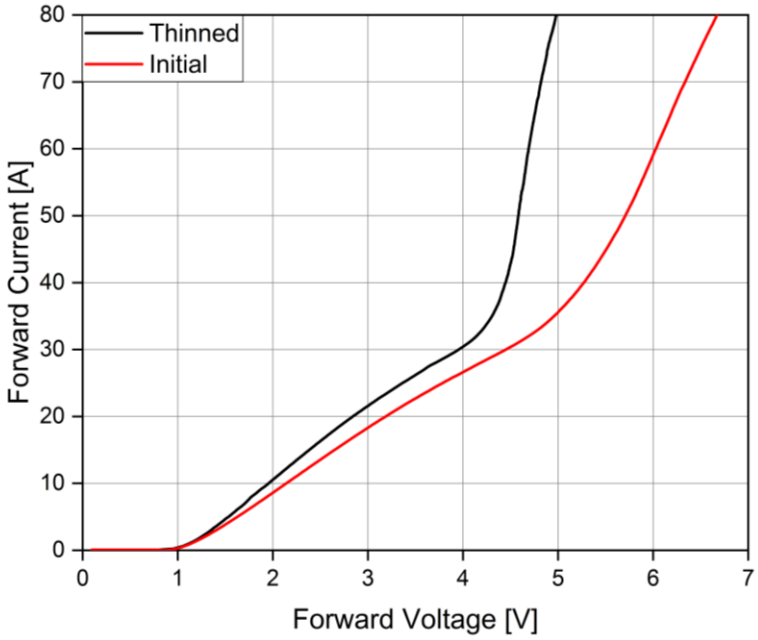
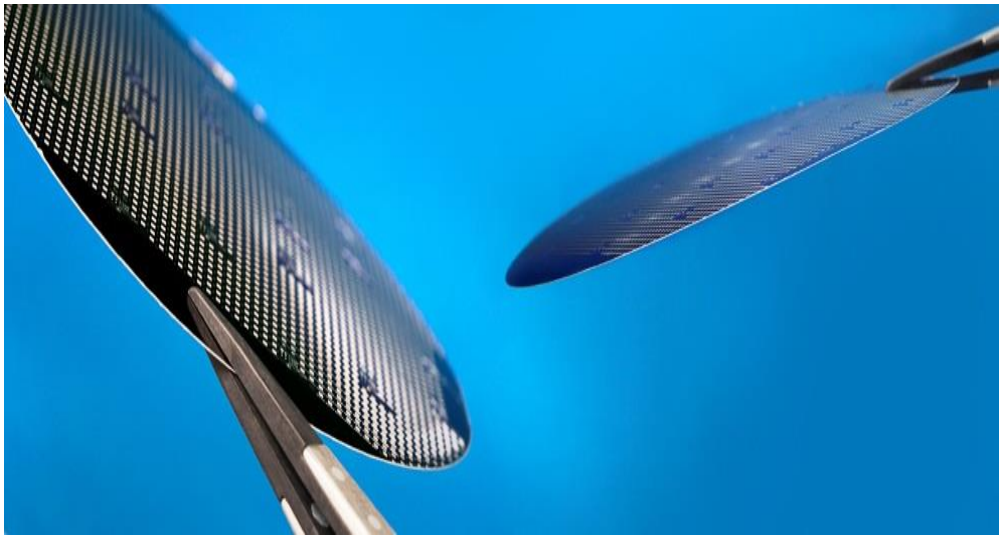
Resistance: substrate

Voltage	650 V	1200 V	1700 V	3300 V
Contribution to R_{DS}(on)	10.6%	8.8%	7.2%	2.6%



Forward characteristics of 6 A / 650 V SiC JBS diodes with and without substrate thinning



- Backside thinnig

→ decrease of substrate resistance

→ more challenging handling and processing of thin wafers

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Resistance: cell design

		Cell design		
		Stripe	Square	Hexagon
Integration coeff.	Channel	1	1.36	1.34
	JFET	1	1.73	1.74
	Source	1	0.46	0.45

- Higher integration coefficient

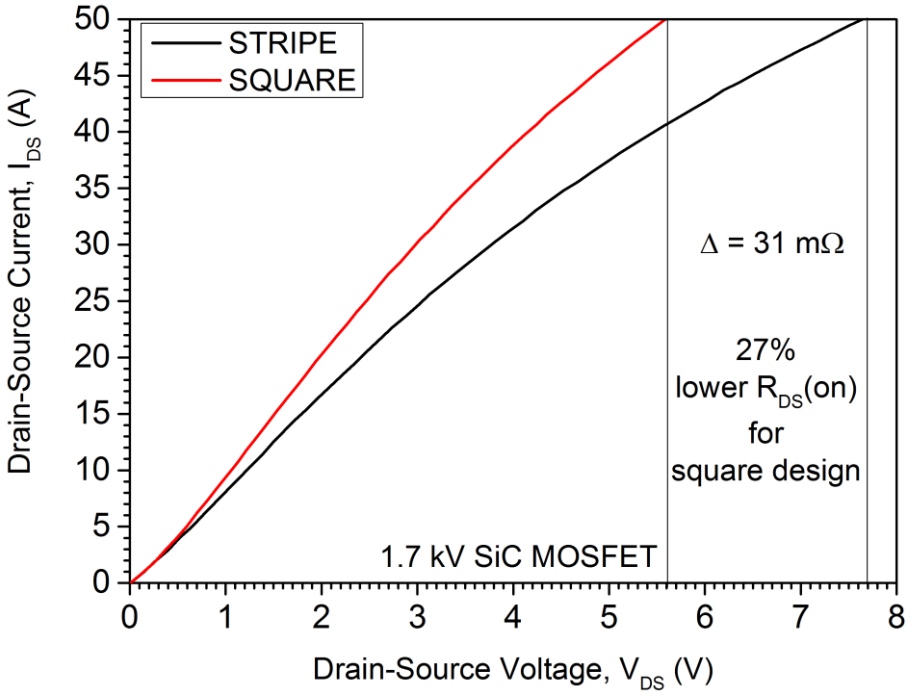
→ lower component resistance

- Square and hexagon design

→ lower total resistance

→ more challenging processing (e.g. lithography)

→ reliability issues (channel, JFET)



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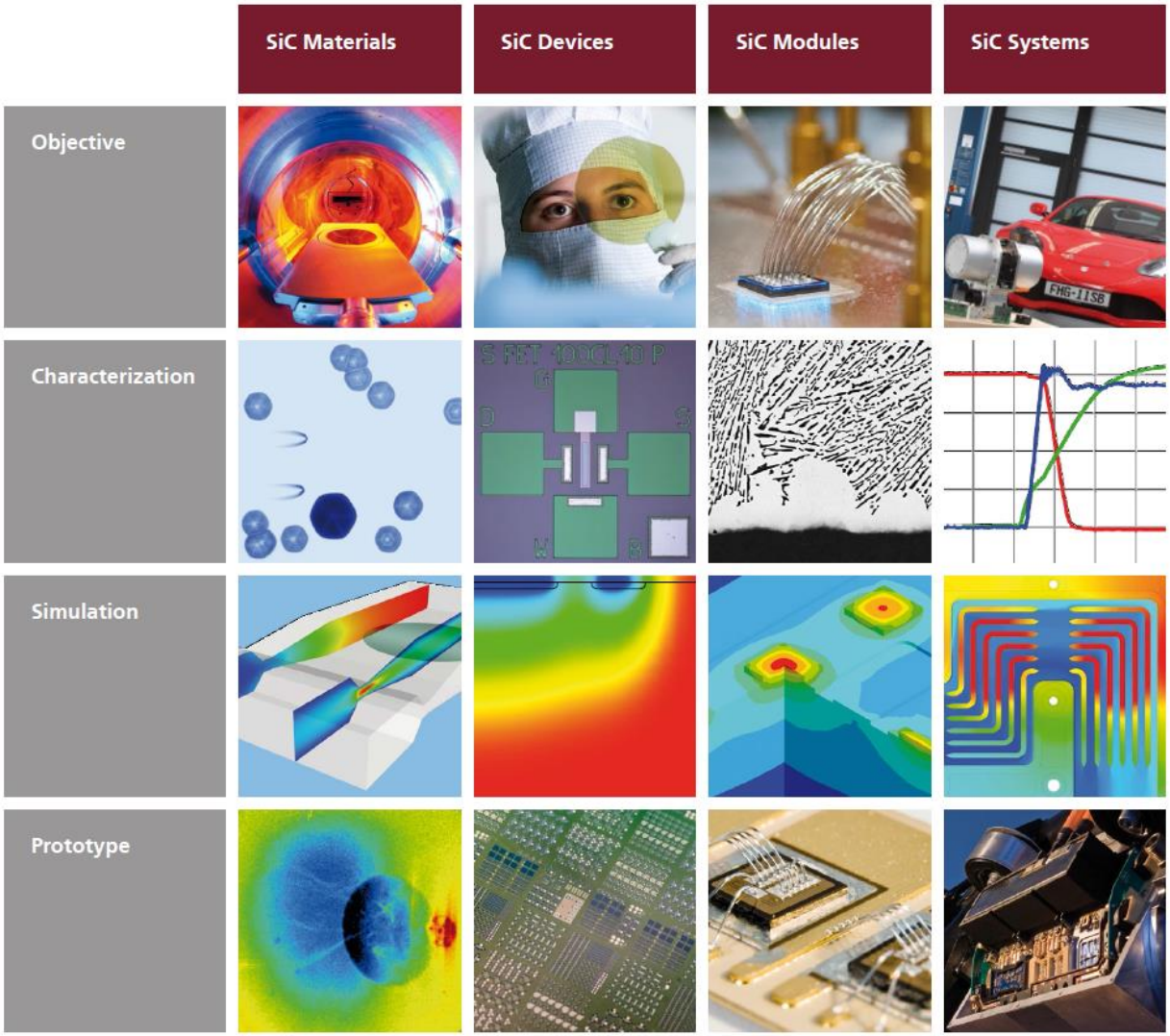
Summary

- Low on-state resistance of SiC Power MOSFET achievable by design and / or process optimization
- Dominant components of total on-state resistance dependent on the device blocking voltage
- Very low on-state resistance usually paid with lower reliability



SiC TOOL BOX

Thank you for attention

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