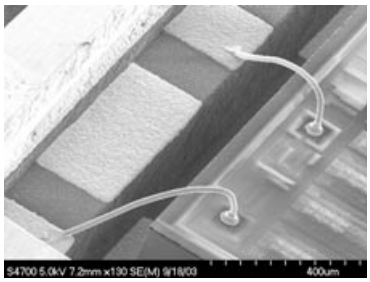
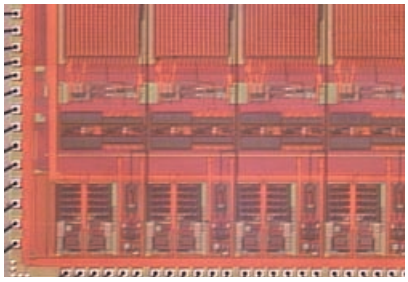
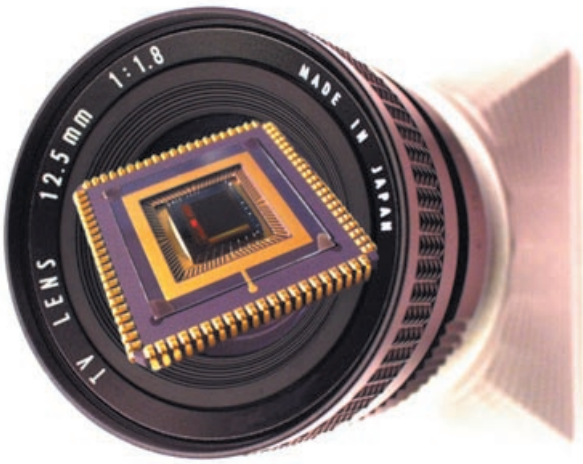
Fraunhofer Institut Mikroelektronische Schaltungen und Systeme

Annual Report 2003







Annual Report of the
Fraunhofer-Institut
für Mikroelektronische
Schaltungen und Systeme IMS
Duisburg
2003

Preface

During 2003, the 19th year of existence of IMS, application industry still had been very cautious with investment in innovative developments. This showed some influence in the quantitative development of our institute this year.

We managed to reach an annual turnover of more than 15 million Euros, the industrial revenues reached about 32 %. The volume of CMOS production could be stabilized at nearly last year's level.

Consequently, we did not augment our staff in these days, but concentrated in training our collaborators the most efficient way by intensive practice.

The good cooperation with "Fraunhofer Institute of Photonic Microsystems (IPMS)" in Dresden in the fields of ASIC production, test and mask fabrication turned out to remain an important factor of our concept. The detailed knowledge of each other and confidence has grown over the last 12 years, so the relation is very close and trustworthy.

The planning of the fourth section of our institute building had been completed during this year, we hope that the construction work will start in spring 2004.

In 2003 the biggest annual investment in our history was placed in our CMOS line for state of the art equipment. It was quite a challenge for our team, besides the continuous production in the existing CMOS line, to install the new equipment and bring it into operation. During the first half of 2004 we will switch from 6" to 8" wafers and start implementing an additional process with 0.25 µm structural width. So, beginning in the second half of the year, our customers will profit from the more rational way of our production and the smaller structural size of our

process. The bigger throughput will help customers with increasing mid-size volume requirements to be served in shorter terms.

In June 2003 our Smart Home "InHaus" was completed by the ceremonial opening of our Smart Garden with automated maintenance functionality. In November 2003 the periodical "InHaus-Forum" took place with participation of leading international companies in that field, and local and regional public authorities. Main topic this year was the combined marketing of new products and services by the partners.

Taking chance of our close neighbourhood to Dutch partners, we succeeded starting a EUREGIO-Project concerning "micro reactors" in autumn 2003.

In these days, the continuous confidence of our customers, business partners and public authorities is even more important for us, than in other years in the past. So we thank them, and also all our employees for their contributions to our work. Our future success will depend on their further R&D work in the fields of Microelectronics, Sensors, Wireless Chips and Systems.

Günter Zimmer
(Director of IMS)

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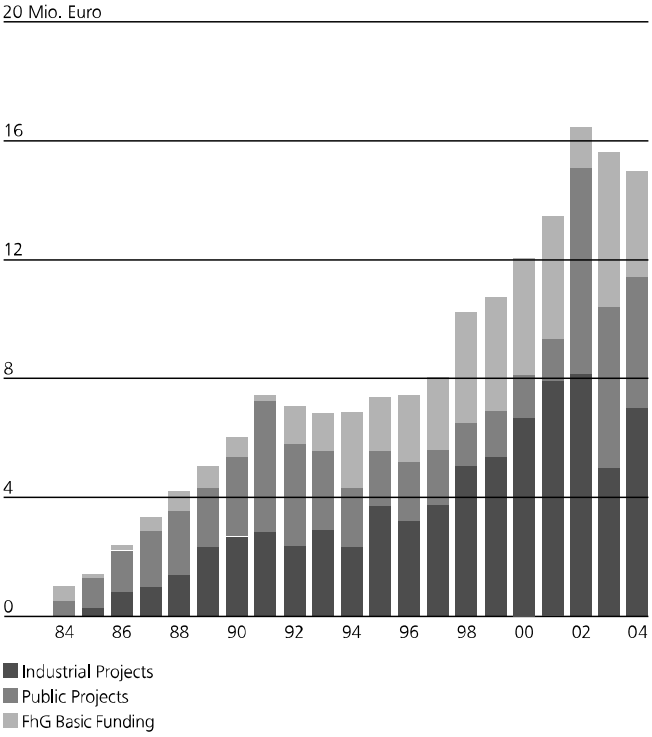

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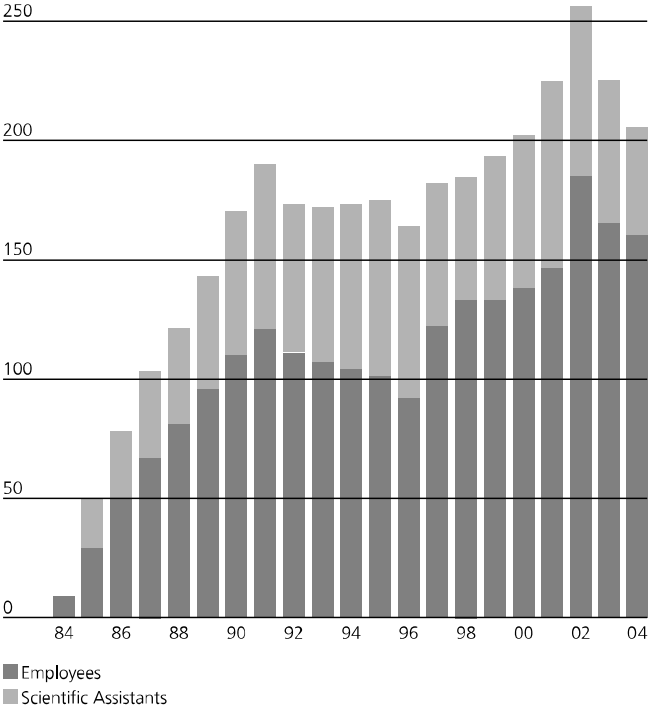

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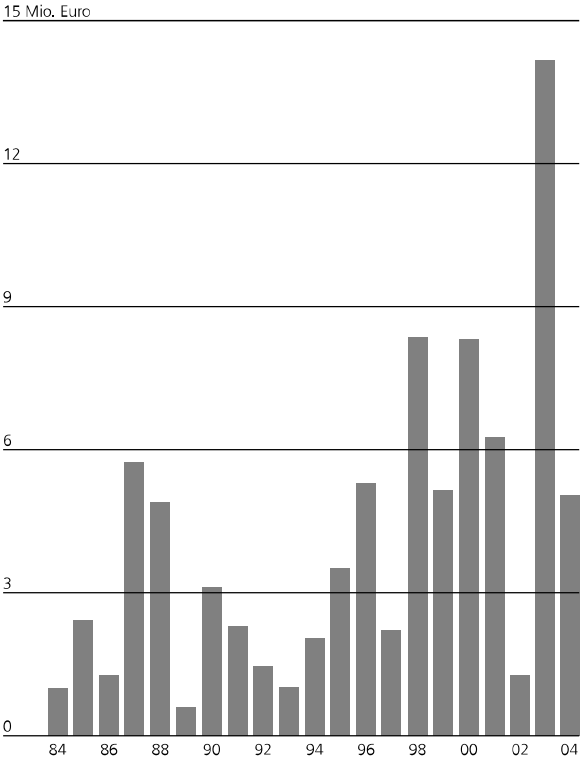

Selected Projects of the Year 2003

Production of Customer ICs at IMS

H. Vogt, U. Paschen

Introduction

IMS offers a broad spectrum of services in the field of microelectronics and micro electromechanical systems (MEMS). With several design departments the development of application specific integrated circuits (ASICs) can be realised according to the customer needs. In addition IMS also has the capability to fabricate these circuits with several advanced CMOS processes with volumes ranging from small numbers for prototypes up to medium volume production numbers.

Fabrication

IMS currently runs a fabrication line for wafers with a diameter of 150 mm. Recently, the cleanroom was expanded to about 1000 m^2 (see Figure 1), providing space for new equipment that increases the capacities both for production and technological R&D activities.

The basis of the IMS fabrication activities are CMOS processes, currently with a minimal structure size of 0,5 micron. Several process options and add-ons have been developed in order to increase the versatility of the IMS products. For example the processes offer options for special devices like high voltage transistors for interfacing with an electrical harsh environment. Also available are voltage independent capacitors and high resistance polysilicon enabling the realisation of analog and mixed signal circuits (that is the combination of analog and digital functionality on one chip), for example for highly demanding sensor signal processing. Another strong focus is the fabrication of optical sensors based on CMOS technology, e.g. high speed camera chips or camera chips with an extremely large sensitivity range. A further strength of IMS is an integrated pressure sensor, which can be fabricated together with CMOS circuitry in one process. Thus, the sensor can directly be integrated on one chip together with versatile electronics. This offers the possibility to realize complete sensor systems with extremely small size, including signal conditioning and communication electronics.

Typical applications of chips designed and fabricated at IMS cover a very broad spectrum, ranging from consumer products to highly demanding industrial fields.

Product examples are optical sensor ICs, smart labels for several applications, smart power ICs that combine "intelligent" logic functions with high power capability and integrated pressure sensors for medical, industrial and automotive applications as well as circuits with very specialised functionalities for specific customer applications.

Production volumes range from very few chips (MPC service) for the realisation of first prototype systems to small and medium volume fabrication. This flexibility makes IMS especially attractive for small and medium enterprises.

IMS has also upgraded its packaging capabilities. In order to offer the full production chain from silicon to packaged IC or module an automated packaging line for ceramic substrates or PCBs has been installed.

Outlook

In 2004 the IMS production line will be upgraded for the fabrication with 200 mm wafers, which will be a significant increase in production and R&D capacity. The larger usable area per wafer alone accounts for an increase of about 80 %. Due to the new

equipment several bottlenecks that limit wafer throughput today will be eliminated. Therefore, not only the wafersize increases but also the wafer fabrication capacity per year increases as well.

In addition to the upgrade to 200 mm wafers we will also install an industrial quarter micron CMOS process. This offers the possibility to realize very high density digital cores that together with analog functionality build the basis of intelligent analog systems and enables for example very small transponders or improved optical sensors. Also the application of advanced equipment with a minimum structure size of 250 nm offers new and exciting possibilities for new devices, for example very low resistance and highly robust power devices. Thus, this extension of IMS capabilities to smaller structure sizes together with increased production volume will secure and broaden the position of IMS as a developer and supplier of advanced products in the field of microelectronic circuits and systems.

Figure 1: Part of the cleanroom facilities at IMS

Active Defect Reduction Program at IMS

S. Linnenberg, J. Peter-Weidemann, B. Heinicke, U. Paschen

Introduction

In order to solve yield problems due to defects and to continuously increase the circuit yield, it is necessary to know the exact nature and cause of the defects. For this reason a stringent monitoring of defect occurrence is indispensable for all the critical process steps. At IMS an active defect reduction program is carried out for continuous yield improvement. While small defect levels and the highest possible yield are an important issue in any IC fabrication, extremely low defect densities are a mandatory requirement for very large chips like for example optical image sensors with chip areas of the order of square centimetres and more (figure 1). Most of the optical image sensors at IMS are manufactured in a 0,5 µm CMOS technology with 3 metal layers. For the planarisation of the intermetal oxides a CMP process is used. The contacts and vias are realized by tungsten plugs (tungsten deposition and back-etch). Because the small structure size and the large areas of image sensors put the highest demands on technology they are used here as an example, even though similar measures are carried out for other circuits and processes.

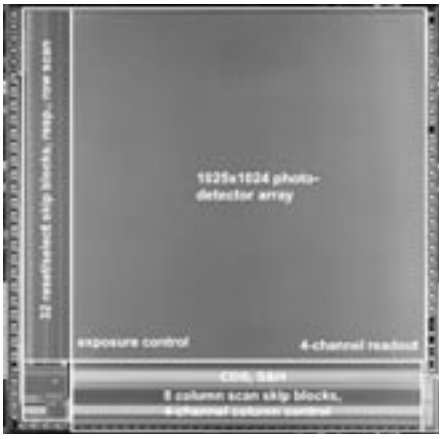

Figure 1: Example of a CMOS image sensor with 168 mm² chip area and 1025 by 1024 pixel

Active Defect Monitoring

In order to ensure a stable and high quality IC production in the IMS fabrication line, regular machine dependent particle generation tests are carried out. This keeps the overall defect level small. Beside these general machine dependent defects there is also a possibility of process dependent or even product dependent defects. In order to keep their level as low as possible a more exact investigation and active defect monitoring is employed.

For the automatic defect identification a WF-720 wafer inspection system from Orbot Instruments is used. This system works with Perspective Darkfield Imaging (PDI™) combined with pixel-by-pixel die-to-die comparison. The data obtained with this instrument are the basis for all further investigations and measures.
The defect coordinates are subsequently transferred to an inspection microscope INS 3000 from LEICA Microsystems whereby the defects can be analysed in detail. Thus, each defect can be classified and pictures of the defects can be stored for further reference.
For a more detailed investigation the defects can also be analysed in a Scanning Electron Microscope S-7800 H from HITACHI.

This defect monitoring is performed on all critical levels of the front end and back end fabrication of the 0,5 µm CMOS process (active area, poly level, tungsten levels, metal levels). The defect inspection system is capable to automatically recognize already observed defects of deeper levels, thus, simplifying the evaluation of the data significantly.

Some defects, like scratches due to handling problems of a machine, are easily identified and easily attributed to the critical process step. In other cases only a very thorough investigation can reveal the nature and the origin of the defects.
As an example figure 2 shows a defect in the metal level, which could be a cause for circuit failure if located between two metal lines with minimum distance.

The acquired defect data can be evaluated statistically with the program ®YIELD Manager from EGsoft, which allows for a versatile analysis, with respect to defect class, defect size and spatial distribution.

The analysis of the data revealed that a small number of process steps is responsible for most of the defects. Most of these defects are of very small size (approximately 1 μm^2) but this is still large enough to make then a potential source of electrical failures in submicron technologies.

Since each defect is stored with defect position, observation-level, defect type and defect size, it is possible to compare the results of the electrical circuit test of the image sensors with the defect monitoring data. Thus, specific pixel, line or column failures can be directly attributed to individual defects. Additional methods like liquid crystal measurements can also be employed to localise the position where the malfunction occurs. This comparison of the electrical circuit test data with the defect monitoring data is an important step of the active defect monitoring.

Taking all these information into account the critical process steps can be identified and subsequently be optimised, thus ensuring a continuous improvement of yield and quality.

Discussion and Conclusions

With the help of specialised automated defect inspection tools and a continuous program to identify critical process steps and optimise them even very demanding circuits with submicron structure size and very large chip areas can be fabricated with high quality and yield.

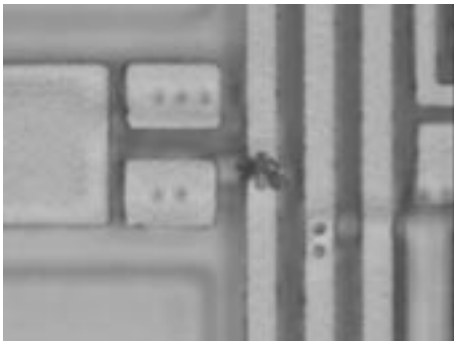

Figure 2: Example of a defect in the metal level

Turn-key Assembly of Integrated Pressure Sensors

O. Köster, H. K. Trieu

1. Introduction

The continuing demand for sensor products with higher performance, light weight and small dimensions is requiring levels of package performance of microelectromechanical devices that were not attainable by the molded plastic and ceramic packages of the past decade. Portable devices and cost effectiveness are strong drivers of packaging technologies for sensor products. Pressure sensor systems with minor temperature drift and small form factor, i. e. calibrated pressure sensors within miniaturized housings, will play a major role. For example altimeters and barometers are already incorporated in clocks and pocket knives [1; 2]. In order to provide its customers with a turn-key solution, FhG-IMS Duisburg has built a fabrication line for test, calibration and assembly of integrated pressure sensors. The chosen housings are CLCC8 with the outer dimensions of 5 x 5 x 1.7 mm^3.

2. Wafer level Calibration of integrated Pressure Sensors

IMS has set up a method for wafer level calibration of integrated surface micromachined absolute pressure sensors in the low pressure range [3 - 6]. The necessary equipment for sensor calibration has been added to a standard test arrangement for microelectronic circuit testing consisting of an automatic waferprober EG2010 from Electroglass Corportion, USA, and a test system M3610 from SZ Testsysteme AG, Amerang, Germany (figure 1). The waferprober is connected to the serial interface of the workstation of the test system. Thus, the pressure sensor calibration is performed at the same time as the circuit test. In order to apply different pressures to the chips the conventional probe card has been modified to get a miniaturized pressure chamber (figure 2).

The wafer level pressure sensor calibration is performed at discrete temperatures and at three different applied pressures at each applied temperature. The chamber pressure is switched rapidly via valves. The chamber pressure is measured by means of a calibrated reference pressure gauge. All data from the test runs are stored in a data file. Finally the calibration coefficients are calculated and then directly stored within the integrated EEPROM of the pressure sensor. At the same time calibration coefficients for an integrated temperature sensor may also be calculated and stored. Then the bad dice will be marked with an ink dot and the wafer is subsequently forwarded to the assembly line.

Figure 1: Wafer level calibration system

3. Chip Assembly

Figure 3 depicts the assembly process flow. The whole assembly line is set up for cassette-to-cassette operation. Each cassette contains 20 Auer-Boats, whereas each Auer-Boat takes up 42 pressure sensors. Die bonding and lid attach is performed at a fully automated standard Die Bonder ESEC 2007. Wire bonding is performed at a fully automated standard Ball-Wedge Wire Bonder ESEC 3088. In figure 4 an X-ray microphotograph of a bonded pressure sensor in a CLCC8 housing is shown. The final functional test and subsequently the packaging within "Tape&Reel" is performed by a custom specific machine from Fritsch GmbH. Figure 5 depicts the top and rear side view of a barometric sensor. The pressure conveyance is realized from the side walls. To our knowledge this integrated pressure sensor has got the smallest dimensions all over the world.

4. Summary

The presented approach for an wafer level calibration of micromachined pressure sensors has already achieved high accuracy. In addition, the outlined test system may as well be used for wafer level quality control of pressure sensors and pre-selection prior to assembly. The assembly line is currently in the ramp-up phase. The equipment was chosen for a planned throughput of several million sensors per year.

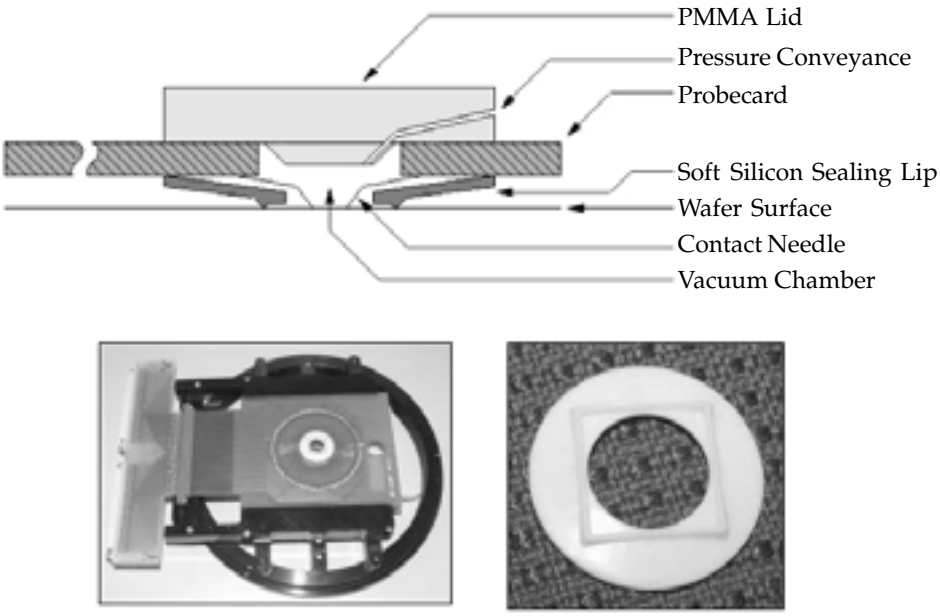

Figure 2: Sketch of modified probe card

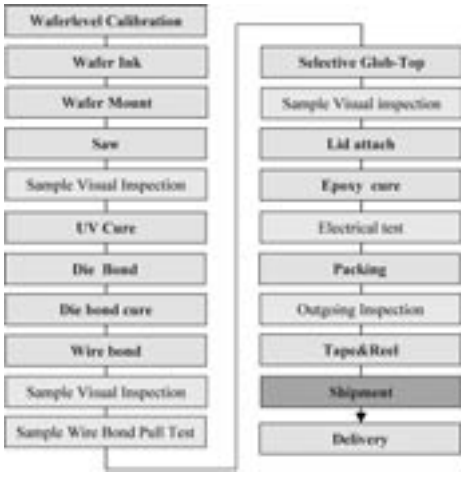

Figure 3: Summarized assembly processflow

Figure 4: X-ray microphotograph of a bonded pressure sensor

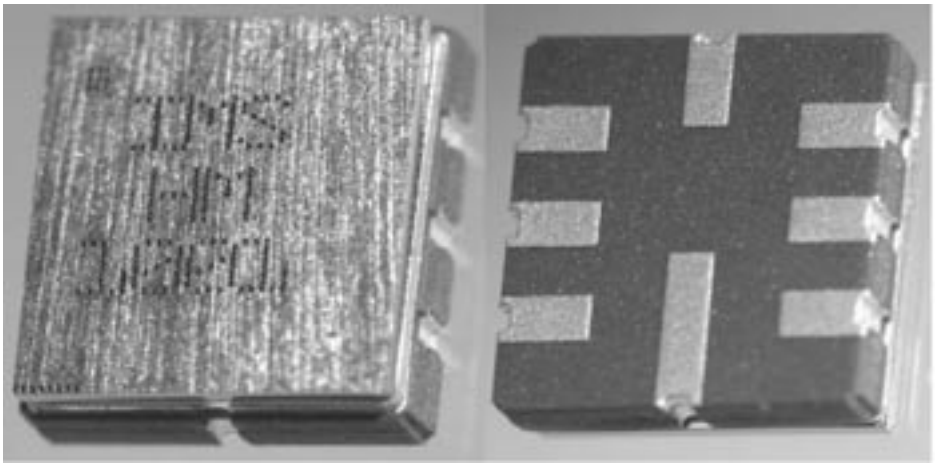

Figure 5: Ultra small packaged integrated pressure sensor

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CMOS-Based Detectors for Optical Communications and Mass Storage

I. Hehemann, A. Kemna

Introduction

Today the area of mass storage and optical communications represents a high volume market with increasing potential for the future. In 2002, for example, 31.5 Mio. DVD players were sold worldwide, and, considering the increasing storage needs and upcoming products, higher sales figures are predicted for the next years. Furthermore, although there is a trend towards systems on chip, a steady growth of the data transfer on board level and the short-haul can be observed. Due to the limited data rate of wire line transmission systems, caused by cross-talk phenomena, reflections, and the damping behaviour, this type of communication will be performed optically in the future. At latest with the use of optical communication systems within PC systems, an enormous increase of this market will occur.

Although the CMOS technology is the technology of choice for commercial products, the vast majority of photo detectors for both applications is based on BiCMOS-, III/V, or hybrid technologies. This is due to the fact that early systems were based on light of the infrared spectrum which is difficult to detect with CMOS based sensors. However, in the field of optical storage as well as in the short-haul optical communication the tendency goes towards shorter wavelengths of the visible spectrum. In the first case this trend is pushed by the inherent increase of the storage capacity, in the latter case by the availability of low cost light sources and the fact that for short distances the damping behaviour of fibres is negligible [1, 2]. Since light of the wavelength region from 400 nm to 800 nm can be detected with CMOS-based detectors, the use of that technology is desirable for the implementation of low cost components.

Photodiodes for the visible light spectrum

Up to now, integrated optical detectors have mainly been used for applications where the input signal bandwidth is in the kilohertz range, e. g. imagers or x-ray detectors. Due to this, the frequency behaviour of CMOS photodiodes could generally be neglected. With the applications aimed at here, signal bandwidths of some hundred Megahertz have to be processed so that the photodiode bandwidth plays a significant role.

For the investigation of the behaviour of photodiodes device simulations as well as analytical calculations that allow

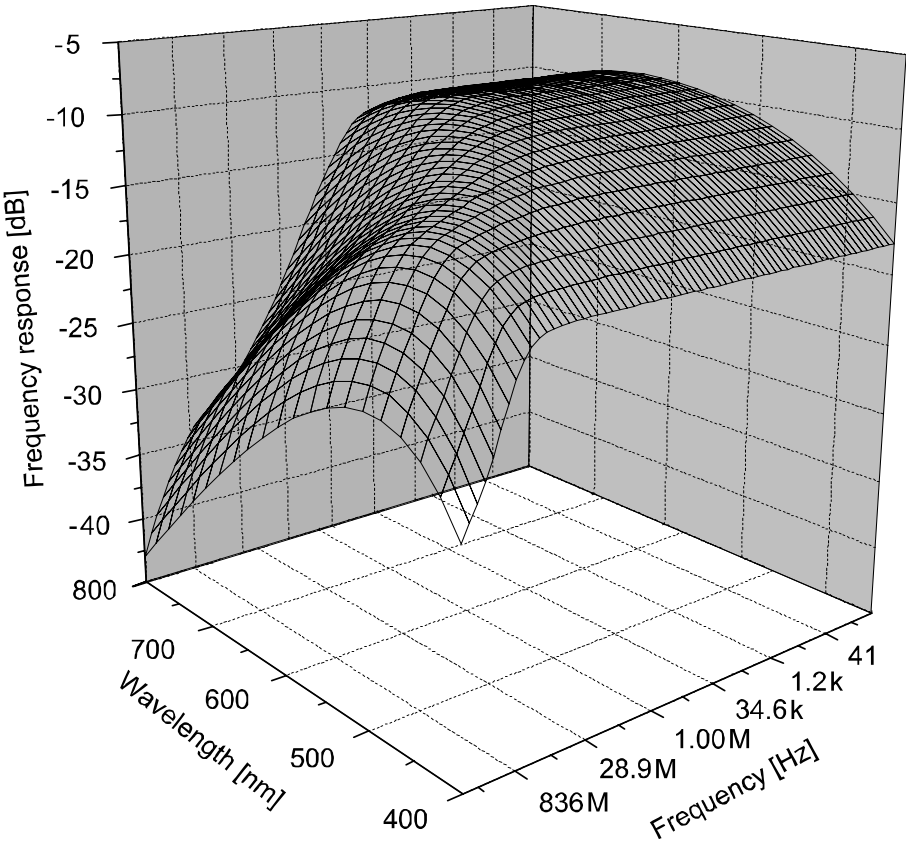

Figure 1: Frequency plot of the spectral responsivity of a vertical pn-junction (normalized by 1 A/W).

to evaluate the influence of different process parameters are used. Figure 1 shows the calculated frequency behaviour of the spectral responsivity in dependence of the stimulating wavelength of a vertical pn-junction. Due to the different penetration depth of the radiation into silicon at different wavelengths, the contribution of drifting and diffusing charges to the overall photocurrent varies. This causes a heavy dependence of the bandwidth on the wavelength yielding values from several Megahertz for the near infrared going up to almost one Gigahertz for the near ultraviolet.

For the characterization of test structures a hybrid measurement method has been developed (see Figure 2). To process the photocurrent a discrete transimpedance amplifier with sufficient bandwidth is contacted to the wafer using microwave probes, the stimulation is done employing fibre coupled laser diodes with wavelengths relevant for optical storage systems, namely 785 nm (CD-ROM), 670 nm (DVD), 405 nm (Blu-ray). Measurements have shown that for both applications mentioned above photodiodes with sufficient performance are realizable in the C0512 IMS CMOS technology.

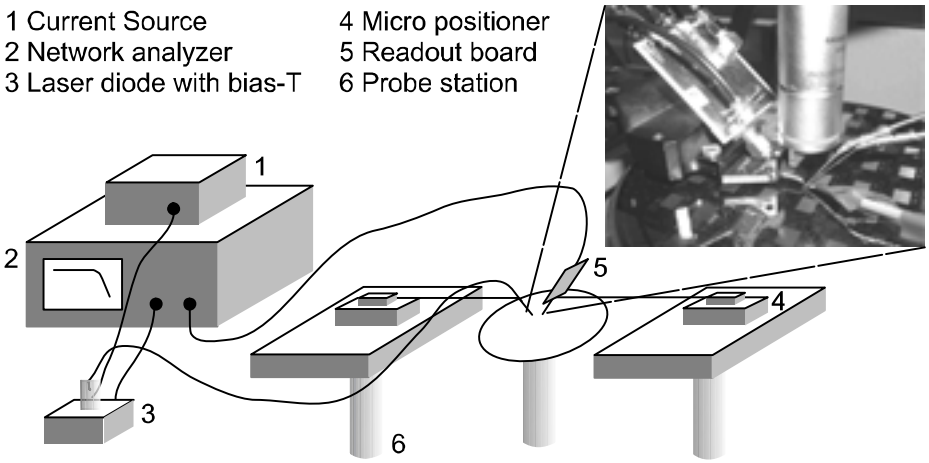

Figure 2: Measurement setup for transient characterization of photodiodes.

Readout Circuits

The readout circuits for both sorts of detectors have to meet hard specifications concerning gain, bandwidth, and noise requirements. To implement circuits with sufficient performance, a detailed analysis of the transimpedance amplifier configuration was carried out and ways for its optimisation have been developed.

Different novel circuit topologies have been investigated. For the field of optical communication a transimpedance amplifier suitable for SONET STS-24 has been realized. Including the photodiode on-chip, the circuit exhibits a transimpedance gain of 64.2 dBΩ, a bandwidth of 680 MHz, and a sensitivity of -15.1 dBm at 405 nm wavelength.

The feedforward concept has been employed to realize transimpedance amplifiers suitable for the use within detectors for optical storage systems. Using this approach, circuits with improved noise behaviour and power consumption could be implemented. A transimpedance gain of 96.0dbΩ, a bandwidth of 83.7 MHz, and an equivalent input noise current of 8.49 nArms while dissipating a power of only 1.73 mW was achieved with a two stage architecture, for example. Furthermore, by using the bootstrapping concept, performance values above what is achievable with the standard transimpedance amplifier configuration have been obtained. In this way a circuit that reads out a photodiode with 4 pF additional capacitance with a gain of 95.86 dBΩ and a bandwidth of 75.4 MHz was realized (Figure 3).

Advanced Detectors for optical storage systems

Detectors for optical storage systems usually are simple multi quadrant structures. They provide only spare information about the impinging light signal so that the performance of the signal processing algorithms is low. This results in the need for high quality optical components and cost intensive alignment steps during the fabrication of the systems.

To improve the functionality of such detectors a novel structure has been developed that in-situ combines demodulating and integrating readout approaches (Figure 4) [3]. This allows to extend the information gained in the low frequency spectrum without disturbing the structure for demodulation needed to meet existing standards. The additional data can be used to improve the signal processing, finally leading to a cost reduction for the overall system.

Conclusions

The feasibility of fast and highly sensitive, fully integrated optoelectronic circuits in a CMOS technology has been shown. Furthermore, a novel detector architecture for optical storage systems has been implemented and successfully tested. Current work is dealing with investigations concerning the integration of this detector in a system and the perspective of CMOS technologies for spatial division multiplexed optical communications.

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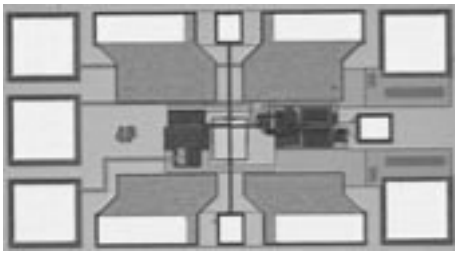

Figure 3: Chip micrograph of a bootstrapping transimpedance amplifier.

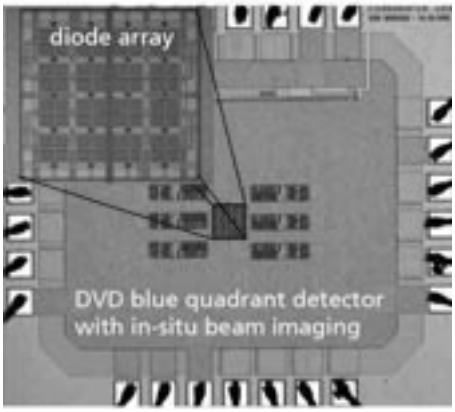

Figure 4: Chip micrograph of a detector with combined integrating and demodulating readout.

Dependable Sensor Systems

Dr. D. Weiler

Introduction

Smart sensors play a critical role in many applications. While in general sensor failure can cause machine damage or inferior product quality, many sensors are employed in safety-critical applications and their failure could cause injury or even death of humans [1]. A second argument for error detection of sensor elements are costs. After fabrication a functionality test follows. To test the full functionality often a complete assembly including the cost expensive packaging is necessary to enable the non-electrical stimulation for full sensor testing. There is a great potential of cost savings if the assembly of defective sensor systems could be avoided by using a test on wafer level. Hence, there is a great need for dependable sensor systems. The presented concept of detection of faulty sensor elements is the key part of a dependable smart sensor system (Figure 1) [2].

A dependable sensor system contains error detection, error analysis, error removal, and error indication functions.

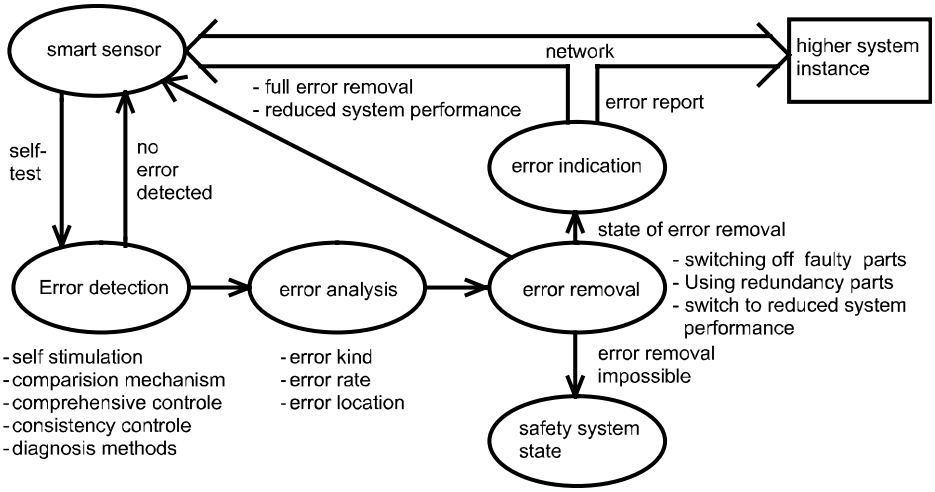

Figure 1: State diagram of a dependable sensor system

The error detection must be developed under aspects of real-time capability and economical costs. If an error occurs the error analysis determines the error type, error rate, and error location for the following error removal. The aim of a dependable sensor system development is to obtain a sensor functionality even in the case of a fault. If a full error removal is not possible a mild or partial performance degradation can be the result if acceptable. If he error removal not possible the system has to reach its safety state. The state of the error removal must be reported to higher system instances.

Error Detection Concept

The error detection plays the key role in a dependable sensor systems because sensor elements are usually exposed to rough environments, no conventional self-testing strategy for non-electrical stimulation is available, and because possible sensor errors may appear "hidden" by the following signal processing. Conventional error detection methods are based on redundancy, evaluation of mathematical models of the observed process, or knowledge-based models. Use of redundancy incurs additional costs and fails when common mode failures occur. Mathematic models have problems with model uncertainties and robust detection and need complex algorithms which cannot be implemented economically in smart sensors.

Our error detection is based on electrical self-stimulation of the sensor element combined with matched filtering for detection of the stimulation. Figure 2 shows the block diagram of the error detection method.

The non-electrical quantity x interacts with the sensor element and is conver-

ted into an electrical signal $s_{SE}(t)$. This signal is read out and digitized using a $\sum\Delta$-modulator. This sensor system is complemented by the error detector containing a PRBS-generator, a stimulating device, a matched filter, and a threshold comparator.

A PRBS-generator creates an additional stimulus for the sensor element. Therefore the stimulation device interacts directly or indirectly by using cross-sensitivity of the sensor element. Stimulation devices can be resistors for thermal stimulation, coils for magnetic stimulation, or plates for electrostatic stimulation.

In a defect-free sensor system the PRBS can be detected at the output signal of the system. Under the assumption that the stimulation frequency f_{Stim} is lower than the corner frequency of the sensor system f_{sensor}, the PRBS appears at the output of the sensor system only attentuated by a factor ε_{Stim}. The output of the sensor system is fed into the matched filter, which is used to detect the PRBS. A matched filter reduces the amplitude of the stimulation to be detected. Only a small stimulation amplitude V_0 allows an on-line error detection with a minimum disturbance of the measurement of the non-electrical quantity x. The output of the matched filter is sampled every $n \cdot T_0$ times, when the correlation peak occurs. The last part of the error detection concept is a threshold comparator which compares the sampled matched filter output to a prescribed threshold C. According to the value of the sampled output the error status is determined. Zero values indicate a defect of the sensor element or of the $\sum\Delta$-modulator, while values between zero and the prescribed threshold C indicate a reduced sensitivity of the sensor element. In the case of values greater than the prescribed threshold C the sensor system is defect-free.

Using correlation technique the probability for a false alarm $P_{e,\,min}$ depends only of the signal/noise ratio SNR, which is the quotient between the stimulation energy E_{stim} and the noise density N_0 at the output of the matched filter.

System Realization

To prove the functionality of the error detection a temperature sensor as an example for a sensor system has been realized. The sensor system consists of a temperature sensor element and a first order $\sum\Delta$-modulator. The temperature sensor contains of lateral PNP bipolar transistors with different emitter areas [3]. A positive temperature coefficient derived from the difference of the base-emitter voltage of these transistors is converted by the $\sum\Delta$-modulators into a pulse density binary stream. The analog/digital converter based on the $\sum\Delta$-principle achieves a high signal-to-noise ratio (SNR) by combining oversampling, interpolation, and noise-shaping while dispensing of the need

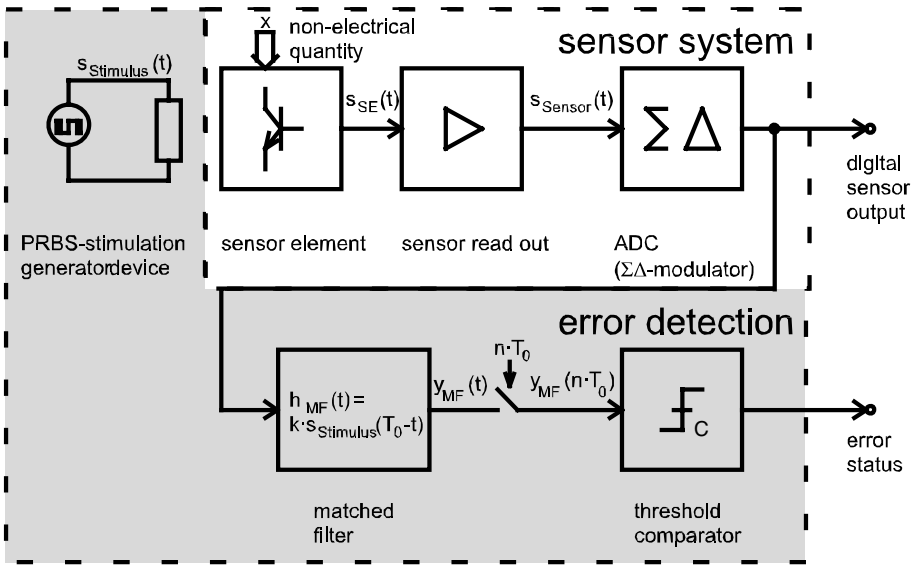

Figure 2: Block diagram of the error detection

of high precision analog components [4]. ∑Δ-modulators rely on the noise spectrum of coarsely quantized input signal being shaped and shifted out of the signal band to higher frequencies to achieve fine quantization. The ADC consists of the ∑Δ-modulator followed by a decimator. This sensor system is complemented by the error detector containing a PRBS-generator, a heating source as the stimulator, a matched-filter, and a threshold comparator. The pseudo random binary sequence is derived from irreducible codes (m-sequences) using feedback shift registers [5]. The characteristical polynomial used for the PRBS with a period of 7 is:

$$P(x) = X^3 + x + 1.$$

To avoid a temperature dependence of the threshold of the sampled matched filter output a PRBS with same number of "0" and "1" is needed. Generators using m-sequences generate an odd-number length of the PRBS, so we use for the first half of the PRBS the non-inverting and for the second part the inverted m-sequence thus obtaining a sequence with the PRBS length of 14. Due to the low-pass character of the heat propagation in the silicon substrate we use a pulse length of $T_{pulse} = 5s$. Using a length of the PRBS of 14 every 70s is the error status updated. A resistor acts as the heating source modulated with the PRBS which converts the electrical power into a temperature variation ΔT_{heat} of the sensor system. The matched filter has been realized as a correlator consisting of a multiplier and an integrator. Both inputs of the matched filter are digital so there is a simple realization of the correlator using an EXOR-gate for the multiplication of the two input signals $s_{\Sigma\Delta}(t)$ and $s_{PRBS}(t)$ and an up/down-counter for the integration. If both input signals are equal the counter counts up and if they are not equal the counter counts down. At the end of the PRBS the counter is read out and its value is compared to the threshold C.

The sensor system has being fabricated in a standard 1.2 µm n-well silicon-gate CMOS technology (Figure 3). The die area of the chip is ca. 5.7 mm². Comparing to the same temperature sensor without any error detecting the area has increased by 0.52 mm² due the PRBS generator, the matched filter, and the threshold decision circuitry. The polysilicon heating resistor has been placed near the bipolar PNP transistors without an additional area consumption.

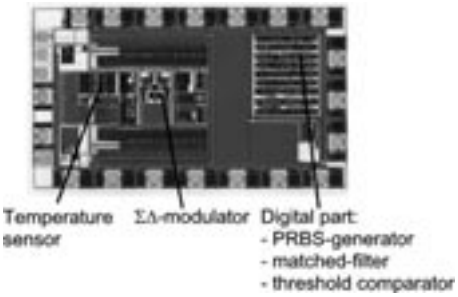

Figure 3: Chip photo of the temperature sensor including error detection

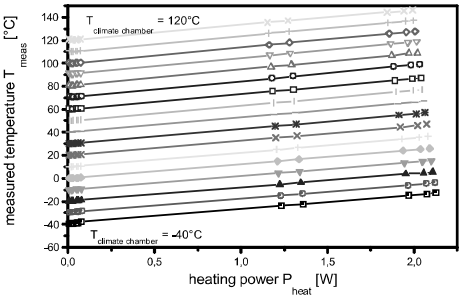

Figure 4: Temperature change caused by a constant heating power

Measurement results

The output of the integrated temperature sensor system is a binary pulse density stream generated by the ∑Δ-modulator. The pulse density exhibits a linear dependence on the temperature with a relatively low slope of 0.3 %/°C due to special requirements of the application for the temperature sensor. When stimulated the heating resistor converts the electrical power Pheat into a temperature change ΔT_{heat} of the temperature sensor. The temperature change for a constant heating power for different ambient temperatures in the range between -40 °C and 120 °C is shown in Figure 4:
The measured temperature T_{meas} rises linearly with the constant heating power P_{heat}. The measured conversion factor is $R_{th} = 9$ °C/W. This means that for a temperature rise of ΔTheat = 1.0 °C an electrical power of $P_{heat} \approx 0.11$ W is needed. By optimizing the design of the heating resistor we aim to reduce the electrical power needed to stimulate.

For the error detection the temperature sensor is stimulated by applying the PRBS to the heating resistor. The samp-

led matched filter output shows Figure 5 for different heating power values.

In the case of an faulty sensor the sampled output is around zero, i. e. $y_{MF}(nT_0) = 0$, which is independent of the temperature. In the case of an operating temperature sensor cases the pseudo random stimulation causes a sampled output of the matched filter to be much greater than zero. By using a heating power of 0.1 W the difference between operating an faulty temperature sensor is ca. 900. This threshold is easy to detect and yields a negligable false alarm rate. The stimulation using a heating power of $P_{heat} = 0.1$ W results in a temperature raise of ca. $\Delta T_{heat} = 1$ °C which is small enough not to disturb the temperature measurement. The described error detection method is so powerful that a change of 0.3 % of the pulse density of the $\sum\Delta$-modulator can be surely detected.

Conclusion

We have presented an error detection concept based on pseudo random stimulation of the sensor element and detection of the stimulation using a matched filter. The concept has been realized using a temperature sensor as an example of the sensor element. The functionality of the error detection method has been proven. With this method it is also possible to determine the sensitivity of the sensor element. The output signal of the system yields a digitized sensor signal. When using electrical or magnetic fields for stimulation a wide variety of sensor elements can be stimulated and in this way a dependable sensor system with error detection can be implemented. Our next goal is to use this error detection method with a capacitive pressure sensor and apply an electrostatic stimulation.

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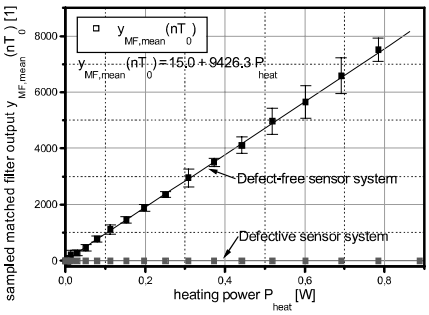

Figure 5: Sampled matched-filter output

CMOS Line Image Sensors in the FhG-IMS

A. Kemna, W. Brockherde

1. Introduction

Linear image sensors are used in numerous commercial and industrial applications, e.g., bar code readers, line cameras, scanners, copiers, facsimile machines, and optical range sensors.

The classical approach to the realization of such arrays is based on using one-dimensional CCD arrays. This technique has matured during the last 25 years and CCD users got accustomed to their limitations in resolution, dynamic range, temperature behaviour, and the complex interfacing. Though the first silicon image sensor was fabricated in a MOS process this approach has been neglected by image sensor developers. But today's submicron CMOS processes can compete with CCDs in performance and offer a lot of additional features: wide temperature range, random pixel access, and, above all, the possibility of cointegration of complex electronic circuitry in a standard CMOS process.

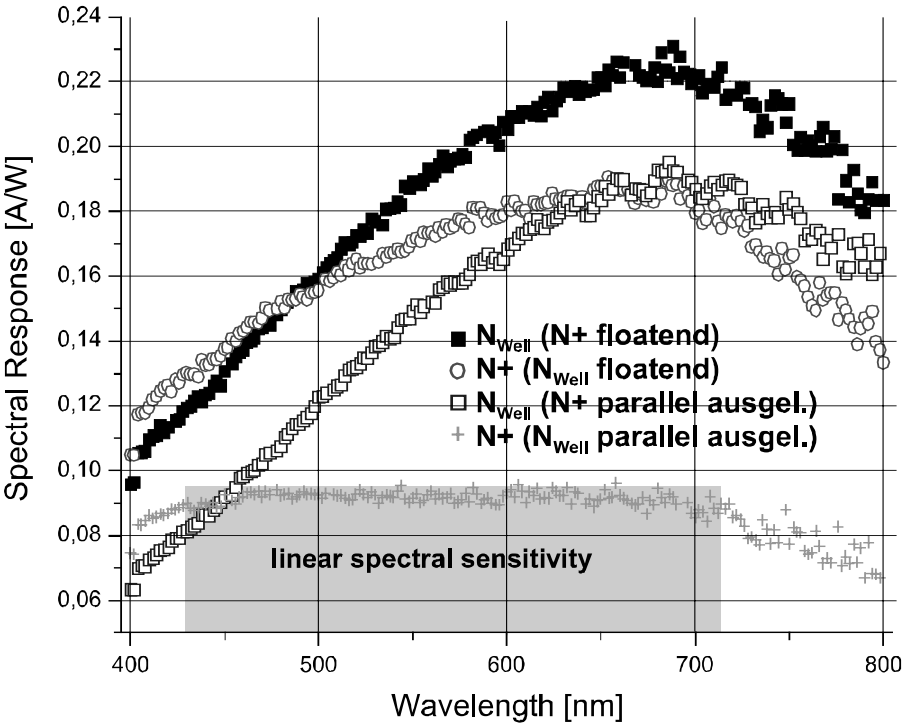

Figure 1: Layout-Optimization for linear spectral response of N+/P-Substrate photodiodes

2. Photdetector Devices

In CMOS area imagers mainly standard photodiodes are used as light sensing elements. Photodiodes can be formed by any combination of P- an N-type layers. Due to the wide varieties of pn-junction and layout variations available in a standard CMOS process the photodiodes can be particularly optimised for many parameters e.g. spectral sensitivity, dark current, detector capacitance, low noise, and high speed [1, 2]. As an example the layout linearization of the photodiode spectral sensitivity is shown in Figure 1.

Another photo sensing element which is very attractive for line sensor application too: the photo MOSFET device which is formed by a standard PMOS transistor located in a floating n-well (Figure 2). Even though the phototransistor can not be particularly optimised for such a wide variety of parameters, the element exhibits extremely high photosensitivity and dynamic range. It can be operate up to several 1000 A/W at low irradiation levels due to intrinsic transistor amplification. The device exhibits a wide temperature range (min. -40 °C to +125 °C) and the minimum detectable illumination is below 1 mlx.

Both photodetector devices enable arbitrary pixel geometry and the realization of smart photodetector arrays by CMOS integration of functional blocks, like random pixel access, noise reduction and signal processing blocks as well as on chip analog-to-digital conversion.

3. IMS CMOS Line Sensors

To demonstrate the performance and the enormous potential of this sensor

type we developed and fabricated various CMOS line sensor ICs.

3.1 Fast edge extraction sensor

In Figure 3 a circuit schematic of a CMOS linear photosensor array with fast on-chip edge extraction is shown. It features a 1-D array connected to a distributed resistive lattice network that approximates a spatial Gaussian low-pass filter. Resistors R_1 and R_2 determine the spatial corner frequency and signal gain. Since highly sensitive photo-MOS transistors are used instead of photo-diodes, the resistor values can be low and their size is small. For the lateral resistors we have employed tunable resistors based on N-type native MOS transistors operating in the linear region. This enables programmable sequential lowpass filtering of the acquired image at two different spatial frequencies during two subsequent clock phases [3]. An auto-zeroed comparator creates the digital difference signal: the entire operation corresponds to on-chip spatial bandpass filtering followed by a binarization operation and serves to extract edges in images. In addition to the information about edge location, the gradient direction of the edge is also available as a binary signal at the output. A monitoring photosensor array thas uses time-integrated current readout has been laid out in parallel to the edge extraction array in order to enable monitoring of the acquired images without filtering. The 64 pixel edge extraction sensor with a 52 µm pixel pitch has been realized in 1.5 µm double metal n-well CMOS technology and occupies a silicon area of 7.7 mm² including the 64 pixel monitor line (Figure 4). The chip needs a single 5 Volt supply and at a readout clock frequency of 16 MHz, a complete edge extraction takes 8 µs. The fixed-pattern noise (FPN) was measured to be about 0.6 %.

The inclusion of median filters and non linear filter functions are promising further improvements in edge detection performance in the future.

3.2 2048 pixel line sensor

The chip photomicrograph of a second example is shown in Figure 5. The device is a 2048 pixel line sensor with 15 µm pixel pitch employing the photo MOSFET as sensing element. Since the 2048 pixel sensor with a pixel pitch of 15 µm exceed the standard size of a reticle used for lithography during wafer processing, 9 submasks, one for each corner, one for each side and a centre mask are stitched together forming a line sensor 31.4 mm x 3.7 mm of size. Stitching technology is well established in the FhG-IMS. No yield reduction could be observed in addition to the normal chip area determined yield figures.

The device features random block access for fast readout of "regions of interest", dark current compensation, and internal temperature compensation. High photosensitivity, low FPN, and a temperature range of -40 to +125 °C are also important properties. With

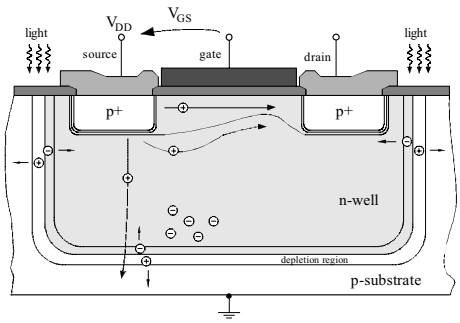

Figure 2: Cross section of photosensitive PMOS Transistor

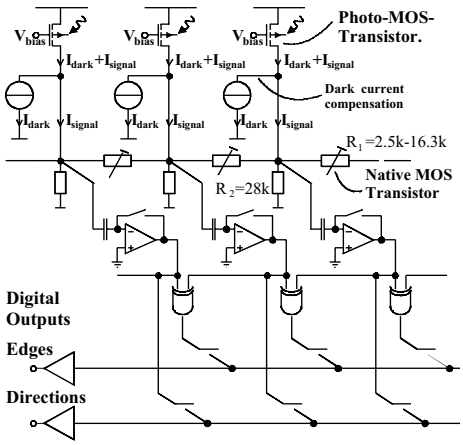

Figure 3: Schematic of edge detection circuit

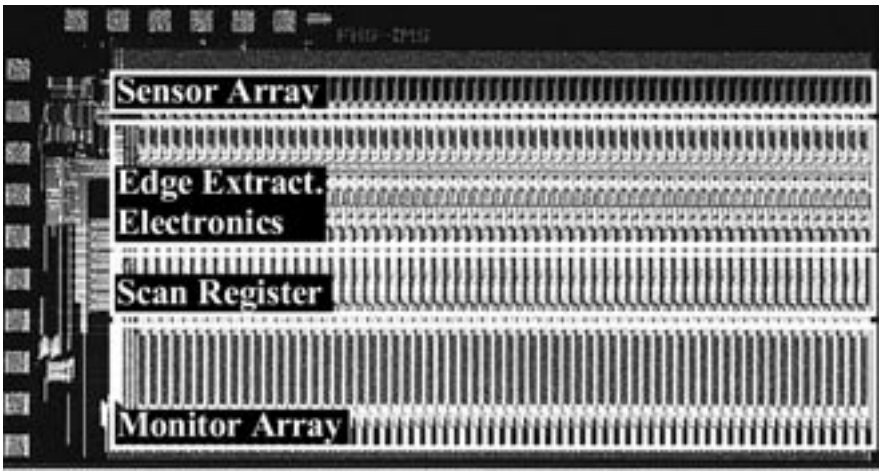

Figure 4: Chip photomicrograph of the CMOS linear photosensor array with edge extraction

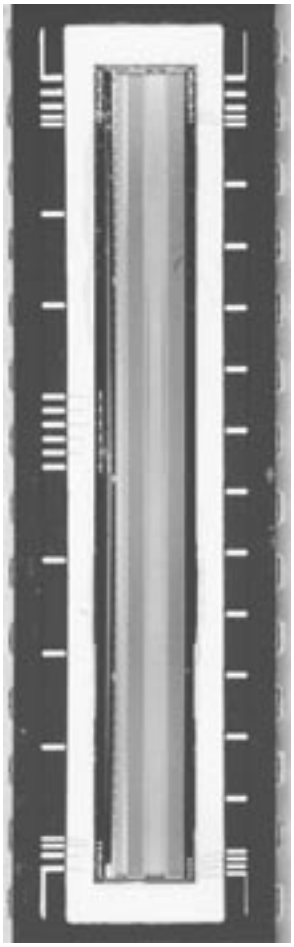

Figure 5: Chip micrograph of 2048 pixel line sensor

variation of the integration time between a few microseconds and several seconds, the chip covers a dynamic illumination range of 177 dB (Figure 6, [4]). Interfacing the sensor is quite simple since it uses a single 5 V supply and a single external clock (up to 10 MHz) for readout. The sensor can be used for various applications like optical measurement, spectroscopy, or scanner applications.

4. Summary

In addition to the presented devices we have prototyped several other CMOS line sensors. These include a velocity sensor for contactless speed measurement, a high speed triangulation line sensor for accurate distance measurement, and a sensor with an analog EEPROM in each pixel to perform automatic FPN correction and on-line subtraction of shading and background patterns.

To summarize, the integration of optical line sensors in standard CMOS technology offers an enormous potential for improvement of sensor performance and addition of on-chip signal processing which will lead to new applications and products in the near future.

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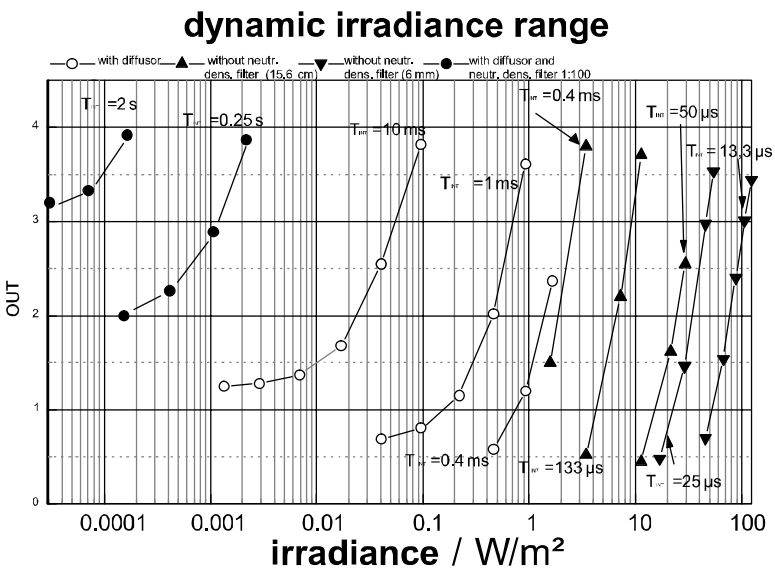

Figure 6: Dynamic input range of 2048 phototransistor pixel line sensor

Automotive CMOS Camera

W. Brockherde, C. Nitta

Introduction

Today, the exploding market of digital cameras fuels the development of CMOS image sensors. Though most of the CMOS imager suppliers focus on low cost "single chip cameras" (i. e. combining image sensor and camera electronics on a single CMOS chip) for consumer applications there is a lot of demand for CMOS image sensors for "non-consumer" applications. Besides the possibility of cointegration of sensors and electronics CMOS has some heavy potential advantages: high dynamic range, high temperature range, no blooming, smearing, or time lag, random access, and versatile electronic shutter control. The approach of Fraunhofer IMS is to use these new features to create improved solutions for existing and new imaging and optical sensory applications.

One of the most important and promising fields of advanced CMOS imager applications is that of automotive engineering. This includes on the one hand vision-based applications such as driver assistance systems, collision avoidance, driver monitoring, and rear view and blind spot vision. On the other hand imaging enables a wide variety of optical detection, sensing, and measurements, e.g. for obstacle detection, ranging, and occupancy and precrash sensing.

CMOS-based imaging and optical sensing technologies offer significant advantages. These include low fabrication costs owing to the fact that CMOS is the standard IC technology widely available, wide operating temperature range (>100 °C), and single-chip integration capability.

The CMOS imaging technology, however, offers even more features that elude any comparison with older technologies previously used. Thus CMOS imagers can be employed as "dual"- or "multiple"-use devices as they can be easily programmed, reconfigured, or multiplexed. E.g., the same CMOS imager can be used for seat occupancy monitoring when the vehicle is in motion or for intrusion detection while it is stationary and burglary alarm is activated. The requirements for both applications greatly differ: this applies not only to image acquisition and signal processing but also to power dissipation. Thus in the latter case the "intrusion detector" runs on battery as the car engine is shut down. Hence low power operation is mandatory in this case.

However, most challenging automotive imaging applications are based on cameras looking outside the vehicle. Let us consider those imposed on cameras for autonomous cruise control (ACC). Such cameras are operated in conjunction with a distance radar: their purpose is to extract the highway lane markings so that the ACC computer can determine whether a vehicle detected by the radar occupies the same lane as the vehicle carrying the ACC. Nevertheless, road illumination conditions can vastly vary not only between the scenes but also within a single scene due to inhomogenous illumination. ACC cameras have thus to exhibit extremely high "optical" dynamic range in order to be able to capture all scene details at night and also with bright sunlight.

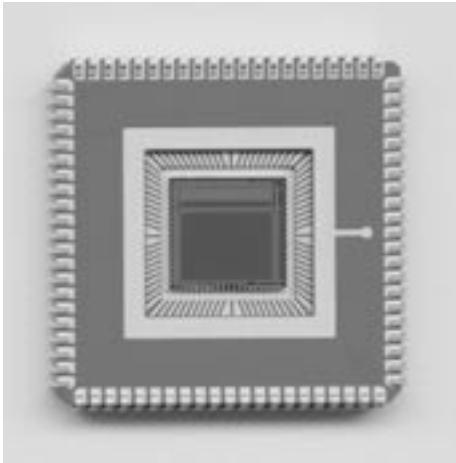

Figure 1: Chip photomicrograph of the 768 x 576 pixel imager array for automotive camera

Highly sensitive CMOS sensor

The Fraunhofer Institute of Microelectronic Circuits and Systems in Duisburg now has developed an automotive camera that satisfies the requirements mentioned above. This 2nd generation High-Dynamic-Range Camera is based on a novel CMOS imager that was also

Figure 2: Raw image (single integration time) taken with the new sensor

Figure 3: Demonstrator camera with Firewire interface

designed by the group and fabricated in 0.5 µm standard CMOS technology available at the institute (see Figure 1). Unlike competing high dynamic range CMOS imagers that employ logarithmic dependence on light irradiance, this imager uses linear dependence and thus does not suffer from poor contrast and high noise typical for "logarithmic" CMOS imagers. The high dynamic range of the CMOS "linear" imager used in the camera developed in Duisburg has been achieved using a sophisticated multiexposure algorithm that yields a 120 dB input dynamic range with excellent image quality unrivaled by other "linear" imagers. The chip exhibits a resolution of 768 x 576 pixels (i. e. "picture elements") while delivering 50 frames/ second in progressive scan (rolling shutter) operation. A first raw image taken with the new sensor (using single integration) is depicted in Figure 2.

Demonstrator camera

To demonsrate the performance of the sensor a camera platform has been developed and realized as demonstrator camera for sensor characterization and evaluation (see Figure 3). The camera exhibits an easy to use Firewire interface and transfers 120 dB subimages of 512 x 256 pixels with the full frame rate, i. e. 50 fps.

The camera and the CMOS sensor will be soon available for evaluation purposes. The preliminary data of both, camera and sensor are listed in Table I. Figure 4 shows four subimages of a scene taken with four different integration times. The subsequent calculation to one high dynamic image will be done in the camera.

The sensor and camera development was financed by the German automobile company BMW, Munich.

Figure 4: subframes taken with different integration times; total acquisition time: 18 ms

CMOS image sensor	
Acquisition	Progressive scan, rolling shutter
Sensitive area	768 x 576 pixels
Total # of pixels	796 x 604
Pixel size	10 µm x 10 µm
filling factor	50 %
Total chip area	90 mm² (0,5 µm CMOS)
Power supply	3.3 V
Power consumption	typ. 120 mW
Full frame-rate (20 ms integration time)	50/s
Maximum frame rate (full frame)	66/s
Pixel clock	16 MHz
on chip gain	6
Demonstrator camera	
Interface	IEEE 1394
Full frame (20 ms, 60 dB)	37/s
Subframe (four integrations 512 x 256; 60 dB)	50/s

Table I: Data of CMOS sensor and demonstrator camera

Embedded Microcontroller Applications

H. Kappert, R. Lerch, N. Kordas

Introduction

The use of microcontrollers has proliferated over the past two decades. Todays large scale integration technologies allow the integration of "embedded controllers" together with additional analog and digital electronics on a single microchip. Custom ICs based on microcontrollers are now seen even in the most mundane applications.

However, many of the design approaches use fixed microcontroller cores with invariant standard peripherals, resulting in sub-optimal designs for dedicated applications.

Fraunhofer IMS has realized a new design strategy for microcontroller applications. In the past years, a design environment consisting of a portfolio of microcontroller cores, hardware emulation platforms and a comfortable test and debug concept was established.

IMS has successfully integrated its microcontrollers into various applications, e.g. in data acquisition systems, medical applications, controllers for household appliances or industrial ICs. The actual applications are based mainly on two different controllers: the IMS2205 and the IMS3311 which are opcode compatible to well known industrial microcontrollers from Motorola (MC6805 and MC6811). The continuous success of the IMS strategy is based on a few elements which are highlighted below.

Lean core approach

The typical IPs in the microcontroller business are macros which contain peripherals in a more or less static configuration. All developments start from this macro and typically, the system size is growing from this starting point. Customers having a first contact with our cores usually wonder: why is it only a core? At the first glance, the IMS controller IP is seems to be just a microprocessor core which includes absolutely no peripherals or memories. Indeed, our controller IP also includes a set of standard peripheral IP as independent modules. They can be combined with the processor IP and technology-dependent memory modules into a complete application specific microcontroller system. This allows for a full custom system without any ballast from standard peripherals which are not necessary or oversized for the target application. We call this the lean core approach.

Flexibility

The lean core approach gives the customer high flexibility in his application. Besides the core IP, standard peripherals are available. Several projects have shown that standard peripherals are nice to have but that the main benefit comes from full custom blocks which make an application as powerful as required. With the lean core approach,

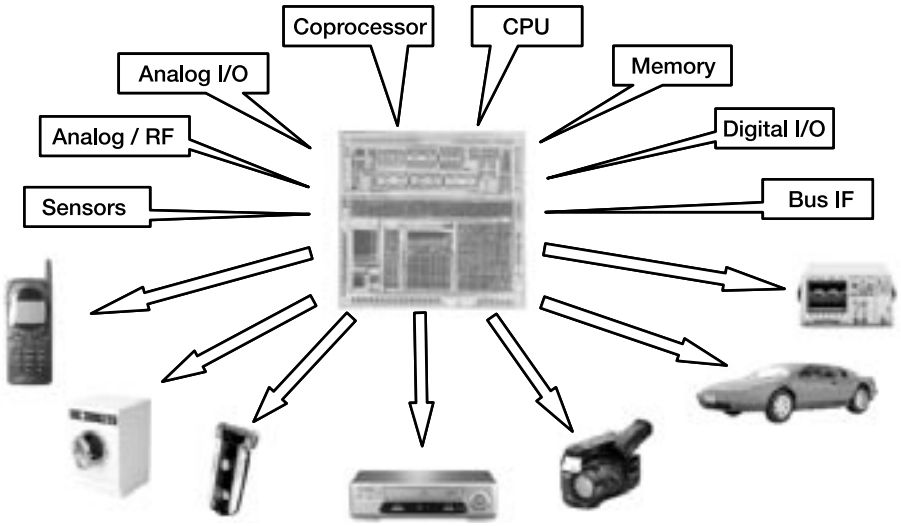

Figure 1: Embedded Microcontroller

a controller system can be integrated around the microprocessor core, which is fully optimized for the application.

Full Custom Peripherals

For the IMS controller cores a growing set of standard peripherals like general-purpose IOs, Serial Communication Interface (SCI, ASIO), Serial Peripheral Interface (SPI), I^2C, CAN, Timer, Watchdog are available. All controllers and digital peripherals are based on hardware description languages and can thus be used in any technology. Besides these pure digital blocks, analog blocks for signal conditioning or mixed analog digital blocks like A/D and D/A converters are also part of the portfolio.

As mentioned above, several projects have shown that the main benefit lies in the full custom design of peripherals. A large number of these peripherals have been developed. Some blocks have been designed for data and memory management, e.g. a Memory Management Unit. Especially in the field of data acquisition, often a large amount of data must be handled. This quickly exceeds the address space of the 8-Bit microcontroller cores. With a Memory Management Unit, memory sizes much larger than the controllers address space can be handled easily. Two other blocks were designed for automatic data management, verification and protection in form of checksum, respectively. For the verification of larger data blocks or the protection of communication frames, a Cyclic Redundancy Check circuit has been developed. For data management a Direct Memory Access module has been designed. Direct Memory Access can be used in many applications, where higher volumes of data have to be moved between memory and peripherals without the need of the controller. This can be used e.g. in measurement systems or communication systems. While data is automatically transferred between memory and peripherals, the controller can perform some calculations or formatting tasks. Alternately, the controller may enter a power-saving idle mode during periods of inactivity, with the DMA module still running.

Another kind of blocks have been integrated which make use of Direct Digital frequency Synthesis. These blocks have been developed for different industrial applications to control freely adjustable frequencies. With the additional capability of pulse width modulation we have used this technique to control single or multiphase bridge configurations for steppers or motors.

Current research activities are in the field of coprocessors which are optimized for data stream processing as needed for data encoding, compression or encryption.

Besides these digital blocks full custom analog peripherals exist like dedicated amplifiers, oscillators or filters.

Emulation

A key aspect of IMS embedded controller development is emulation. It enables the customer to start software development and application debugging in parallel to ASIC development. For several years now, IMS has provided the ASIC emulator, which has been superseded by the SoC-Emulator recently. If higher volumes of emulator prototypes are needed, a dedicated emulator can be developed without the overhead of the general purpose SoC-Emulator.

With the emulator the IMS or the customer are able to rapidly prototype

the new application. The central element is based on one or more FPGAs which allow the full emulation of the digital part. Analog parts are emulated with a functionally compatible replacement based on standard components. Tools have been developed to support FPGA and ASIC synthesis with regard to specific modifications driven by constraints from the FPGAs and the ASIC flow, respectively.

A powerful graphical user interface allows hardware and software debugging on the emulator and ultimately on the ASIC as well. The emulation of the whole digital part leads to a high confidence level for the later ASIC integration and the final application.

Test and Debug

All controller applications based on the IMS microcontroller cores are equipped with a test and debug interface based on the IEEE1149.1 (JTAG) standard, with powerful extensions for internal scan. The number of necessary additional pins can be significantly reduced, down to one or even no additional pin, by multiplexing functional pins in test mode. This technique has already been sucessfully proven in several applications. The JTAG interface and a full scan approach is today's standard to achieve a test coverage of more than 98 % as required by industry. The main advantage of the interface implemented with the IMS cores is its support for hardware and software debugging on the final ASIC, without additional overhead.

Outlook

The IMS controller integration team intends to extend the portfolio by a RISC-based scaleable architecture in the field of up to 16 bit controllers. Special research activities center on low power applications and coprocessors.

Summary

This article has highlighted the IMS activities on microcontrollers and has outlined the many advantages of our methodology. It's key idea is to leverage a lean core strategy to provide the flexibility necessary to optimize the system according to the application requirements. This results in optimized full custom devices with a minimum of overhead. With the complete design flow starting with rapid prototyping via the system integration up to the final test and debug, IMS provides a powerful way to integrate full custom microcontroller systems. Especially the early prototyping leads to a high confidence level for the final ASIC and the success of the application.

Figure 2: SoC Emulator Prototype

Digital Sinc-Filter for High Order Sigma-Delta-Modulators

M. Gnade, A. Kemna

Introduction

In numerous sensor applications an immediate analog to digital conversion of the acquired sensor signal is desired. For an integration of the sensing element and the readout circuitry on a single chip one particular ADC architecture has proven to be very suitable. Sigma delta modulators of higher order are capable of achieving very high resolution for a limited signal band without making high demands on technology parameters. The output of such a sigma delta modulator, a pulse density modulated signal at a very high clock frequency, has to be decimated in order to obtain a digital PCM signal out of it. The combination of the sigma delta modulator and the decimation filter forms the complete ADC. Since the signals are in a digital format right at the output of the modulator there is no need to implement the decimation filter on the same chip as the sensing element and the readout circuit. Thus the decimation filter can be realized using different technologies like an FPGA or an ASIC based on a pure digital CMOS technology exhibiting a minimum feature sizes of 130 nm.

Filter description

Digital sinc filters are commonly used to implement decimation by large factors without using complex digital circuitry. To obtain an optimum the filter order should exceed the order of the sigma delta modulator by one [1]. The corresponding transfer function in the z-domain is

$$H(z) = \left(\frac{1}{N} \cdot \frac{1 - z^{-N}}{1 - z^{-1}}\right)^{K}$$

where N is the decimation ratio and k the order of the sinc filter.

The transfer function of a sinc filter of 4th order designed to decimate the output signal of a 3rd order sigma delta modulator is plotted against the frequency in Figure 1. Since the transition from the passband to the stopband is not very steep the sinc filter is only suitable for the first stage of a multi-stage decimation filter. The minimum output clock frequency should be 4 times the Nyquist frequency in order not to loose too much signal power by filtering. The sinc filter is built up of three subassemblies, an IIR part consisting of digital accumulators, an FIR part, comprising digital differentiators, and a subsampler. Figure 2 shows a block diagram of a sinc filter of 4th order.

The above mentioned sigma delta modulator which the sinc filter is designed for is of 3rd order, it has a signal bandwith of 3.6 kHz and an oversampling ratio of 150. With an ideal low pass filter this modulator is able to reach a signal-to-noise ratio of 98.52 dB which corresponds to a resolution of 16.36 bits. Thus the described sinc filter has to be of 4th order and it implements decimation by a factor of 30. Consequently the oversampling ratio behind the sinc filter is 5. With these boundary conditions the whole system consisting of sigma delta modulator and sinc filter is able to reach a signal-to-noise ratio of 68.92 dB and, therefore, a resolution of 11.45 bits. This loss in resolution of nearly 5 bits can be outweighed by using a second filter stage performing an additional decimation by a factor of 5.

The minimum word length w of the registers of that the accumulators and differentiators in Figure 2 are built of is calculated by

$$w = k \cdot \log_2(N) + b$$

where k is the order of the sinc filter, N is the decimation ratio, and b is word-

length of the pulse density modulated signal to be decimated [2]. For the realized filter this equation yields a word length of 21 bits. With this condition the accumulators are allowed to overflow without having an influence on the signal integrity. Both, a realization in an FPGA and the integration as an ASIC of this decimation filter is possible.

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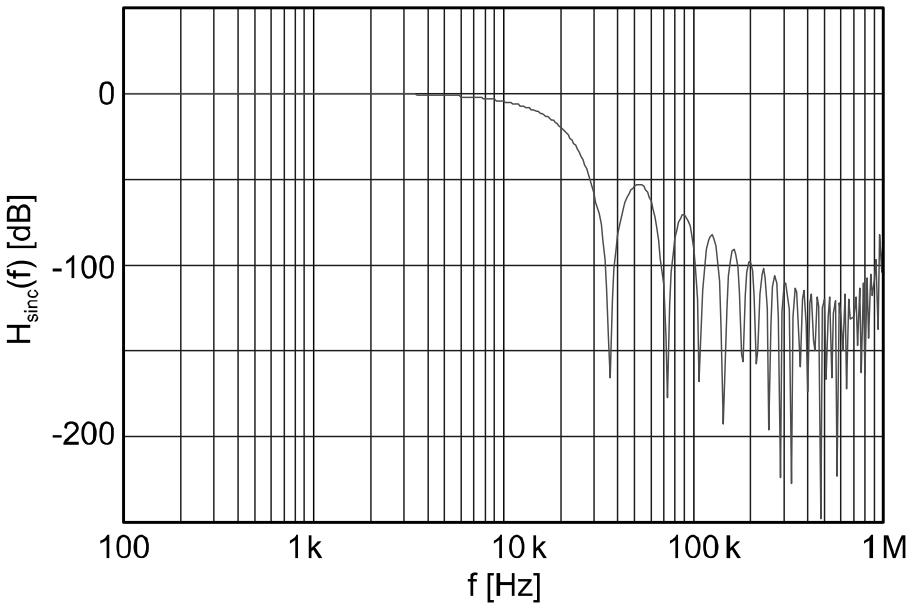

Figure 1: Frequency response of the sinc filter

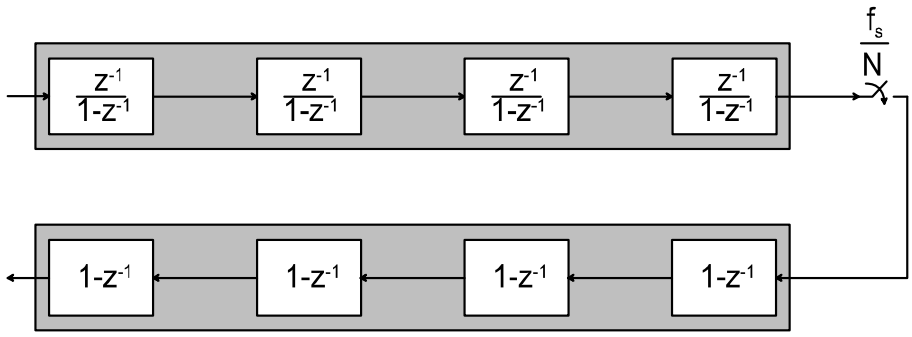

Figure 2: Block diagram of the 4th order sinc filter

Cascaded Sigma-Delta-Modulators of Higher Order Without Stability Problems

Dr. D. Weiler

Introduction

Analog/Digital converter (ADC) based on the sigma-delta(∑Δ)-principle achieve a high signal to noise ratio (SNR) by combining oversampling, interpolation, and noise shaping while dispensing with the need of high precision analog components [1]. A ∑Δ-ADC consists of a ∑Δ-modulator followed by a decimator (Figure 1). The SNR of the ADC is mainly determined by the ∑Δ-modulator. The parameters of the ∑Δ-modulator are oversampling ratio OSR, order of the modulator L, resolution of the internal ADC B, and the architecture. An increase of the OSR, order L, or the resolution B will increase the SNR of the ADC. The choice of using a high OSR has the disadvantage of high power consumption and the maximum sampling frequency is limited by the technology. Therefore, a moderate OSR is a better choice. The consequence is that a high order loop filter or multi-bit quantization is necessary. Both approaches can be realized using different architectures: single-loop or cascaded ∑Δ-modulator. A 3rd order single-loop ∑Δ-modulator has been well implemented at the IMS in the last years. Further increasing of the order will result in serious stability problems. The high sensitivity to DAC non-linearity using multi-bit quantization requires correction mechanism and therefore increase the complexity. To overcome stability problems and DAC non-linearity cascading of ∑Δ-modulators can be a solution.

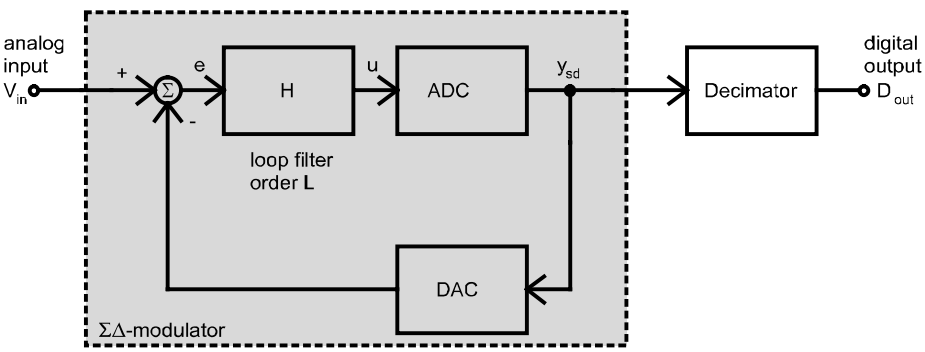

Figure 1: ∑Δ-ADC with single-loop ∑Δ-modulator

Cascades ∑Δ-modulators

Cascaded ∑Δ-modulators consist of stable 1st or 2nd order ∑Δ-modulators. Since the cascaded ∑Δ-modulator contain only feedforward paths and there is no feedback between the single-loop modulators they have inherently no stability problems for higher orders [2]. By using only multi-bit quantization at the last cascade the sensitivity to DAC non-linearity can be drastically reduced [3]. The disadvantage of cascaded ∑Δ-modulators is their higher sensitivity to other circuit imperfections like capacitor mismatching.

The general architecture of a cascaded ∑Δ-modulator shows Figure 2. The cascaded ∑Δ-modulator consists of several low order single-loop ∑Δ-modulators, each with its own quantizer. Each ∑Δ-modulator in the cascade converts the quantization error E of the previous modulator. The quantization error of all modulators with the exception of the last stage will be eliminated digitally by the cancellation logic. The total order of the cascaded ∑Δ-modulator is the sum of the used single-loop modulators:

$$L = L_1 + L_2 + K + L_n$$

The output signal of the ∑Δ-modulator after the cancellation logic

$$Y(z) = z^{-1} \cdot X(z) + d \cdot (1-z^{-1})^{L} \cdot Q_n(z) - d \cdot (1-z^{-1})^{L-L_n} \cdot E_D(z)$$

consists of the input signal X(z), the Lth order noise shaping of the last-stage

quantization error, and the $(L-L_n)^{th}$ order shaping of the DAC error in the last stage [4]. The attenuation of the DAC error is only valid in the described architecture with single-bit quantizer in all but the last stage and multi-bit quantization only in the last stage.

Since the 1st order ∑Δ-modulator has a poor idle-tone performance it is better to use a 2nd order ∑Δ-modulator as the first stage of the cascaded ∑Δ-modulator. Imperfect cancellation because of mismatch could degrade the overall idle-tone performance to be determined by the first stage.

Simulation results

Since ∑Δ-modulators represent heavily non-linear systems, an exact mathematical analysis is extremely difficult [2]. To predict the SNR of cascaded ∑Δ-modulators simulations are the only accurate method. All simulation results in this communication obtained using behavior simulations based on SIMULINK models. Several circuit non-idealities affecting the SNR, and, therefore the resolution are considered in the models. Relevant non-idealities in switched capacitor realizations are: capacitor mismatch, sampling jitter, kT/C-noise, and the OTA-non-idealities including finite DC gain A_{v0}, gain-bandwidth GBW, slew-rate SR, and OTA-noise.

The simulation results compare different architectures with an order of 3. The first used architecture is a 1-1-1 ∑Δ-modulator, which consists of three 1st order single-loop ∑Δ-modulators. The second architecture is a 2-1 ∑Δ-modulator with a 2nd order ∑Δ-modulator at the first stage and a 1st order a the second stage. Both cascaded ∑Δ-modulators are compared to a single-loop 3rd order ∑Δ-Modulator. Figure 3 shows a FFT of the output $y_{\Sigma\Delta}$ of a 1-1-1 ∑Δ-modulator with an input frequency of f_{in} = 1 kHz and a sampling frequency of f_s = 128 kHz. This plot shows the characteristic rise of the shaped quantization noise with 60 dB/dec for a 3rd order ∑Δ-modulator. Due to nearly ideal cancellation no idle-tones occur.

Figure 4 shows the sweep of the input amplitude versus the SNR for all three modulator architectures. A ∑Δ-modulator containing only 1st order modulators shows no overloading effect. A 2nd order ∑Δ-modulator becomes unstable for input amplitudes above 80 % of the reference voltage of the feedback DAC and for a 3rd order ∑Δ-modulator the overload limit is at ca.70 %. This figure shows one advantage of cascaded ∑Δ-modulators compared to high-order single-loop modulators concerning the dynamic input range.

The serious problem of cascaded ∑Δ-modulator is their mismatch dependence

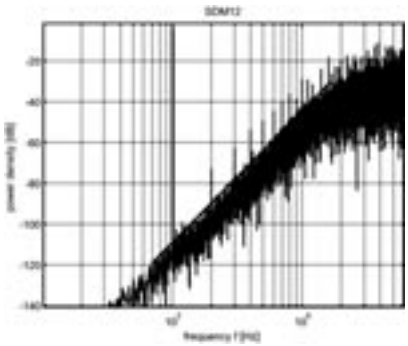

Figure 3: FFT of the output of a 1-1-1 cascaded ∑Δ-modulator

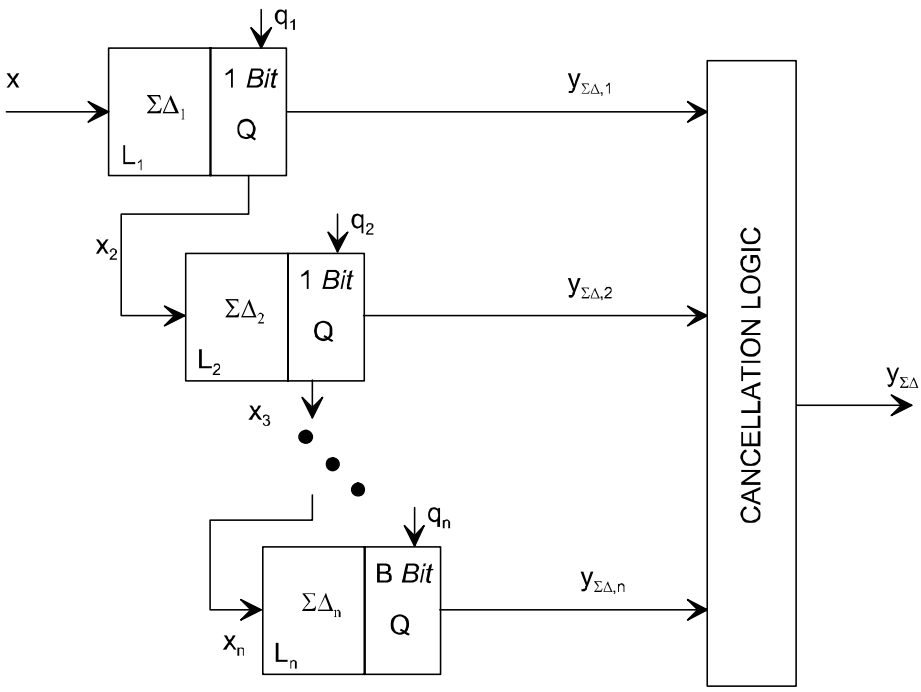

Figure 2: General architecture of a cascaded ∑Δ-modulator

because of imperfect noise cancellation in the analog part. Figure 5 shows the standard deviation of the SNR for different capacitor mismatch values [5]. This simulation result has been archived by repeating 1000 simulations with randomized gain factors, which represent the mismatch. The single-loop ∑Δ-modulators shows no SNR-dependence on mismatch. A variation of the gain factors results only in a very small modification of the noise-shaping and therefor in the SNR. A different dependence show the cascaded modulators. The standard deviation of the SNR raises for increased mismatch. Mismatch above 1 % results in a poor noise cancellation and, therefore, in a reduced SNR. The effect becomes more pronounced if the number of single-loop stages increases. This limits the order of cascades ∑Δ-modulators to L = 6.

The effect of sampling jitter is independent of the modulator architecture because it affects only the sampling stage. Sampling jitter has a heavy effect on the SNR and, therefore, the sampling state needs a careful design.

Other non-idealities of the OTA affect the SNR in both architectures in similar manner.

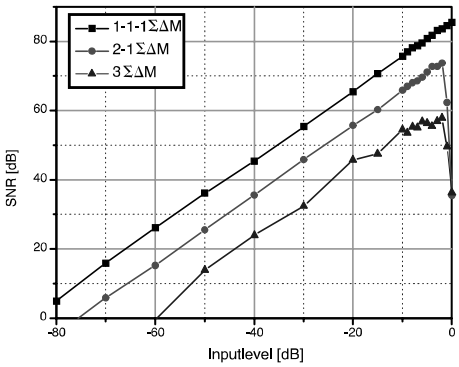

Figure 4: Overload effect of high order ∑Δ-modulators

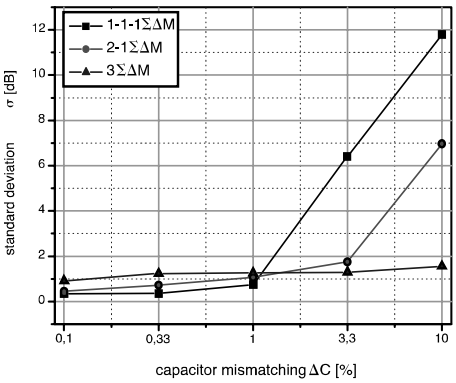

Figure 5: Standard deviation of the SNR due to capacitor mismatching

Conclusion

A comparison of single-loop and cascaded ∑Δ-modulators have been derived using SIMULINK behavior simulation. To overcome stability problems of high order single-loop ∑Δ-modulators cascaded modulators are an alternative. The effect of capacitor mismatch can be tolerated for technologies with a matching of better 1 % for modulator order smaller than L = 6. The consisting disadvantage of cascaded ∑Δ-modulators is their area-overhead due to the quantizers located at each single stage.

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Rapid Prototyping for Wireless System-on-Chip Solutions

M. Marx, H.-C. Müller, R. Kokozinski

Introduction

The improvements in the area of microelectronics lead to shorter design cycles and rapidly rising complexity of electronic designs. Therefore, developers are forced to refine the system development process to avoid a productivity gap. *Rapid prototyping* (RP) is a technique to support the system development. The term rapid prototyping is defined as a type of prototyping in which emphasis is placed on developing prototypes early in the development process to permit early feedback and analysis.

The IMS design-flow for wireless System-on-Chip is based on the traditional development process which can be represented in the V-model. The V-model enhanced by different levels of rapid prototyping is called VP-model [2] (Figure 1). The idea of rapid prototyping is to skip time intensive steps of the development process, and reduce the time to get a first functional prototype of the entire system or a part of the system. This prototype allows the validation of functionality and early performance tests. The comparison between different design alternatives can be simplified and therefore the conceptual validation rises.

Also in future, wireless systems (WS) will be implemented by a mixed analogue and digital signal processing but the ratio of *digital* functions in the value-added chain is increasing rapidly. This contribution focuses on RP to speed up the design flow for *digital* WS.

Prototyping versus Simulation

A first rough behaviour modelling of the system under test (SUT) is achievable in a system simulation tool like Matlab/Simulink. Normally, every system under test interacts with a real environment. For simulation, these interactions must be emulated, too. Thus, in most applications a second rough emulation – an artificial environment model (AEM) – of the real environment is necessary, where the SUT is embedded in.

For example, to verify the digital base band concept in a wireless system, first an appropriate model for the SUT is developed. In reality the signal at the output of the base band module passes through the analogue radio frequency (RF) module in the transmitter (Tx), the physical channel of the air link and the RF module in the receiver (Rx) until it stimulates again the inputs of the base band module in receiver (figure 2). On this path the signals are distorted by non idealities in the analogue RF and effects like doppler shift and reflection in the physical channel. For simulation, an AEM of this real environment is required. The modelling of such a real environment is very complex, thus afford limitation requires to design an AEM which is only able to describe some basically issues of the reality.

By this approach fast first results of the SUT behaviour are achieved, but at the expense of a roughly modelled AEM.

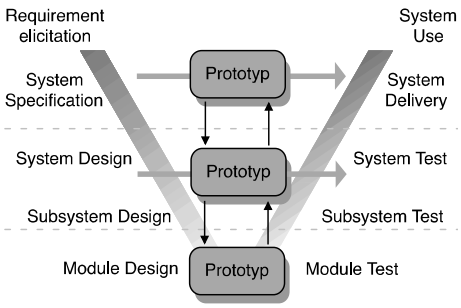

Figure 1: Development process as VP-model

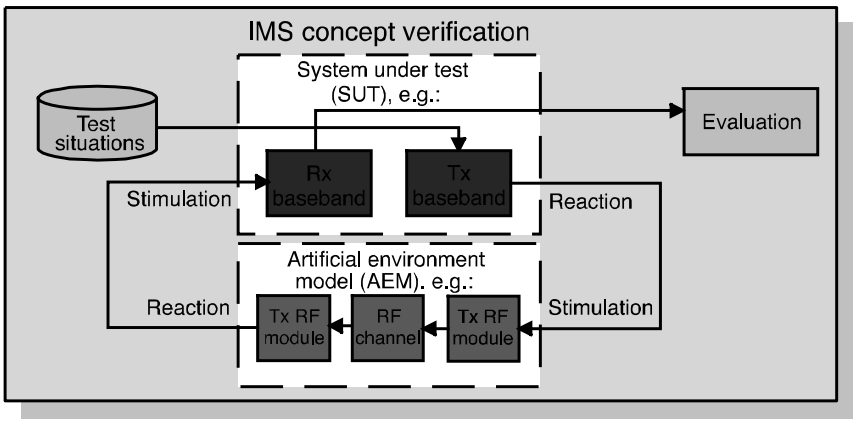

Figure 2: IMS Concept Verification

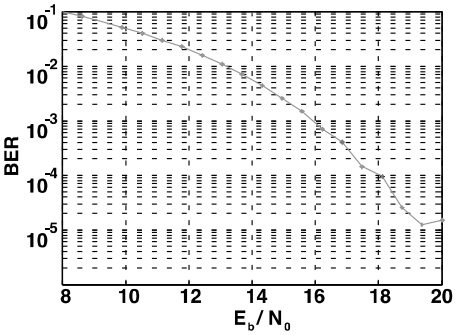

Figure 3: BER Curve of BT path

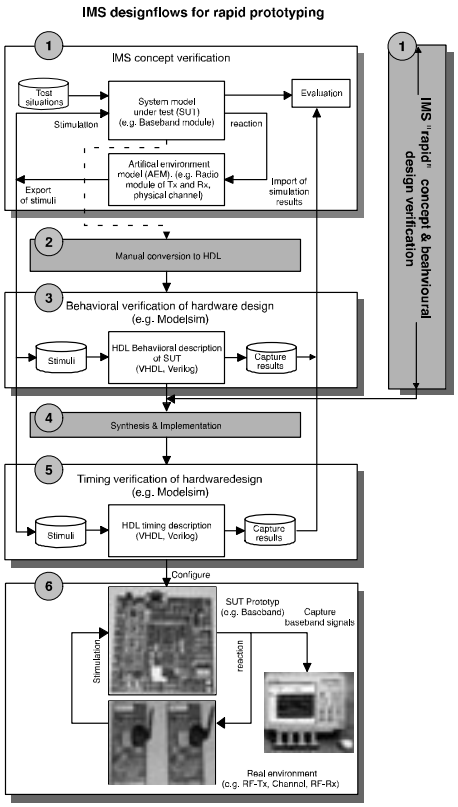

Figure 4: IMS RP design flow

Further the timing analysis contribution with real time operating systems becomes difficult.

By using a prototype of the SUT, embedded in the real environment, a more realistic verifying of the concept is possible and the effort to model a very realistic AEM is avoided, respectively.

Figure 3 shows a BER curve of the bluetooth path for the IMS multi-standard CMOS transceiver that is generated using the described approach.

The arrangements to develop a rapid prototype at this early development process will be described further on.

Rapid Prototyping for Wireless Digital Systems

The long iteration times of ASIC prototypes are circumvented by programming the digital design of the prototype into an FPGA (Field Programmable Gate Array).
By using FPGAs, the behaviour of the whole later digital design is pre-determinable. Dedicated software tools for FPGAs support the appropriate design flow.

Classical Design Flow for FPGA based Prototyping

The classical design flow for an FPGA design consist of the steps:
1. Concept Verification
2. Hardware Description (HD) Design Entry
3. HD Behavioural Verification
4. HD Synthesis & Implementation
5. HD Timing Verification
6. Real Prototyping Test

(See figure 4).

In step 1 the concept is verified by simulating the SUT model and the AEM.

In the second step the digital architecture of the design is described by using a hardware description language like VHDL or Verilog. This step is done again manually by the designer. Basing on the HDL description a *behavioural verification* (step 3) of the SUT is possible. Therefore the HDL model is also embedded in a HDL test bench (TB). Since it is normally too much effort to translate the AEM into a HDL description, for each test situation to be verified a new stimuli pattern is extracted from the outputs of the arbitrary environment model of concept simulation (step 1) and imported into the test bench.

In the steps *synthesis & implementation* (4) the HDL behavioural description is compiled into a net list only consisting of basic logical gates. Afterwards it is placed onto the configurable logic blocks of the FPGA and routed. These steps are done automatically by EDA tools.

The result of synthesis and implementation is a description of the digital design, mapped onto the FPGA architecture. This timing HDL description considers also the timing properties of all elements within the FPGA and enables an exactly timing simulation (step 5) of the design.

After downloading the configuration bit stream onto FPGA, the SUT prototype can be tested by artificial stimulation (Picture 1) or embedding in real environment.

This classical design process has two drawbacks:
First, the designer is forced to describe the SUT model two times, one time for the concept verification and one time in a HDL.

Second, the *behavioural verification* takes additional time if several situations are required to verify, since the stimuli pattern for each test situation is imported in the HDL test bench for behavioural verification.

"Rapid" Wireless Design Flow for FPGA based Prototyping

Currently, a "rapid" design flow is evaluated in the department WCS, which avoids these drawbacks. Here the SUT model for step 1 is described by using a dedicated XILINX block set library. This SUT description behaves like the later hardware. Further it allows the use of a system generator tool, which generates automatically a description of the SUT hardware architecture. The description of the SUT is faithful in that the system model and hardware implementation are bit identical and cycle identical at defined sample times. Thus also the third step, the behavioural verification is dispensable and steps 1, 2 and 3 are merged together to one new step "concept & *behavioural design verification*". This approach enables also a comfortable design verification of a system, where the loop of SUT and AEM is closed (e.g. for feedback control systems).

In some modest applications also the timing simulation (Step 5) may be skipped, thus reducing the engineering time to only two steps.

Currently projects at IMS like the "Multi Standard Single Chip Transceiver (MUSTANG)" [1] will gain by this approach.

Conclusion

Rapid prototyping enables an early design verification in the real environment. Beside this technics, at IMS a new approach for rapid prototyping is used which merges the processes concept verification, design entry and design verification to one step, which can increase efficiency and flexibility considerably.

References

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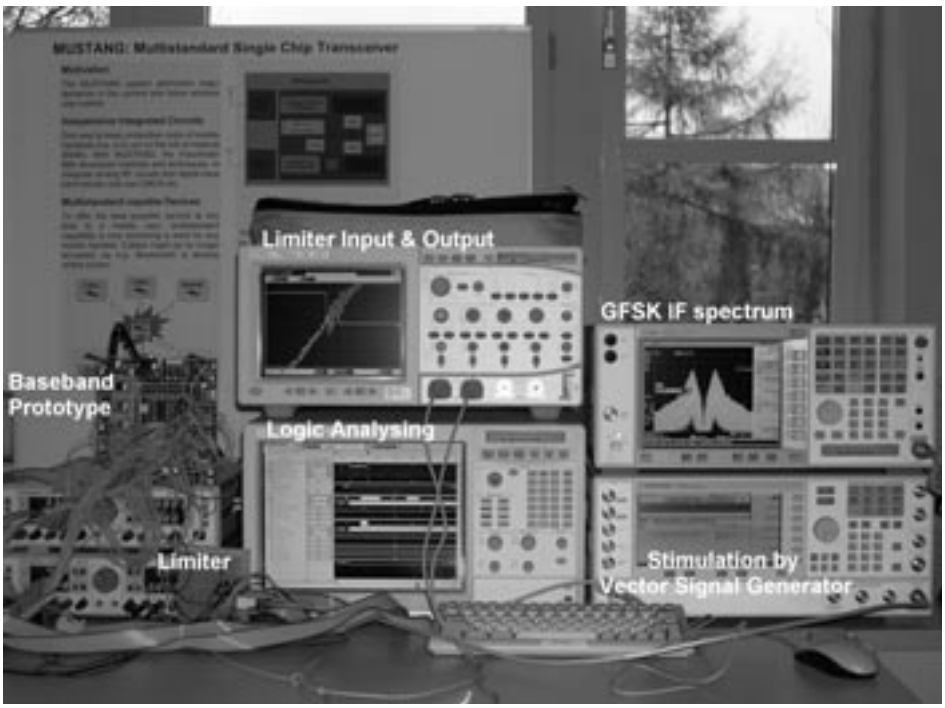

Picture 1: Design evaluation

Low power four channel Central Office ADSL Solution

M. Bresch, R. Kokozinski

Increasing demand for data transmission

As the demand for data-transmission especially for internet applications rapidly increases, new transmission schemes have to be provided. Since providing every household with new high-speed data links (e.g. "fiber to the home") is very costly and time consuming, the existing telephone system has to be used for this new transmission scheme. The last mile from the central office to the home accounts for 80 % of the total installation costs – no telecommunication company would be able to stem these costs. Moreover, implementing a new high-speed data transmission system would take a couple of decades. Digital subscriber line (DSL) technology offers high-bandwidth data communication links to home and office by using this previously untapped capacity of already installed twisted-pair telephone wiring. However, the existing telephone network had been designed for mere DC to 4 kHz, and not for high-speed internet access up to 1.1 MHz. Therefore, this twisted-pair telephone wiring is not suitable for a digital data transmission, because it fails to high attenuation and cross-talk at transmission frequencies higher than 1 MHz. Therefore, digital data have to be converted into an analog signal for transmission at one termination and be digitized back at the opposite termination.

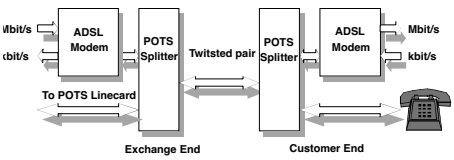

Figure 1: ADSL modem structure

Data transmission employing ADSL

The analog modulation of ADSL is discrete multi-tone (DMT). It is used to transform the high speed digital data into a large number of equally spaced Quadrature Amplitude Modulated (QAM) carriers. Thanks to the DMT modulation, the ADSL modem operates like a large number of QAM-modems in parallel. Depending on POTS or ISDN mode, three or four information channels are transmitted in parallel: a high speed down-stream channel, a medium speed duplex or up-stream channel, depending on the implementation of the ADSL architecture, and a POTS (Plain Old Telephone Service) or an ISDN channel. The POTS channel and the ISDN channel are split off from the digital modem by filters, thus guaranteeing uninterrupted POTS/ISDN interconnection in parallel to the digital subscriber line. Figure 1 shows an example for an ADSL modem structure. For the purpose of POTS/ISDN operation in parallel, a splitter outside the Modem is necessary. The location of the three information channels in POTS mode and the four channels in ISDN mode is shown in Figure 2. The DMT modulation acts like a fast Fourier transform of the digital data in order to distribute the data into the up to 255 channels between 7 kHz and 1.1 MHz. This leads to vast signal processing efforts. The high demands for both digital data processing and analog transmission lead to the concept of dividing the modem into a digital

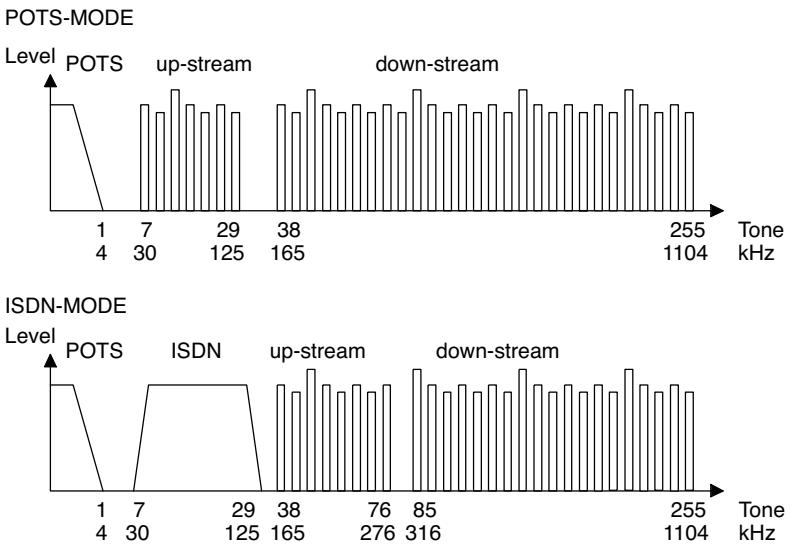

Figure 2: POTS/ISDN and ADSL information channels

signal processor and an analog front-end, which has been designed by IMS for TOSHIBA. The digital signal processor is responsible for coding, error correction, modulation, channel allocation etc.
The analog front-end's task is digital-to-analog (and back) conversion, line driving, filtering the signal to divide it into up-stream and down-stream, amplify the signal and anti-aliasing. The signal amplitude and line quality severely depend on the household's location. If a household is located rather close to the central office, the copper wire attenuates the signal only a little bit – reducing the demand for amplification and filtering. However, the distance between a household and the central office may be up to 6 km. In this case, the signal is attenuated by up to 30 dB and has to be amplified at high gain, increasing the noise sensitivity. Therefore, gain of amplifiers and drivers must be programmable and filter cutoff frequencies must be programmable as well in order to ensure high quality communication everywhere.

ADSL Analog Front-End for four channels

In order to cope with high attenuation and large echo return, the analog front-end features low noise and a high dynamic range. Figure 3 shows the structure of the four-line analog front-end. In the receive path (RX), a low-noise variable gain amplifier (LNA) provides gain scaling (0-31 dB) of the incoming signal, since the LNA has to yield high gain at high bandwidth in combination with a high input impedance. High bandwidth is necessary, since the gain of up to 31 dB has to hold in the entire up-stream and down-stream range. An instrumentation amplifier structure with a gain-dependent frequency compensation scheme is used in order to keep the internal open loop amplifier gain at 30 dB above the total LNA gain. An attenuator from 0 to -15 dB widens the RX path gain to a range from -15 dB to 31 dB.

The LNA output signal in the up-stream path is filtered by an RC-network to reduce NEXT, alias, and out-of band distortions. Since the requirements for the up-stream filter is low, a simple second-order passive RC-network suffices. Its cut off frequency is in the range between about 500 kHz to 1000 kHz. The up-stream filter's output signal is sent to the ADC.

Since ADSL (Asymmetric Digital Subscriber Line) consists of two different channels – the up-stream channel is much narrower than the down-stream channel – the line termination in the central office receives much less data per line than the network termination in the household. Therefore, in the central office, the ADC can acquire incoming data from more than one line as multiplex. While the sampling rate of the network termination side in the household has to be 8.8 MS/s, the line termination side at the central office only demands 2.2 Ms/s per line. Hence, four lines can be served by one line termination analog front-end in parallel. For this purpose, a four-line analog front-end for the central office has been developed for TOSHIBA by IMS.

The up-stream filter's output signal is digitized using a 13Bit@4x2.2Ms/s pipelined ADC, which is composed of six stages each producing 3 Bit raw data. The total 18 Bit raw data are converted into a 13 Bit digital output code by a digital error correction module. A multiplexer at the ADC input distributes the input signal to the four referring lines. The digital output code is sent through a 4Bit@35MHz high speed RXD interface to a digital signal processor IC.

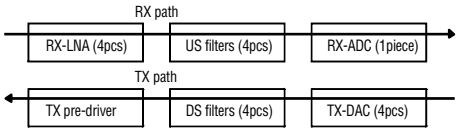

Figure 3: ADSL four-line AFE structure

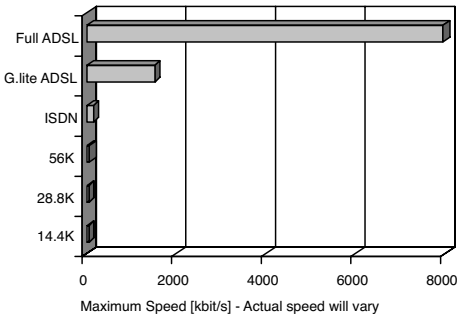

Figure 4: Data rates

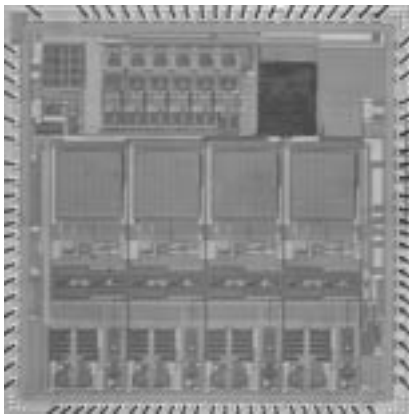
Figure 5: Microphotograph of the four-line ADSL Analog Front-End

ADSL four channel ASIC performance

In the transmit direction (TX), the digital data received from the digital signal processor IC are fed through a similar 4Bit@35MHz TXD interface to the four 12 Bit current steering 8.8 Ms/s DACs. Reconstruction of the signal is performed in the following R-MOSFET-C down-stream filter in order to remove image frequencies and out-of-band noise. A programmable gain (-9 dB to 6 dB) class AB amplifier is used as a pre-driver to adapt the transmit power to the line characteristics. The maximum output signal is 4Vppdiff. Both ADC's and DAC's DNL are less than 1LSB, INL of DAC is 2LSB, INL of ADC is 6LSB. The accuracy of the amplifiers is 0.3 dB. The input referred noise of the LNA is 12 nV/sqrt(Hz), the S/IM3 ratio is higher than 60 dB in the total TX path and also in the total RX path [1].

The advantage of a four-line analog front-end is less power consumption (only one ADC, the most consuming component) and less space demand compared to four one-line analog front-ends. The four-line analog front-end comprises for each of the four lines one active down-stream filter, one passive up-stream filter, one DAC, one LNA, and one TX driver. And it comprises one ADC in total, multiplexing data received from the four lines.

The design strategy has relied on the use of a fully differential analog signal path combined with a triple-well mixed signal technology process and usage of separated power supplies for digital I/O cells, digital interface core, and the analog modules in order to minimize parasitic coupling and noise injection through the substrate and the power lines. The chip was realized in a 0.25 µm CMOS technology at a power supply of 2.5 V. Figure 4 compares the data rates, while Figure 5 shows a microphotograph of the chip [2,3,4]. The ASIC is a special design for testability, that enables evaluation of each component and analysis of raw 18 Bit ADC data, provides a one-line mode and a loop-back test, and is therefore suitable for dedicated test equipment [5].

Figure 6 shows the ADSL applications, while Figure 7 gives an impression of future market volumes and possible network architectures. The potential revenue is estimated to be tens of Euro monthly per user in the 3rd wave.

Conclusion

A novel low-power low-voltage 0.25 µm CMOS ADSL analog front-end operating with four lines has been developed for TOSHIBA. The analog front-end consists of four LNAs, four active down-stream filters, four passive up-stream filters, four TX pre-drivers, four TX-DACs and one RX-ADC. All amplifiers feature highly accurate programmable gain. The filters for up-stream feature highly accurate programmable cutoff frequencies. The high speed digital-to-analog converter has 12 Bit resolution @8.8 MHz sampling rate and the output signal is 2.2Vppdiff. The high speed analog-to-digital converter has 13Bit resolution@ 4 x 2.2 MHz sampling rate and an input range of 2.2 Vppdiff. The ADC distributes the incoming data to the four channels by multiplexing. All components feature high linearity and low noise. A novel triple-well mixed signal technique with separated power supplies has been applied.

Figure 6: ADSL Applications

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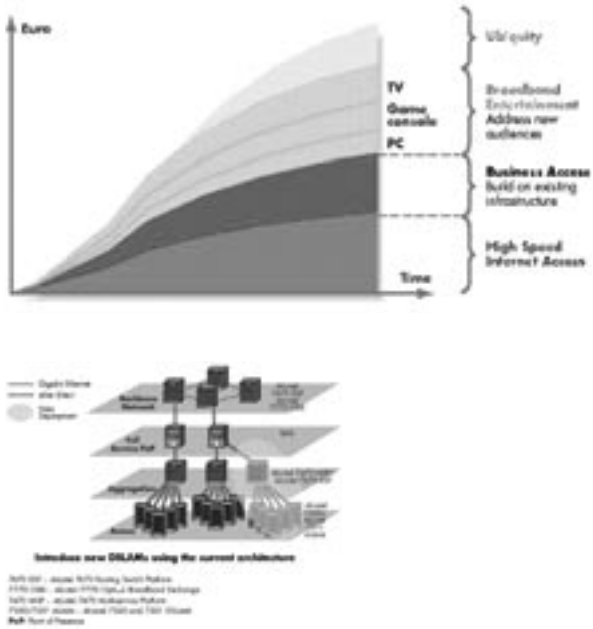

Figure 7: Market Outlook: a) Increasing demand, b) Network topology

CMOS IP for Short Range Wireless Communication Systemes

N. Christoffers, R. Kokozinski

Introduction

The industry is calling for standards of networking that are both wireless and can offer communication between devices, be it sensory information, data acquisition or control applications. Such applications need to be able to cover a range of possible uses, including home networking, building automation, supply chain management, metering, agriculture, industrial automation and patient monitoring. IMS has developed fully-customised multi-standard wireless applications based on hardware platforms, giving system designers the freedom to focus on sensors, actuators and back-end data collection. It is Fraunhofer-IMS's expertise in this field that allows wireless system designs to be developed in accordance with the needs of the aforementioned industries. The goal is to equip them with systems which combine simplicity, low costs and low power usage whilst providing low-data rate wireless connectivity amongst inexpensive equipment, be it fixed, portable or moving. Ultimately, this will result in applications with mulit-hop and ad-hoc functionality. Their reliability will be ensured by fault-tolerant redundant paths acting between all network nodes.

ZigBee, a new standard of networking based on IEEE 802.15.4 can operate in 868 MHz, 915 MHz, or 2.4 GHz frequency bands (Fig. 1), The resulting data rates are 20 kb/s, 40 kb/s, and 250 kb/s respectively. IMS multi-standard CMOS IP allow the integration of the physical layer in a single IC. Due to the very small physical size of a module, the wireless connection can be easily embedded in systems with small form factors, since the transceiver adds only a small overhead to the system size. Hence, this technology can become invaluable in many sensor, automation or networking applications, as well as Body Area networks and patient monitoring systems. It is in these areas in particular that system size, power consumption, flexibility and reliability are paramount.

IMS IP based System-on-Chip solutions (SoC) allow a combination of sensing and wireless connections on very small modules or even on single chip ICs. This has already been demonstrated in several sensing applications including patient monitoring and industrial equipment. Multi-standard CMOS IP like e.g. filters, frequency synthezeisers, and oszillatos has been developed in order to allow short design cycles and thus short time-to-marked. Wireless SoC will be a key element in future intelligent systems containing networked, embedded devices. Embedded internet devices will allow communication with remote networks, thanks to the inclusion of additional wireless data links (Fig. 2). The result of this will be a whole new range of services and applications.

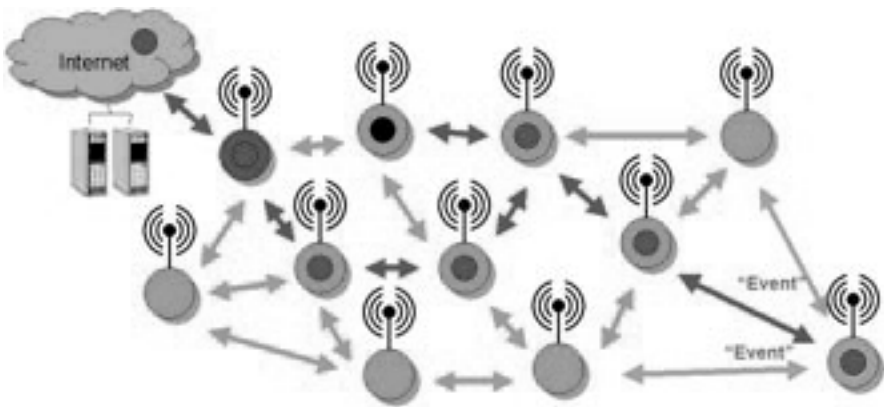

Figure 2: Wireless multi-hop network

	Band	Coverage	Data Rate	Channel Numbers
868 MHz		Europe	20 kbps	0
915 MHz	ISM	America	40 kbps	1 – 10
2.4 GHz	ISM	Worldwide	250 kbps	11 – 26

Figure 1: Frequency bands for communication

In addition to the internet, connected local wireless devices will also be fundamental to smart environments. Properly developed, connected wireless smart modules will allow a whole range of new internet-based services, closing the gap between the internet and the real world. Wireless SoC solutions will be fundamental to the success of these kinds of developments.

The ZigBee protocol is especially well suited to timing critical applications like remote sensing and automation. Connection time, response time and data latency will all be significantly shortened. Even in the case of multi-hop structures, sensor data will be transmitted in tens of milliseconds. Nevertheless, in some applications data latency is less critical than battery life. In cases like these, relaxed data latency power-safe modes will be used, extending battery life for years.

IMS platform-based wireless technology is perfect for the development of flexible, tailored systems, particularly in areas where system costs, data reliability, battery life, small form factor and flexible networking are essential. It is in the areas of sensing, automation and control in large fields of application where this technology will prove fundamental.

The IMS SoC development platform is constituted by key expertise for RF building blocks and predefined reusable circuits. In such a way system aspects can become the focus for the customer and time-to-market is minimized since circuit level details and their impact on the application are best anticipated. Examples for such expertise are micro-electronic high-Q-current-mode (gm-C-) filters operating at high frequencies, low noise and low power-consumption. These can be employed for intermediate frequency filtering as well as loop filtering in powerfull PLL based frequency synthesizers based on a novel architecture which has been developed at the IMS. A synthesizer producing low spurious emissions at a low settling time requires also micro-electronic high-frequency components. Especially high frequency voltage controlled oscillators comprising spiral inductors are non-standard building blocks but have been realized in our CMOS technology. These examples are detailed further in the following.

Current-Mode Gm-C-Filters

The basic idea of the current-mode technique is to use current instead of voltage as the signal representation. This entails two major benefits. Firstly, to integrate the signal simply a capacitor can be employed. The voltage across its terminals will be proportional to the integrated current. Capacitors are easiliy available in CMOS processes. Secondly, a summing network can be realized simply using a circuit node. Since the input signals are currents the addition results directly from Kirchhoff's Current Law (KCL) which does not describe any frequency dependence, nonlinearity or noise. Thus, excellent broadband linearity and noise performance can be obtained for current-mode filters, too.

A very important subcircuit in micro-electronic filters is the biquadratic filter (biquad) the block level schematic of

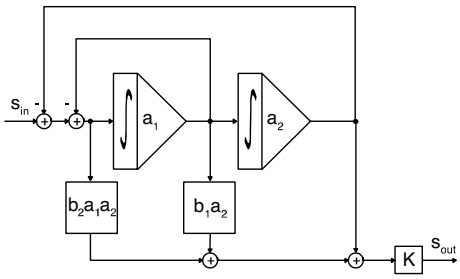

Figure 3: Block level schematic of a biquad

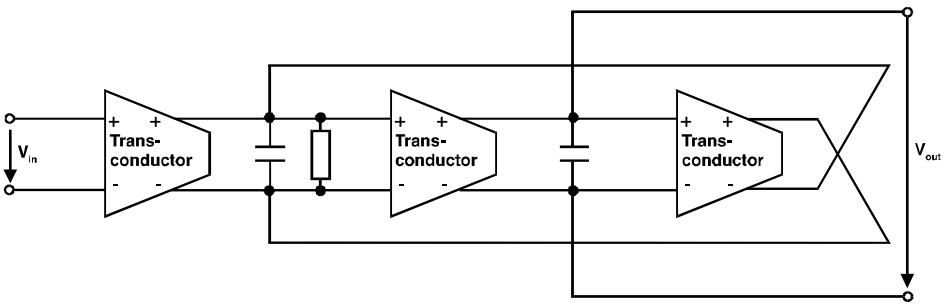

Figure 4: CMOS realization of a biquad

which is shown in Figure 3. Note that only building blocks that are easily available – namely integrators and summing networks – are required. The circuit realization of a low pass biquad derived from Figure 3 is depicted in Figure 4. In addition to capacitors and circuit nodes transconductors are necessary to convert the voltage across the integrating capacitors into currents again. Note that by definition the biquad shown in Figure 4 is a voltage-mode biquad since the input signal here is a voltage. However the component directly at its input is a transconductor that turns the voltage into a current which then drives an actual current-mode filter.

The performance of a biquad depends on the design of the transconductors employed. They must maintain a high output resistance in order to establish a high integrator-Q. Additionally, the designer has to ensure that the transconductance is only a weak function of frequency in the desired frequency band. No phase shifts between input voltage and output current are acceptable. The performance of a biquad realized using transconductors realized by designers in the IMS is demonstrated in Figure 5. From the simulated transfer function depicted as magnitude and phase it can be noticed that parasitic zeros or poles are located at frequencies in the range of several hundred MHz. Before that perfect biquad behaviour can be observed, i.e. a phase of zero and a constant magnitude before and a phase of -180 degrees and a magnitude falling at -40 dB/dec after the cutoff frequency. In spite of these good high frequency characteristics the current drawn from the power supply was as low as 30 uA for each of the transconductors.

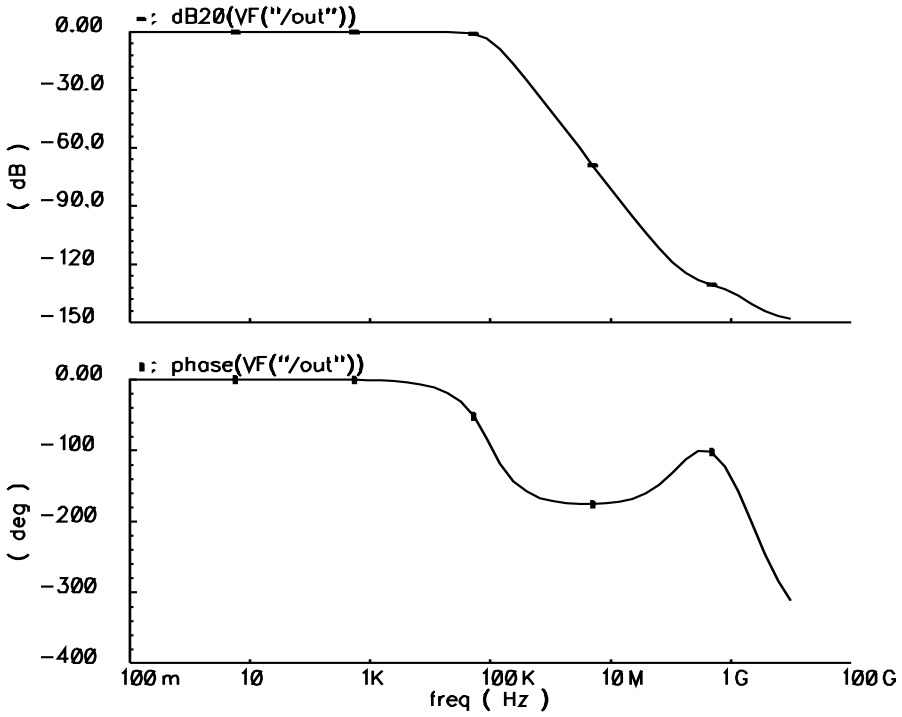

Figure 5: Frequency response of a CMOS biquad

Modulatable Sigma-Delta Frequency Synthesizer

The biquad filters mentioned in the foregoing can be applied as components of the loop filters of so called PLL based Sigma-Delta-Fractional-N frequency-synthesizers. The block level schematic of a general PLL based frequency synthesizer is shown in Figure 6. It is identical to that of a classical PLL except for the frequency divider between VCO and phase detector which ensures that the output frequency is the N-fold of the reference frequency. The key feature of a Sigma-Delta-Fractioanal-N frequency synthesizer is that the divide ratio N of the frequency divider and hence the output frequency can be varied in very fine and precise steps. This quasicontinuos adjustability allows direct modulation of the VCO while stabilized in a control loop. Thus, frequency drift or pulling due to crosstalk do not play any role when a frequency modulated signal has to be generated in a manner as simple as possible, which makes this approach especially suitable for multi-standard systems.

The Sigma-Delta Frequency Synthesizer, therefore, has become a common choice also in FSK-systems even though it suffers from one drawback: excessive densely spaced spurious tones (often falsely referred to as phase noise) pertube the output signal. To lower them the loop filter transfer function must assume very low magnitudes at relatively low frequencies. Therefore the bandwidth of the loop filter must be low and the synthesizer becomes very slow. However, the biquads mentioned in the foregoing cause a faster rolloff of the loop filter transfer function and thereby allow higher bandwidths and lower settling time at a constant spur level. Settling time is one of the most important requirements in ZigBee, since very quick startup of the transceivers is demanded.

The IMS has developed a numerical optimization tool in order to place the poles of the loop filter in an optimum way. The results of such an optimization are given in Figure 7. The settling time as a function of reference frequency is given for a PLL with and without biquadratic components in the loop filter at a constant spur level at a certain offset. Note the drastic improvement of the settling time.

Figure 8 shows a chip foto of a single VCO which was fabricated at IMS and is a substantial component of the syntheziser. It was designed to oscillate at a frequency of 2.45 GHz. Note the integrated inductors exhibiting sufficiently high Q to allow the desired frequency stability at low power consumption.

Summary and Outlook

The expertise in CMOS wireless communication circuits at the IMS provides a customer oriented design platform. The customers can focus on system aspects and device functionality while wireless connectivity is provided by the designers at IMS. One of the addressed applications is ZigBee. However, the RF activities aim at multistandard-capability and the circuit examples presented in the foregoing can be applied in Bluetooth and GSM as well.

Low noise, good linearity and low power consumption of embedded wireless transceivers is based on predefined circuit building blocks and architectures with superior performance such as high-Q filters and fast settling frequency synthesizers. They can be cointegrated with other subsystems very quickly.

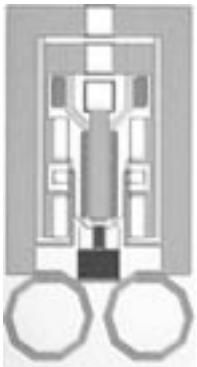

Figure 8: Chip foto of a VCO

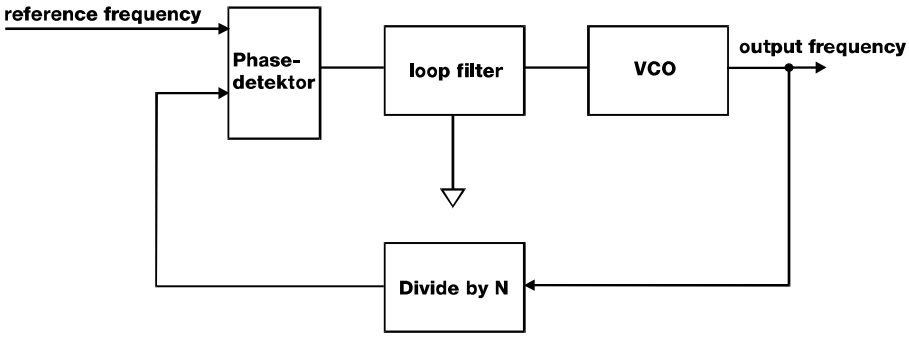

Figure 6: Block level schematic of a PLL based frequency synthesizer

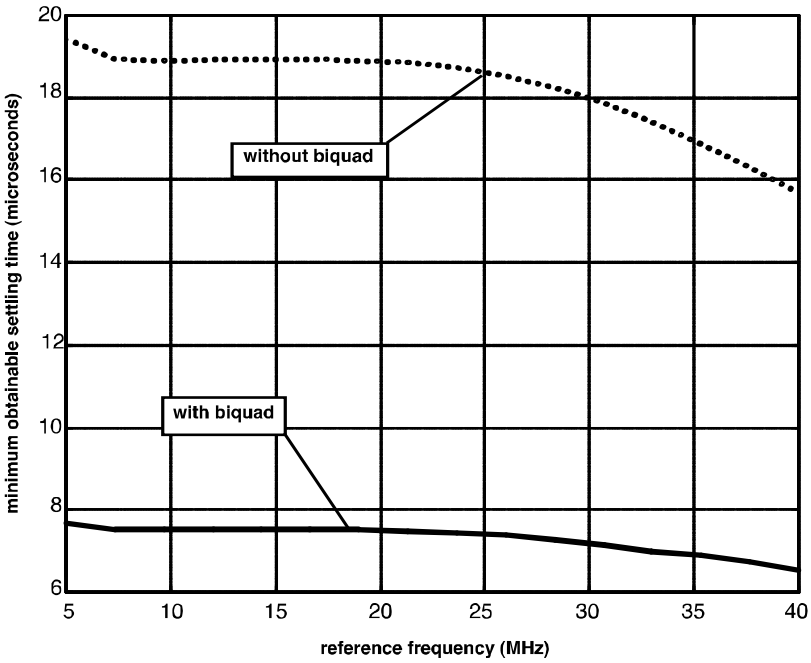

Figure 7: Settling time of a synthesizer versus reference frequency

Smart Label based Medicine Management

Dr.-Ing. G. vom Boegel, Dipl.-Ing. M. Hedtke, Dipl.-Ing. K. Scherer

1. Introduction

At present annually millions of medicines become usually uncontrolled disposed in German homes. Furthermore, no control of the taking takes place with the therapy with medicines. The treating physician gets no feedback over the accomplished dosage and can not effect by wrong or refrained usage. The false usage is in most cases not intended, but simply forgotten. The consequence of these circumstances is a wasting of therapy costs in billion height.

An improvement of this condition can be reached by a set of arrangements. First the introduction of an electronic medicine prescription is planned, so that to first step a new health map will be introduced, which includes beside the medicine data also the dosage regulations. With the use of modern IT infrastructures for data exchange between the involved partners – the physician, the pharmacy, and the patient – the electronic prescription even is useable for further purposes.

Important for control of the usage is an inventory management at home of the medicines. For this "Smart Label" technology can be used. The medicine packing is to be equipped in the future with a label (figure 1), which will already find use for logistic purposes (traceability). This label will be interrogated by a reader, which is e.g. part of the medicine box. Thus an information system existing in the house can evaluate the medicine data and can be used for new functions, e.g. a memory function.

For the avoidance of therapy costs this technology can reorganize the enposal and disposal. A delivery service can be integrated into the supply chain, including the delivery direct to the consumer.

Figure 1: Smart Labels attached to medicine packages

2. State of the art

Succes of the innovation of the micro techniques up to the massive spreading of new products at the market are to be obtained today very rarely with individual products, but with a cross-linking from most different components to a constant technical platform for new and profitable functions up to complex smart services.

The Internet has been developed in parallel to the retail trade as established instrument for product selection and order (e-Shopping). It registers constant growth rates. The classical logistic structure of the supply chain from production to the consumer is subject to new requirements. An important part of the supply chain the home delivery (last mile) is in a restructuring. A key component for intelligent environments

are ‘Smart labels’ and ‘multi-functional micro transponders’. Known are transponders for the identification of objects, as mobile data memories or as telemetriesystems for e.g. transportation monitorings.

3. System components

The topic ”smart fridge“ as a new component of the Internet is in public discussion for some time. During this view, however, only a small part of the possible functions and thus a small effectiveness is pointed out. If the goods are marked by Smart Labels, the entire stock can be captured and administered automated. Beside the refrigerator also the medicine box is included. The data are collected in a local data base. With suitable Web-based user interfaces now services can be realized and offered. This can be the order (also automatic supplementory order) of medicines, message from incoming goods as well as memory messages.

Additionally to this Internet based services also the delivery and disposal are to be included. For flexibility and increasing of security a special home delivery box (here HomeBox) is intended. The HomeBox serves for the delivery and temporary storage. The HomeBox is a access-secured ”pick-up“ box with various units for food, medicines or other goods. The supplier receives an access code for a unique delivery and places the goods into the HomeBox. The stock receipt is acknowledged and notified to the user.

Figure 2: Process chain medicine management

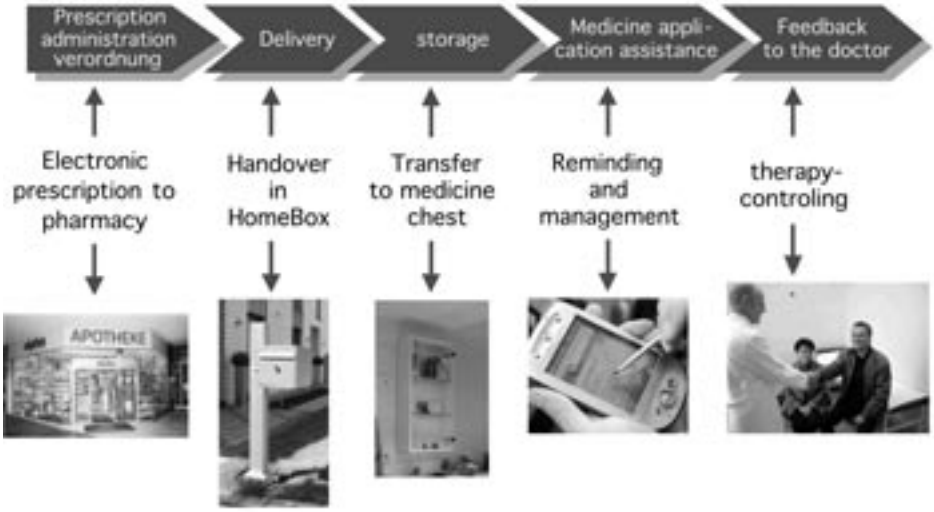

Figure 3: Reminder for an expiration date

The use of Smart Labels in the Supply Chain for Clothing

Dr.-Ing. G. vom Bögel, Dipl.-Ing. M. Hedtke, Dipl.-Ing. M. Németh

Introduction

Due to the high complexity of the logistic chain especially for clothing it is useful to show the potentials of the "Radio Frequency Identification" – technology (RFID) along the supply chain. Aspects like internationality, high quantity of participants and high quantity of necessary activity for finishing have to be considered. Smart Labels equipped within the factory escort the clothes from the production to the "point of sale". Smart Labels (or RFID labels or RFID tags) are nowadays widely used for automatic identification, they are self-adhesive labels with an integrated chip for ID-number and user data.

The Kaufhof Warenhaus AG initiated a pilot project to the RFID – implementation in clothing logistics in co-operation with partners from industry. Scientifically and technically this project is supported of the Fraunhofer society.

Figure 1: Labels attached to commodities

RFID in Logistic Chains

A condition for the smooth operational sequence of logistic processes is the employment of constantly automated identification systems. The rapid technical development and the advanced standardization of the RFID – Technology motivates more and more users to dare the step of using the technology. Simultaneous reading of several transponders (RFID tags) becomes possible, so it promises the exchange of larger data sets without visual contact (line of sight) and the data extension without the attachment of an additional data medium on the channel of distribution for a service provider and wholesale. Numerous logistic processes can be void in the future completely or arranged more efficiently.

Already **the producer,** who attaches the transponder to the clothes after the production process and writes it with data, can access the stored information. The outgoing inspection and inventory monitoring in the finished goods store, order alignment and the production of the delivery note can be automated. All necessary product information are unmistakable stored directly at the product.

The service provider, usually a specialized service provider for textile logistics also uses a camp with collection at the entrance and exit. Here the dressing (so-called 'Finishing' with water vapour up to 120 °C) is done, a commissioning, quality control (rework if necessary following). A transponder is the only possibility for identification, which is not only suitable to store all on the channel of distribution needed information but also has the resilience for the different site conditions. Thus for the service provider work procedures do not apply for the renewed labeling after the rework process also the

attachment of additional price and safety labels are void for the service provider both, since all these information on the transponder can be stored and adapted.

In **the wholesale** generally additionally an abundance of further goods is turned over, stored and picked, which can lead in connection with a large number of suppliers, receivers and a high throughput to an increased data arising. Here transponders can play a crucial role in the data accomplishment, since all necessary data is stored directly at the product without accessing a central data base for the selection of certain information. The transponder employment continues to permit large optimization potentials for all logistic operational sequence in the wholesale. Thus the possibility of the automatically identification and control procedures in the goods in is offered and to exit (no employee required). Since here no visual contact must take place to the transponder, the goods can be completely packed on the charge carrier, whereby a time-consuming sifting of each charge carrier and an individual collection of the goods are void. Besides the transponder employment offers a high transparency concerning the inventory overview and the distribution of goods in the camp. Thus goods will be known when falling below minimum stocks, ordered additionally automatically and on the basis of transponders goods in the camp can be exactly located.

Substantial advantages are offered to the **retail** for the optimization of processes in logistics by the entire product information stored on the transponder.

With the help of a at any time current inventory collection by an automatic alignment when sales and/or supply of goods, as well as an alarm function with to small shelf existence or wrong allocation in the shelf, out of stock should become the foreign word in the retail in future.

Convenience at the "Point of Sale"

Also on sides of the customers a future transponder implementation will revolutionize the shopping. So the customer can get immediately information about availability and location of the desired product. Stock on hand as well as wrongly sorted products are recognized automatically and announced, what ensures a constant disposability of existing goods to the customer. Furthermore long waiting periods at the cashes should belong to the past due to the use of transponder technology soon.

RFID in textile logistics – Pilot project of Gerry Weber and Kaufhof Warenhaus AG

A particularly interesting area of application for the RFID – technology is the clothing logistics, since here the goods go through further manufacture steps up to the store. For the first time the entire channel of distribution of the commodity is pursued by the producer up to the sales in a branch. The logistics chain, with involved Gerry Weber as a producer, Meyer & Meyer as logistic service provider and the Kaufhof Warenhaus AG with one distribution center and two stores expect from the introduction of the transponders to arrange more efficient technology their goods management and to accelerate the process cycles along the process chain.

The following functions are tested in the context of the pilot application:
– identification and control procedures in the goods in and exit of each stage without stuff
– group collection of the goods pre

and after the commissioning at the Service provider
– automatic inventory in the shops by mobile data recording equipments
– automatic collection at the cash of the shops

The transponders are programmed with product data at Gerry Weber and attached as label at the commodity (see figure 1). On the way over logistics service provider and the distribution center to the shop the data is collected at defined measuring points and put down in a central database. The characterized commodity arrive into the Gerry Webers shops at Kaufhof Warenhaus AG, where the transponder label is separated at the cash.

The pilot project analyzes carefully the performance of the RFID – system in a variety of tests at all register places in the process chain (see figure 2). Read times during transponder reading, attachment place of the label and reliability are the important factors, because for a series operation the function may not reach the technically feasible limits, the function must be reliable.

Furthermore, the RFID – technology is subject to the physical laws, so there are similar to other techniques some issues, which have to be considered. For example the reading distance is limited by the procedure of the power supply to quite short distances of about one meter, which itself in this application seams to be not a disadvantage. Rather the small reading range approve to use possible several readers in parallel in direct neighborhood with clear allocation of the read transponders.

The wireless transmission bases on law of the propagation of electromagnetic waves. Connected hereby is the influence of material properties on this propagation. So can e.g. the presence of metal objects may have positive or negative effects. As positive effect the electromagnetic field can be bundled by arrangement of suitable metallic objects, which leads to the increase of the reading distance. A negative effect can result from a shielding, if a large volume metallic object between transponders and reader shields the transponder and thus reduces the reading distance.

Further a mutual influence of the transponders can worsen the reading distance, if these lie directly one on the other. This is done via the coupling of the antennas. A minimum distance from a few millimeters is sufficient however already, in order to ensure the function. This restriction can be repaired by suitable measures with mounting and packing.

This technically – physical characteristics determine the efficiency of the system and therefore are examined and evaluated in detail.

With regard to the logistic characteristics the evaluation of the results from the pilot phase takes place at present. This will bring statements about the increase of efficiency by the introduction of RFID – technology both on the individual distribution stages and along the logistics chain. For an analyze of economic efficiency along the logistics chain all processes must be included, with which the RFID – technology offers an efficiency increase.


Figure 2: Register places in the logistic chain

List of Projects
IMS Duisburg

List of Projects
IMS Duisburg

Project Title	Partner	Project Period
Pulse Generator	Industry	07/1996-06/2003
Office 21	Industry	07/1998-04/2004
Smart Barcode	Industry	03/1998-04/2004
3D-CMOS-Sensor	Industry	07/1999-10/2003
Triangulation Sensor	Industry	10/1999-08/2003
Altitude Measurement IC	Industry	10/1999-04/2003
MIMOS-Smart Pressure Sensor 2	Industry	11/1999-01/2004
Retina Implant C	Funding Authority: BMBF	03/2000-02/2003
Retina Implant F	Funding Authority: BMBF	03/2000-02/2003
MISSY	Funding Authority: EC	08/2001-01/2004
Foundry Jamex 2000	Industry	05/2000-03/2003
IEMK-Integrated Energy Power Supplies for Mobile Systems	FhG defined Project	03/2000-12/2003
Delivery of Pressure Transponder 3	Industry	08/2000-06/2003
Bluetooth-Transceiver	Funding Authority: Local Government NRW	01/2001-12/2004
ITCS ASICs	Industry	01/2001-05/2003
Sensing People	Funding Authority: BMBF	06/2001-12/2003
3 D-CAM	Funding Authority: BMBF	04/2001-12/2003
LIVEfutura	Funding Authority: BMBF	04/2001-12/2003
Distributed Information Network	Funding Authority: BMBF/Industry	07/2001-12/2003
Intelligent Bathroom	Industry	05/2001-03/2003

Mixed ASIC 1	Industry	07/2001-12/2003
Microcontroller ASIC 3	Industry	07/2001-06/2003
Redesign Finger Print Sensor	Industry	08/2001-03/2003
Competence Center "Intelligent House"	Forschungszentrum Jülich	11/2001-10/2003
VAMOS-Sensor	Industry	12/2001-12/2003
Delivery of Memory Tag II	Industry	01/2003-12/2003
Fabrication of 100 K Temperature Transponder	Industry	10/2001-12/2003
EADS Plus	Industry	12/2001-03/2005
HELION	Forschungszentrum Karlsruhe	06/2002-09/2003
IODS – Intra Ocular Pressure Sensor System	Industry Small Redisgn	07/2002-05/2003
Tungsten Plugs	Industry	08/2002-07/2003
Delivery of Memory Tag	Industry	01/2003-12/2003
Pressure Transponder 3	Industry	08/2002-12/2003
OSGI-Gateway InHaus	Industry	08/2002-07/2003
IOS-MPC Intra Ocular Vision Aid	Gerhard Mercator University of Duisburg	09/2002-07/2003
SOLION	Forschungszentrum Karlsruhe	01/2003-12/2003
IMEX Pressure Sensor	Technische Hochschule RWTH Aachen	06/2002-11/2004
ADSLD4 ADC	Industry	10/2002-02/2003
Video ADC	Industry	09/2002-05/2004
OSGI Webserver	Industry	12/2002-05/2003
Telemetric System DiaKra	Funding Authority: BMWI	08/2003-03/2005
Study Strain Gauge Transponder	Industry	01/2003-04/2003

Study Wafer Inspection	Industry	01/2003-06/2003
Study X-Ray Detector	Industry	01/2003-04/2003
High Voltage SOI-CMOS	Industry	01/2003-12/2003
Foundry IVTMX	Industry	01/2003-12/2003
Study Embedded Internet	FhG defined Project	03/2003-12/2003
Study Smart Label	IMS defined Project	04/2003-12/2003
Difference Pressure Sensor	IMS defined Project	01/2002-12/2003
Embedded ADCs	IMS defined Project	01/2002-12/2003
Infrastructure Test House	Industry	02/2003-05/2003
VW-InHaus Connection	Industry	03/2003-12/2003
Study Tire Pressure System	Industry	03/2003-06/2003
Foundry IODS	Industry	04/2003-12/2003
Microreaktors	Funding Authority: EU, Local Government NRW, Province Gelderland	07/2003-06/2007
X-Ray Detectors I	Industry	08/2003-04/2004
X-Ray Detectors II	Industry	08/2003-04/2004
Delievery of Handheld Reader	Industry	08/2003-01/2004
Service Handheld Reader	Industry	01/2003-12/2004
Inhaus	Forschungszentrum Karlsruhe	09/2003-08/2004
Core Service InHaus	Industry	08/2003-11/2003
REOS-Digital II	Industry	10/2003-01/2004
Foundry IODS M	Industry	10/2003-03/2004
Characterisation HDR	Industry	11/2003-02/2004
Foundry Pressure Sensor	Industry	10/2003-12/2003
CIF-Sensor Fabrication	Industry	11/2003-12/2003

3D Cam	IMS defined Project	09/2002-12/2003
Innovative House Control	IMS defined Project	09/2002-12/2003
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5. Patents

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IMS 4 x 64 pixel CMOS line sensor for 3d measurement applications
IMS-Duisburg, 2003

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Board Memberships for Associations and Authorities, 2003

Dr.-Ing. G. vom Bögel

– AIM-Deutschland e. V. Industrieverband für Auto ID und BDE/MDE Systeme

– E-Logistik Plattform Duisburg/Logistik Initiative Duisburg – Niederrhein

Dipl.-Ing. W. Brockherde

– Member of the Technical Program Committee: "European Solid State Circuits Conference"

– Member of "Wissenschaftlich-Technischer Rat (WTR) der Fraunhofer-Gesellschaft"

Prof. Dr.-Ing. H.-L. Fiedler

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM)
Fachausschuss 2.3:
Produkte

Dr.-Ing. V. Grinewitschus

– VDI/VDE Gesellschaft für Mess- und Automatisierungstechnik (GMA)
Fachausschuss 1.8:
Methoden der Steuerungstechnik-Initiative "intelligentes Wohnen" des ZVEI

– "Smart House"-AK des ZVSHK

– Fachbeirat der Messe e/home

Prof. B. J. Hosticka, Ph. D.

– VDE Informationstechnische Gesellschaft (ITG)
Fachausschuss 5.4:
System- und Schaltungstechnik
Fachausschuss 5.5:
Integrierte Elektronik

– Senior Member of IEEE

Dr.-Ing. S. Kolnsberg

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM)

– Deutsche Gesellschaft für Biomedizinische Technik (DGBMT) im VDE

– Member of IEEE

Prof. Dr. rer. nat. W. Mokwa

– Member of "Wissenschaftlicher Beirat des Instituts für Schichten und Grenzflächen des Forschungszentrums Jülich"

– Member of the Program Committee: "Eurosensors"

– Head of "Gutachtergruppe 6 Mess- und Informationstechnik der AIF"

Dipl.-Ing. H.-C. Müller

– Member of "Wissenschaftlich-Technischer Rat (WTR) der Fraunhofer-Gesellschaft"

Dipl.-Phys.-Ing. J. Peter-Weidemann

– Benutzergruppe Ionenimplantation

Dipl.-Ing. J. Pieczynski

– Arbeitskreis MOS-Modelle und Parameterextraktion

Dipl.-Ing. K. Scherer

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM) Fachausschuss 8.4: Beschreibungssprachen und Modellierung von Schaltungen und Systemen

– Beirat VDE Rhein-Ruhr und Leitung Fachgruppe Mikroelektronik

Prof. Dr.-Ing. H. Vogt

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM) Fachausschuss 6.3: Gesamtprozess/Devices

Dipl.-Ing. P. Wiebe

– Universitätszentrum Medizintechnik (UZMT) an der Ruhr Universität Bochum

– Deutsche Gesellschaft für Biomedizinische Technik (DGBMT) im VDE

– Studiengemeinschaft "WORT UND WISSEN e. V."

Chronicle 2003

Micro reactors: Smaller devices for expanding markets

The University of Nijmegen, Wageningen University and Fraunhofer IMS are working since 1. 7. 2003 in a common joined project "Micro reactors: Smaller devices for expanding markets". The project is subsidized by the Euregio Rhein-Waal in the program of the common initiative (PGI) Interreg III A NL-NDS-EU. The project money is coming from the EU, the local government of NRW and the province Gelderland. Another part is coming from the involved universities and the Fraunhofer IMS. The project is running until 30. 6. 2007.

Abstract:

Because the production of so called "Bulk" chemicals (mass production of chemicals) moves more and more from the highly industrialized countries to lower industrialized countries, it becomes very important for the local chemical industry to look for new markets with high priced products and to find production processes with whom these products could be fabricated. One fabrication process, which was shown during the last years by research institutes and universities, is the micro reactor technology. With this new technology very pure chemicals with high quality and a high price level can be produced.

In the frame of this joined project all necessary components for a modular micro reaction system will be developed and the project partners will make these components available for the industry especially for small and medium sized enterprises in the fields of fine chemicals, food technology and life science.

The main challenge which has to be solved during this project is to combine the electronic part with the chemical process technology in a very small scale and to get them working together. Chemical mixers and reactors will be supervised by most modern microelectronic sensors and circuits. These sensors and circuits will be developed at the Fraunhofer IMS and will be produced in the needed quantities.

The figure 1 shows an example of a simple micro reactor. The figure 2 shows a schematic description of how electronics and micro fluidics could be combined to build a working micro reactor system.

At the end of the project so called "evaluation kits" will be available with whom the industry could start to test the new opportunities and begin to develop new products.

The project is subsidized by the following institutions.

euregio

Ministerium für Wirtschaft und Arbeit des Landes Nordrhein-Westfalen NRW.

Ministerie van Economische Zaken

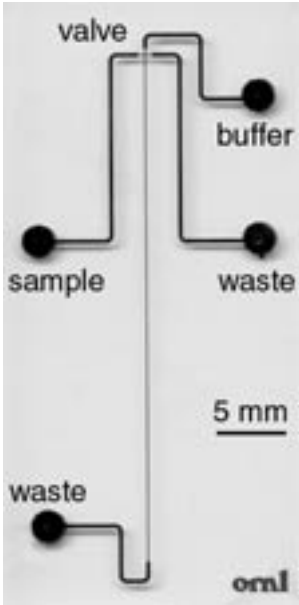


Figure 1

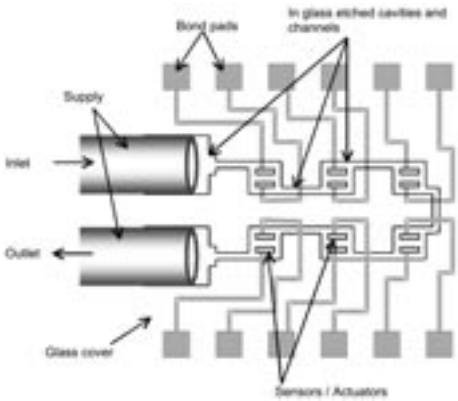


Figure 2

Intelligent security systems between theory and practice

The "smartGarden" of the Centre for intelligent house systems Duisburg, inHaus for short, measures 1.400 m². It was opend in june 2003. Here, security is the ultimate ambition.

The garden and the outdoor facilities of modern architectural objects of all kinds nowadays not only represent recreational sites as a major constituent of the residential home area, but also fire break of the house, space for design and creativity, presentational object, and last but not least venue for fauna and flora.

Landscape gardeners, garden architects, garden markets, gardening services, trade magazines, janitors, professional as well as hobby gardeners – all of these care for this area which is playing an increasingly important role in modern living in their own way.

Materials, equipment and appliances, tools and installations of all kinds help set up and maintain this open-air living-room. Even electrical engineering provides assistance in the form of lights, actuations of fountains, lawn mowers and so on.

But what can modern information technology contribute to the outdoor facilities of our houses?

The inHaus Centre for Intelligent House Systems in Duisburg demonstrates and tests the garden of the future in co-operation with its associated partners on the basis of selected themes and scenarios, such as:

gardening
– automatic irrigation, automatic maintenance of the lawn (lawnmower robot)

security
– smart entrance, smart home-delivery box, smart letter box, monitoring by webcams, as well as tele-surveillance

smart delivery and supply management
– intelligent home delivery service, for example medicaments, by use of the smart home delivery-box

interactive information outdoors
– multi-media information box for informing visitors, also interactive

tele access
– remote controlled monitoring and control of functions via the internet

design
– garden furniture, garden houses, garbage cans, fountains, objects of art, design of the garden, light scenarios

Press Review

Hoher Besuch in der Kraftzentrale: Margeritha Bullinger, Bundeskanzler Gerhard Schröder, Prof. Hans-Jörg Bullinger (Präsident Fraunhofer-Gesellschaft) und NRW-Bauminister Michael Vesper. **WAZ-Bilder (2): Ulla Michels**

Spitzenforscher feierten im alten Hüttenwerk

Kanzler war Gast beim Fraunhofer-Fest

Von Rolf Kiesendahl

Stärker kann ein Kontrast kaum sein: Im alten Meiderich Hüttenwerk feierte die Fraunhofer Gesellschaft, Europas größte Denkfabrik, ihr „Fest der Forschung". Industriegeschichte traf auf Spitzentechnologie. Da war sogar der Bundeskanzler begeistert.

Anlässlich ihrer Jahrestagung hatte die europaweit größte Organisation für angewandte Forschung nach Aachen, zur Mitgliederversammlung nach Oberhausen und zum Festakt in den Landschaftspark gebeten. Eine prima Gelegenheit für den Standort, sich mehreren hundert Wissenschaftlern - viele gehören zur Crème der deutschen Forschung - zu präsentieren.

„Sind wir noch gut genug?", fragte zu Beginn Prof. Hans-Jörg Bullinger, der Präsident der Fraunhofer-Gesellschaft - und kam zu dem Ergebnis, dass Deutschland beim Forschungsaufwand nur Mittelmass verkörpere. „Wir wollen nicht, dass zu viele Forscher deshalb die Grenze überschreiten", sagte Bullinger. Der „Rohstoff" ginge ansonsten verloren.

Höflicher Beifall, als Bundeskanzler Gerhard Schröder in die Kraftzentrale einzog. Starker Applaus, als er sie nach seiner Rede sofort wieder verließ. In gut 40 Minuten machte der Kanzler klar, dass an der Reform der sozialen Sicherungssysteme kein Weg vorbei führe. Nur so könne der Zusammenbruch dieser Systeme vermieden werden. Und nur so könne man jene Ressourcen freibekommen, die für Forschung und Entwicklung, für Bildung und Kinderbetreuung benötigt würden. Letzteres, so Schröder, um Familie und Beruf vereinbar zu machen und das „Reservoir gutausgebildeter Frauen" nutzen zu können. Das Problem Deutschlands sei nicht die Armut, sondern eine Unbeweglichkeit, die aus vergangenen Erfolgen resultiere. Um wieder Erfolg zu haben, müsse diese Unbeweglichkeit überwunden werden. „Wir müssen aus den Subventionen der Vergangenheit Investitionen in die Zukunft machen", rief Schröder - und outete sich nebenher als Montan-Experte. „Hier steht was von Stahlwerk. Dabei sind wir in einem Hüttenwerk. Denen werde ich den Unterschied mal klarmachen", schrieb er seinen Redenschreibern ins Stammbuch.

Vor Beginn der multimedialen Wissenschaftsshow hatte dann OB Bärbel Zieling Gelegenheit, einen Duisburger Träger des Hugo-Geiger-Preises zu ehren. Andreas Schmidt vom Institut für Mikrolektronische Schaltungen (IMS) ist die Entwicklung einer Software gelungen, die eine gesunde Netzhaut simulieren kann.

Andreas Schmidt (l.) vom Duisburger IMS wurde 2. Preisträger des renommierten Hugo-Geiger-Preises.

WAZ 23.10.03

Der geniale Erfinder

Siemens-Erfinderpreise 2002 vergeben

Siemens hat im vergangenen Geschäftsjahr 2002 rund 7000 Erfindungen zum Patent angemeldet. Zwölf „Erfinder des Jahres" wurden am 17. Dezember von Vorstandschef Heinrich v. Pierer im Siemens Forum in München ausgezeichnet. Einer davon ist Peter Mengel aus München, der mit seinem Team eine Kamera auf einem Chip gebaut hat, die in extrem kurzer Zeit dreidimensionale Bilder liefert. Das System funktioniert mit einem Lichtblitz im unsichtbaren Bereich des Spektrums und einem Sensor mit ultraschnellem elektronischen Verschluss. Aus der Zeit, die das Licht zum Objekt und zurück zum Sensor benötigt, wird das Bild errechnet. Mit der Technik, die zusammen mit dem Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme in Duisburg entwickelt wurde, soll eine Kamera arbeiten, die die Reaktion eines Airbags an die Sitzposition der Insassen anpasst.

Die Magnetresonanztomographie (MR) ist eine wichtige Methode für die strahlenfreie schichtweise Untersuchung von weichem Körpergewebe, wie Leber, Muskeln oder Knorpel. Dabei werden die extrem schwachen Signale von Wasserstoffatomkernen aufgezeichnet, die ihre Ausrichtung in einem starken Magnetfeld ändern. Die Methode hängt von vielen Einstellparametern ab. Bisher konnte es sein, dass das nach der Messung erzeugte Bild keine ausreichenden Gewebekontraste hatte. Dann musste die Aufnahme mit anderen Parametern wiederholt werden. Michael Deimling aus Erlangen hat ein Verfahren entwickelt, das es erlaubt, die Kontraste eines Bildes auch nach der Messung zu optimieren. Das erleichtert Ärzten ihre Diagnose und spart Zeit bei der Untersuchung im Krankenhaus.

Messtec 1.3.03

Land fördert Projekte mit 81,7 Mio €

Für wichtige Zukunftsprojekte in Duisburg hat die Landesregierung eine Förderung von zusammen 81,7 Mio Euro beschlossen. Im gesamten Ruhrgebiet sind 49 Projekte bewilligt, weitere 20 in der konkreten Planung. Damit sind bis heute für diese Vorhaben mehr als 600 Millionen Euro Fördermittel bewilligt.

In Duisburg werden folgende Projekte gefördert: Zentrum für Brennstoffzellentechnik (14,8 Mio € Fördermittel), Erweiterung des FhG Instituts IMS für mikrobiologische Schaltungen (20,4 Mio €), Ausbau logport (34,3 Mio €), Kompetenzcenter Logistik (1,3 Mio €), Landschaftspark Duisburg Nord, Gebläsehalle und Kraftzentrale (10,6 Mio Euro), World Games 2005 (300 000 €).

WAZ 16.10.03

Das Retina-Implantat besteht aus einer künstlichen Augenlinse mit integriertem Empfangssystem, einer hochflexiblen Mikroverkabelung und der Stimulationsstruktur

Eine Prothese zum Sehen

Millionen Menschen haben ihr Augenlicht durch Netzhauterkrankungen verloren. Forscher arbeiten an einer elektronischen Sehprothese. Sie soll den Betroffenen etwas Augenlicht wiedergeben.

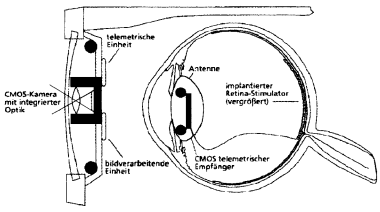
Nachtblindheit, Einengung des Gesichtsfeldes, langsamer Verlust des Kontrast- und Farbensehens - dies sind die ersten Anzeichen für eine Zerstörung der Netzhaut (Retina). Nach und nach sterben die lichtempfindlichen Zellen der Netzhaut ab. Und wo keine Reize mehr durchkommen, empfangen auch die Sehnerven im Augapfel keine Informationen mehr. Die Welt versinkt im Dunkel. Schleichend, im Lauf von vielen Jahren führt die Erbkrankheit Retinitis Pigmentosa zur Erblindung. Insgesamt leiden etwa ein bis drei Millionen Menschen - in der Bundesrepublik Deutschland etwa 30 000 bis 40 000 - an der derzeit noch unheilbaren Krankheit. Forscherteams in aller Welt arbeiten daran, den Patienten zu helfen. Ihr Ziel: Die Entwicklung einer Sehprothese. Mit dem Retina-Implantat sollen die Betroffenen künftig wieder die Form und Position größerer Objekte erkennen können.

Die Forscher nutzen dabei eine Besonderheit der Krankheit: Bei Retinitis Pigmentosa werden nur die lichtempfindlichen Zellen zerstört. Die Nerven, die die Informationen an das Gehirn weiterleiten, sind noch intakt. Überbrückt man die defekte Netzhaut - so die Vision der Wissenschaftler - könnten die Blinden auch wieder sehen. Allerdings ganz wieder herstellen lässt sich das Sehvermögen nicht. „Die Betroffenen werden mithilfe der Sehprothese wieder die Umrisse größerer Objekte sehen können", dämpft Dr. Ingo Krisch zu große Erwartungen. Der Physiker des Fraunhofer-Instituts für Mikroelektronische Schaltungen und Systeme IMS arbeitet gemeinsam mit Medizinern, Neuroinformatikern, Mikroelektronikern, Materialforschern in dem Projekt „Retina-Implant-EPI-RET". Schon seit 1995 wird an der elektronischen Sehprothese geforscht. Nun liegt das neue Retina-Implantat vor und wird im Tierversuch getestet.

„Retina-Implant ist eine lernfähige Sehprothese, die die Funktion des geschädigten Teils der Netzhaut überbrücken soll", erläutert Dr. Ingo Krisch das System. Teil der neuartigen Sehhilfe ist eine Hightech-Brille, in die eine winzige Videokamera und Encoder integriert wird. Der Encoder rechnet die Bildinformationen in nerventaugliche Signale um. Diese werden drahtlos zu einem Empfänger im Auge übertragen und dann über implantierte Mikrokontakte an die Nerven der Netzhaut weitergegeben.

An dem Forschungsvorhaben sind neben diversen Projektpartnern (s. Kasten) verschiedene Fraunhofer-Institute beteiligt. Das IMS entwickelt das Bildaufnahmesystem, den Sender, die Empfangs- und Stimulationselektronik sowie dreidimensionale Elektroden. Außerdem arbeiten die IMS-Forscher eifrig daran, das Implantat monolithisch zu integrieren. Das Fraunhofer-Institut für Bio-

Eine Videokamera in der Hightech-Brille nimmt Bildinformationen auf, ein Encoder rechnet diese in nerventaugliche Signale um. Sie werden zu einem Empfänger im Auge übertragen und über implantierte Mikrokontakte an die Nerven der Netzhaut weitergegeben



beide Abbildungen: Fraunhofer Magazin

Forscher zeigen den Garten der Zukunft

Im Duisburger Innovationszentrum „Intelligentes Haus" – kurz: inHaus – entwickeln und testen Forscher des Fraunhofer Instituts für Mikroelektronische Schaltungen und Systeme (IMS) gemeinsam mit Partnerunternehmen das vernetzte Heim der Zukunft. Das Herzstück des Projekts bildet eine Anlage mit einem experimentellen Wohnhaus, einem Werkstatthaus und einem Multimedia-Fahrzeug. Neu hinzugekommen ist jetzt ein „intelligenter" Garten (Bild ❶), in dem der Gebäudeaußenbereich von morgen untersucht und vorgestellt wird. Dazu gehören eine automatische Bewässerung und eine Rasenpflege per Mähroboter. Im Rahmen der integrierten Sicherheitstechnik stellen die Fraunhofer-Forscher auch den Hauseingang von morgen mit Transponder-, Fingerabdruck-, Gesichts- und Spracherkennung vor. Der Briefkasten meldet eingehende Post, vernetzte Kameras überwachen das Gelände. Eine spezielle Box am Eingang ist Bestandteil eines ausgeklügelten Bestell- und Heimlieferservices, ein Multimedia-Terminal stellt Besuchern interaktive Informationen zur Verfügung. Fast alle Funktionen lässen sich auch über das Internet überwachen und steuern.

Elektropraktiker 01.08.03

Augen Licht 1.4.03

Logistik

Probelauf für die RFID-Technik

Was Transponder-Etiketten in der Praxis bringen, soll ein dreimonatiges Pilotprojekt mit Kaufhäusern und einem Textilunternehmen zeigen. Als Berater beteiligen sich das Duisburger Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) sowie das Institut für Materialfluss und Logistik (IML) in Dortmund.

Industrieanzeiger 29.09.03

Grenzüberschreitende Zukunftstechnologien

Symposium zur Nanotechnologie unter Beteiligung der Niederrheinischen IHK

Am 18. März fand im Mercator Technology & Science Park in Nimwegen das Symposium „Nano- und Mikrosystemtechnologie mit Anwendungen in Life Sciences, Chemie, Pharma und Ernährungstechnologie" statt.

Die Veranstaltung bot Forschern, Unternehmern und weiteren Interessierten die Gelegenheit, sich über die neuesten Entwicklungen im Bereich der Nano- und Mikrosystemtechnologie zu informieren. Ziel des Symposiums war es zu zeigen, dass die Anwendung dieser neuen Technologien auch neue Perspektiven und Möglichkeiten für die Betriebe in der Region bietet. Dieser Miniaturisierungsprozess, der zuerst einen Umbruch im Informations- und Kommunikationsbereich auslöste, ist jetzt auch dabei, in den Bereichen Life Sciences, Chemie, Pharma und Ernährungstechnologie für eine grundsätzliche Veränderung zu sorgen. In den Fachvorträgen erläuterten die Referenten der Universitäten Nimwegen und Wageningen, des Fraunhofer Instituts für Mikroelektronische Schaltungen und Systeme Duisburg (IMS), des niederländischen Chemie- und Life Scienceskonzerns DSM und des niederländischen Unternehmens Aquamarijn Micro Filtration B.V. neue Entwicklungen und Anwendungen der Nano- und Mikrosystemtechnologie und stellten Beispiele aus den medizin- und ernährungstechnologischen Bereichen vor. In den anschließenden Gesprächen mit Referenten und Teilnehmern konnten die Kenntnisse über diese technologischen Fortschritte weiter vertieft werden.

Das Symposium, das im Rahmen des grenzüberschreitenden Technologie Netzwerkes Rhein/Waal organisiert wurde, war mit etwa 90 Teilnehmern eine erfolgreiche Veranstaltung. Das Technologie Netzwerk Rhein/Waal ist ein Zusammenschluss der sieben Technologiezentren und -Parks in der Euregio Rhein-Waal, der Niederrheinischen Industrie- und Handelskammer sowie der niederländischen Kamer van Koophandel Centraal Gelderland.

Die Projekte des Netzwerkes werden kofinanziert durch das EU-Programm INTERREG IIIA der Euregio Rhein-Waal sowie durch die Wirtschaftsministerien der Niederlande und Nordrhein-Westfalens. ■

Weitere Informationen zum Symposium und zum Technologie Netzwerk Rhein/Waal erhalten Interessenten bei der Geschäftsstelle des Netzwerkes im Technologie-Zentrum Kleve, Boschstraße 16, 47533 Kleve, Telefon 0 28 21/89 45 80, E-Mail tzk.brut@t-online.de

Thema Wirtschaft 9.6.03

„..ich seh in 3D!"

Dreidimensional sehende CMOS Bildsensoren

In den letzten Jahren ist eine stetig steigende Nachfrage nach Lösungskonzepten für intelligente Kameras und Sensoren, welche Anwendungen der industriellen und automotiven Bildverarbeitung integrieren, zu verzeichnen. Dieser Artikel zeigt die Möglichkeiten, die die sog. 3D-CMOS-Bildsensorik in diesem Zusammenhang bietet. Insbesondere auf dem Gebiet der Überwachung von Gefahrenbereichen, durch aktive Erfassung der gefährdeten Personen, besteht ein hoher Bedarf an zuverlässigen Sensorsystemen. Hierfür sind neben dem reinen Kamerabild aussagekräftige Parameter über die Szenenobjekte zu ermitteln. Aktive Sensoren wie z.B. IR-Sensoren mit integrierten, pulsgetriebenen IR-Sendern gewinnen dabei zunehmend an Bedeutung. Durch geeignete IR-Ausleuchtung lassen sich Objekte erkennen und im 3D-Raum vermessen. In enger Zusammenarbeit mit der Siemens AG wurden vom Fraunhofer Institut für Mikroelektronische Schaltungen und Systeme (IMS) in Duisburg 3D Kamerasysteme entwickelt, die dreidimensional „sehen" können.

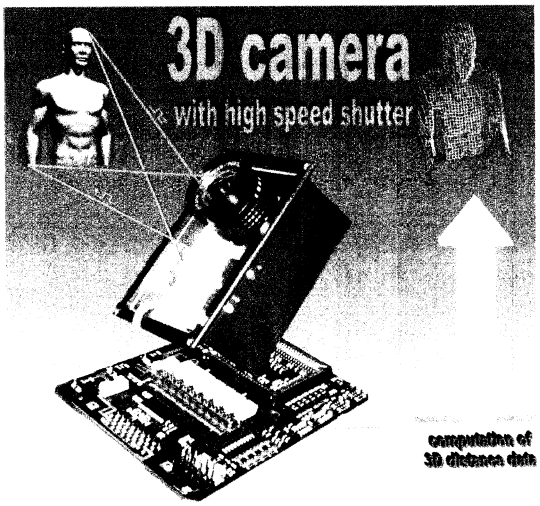


Abb. 1: Prinzip der „Time Of Flight" (TOF) Messmethode

Existierende 3D Messsysteme können lediglich eine 2D Projektion einer dreidimensionalen Szene bei gleichzeitig hoher Empfindlichkeit gegenüber Hintergrundlicht, Reflektanzvariationen und bewegten Objekten aufnehmen. Ihre Zuverlässigkeit ist daher oft nicht zufriedenstellend und nicht ausreichend für Anwendungsgebiete in der Sicherheitstechnik, Überwachung, Automotive, Transportsteuerung, Automatisierung, etc. Das neuartige 3D CMOS-Kamerasystem nimmt eine echte 3D Messung durch Verwendung der sogenannten „Time Of Flight" (TOF) Messmethode mit Kurzzeit-Pulslaser-Beleuchtung vor. Die TOF-Messmethode berechnet die Abstandswerte basierend auf der Laufzeit eines Laserpulses und Mehrfachbelichtung („multiple double short time integration"- MDSI-Prinzip). Das Prinzip ist in Abb. 1 gezeigt.

Laufzeitbasierte 3D-Abstandsmessung

Je größer die Objektentfernung, desto länger dauert es, bis der vom Objektpunkt reflektierte Laserpuls wieder den 3D CMOS-Sensor erreicht. In CMOS-Technologie werden die empfangenen Laserpulse auf dem Chip weiter analog vorverarbeitet. Reflektanz- und Beleuchtungsunabhängigkeit werden mittels einer Doppelbelichtung, die durch Auslese zweier Bilder bei zwei verschiedenen Shutterzeiten realisiert wird, erreicht. Der Vorgang wird mit einer Folge von Laserpulsen wiederholt (multiple accumulation), um zum einen ein hohes Signal-/Rauschverhältnis zu erzielen und zum anderen die einzusetzende Laserleistung noch weiter zu reduzieren (Augensicherheit). Die nachfolgende digitale Signalverarbeitung berechnet daraus die Abstandswerte. TOF-MDSI Zeilensensoren erreichen lateral eine Auflösung bis 128 Pixel bei einer Entfernungsauflösung

Messtec 1.4.03

TECHNIK

Sensor im Reifen

Winzige Sensoren für Lkw-Reifen hat Michael Bollerott vom Fraunhofer-Institut für Mikroelektronische Schaltungen (IMS) in Duisburg entwickelt, die ohne eigene Energieversorgung Druck und Temperatur messen. Zwar warnen ähnliche Sensoren bereits in manchen Luxuslimousinen den Fahrer vor bald platzenden Reifen. Deren Batterie aber hat nur eine begrenzte Lebensdauer. Deshalb strahlen die IMS-Ingenieure von außen ein elektromagnetisches Feld auf ihren Transponder und versorgen so den Sensor ohne Batterie mit Energie. Auf einer Fläche von 2,5 mal 3,2 Millimetern haben die Forscher einen Energiewandler, Sensorelemente, einen Mikroprozessor, einen Speicher und einen Sender untergebracht. Der Transponder wiegt knapp 100 Gramm und wird in der Nähe des Ventils montiert. Über einen Empfänger registriert der Sensor sowohl Druckverluste als auch steigende Temperaturen, so dass rechzeitig vor dem Platzen eines Reifens gewarnt werden kann. *RHK*

Die Welt 15.8.03

Chip fährt im Reifen mit

Am Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) in Duisburg wurde ein Transponderchip entwickelt, der im Reifen mitfährt und drahtlos Reifendruck und Temperatur übermittelt. Bei dem nur 2,5 mal 3,2 Millimeter großen Miniwächter sind alle Schaltungsbestandteile auf einem Siliziumbaustein vereint.

Rheinische Post 2.7.03

LOGISTIK: permanente Inventur per Transponder

In einem dreimonatigen Pilotprojekt testet jetzt die Kaufhof Warenhaus AG zusammen mit dem Textilunternehmen Gerry Weber eine Technik zur berührungslosen Datenübermittlung per Transponder-Etikett. Dabei werden sie beraten vom Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme IMS und dem Institut für Materialfluss und Logistik IML. Die verwendeten Transponder arbeiten auf Basis der Radio-Frequency-Identification-Technik (RFID). Ähnlich wie Etiketten zur Warensicherung bestehen sie aus einem kleinen Speicherchip, der detaillierte Informationen über das Kleidungsstück enthält, und einer Antenne. Sobald ein Hemd eine Schleuse mit Sende- und Empfangseinheit passiert, sendet der Transponder alle Informationen über Farbe, Größe oder Artikelnummer. Im Wareneingang lassen sich so ganze Stangen an Bekleidung automatisch erfassen, ohne dass sie in die Hand genommen werden müssen. Die technische Herausforderung liegt im möglichst schnellen Auslesen der Transponder. „Im Gegensatz zu einem Sicherungsetikett geht es nicht nur um die geringe Informationsmenge ›scharf - entschärft‹, sondern um alle Daten des Artikels", erklärt IMS-Forscher Dr. Gerd vom Bögel. Durch die RFID-Etiketten (Tags) lässt sich die gesamte logistische Kette vom Hersteller über das Kaufhof-Lager bis zu den beiden am Projekt beteiligten Filialen in Münster und Wesel verfolgen. Der Transponder ist ein robustes Identifikationsmittel auf dem langen Weg der Qualitätskontrolle, Nachbearbeitung, Versand. Im Verkaufsraum selbst können die Mitarbeiter den Bestand mit mobilen Lesegeräten erfassen. Zusätzlich registrieren Lesegeräte am Regal Warenbewegungen. Auch an den Kassen sind Leser angebracht, um die Abwicklung zu beschleunigen. Beim Verkauf werden die Transponder schließlich entfernt. Tel. 0203-3783-228, Fax -266 und Tel. 0231-9743-310, Fax –211, E-Mail: gerd.vomboegel@ims.fraunhofer.de - Internet: http://www.ims.fraunhofer.de/

Wirtschaft-Wissenschaft-Politik 8.9.03

MEDIZIN

Messsonde in den Adern

■ Wie ein Bergsteiger, der sich mit Händen und Füßen in eine Felsspalte, einen so genannten Kamin klemmt, hält sich eine Sonde in der Ader fest. Sie fährt drei kleine Beinchen aus, die sich gegen den Blutstrom stemmen. Die Sonde, voll gestopft mit Elektronik, misst vor Ort die wesentlichen Kennwerte des Blutkreislaufs: Blutdruck und Temperatur. Der integrierte Sender übermittelt die Daten an einen Speicher, den der Patient am Körper trägt. Die Sonde, die einen Durchmesser von nur zwei Millimetern hat, wird mit einem Katheter in eine Ader im Pobereich befördert, die besonders leicht zu erreichen ist. Bisher sind Langzeitmessungen, die für die Einschätzung der Risiken bei Hochdruckpatienten wichtig sind, nur mit lästigen, automatisch arbeitenden Geräten möglich, bei denen in regelmäßigem Abstand eine Manschette am Oberarm aufgeblasen wird. Dazu sind diese Messungen unpräzise. Die Sonde haben Werkstoffwissenschaftler und Ärzte an der Technischen Hochschule Aachen und am Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme in Duisburg entwickelt.

ELEKTRONIK DER MINIATURSONDE ZUR BLUTDRUCKBESTIMMUNG Ersatz für die lästige Manschette, die für jede Messung automatisch aufgeblasen wird

Die Wirtschaftswoche 20.2.03

Industrieanzeiger 3.2.03

Fraunhofer IMS

Software beschleunigt Internet-Übertragung in mobile Endgeräte

Das Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS), Duisburg, hat eine Software entwickelt, die die Übertragung von Internet-Inhalten in mobile Endgeräte um das Zwei- bis Dreifache beschleunigen soll. Nach Angaben der Forscher reduziert die sogenannte Kompressionssoftware die Auflösung von Grafikelementen und komprimiert sie, ohne dass der Nutzer es merkt. Bei mobilen Endgeräten wie PDA oder Palmtop sei es wegen der geringen Auflösung der Displays gar nicht notwendig, die Elemente einer für große Monitore produzierten Website hochauflösend zu übertragen, erklären die Wissenschaftler die Idee. Das Verfahren funktioniert den Angaben zufolge mit allen Geräten, die die Programmiersprache Java unterstützen.

Smartgarden: Einen von IT-Systemen gemanagten Garten hat das **Fraunhofer-Institut für Mikroelektronische Schaltungen** in der Demoanlage Inhaus Zentrum für intelligente Haussysteme in Duisburg aufgebaut. Der Smartgarden bewässert sich selbst und sorgt für geschnittenen Rasen. Er gehört zur zentralen deutschen Testeinrichtung für Domotik und Hausvernetzung.

Computer Zeitung 23.6.03

Datenkompressor für den PDA

Alexander Coers vom Fraunhofer Institut hat einen Proxy-Server entwickelt, der Internet-Seiten dreimal schneller als üblich an Personal Digital Assistants (PDAs) schickt. Er reduziert dabei vornehmlich Bilddaten auf das passende Format. Zwar bieten auch Provider solche Kompressionen an, doch schränkt dies die Nutzer auf vorangemeldete Seiten ein. Bei der Fraunhofer-Lösung fordert der PDA-Browser beliebige Seiten bei einem Proxy-Server an.

CIO-IT-Strategie für Manager 1.3.03

Das „intelligente Haus" des Fraunhofer-Instituts verblüfft mit seinen Fähigkeiten. So könnte die Lieferbox anzeigen, wenn das Pizzataxi geliefert hat. Ingenieur **Michael Hedtke** kam die Idee dann aber doch etwas seltsam vor: „Das ist wohl nur Theorie. Wenn das Pizzataxi kommt, würde ich die Pizza lieber selbst in Empfang nehmen – sie wird doch sonst kalt."

Rheinische Post 28.6.03

Nach dem Haus wird jetzt auch der Garten schlau

FORSCHUNG / Ein Garten, der sich selbst bewässert, den Rasen schneidet und selbst bewacht.

STEFAN ENDELL

In Duisburg, auf dem Gelände der Universität an der Lotharstraße, so haben wir schon mehrfach berichtet, steht das schlauste Haus Deutschlands. Es kann hören, sehen, sprechen, selbstständig telefonieren, Licht, Wasser und Strom bedienen und noch viel mehr. Jetzt hat das intelligente Haus - eine europaweit einmalige, Hersteller unabhängige Test- und Demonstrations-Anlage des Fraunhofer Instituts für mikroelektronische Schaltungen und Systeme - eine kleine Schwester bekommen: Den „SmartGarden", was soviel heißen soll wie „der intelligente Garten." Gestern war Besuchstag im „SmartGarden".

Im Garten der Zukunft geht alles automatisch

Genau wie beim großen Bruder geht es auch im Garten der Zukunft zu: alles automatisch, alles auch ganz aus der Ferne über ein Laptop im Urlaubshotel oder über ein modernes Handy bedienbar. Zum Beispiel die Bewässerung des Gartens. Vom Urlaubsort kann der besorgte Hausbesitzer feststellen, ob auch daheim im Garten schädliche Trockenheit ausgebrochen ist, oder ob die heimische Bewässerungsanlage gesteuert durch Feuchtesensoren im Boden brav gegen die starke Trockenheit angekämpft hat.

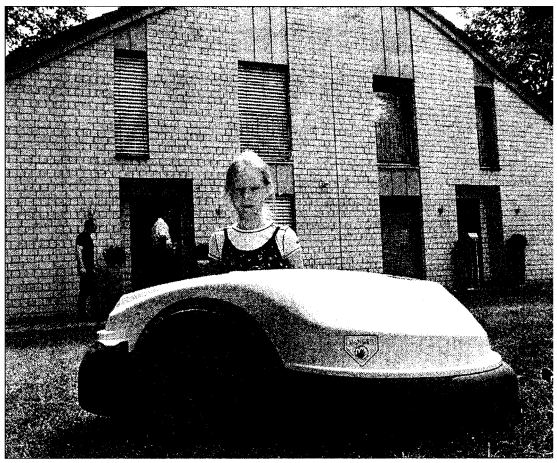
Zurück vom Urlaub hat der Gartenbesitzer keinerlei Lust aufs Rasenmähen, er kann es von einem Rasenmäh-Roboter erledigen lassen. Selbstständig brummt er nach einem Startbefehl sytematisch übers Grün und häckselt den Grünschnitt so klein, dass er wieder auf den Rasen fallen darf.

Um das Haus herum im Garten: Beleuchtung auf Wegen und Stegen, in Bäumen, im Boden, am Dach und natürlich Überwachungs-Kameras. Diese auch an der smarten Haustüre, wo eine Kamera die biometrischen Daten (Augen, Kopfform etc.) des Einlass-Begehrenden abliest, oder die Stimme abfragt bzw. einen Fingerabdruck verlangt. Ist er einlassberechtigt, öffnet sich die Türe automatisch. Alles gesteuert - wie auch die Technik im Haus - über ein einziges vernetztes System, auf dass der Nutzer immer auch von außen via Internet zugreifen kann.

Vergessen wir nicht die „Homebox": Ein schlaues Kästchen an der Eingangstüre oder freistehend im Garten: Hier hinein legt der Lieferant (z.B. die von außerhalb per Internet oder Handy) bestellte Ware. Liegt die Ware in der Box, meldet sie an ihren Besitzer: Das Medikament YX liegt in der Box. Woher die Box das weiß? Weil auch das Medikament schon aus der Zukunft stammt: Es hat bereits ein „smart Label" - ein Funketikett

■ **www.inhaus-duisburg.de**

NRZ 28.6.03



Kinder, Finger weg: Dieser Rasen-Mäh-Roboter zieht selbstständig und systematisch seine Wege über den Rasen. Er ist Teil des „Smart Gardens", den gestern das Fraunhofer IMS vorstellte. (Foto: Foltin)

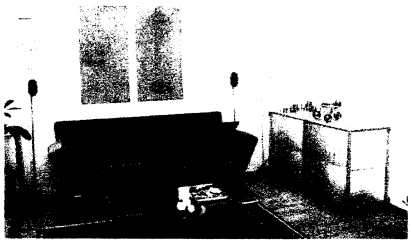
Von außen ein ganz normales Wohnhaus: Das „Wohn-Labor" des Fraunhofer IMS in Duisburg.

Das Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) betreibt in Duisburg das Innovationszentrum intelligentes Haus. Haustechnische Systeme gibt es mittlerweile wie Sand am Meer: Ob Jalousiesteuerung, Türsprechanlage, EIB, ISDN, Computernetzwerk oder Unterhaltungselektronik: Der Systemgedanke verdrängt immer mehr die isolierten Einzelgeräte. Aber wie kann man diese vielen unterschiedlichen Systeme sinnvoll miteinander verbinden? Das Fraunhofer IMS arbeitet an der Lösung, und G&H hat sich das Haus angesehen, in dem die Systemvernetzung zur Vollendung gebracht wird.

Sonja Pfaff

Aus Inseln wird ein sinnvolles Ganzes

Besuch im Innovationszentrum intelligentes Haus



Vom Feinsten: Innenarchitekten haben die Gestaltung des bewohnbaren Bereichs des In-Hauses übernommen. Selbst die Möbel wurden in das Netzwerk integriert. Je nach gewünschter Stimmung werden die Glasschränke in unterschiedlicher Farbe und Intensität beleuchtet.

Das moderne Zweifamilienhaus befindet sich mitten auf dem Duisburger Universitätsgelände. Eingerahmt von Instituten und Forschungszentren fällt es erst auf den zweiten Blick ins Auge. Wäre da nicht die rot-weiße Schranke, die die Zufahrt absperrt, dann sähe es mit seiner Weihnachtsbeleuchtung an diesem trüben Wintertag wirklich aus wie das gemütliche Wohnhaus einer ganz normalen Familie. Doch schon an der Haustür stellt man fest, daß hier alles etwas anders ist. Statt einen Schlüssel aus der Tasche zu ziehen, öffnet Klaus Scherer, der uns durch das Haus führen wird, die Haustür per Fingerabdruck. Hand Auflegen genügt – schon öffnet das Schloß, und die Haustechnik weiß auch schon, wer gerade hereinkommt. Ein persönlicher Gruß ertönt aus dem Lautsprecher neben der Tür.

Auch sonst ist das Haus gespickt mit allen technischen Finessen, die die Elektronik-Industrie heute bietet. An der Wohnzimmerwand prangt wie ein Gemälde ein Plasmabildschirm gleich

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