Challenges in TCAD Simulations of Tunneling Field Effect Transistors

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Introduction

- Tunneling field effect transistors (TFETs) have potentially a better sub-threshold behavior than conventional MOSFETs, inverse sub-threshold slope S can be lower than 60 mV/dec at room temperature in TFETs
- Therefore, TFETs can have potentially lower leakage currents and are promising candidates for low power applications
- Not only leakage currents are low in TFETs, on-currents also are low → optimization of TFETs is necessary → TCAD simulation → Quantitative tunneling models are necessary
- State-of-the-art: The results of conventional tunneling models dramatically differ among themselves and distinctly deviate from experimental results
- Goal of this work: To find physical models that can reproduce the results of electrical measurements on TFETs and to find such model parameters which allow a quantitative modeling of TFETs

Models for tunneling simulation in field effect transistors (1)

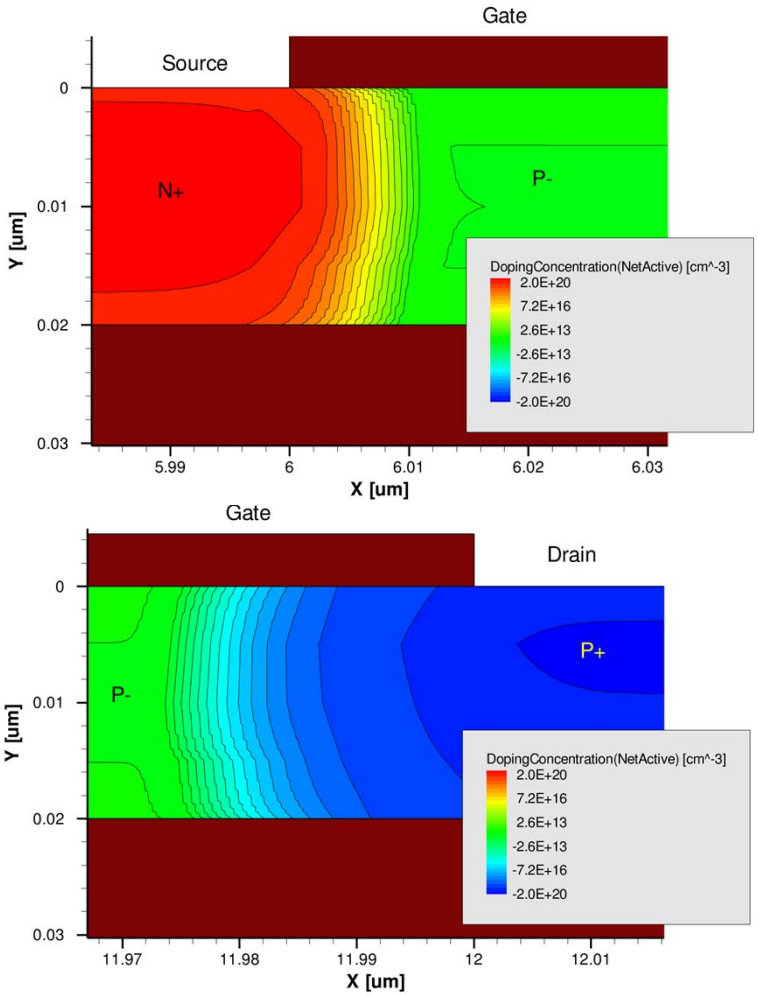
- Tunneling effect have to be considered not only in specially designed TFETs, but always when the electric field in semiconductor material is high and energy bands of electron and holes are strongly bent.
- Conventional tunneling models use the approximation of a mean local electric field, electrons and holes are assumed to be generated due to tunneling effect at the same place where the relevant field is located
- Several variants of local band-to-band tunneling models were tested
  - Kane model, *J. Appl. Phys. 1961, v. 32, p. 83.*
  - Hurkx model, *IEEE Trans. ED, 1992, v. 39, p. 339.*
  - Schenk model, *Solid-State Electronics 1993, v. 36, p. 19.*
- Implementation of these models in Sentaurus Device of Synopsys was used in numerical simulations

Models for tunneling simulation in field effect transistors (2)

- Non-local tunneling models: Difference in the location of electrons and holes created due to tunneling effect is considered, the finite spatial extension of the tunneling barrier is accounted for → better description of experimentally observed trends in current-voltage characteristics
- Dynamic non-local band-to-band tunneling model of Ieong et al. (*IEDM 1998*) implemented in Sentaurus builds the basis for the interpretation of the experimental results in this work
- The advantage of this model is the possibility to combine different tunneling paths in one simulation
- Three tunneling paths were accounted for
  - Direct band-to-band tunneling, dominant at higher voltages
  - Phonon assisted band-to-band tunneling, important contribution in silicon
  - Trap assisted band-to-band tunneling (was treated in Kane approximation)

SOI TFET device geometry and doping

- **SOI TFET implemented by Sandow et al.**
- Gate length: 2 to 12 µm
- Gate oxide: 3.5 and 4.5 nm
- Silicon body thickness: 20 nm
- Source ion implantation: Arsenic, 5 keV, $3 \cdot 10^{15}$ cm^{-2}
- Drain ion implantation: Boron, 1.5 keV, $3 \cdot 10^{15}$ cm^{-2}
- Channel doping: Boron, concentration $1 \cdot 10^{15}$ cm^{-3}
- Activation RTA: 1000ºC, 1 s



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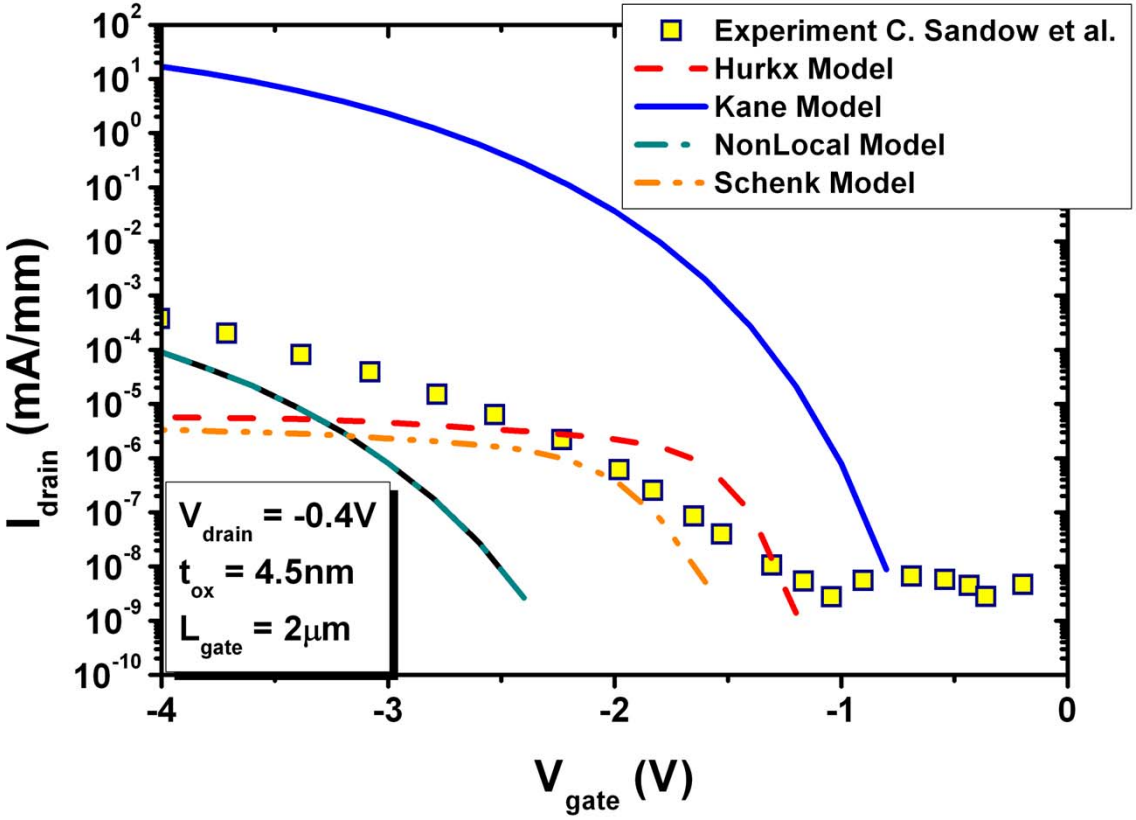
Comparison of the state-of-the-art tunneling models with experimental data

- Experiment: Transfer characteristic of SOI TFET of Sandow et al.
- Simulation:
  - Hurkx model
  - Kane model
  - Schenk model
  - Ieong non-local model
- Conclusion:
  - Several orders of magnitude difference between the models
  - No model reproduces the measurement



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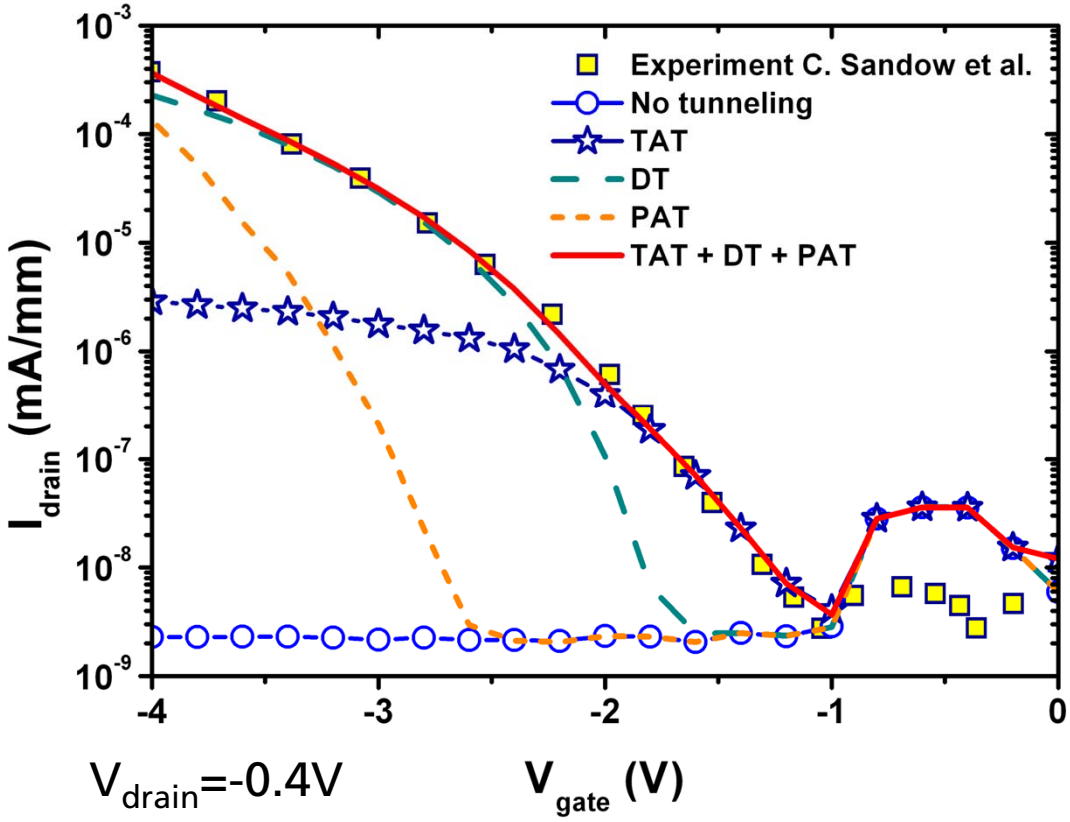
Calibration of non-local tunneling model, comparison with experimental data

- Experiment: Transfer characteristic of SOI TFET
- Simulation taking into account different tunneling paths:
  - DT – direct tunneling
  - PAT – phonon assisted tunneling
  - TAT – trap assisted tunneling
- Conclusion: Non-local tunneling model with several tunneling paths can reproduce the results of the measurements



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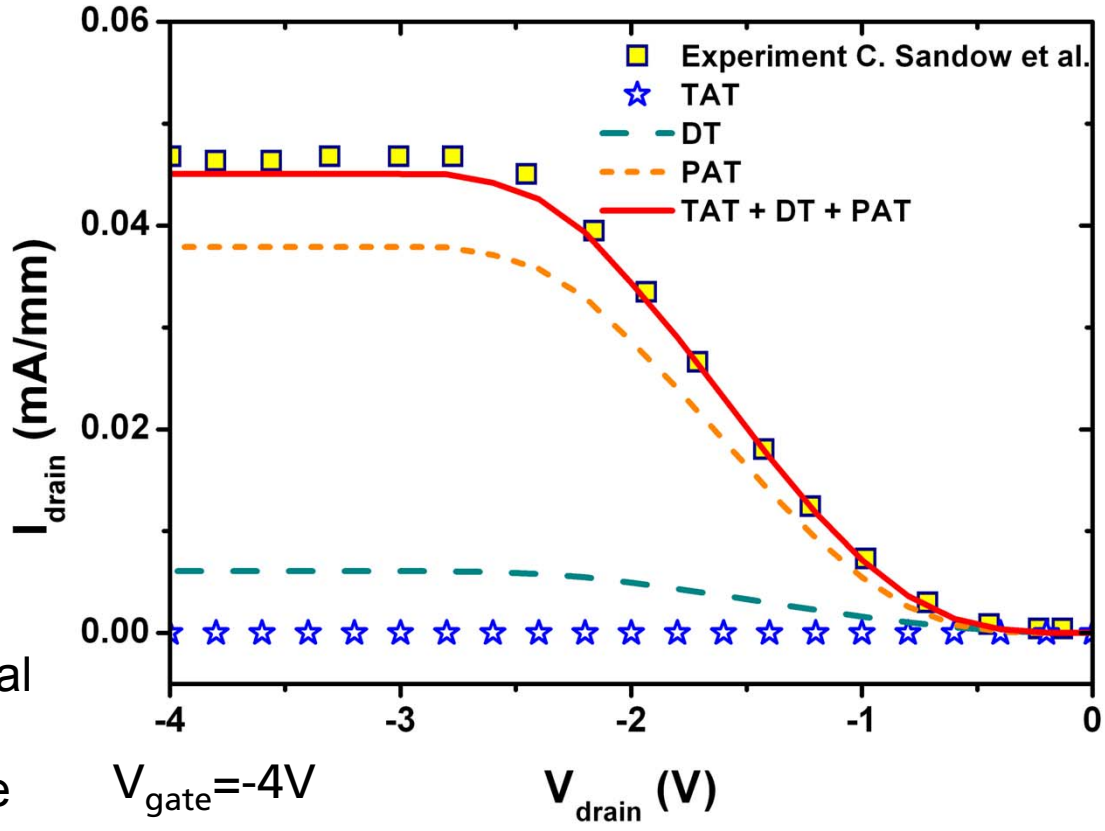
Contributions of different tunneling paths in the non-local tunneling model, comparison with experiment

- Experiment: Output characteristic of SOI TFET
- Simulation taking into account different tunneling paths:
  - DT – direct tunneling
  - PAT – phonon assisted tunneling
  - TAT – trap assisted tunneling
- Conclusion: Non-local tunneling model with several tunneling paths can reproduce the results of the measurements



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Calibrated parameters of the dynamic non-local tunneling model

Parameter → Tunneling path ↓	A(1/(cm^{3}s))	B(V/cm)	Δc(eV)	E_{ph}(eV)
Phonon assisted tunneling	$12 \cdot 10^{15}$	$2.2 \cdot 10^{7}$	0.15	0.068
Direct tunneling	$3.5 \cdot 10^{15}$	$6.3 \cdot 10^{6}$	0.0	0.0

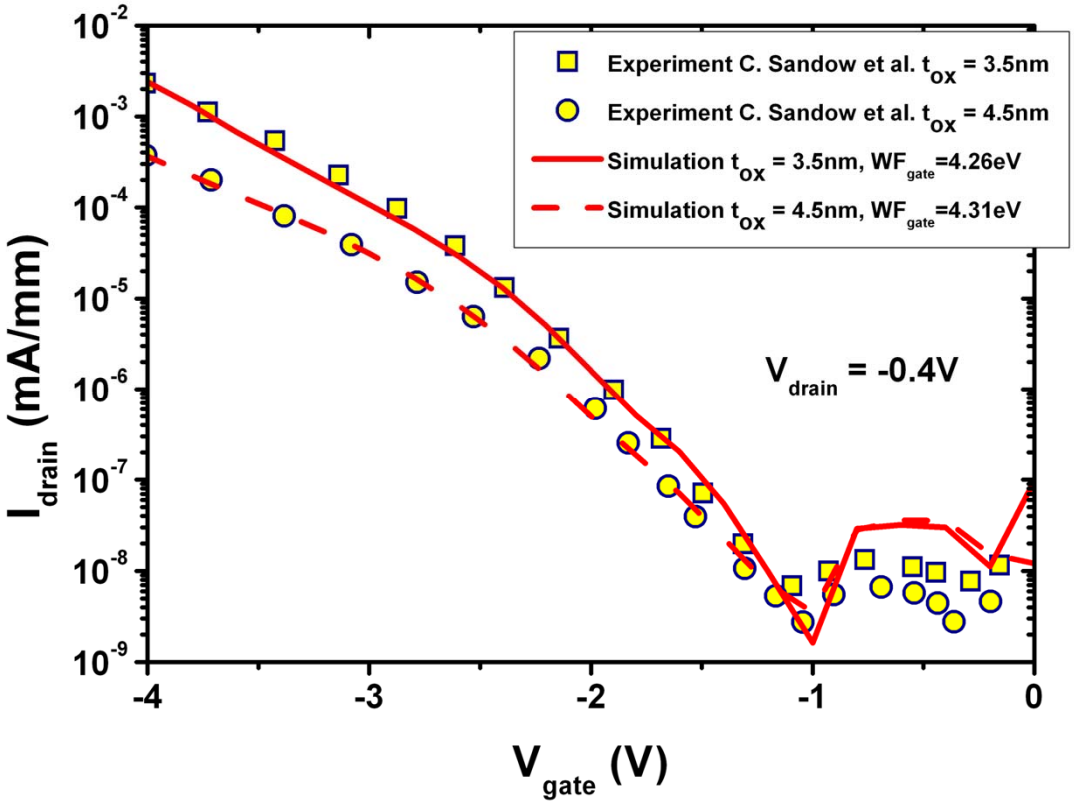
Simplified charge generation rate due to tunneling

$$R = A(F/F_0)^P \exp(B/F)$$

Where F is the local electric field, F_0 is a reference field of 1eV/cm,
P=2 for direct tunneling, P=2.5 for phonon assisted tunneling
Δ_c is the conduction band off-set
E_{ph} is the characteristic phonon energy

Simulation results for different gate oxide thicknesses, comparison with experimental data (1)

- Experiment: Transfer characteristics of SOI TFET at drain voltage of -0.4V for two values of the gate oxide thickness: 3.5 and 4.5nm
- Conclusion: Calibrated tunneling model with several tunneling paths can predict variations of the current-voltage characteristics when gate oxide thickness is varied



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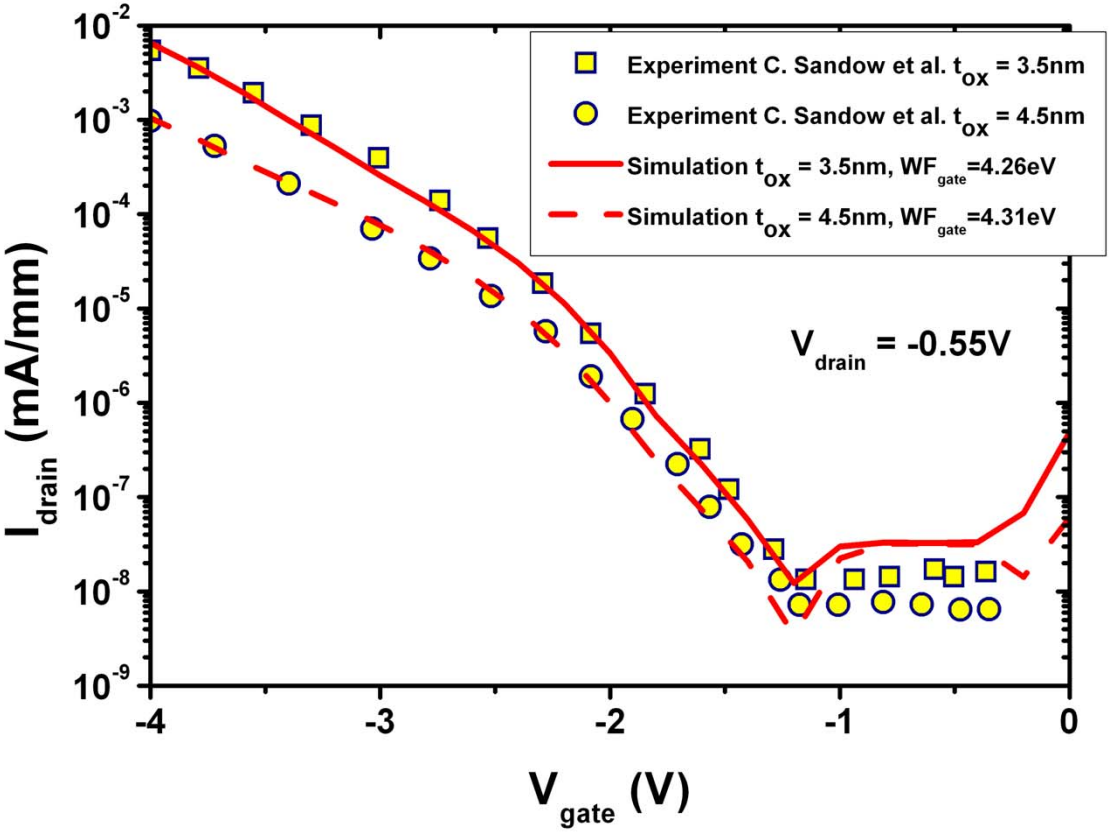
Simulation results for different gate oxide thicknesses, comparison with experimental data (2)

- Experiment: Transfer characteristics of SOI TFET at drain voltage of -0.55V for two values of the gate oxide thickness: 3.5 and 4.5nm
- Conclusion: Calibrated tunneling model with several tunneling paths can predict variations of the current-voltage characteristics when gate oxide thickness is varied



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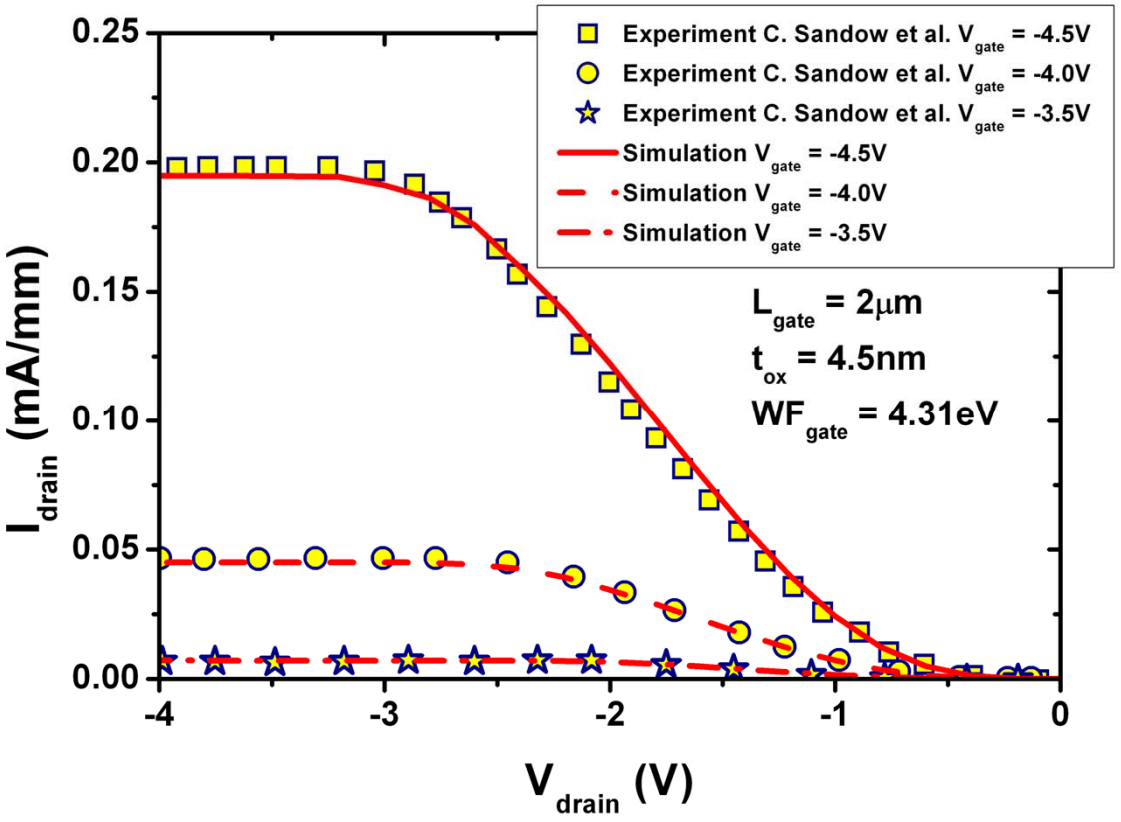
Simulation results for different gate lengths, comparison with experimental data (1)

- Experiment: Output characteristics of a SOI TFET at drain voltages specified in the figure for gate length of 2µm
- Conclusion: Calibrated tunneling model with several tunneling paths well reproduces the variations of output characteristics when gate length and gate voltage is varied



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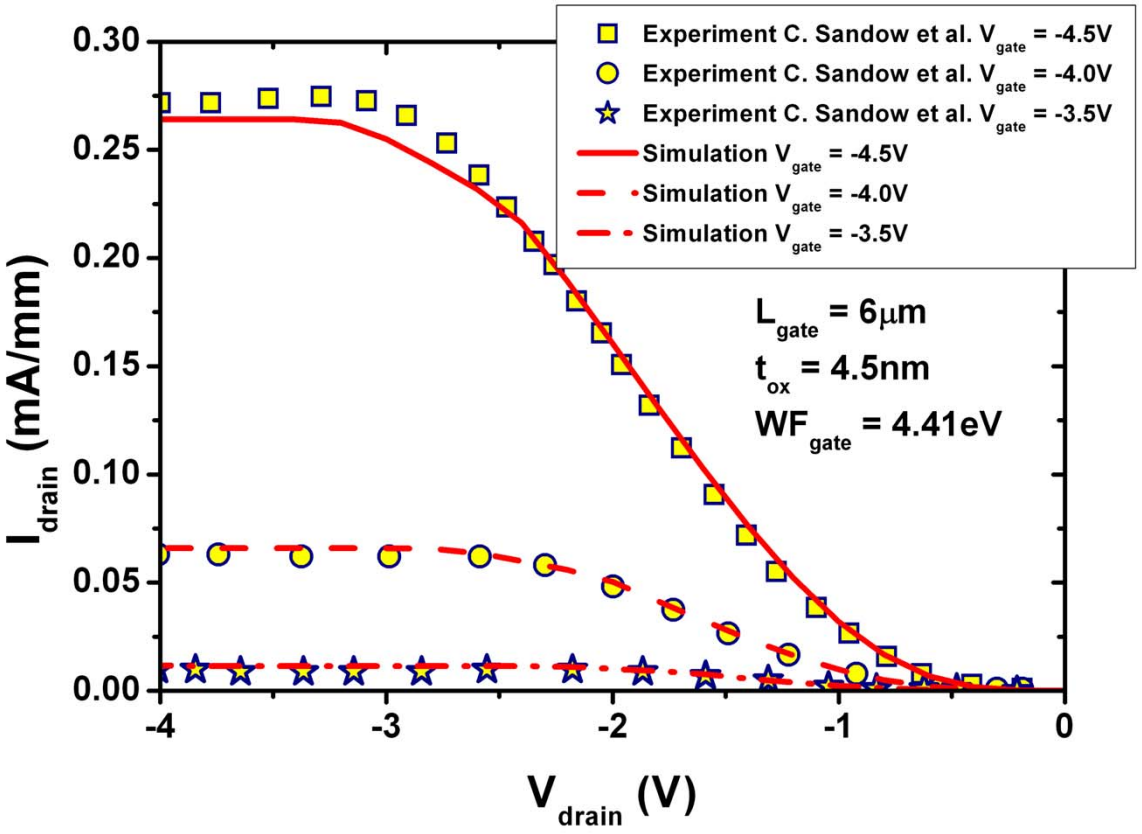
Simulation results for different gate lengths, comparison with experimental data (2)

- Experiment: Output characteristics of a SOI TFET at drain voltages specified in the figure for gate length of 6µm
- Conclusion: Calibrated tunneling model with several tunneling paths well reproduces the variations of output characteristics when gate length and gate voltage is varied



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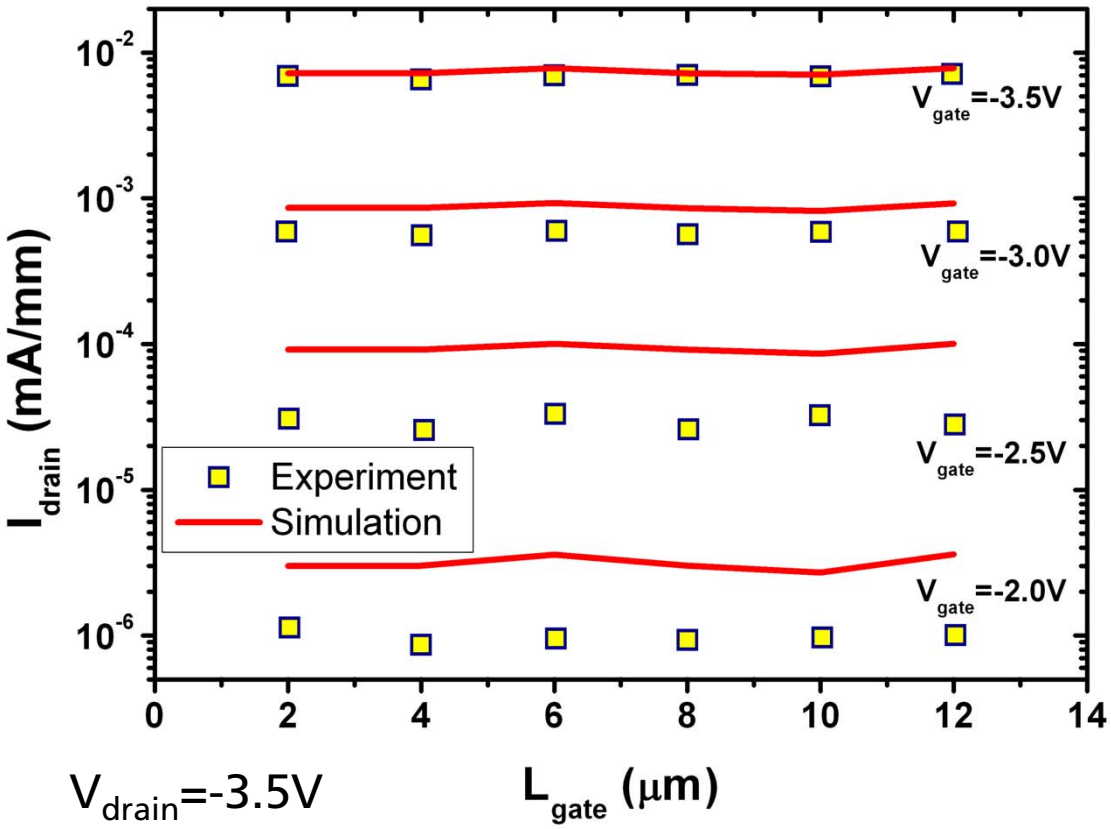
Simulation results for different gate lengths, comparison with experimental data (3)

- Experiment: Gate length dependence of the drain current of a SOI TFET at gate voltages specified in the figure
- There is a negligible dependence of the drain current of TFETs on the gate length
- Simulation using the suggested model confirms this important feature of TFETs



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Conclusion

- An extensive comparison of experiments and simulations for SOI tunneling field effect transistors is presented in this work
- Significant differences between different variants of the band-to-band tunneling models were found and discussed
- A combination of phonon-assisted tunneling and direct band-to-band tunneling in a non-local formulation with trap-assisted tunneling was found to be a suitable model to describe the observed current-voltage characteristics of SOI TFETs
- After the parameters of the tunneling model were calibrated for a fixed set of geometrical transistor parameters, the model was able to predict variations of the current-voltage characteristics due to variations of the gate oxide thickness and demonstrates a negligible dependence of the tunneling currents on the transistor gate length in agreement with experimental results