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Frabrication and Evaluation of 4H-SiC Double Trench MOSFETs on 6-inch Wafer

Minwho Lim[1], Seongjun Kim[2], Oleg Rusch[1], Min-Jae Kang[2], Min-Je Sung[2], Juyoung Kwak[2], Nam-Suk Lee[2], Hoon-Kyu Shin[2], Tobias Erlbacher[1], Anton Bauer[1]

[1]Fraunhofer Institute for Integrated Systems and Device Technology IISB, Germany
[2]National Institute for Nanomaterials Technology, Pohang University of Science and Technology, Korea

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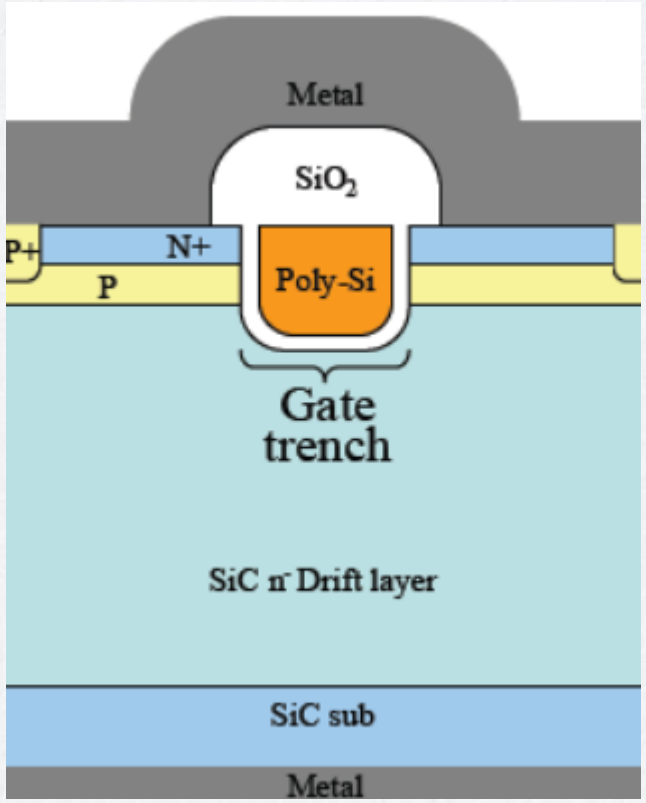
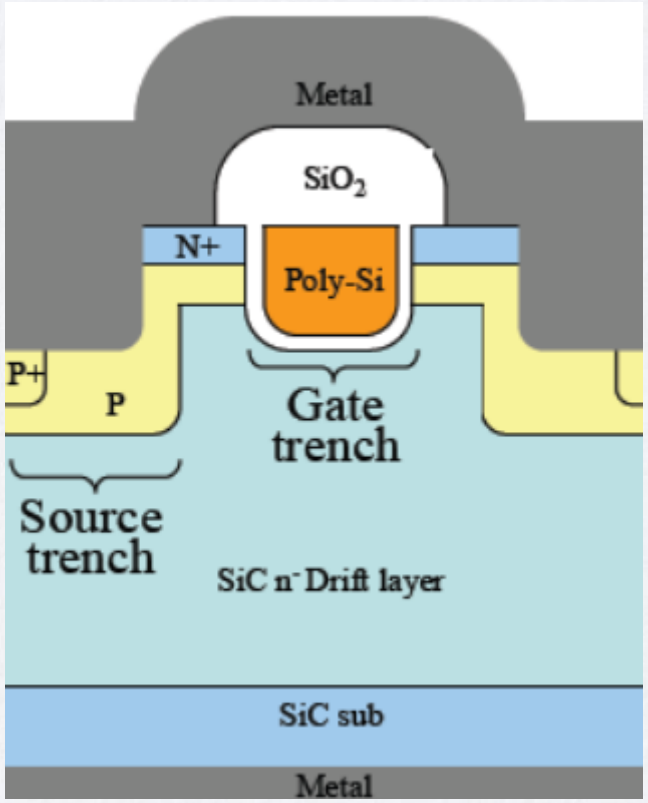
Concept of TrenchMOS for Additional Shielding

- Trench structure compared to planar structure
  - ☺ Higher cell density w/o JFET region
  - ☺ Higher mobility due to vertical channels
    → Reduction of resistance
    → Saving chip area and chip cost
  - ☹ Needed stable technology for trench etching
  - ☹ Gate oxide reliability has to be improved
    → Additional shielding required
- Double-TrenchMOS
  - Deep p-well by double trench for shielding
  - V_{block} = 1746 V demonstrated
  - ρ_{on} = 2.8 mΩcm^2 demonstrated (ROHM)



Conventional TrenchMOS

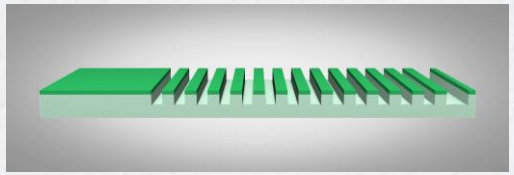


Double-TrenchMOS

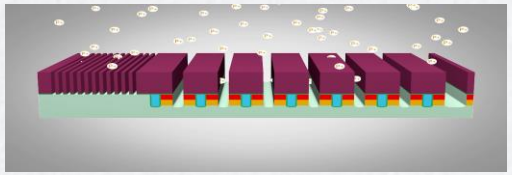
K. Okumura, N. Hase, K. Ino, Ultra Low On-Resistance SiC Trench Devices, www.rohm.com/eu

Fabrication Process

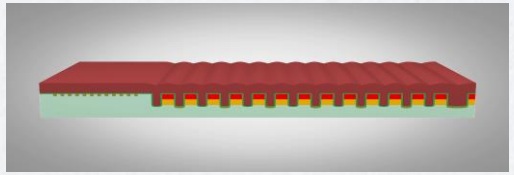
Double Trench MOSFET Fabrication (Four 6” SiC Epi-wafers)



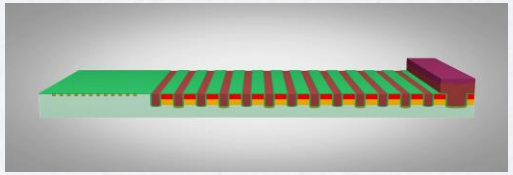
Trench Etching



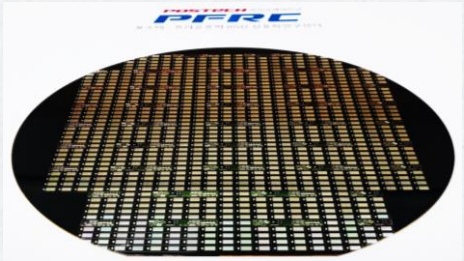
Ion Implantation

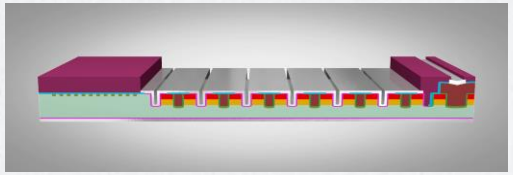


Gate Ox. & Poly Dep.

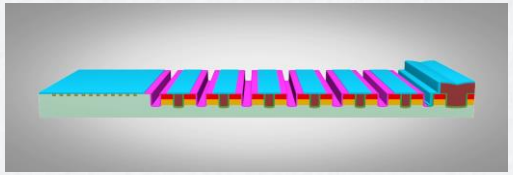


Planarization

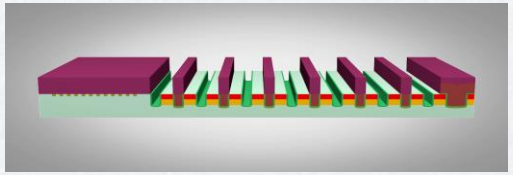




Gate Cont. & Passiv.

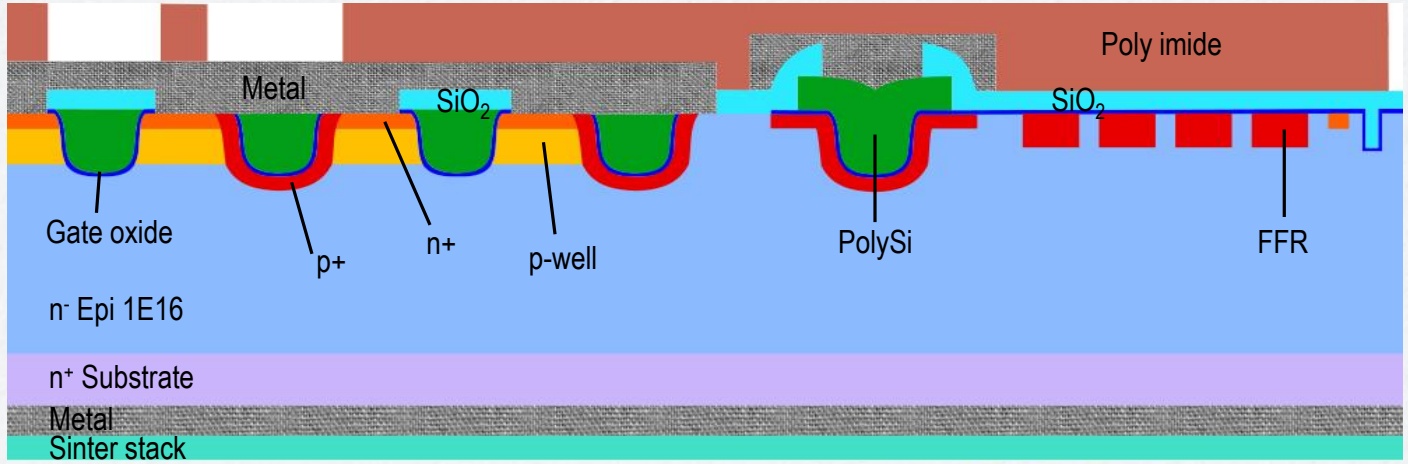


Field Ox. & Ohmic Cont.



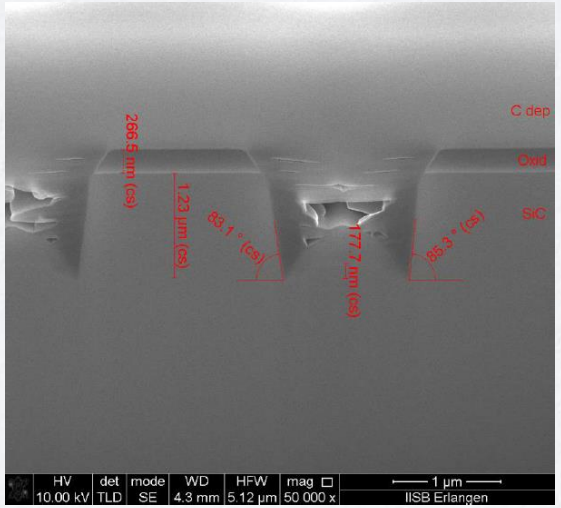
PolyPlug

- Target 1200 V / 20 A
- 6 inch SiC Epi-wafers
- Design the active area and edge termination
- Fabrication and electrical characterization performed at POSTECH-NINT and Fraunhofer IISB

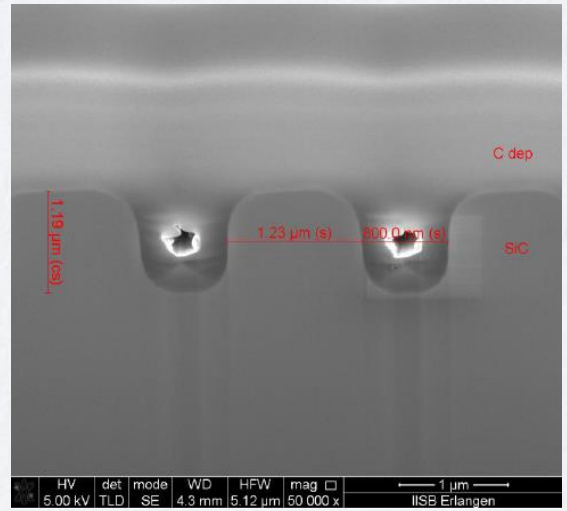


Reshaped Trench Patterning

- Trench patterning by using oxide hard mask
  - PECVD oxide → Photolithography → Wet etching PR → Dry etching hard mask and SiC
- Trench reshape by using high temperature annealing in H_2 ambient
  - Beneficial for shielding efficiency verified by TCAD simulation
  - As pre-treatment for gate oxide → Improved SiC-surface quality

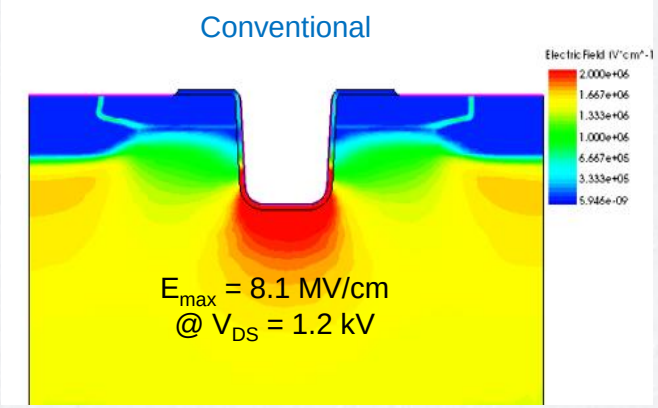


Trench Patterning

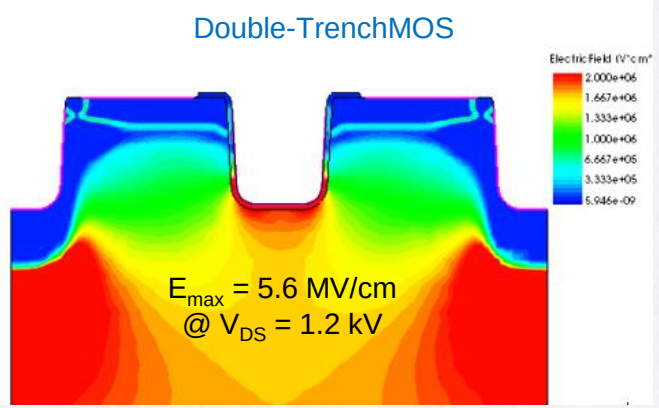


Trench Reshape

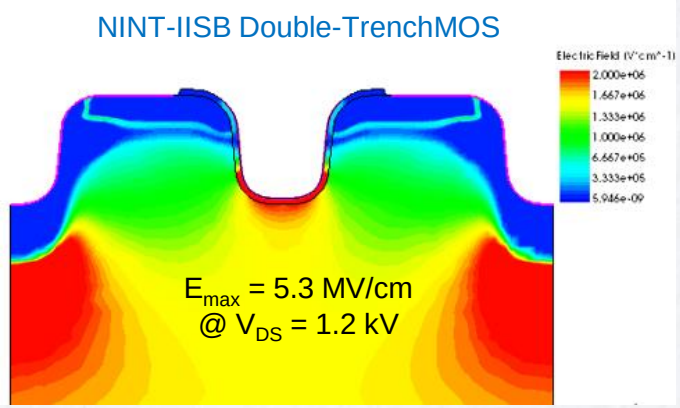
Conventional



Double-TrenchMOS



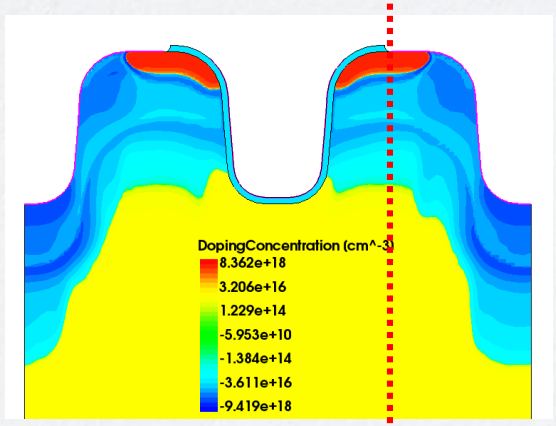
NINT-IISB Double-TrenchMOS



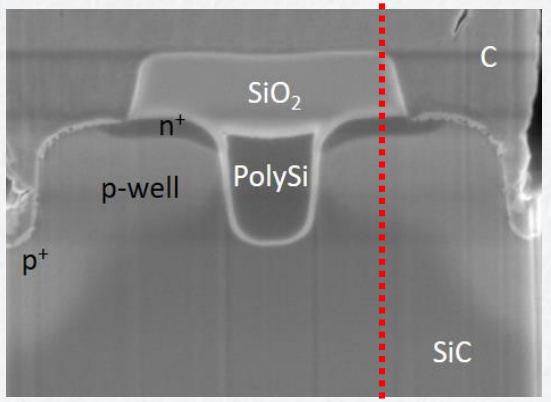
Verification Ion Implantation

- TrenchMOS device modeled by
  - TCAD process- and device simulation implemented in Synopsis Sentaurus
  - Kinetic Monte Carlo (KMC) ion-implantation with various doses, energies and tilt angles of ion-beam
  - Imitated actual unit cell formation (depth, width, flanken angle etc.)
  - Device simulation for on- and off-state performd with appropriate definition of external bias, blocking model, interface density and electrode resistance

- TCAD process simulation calibrated by
  - SEM dopant contrast (quantitative)
  - SIMS measurement (qualitative)

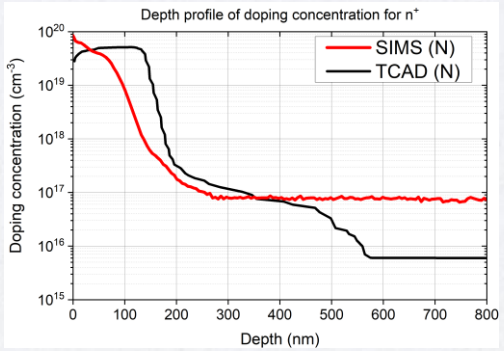


TCAD process model

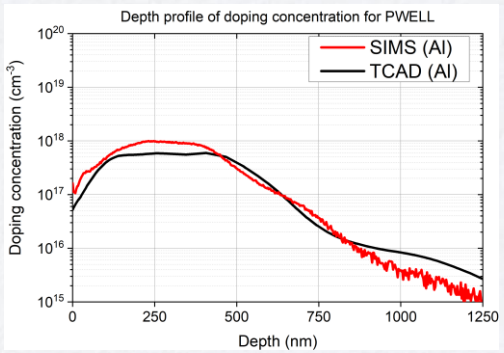


Fabricated TrenchMOS

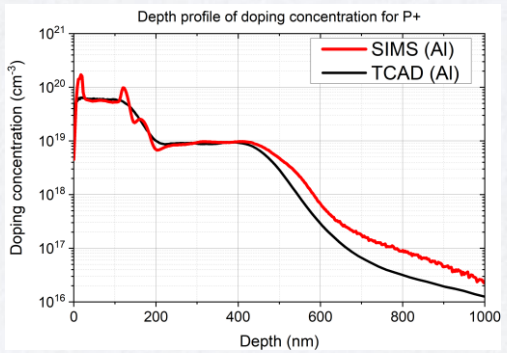
n+ Source



p-well

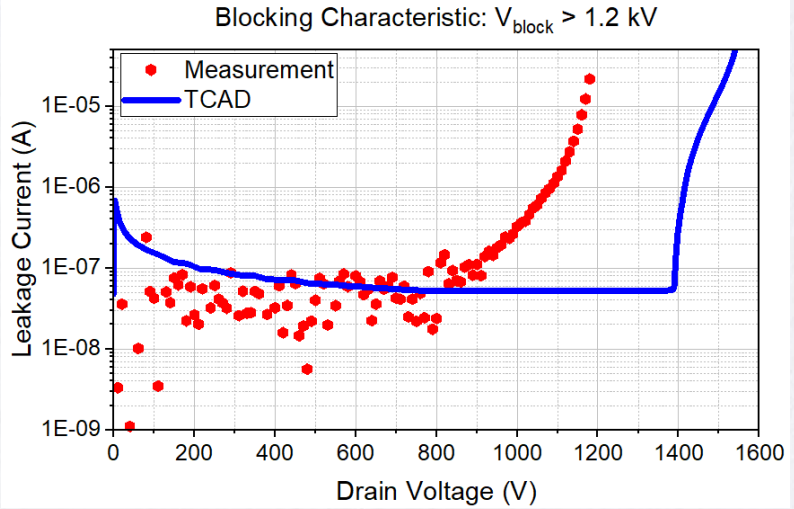


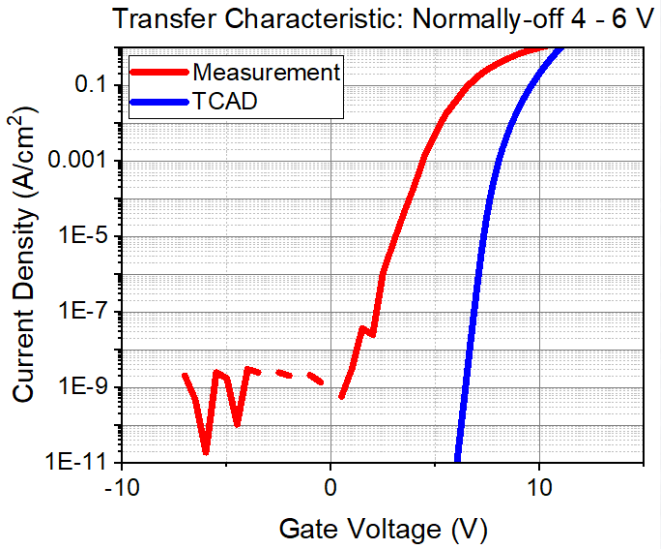
p+ shielding

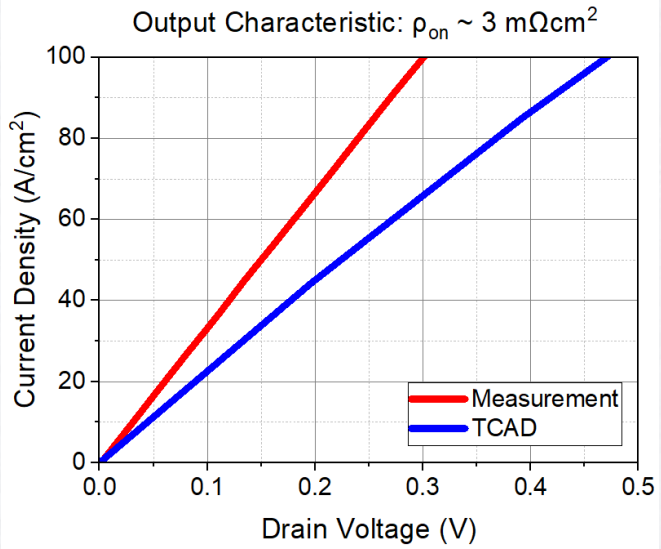


Electrical Characteristics

- 1200 V / 20 A achieved
- Room for improvement in the electrical characteristics
- Blocking capability
  - Short channel effect: Possibility for higher blocking voltage (~ 1.6 kV) with optimized p-well implantation parameters determine the vertical channel length
- Output- and transfer characteristic
  - Design optimization: Short circuit between source and gate via → Increased leakage current
  - Misalignment of field oxide and loss of shallow n^+ source region caused by dry etching and thermic oxidation should undergo improvement
  - Gate oxide optimization for higher mobility, dielectric breakdown field strength and improved threshold voltage shift







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Electrical Characteristics

Thank You!