In-Situ CCVD Grown Graphene Transistors with Ultra-High On/Off-Current Ratio in Silicon CMOS Compatible Processing

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Abstract. We invented a novel method to fabricate graphene transistors on oxidized silicon wafers without the need to transfer graphene layers. By means of catalytic chemical vapor deposition (CCVD) the in-situ grown monolayer graphene field-effect transistors (MoLGFETs) and bilayer graphene transistors (BiLGFETs) are realized directly on oxidized silicon substrate, whereby the number of stacked graphene layers is determined by the selected CCVD process parameters. In-situ grown MoLGFETs exhibit the expected Dirac point together with the typical low on/off-current ratios between 16 (hole conduction) and 8 (electron conduction), respectively. In contrast, our BiLGFETs possess unipolar p-type device characteristics with an extremely high on/off-current ratio up to $1x10^7$ exceeding previously reported values by several orders of magnitude. We explain the improved device characteristics by a combination of effects, in particular graphene-substrate interactions, hydrogen doping and Schottky-barrier effects at the source/drain contacts as well. Besides the excellent device characteristics, the complete CCVD fabrication process is silicon CMOS compatible. This will allow the usage of BiLGFETs for digital applications in a hybrid silicon CMOS environment.

Introduction

A monolayer of graphene consists of carbon atoms which are arranged in a quasi planar honeycomb lattice structure. It is a true 2D material which has been exfoliated from graphite for the first time by A. Geim and K. Novoselov [1] in 2004. However, size and position of the exfoliated graphene flakes varies randomly. In addition to this difficulty, adsorbed molecules like O_2 and H_2O often accumulate at the interface between graphene and the substrate surface [2].

Various methods to produce graphene have been invented [3]. In order to avoid graphene transfer, epitaxial graphene grown on silicon carbide (SiC) has been proposed by de Heer and Berger [4]. Using this method fairly large graphene sheets can be realized on a SiC wafer without the need to transfer. However, when comparing with conventional silicon processing, this method is more expensive because of the SiC substrate. Furthermore, the process requires extraordinary high growth temperatures of about 1400°C and is therefore not compatible with conventional silicon CMOS processing. Although graphene growth on dielectrics has been demonstrated by various research groups [5-10], none of these research groups is growing graphene or graphite directly on thermally grown SiO_2 using conventional silicon substrates. Some of the materials are either extremely expensive or completely incompatible with CMOS process technology.

We have developed a dedicated in-situ CVD-based growth method for graphene on oxidized silicon wafers in order to avoid the above mentioned drawbacks. First experimental evidence demonstrating the feasibility of this transfer-free graphene growth method has already been published in November 2009 [11, 12].

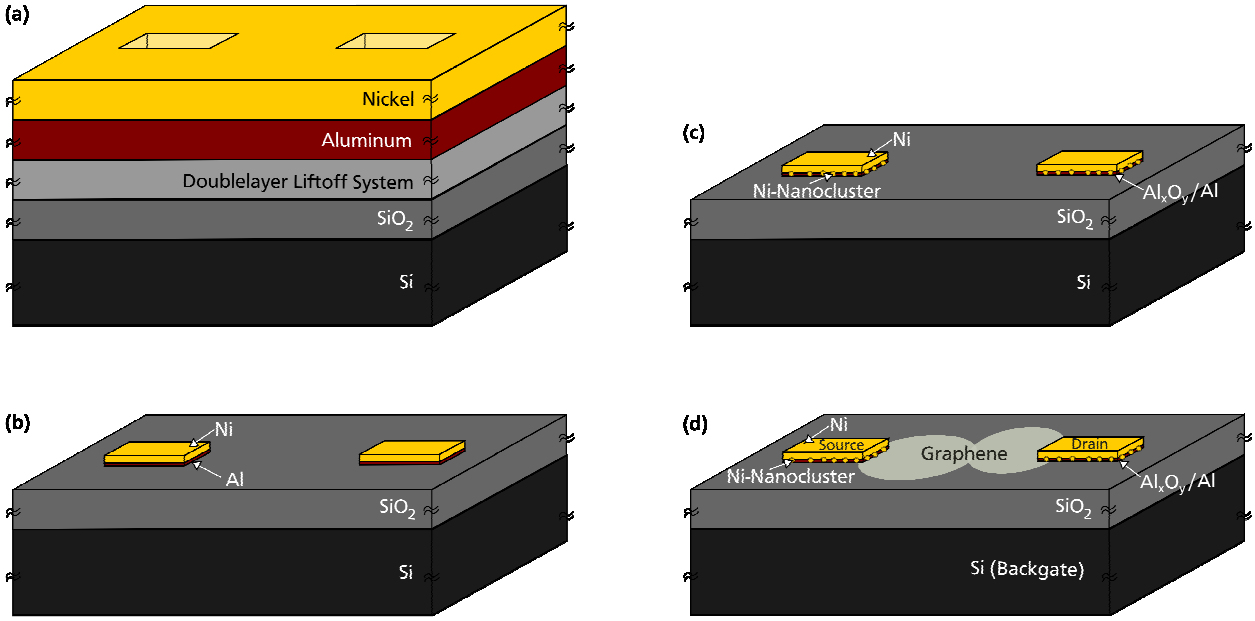

Figure 1. Schematic drawings illustrating the fabrication process of graphene transistors: (a) Double layer liftoff system used to pattern the catalyst areas. (b) Catalytic areas on top of the silicon dioxide substrate after liftoff. (c) Catalytic areas and nickel nanoclusters after annealing. (d) Graphene FET structure produced by CCVD using an aluminum/nickel catalyst system. Note that the catalyst areas are simultaneously used as source/drain contacts.

Fabrication

In preparation for CCVD a silicon wafer is oxidized in dry ambient at 1000°C for 120 min to obtain a 100nm thick SiO_2 film. Afterwards several lithography steps follow and a structured liftoff system remains on the wafer surface [13]. Thin aluminum and nickel layers (5nm to 15 nm each) are evaporated over the whole substrate surface (cf. Fig 1a) and are structured via liftoff (cf. Fig 1b). By annealing the wafer at 800°C to 900°C for 3 to 15 minutes the aluminum transforms itself partially into aluminumoxide-like insulator (Al_xO_y) while the nickel (Ni) layer generates several nickel nanoclusters at the border of the catalyst system (cf. Fig 1c). In the subsequent methane-based CCVD process, graphene layers are growing on top of the silicon dioxide surface (cf. Fig. 1d), while the number of the stacked graphene layers depends on the adjusted process parameters in particular process time and temperature. The methane flow rates are typically in the range of 4 to 15 litres per minute while the methane can be diluted by hydrogen with a flow rate of 3 litres per minute at maximum at atmospheric pressure [13].

When using a suitable device layout, several hundred of graphene FETs are fabricated simultaneously on one 2'' wafer and the graphene transistors are functional directly after the CCVD growth process and can be contacted directly via the catalytic source/drain areas (cf. Fig. 1d) for electrical characterization. Furthermore, by adjusting the CCVD process conditions we can adjust the number of grown graphene layers giving us the unique capability to investigate the physical and electrical properties of various in-situ grown graphene films at the device level [13, 14].

These graphene devices possess well defined channel lengths in the range of 1.6µm to 5µm while the channel widths vary arbitrarily from approximately 0.1µm to several microns, depending on local growth conditions. The in-situ grown graphene layers extend only a few microns on the SiO_2 surface and therefore do not always fill up the maximum designed channel width. In addition to the

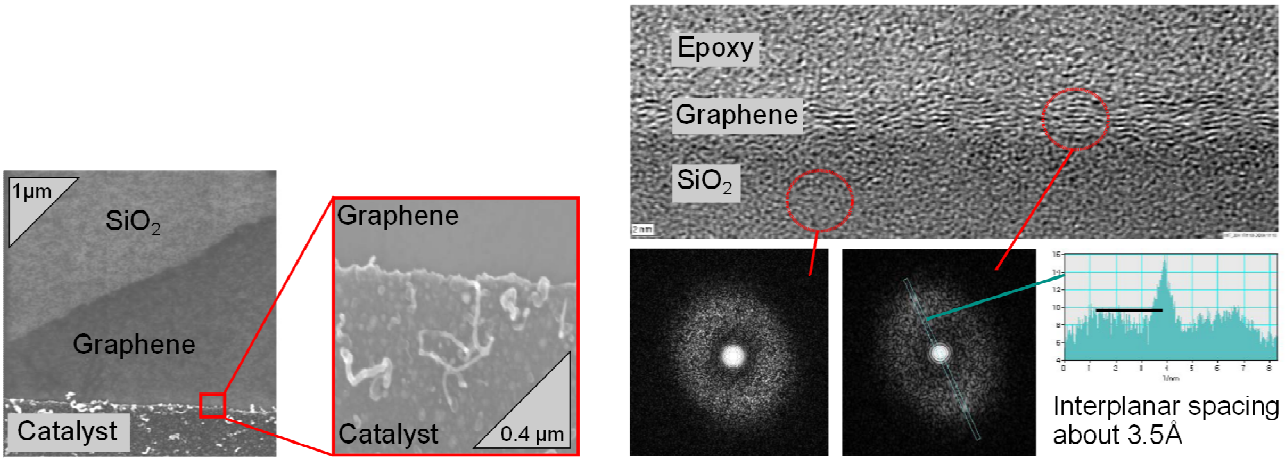

Figure 2. (a) High resolution scanning electron microscopy image of the probe at the catalyst graphene junction (b) Structural transmission electron microscopy examination of a multilayer graphene sample on a silicon dioxide surface with Fourier analysis.

grown graphene layers on the oxide surface further carbon deposits are present on top of the catalytic areas as evident from the enlargement shown in figure 2a. Detailed examination by means of scanning electron microscopy indicates that the spread of the CNTs and the additional carbon deposits occur exclusively on the top of catalyst source/drain areas. The total processing time for the wafers within the CVD chamber (Applied Materials AMV 1200) is in the range of 30 to 60 minutes.

Structural transmission electron microscopy examination

A scanning electron microscopy image of a multilayer graphene sample at the catalyst to graphene transition can be seen in figure 2a. The surface of the catalyst area is rough and some carbon nanotubes growing from the nickel cluster are visible, as expected [11, 12]. Figure 2b shows the transmission electron microscopy (TEM) screening of the sample. Therefore the sample was mould in an epoxy resin. The Fourier analysis of structural transmission electron microscopy examination of the CCVD grown graphene multilayer on silicon dioxide shows an interplanar spacing of 3.5Å. This is a strong evidence for the existence of graphene grown by means of catalytic CVD [15].

Raman Spectroscopy

A Raman spectroscopy of graphene transistors is performed within the channel region in between the catalytic areas (cf. Fig. 1). A Renishaw spectrometer at 633 nm at room temperature for the examination of the monolayer and bilayer graphene sample was used as well as a confocal Raman microscope with a 633nm laser at room temperature to analyze the fewlayer graphene sample. In Raman spectra of graphene three main peaks can be determined. The D and G peak at 1338 cm^{-1} and 1578 cm^{-1} respectively, represent the graphitic sp^2-structure (G peak) and the defects in the graphene lattice, as holes and edges (D peak). The shape of the 2D band around 2650 cm^{-1} is characteristic for the number of stacked graphene layers [17]. Comparing Fig. 3 with Raman data from A. Ferrari [17] suggests the presence of monolayer and bilayer graphene in our samples. The characteristic Raman G and D peaks as well as the 2D band are located at similar Raman shift positions found by Ferrari and exhibit the expected shape.

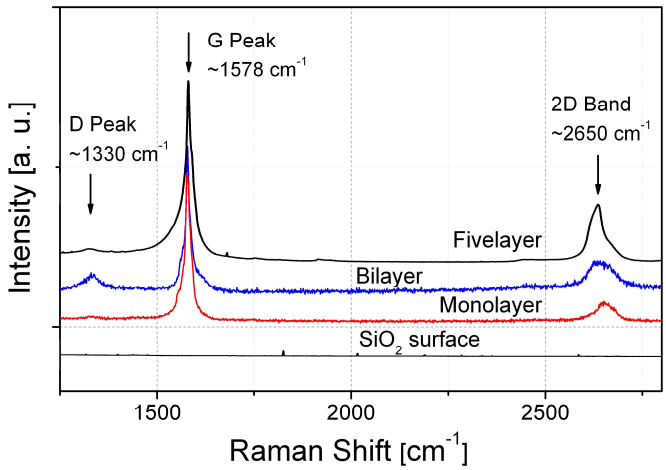

Figure 3. Raman spectra of in-situ CCVD grown fewlayer, bilayer and monolayer graphene measured within the channel region at room temperature. In addition, Raman measurements in approximately 50µm distance to the channel region were performed to establish a reference of the graphene-free silicon dioxide surface. The Raman spectrum of fewlayer graphene at the top is measured using confocal Raman microscope with a 633nm laser. Comparing the shape of 2D band with [17] the presence of five-layer graphene is deduced. The two lower Raman-spectra are measured using a Renishaw spectrometer at 633nm. The overall shape and peak positions indicate the presence of monolayer and bilayer graphene, respectively, when comparing with data from [17], [18] and [19].

However, a difference in the intensity ratio I(2D)/I(G) is observed especially for the monolayer graphene sample. These differences indicate strong interactions of graphene with underlying silicon dioxide [18, 19] which are due to the in-situ growth at moderate temperatures [16]. In contrast, for externally grown graphene with subsequent transfer such intensive interactions between graphene and silicon dioxide are largely reduced in presence of adsorbed molecules, e.g. O_2 and H_2O.

Electrical Characterization

The electrical characterization of the graphene devices is performed using a Keithley SCS 4200 semiconductor analyzer. The metal catalyst areas are directly used as source and drain contacts (cf. Fig. 2d). However, for in-situ CCVD grown graphene FETs the maximum current is limited by the thin nickel conducting paths as well as the high contact resistance caused by some carbon deposits on top of the source drain regions. Figure 4a shows the transfer characteristic of the same MoLGFET, on which the previously discussed Raman spectrum of monolayer graphene has been obtained in the channel region between the soured/drain contacts. The characteristic Dirac-point at V_{BG} = -6V confirms the co-existence of hole and electron conduction together with the typical low on/off-current ratios, as expected for monolayer graphene [20]. However, a slightly unsymmetrical current-voltage characteristic is noted in figure 4a, leading to different on/off-current ratios of 16 for hole-conduction and 8 for electron-conduction, respectively. Obviously, hole-conduction is preferred in our in-situ CCVD grown graphene, which appears typical for CVD grown graphene according to Hall-effect measurements reported from other groups [21]. Furthermore, figure 4b shows the corresponding output characteristics which exhibit the typical three region behavior of a large area monolayer graphene transistor as described in [20], confirming the existence of transfer-free and in-situ CCVD grown monolayer graphene and substantiate the prediction of the Raman spectra. Changing the sweep direction shifts the Dirac point from V_{BG} = -6V to V_{BG} = +11V which

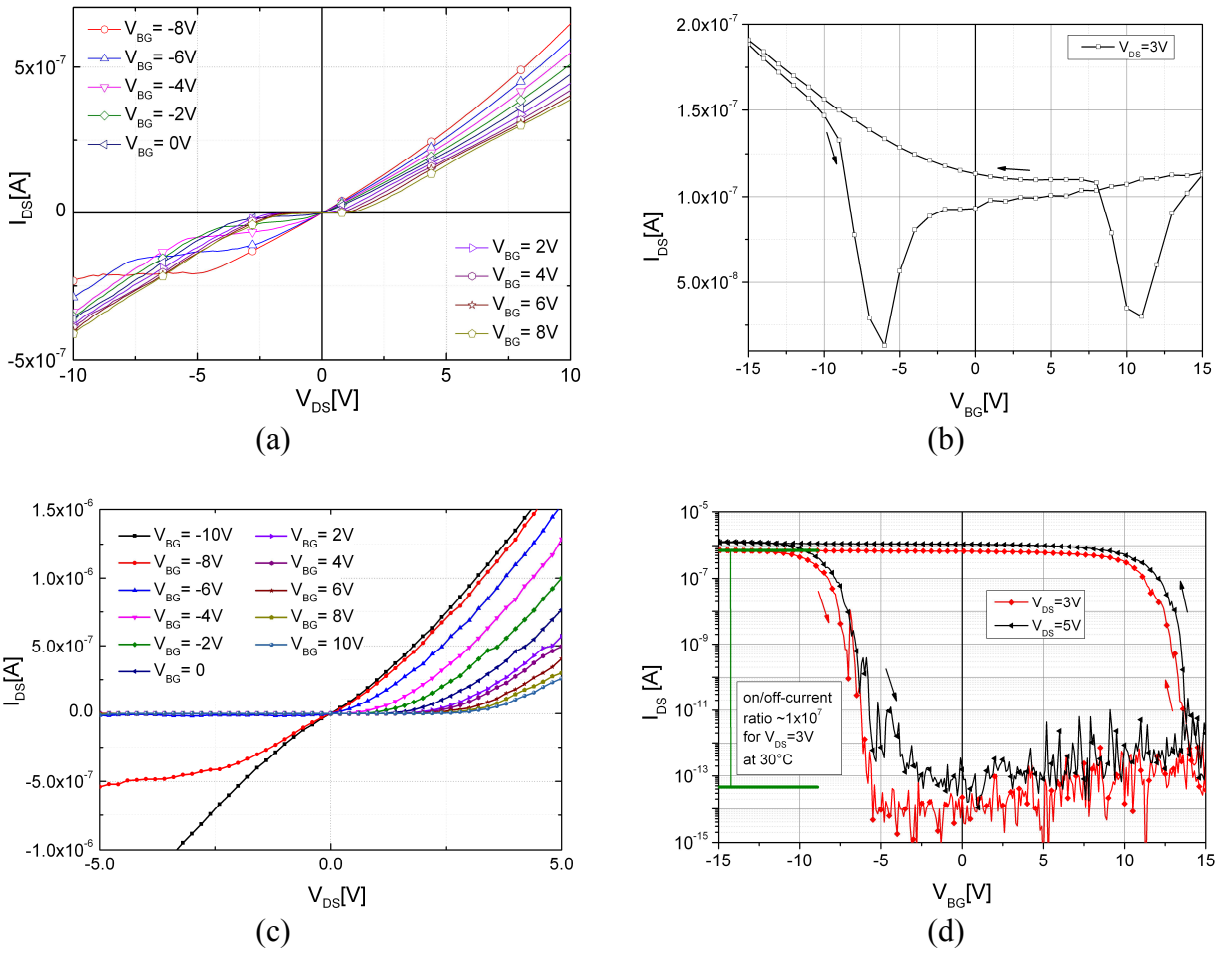

Figure 4. (a) The output characteristic of a monolayer graphene transistor (MoLGFET) exhibits typical three region behavior. (b) Current vs. gate-voltage characteristic of monolayer graphene. The Dirac point indicates simultaneous electron and hole conduction.
(c) Output characteristic of a bilayer graphene field effect transistor at different backgate voltages V_{BG} while the drain/source voltage V_{DS} is swept from -5V to 5V. (d) Current vs. gate-voltage characteristic of a bilayer graphene transistor. The backgate voltage V_{BG} is swept from -15V to 15V while a constant voltage V_{DS} of 3V is applied between drain and source. Extremely high on/off-current ratios of $1x10^7$ are observed at 30°C for the bilayer graphene transistor.

is equivalent to a hysteresis of ΔV_{BG} = 17 V [16]. Lemme [2] reports a hysteresis of ΔV_{BG} = 22 V for a front gated MoLGFET on silicon dioxide substrate. Top contacted graphene ribbons on Al_2O_3 substrate are examined by Kumar et al. [21], exhibiting a hysteresis of $\Delta V_{BG} \sim 20$ V. Wang et al. [19] show current voltage characteristics of a bilayer graphene device on SiO_2 exhibiting a positive hysteresis of the same order of magnitude as found in both [2] and [21] as well as in our work.

Figure 3a shows the output characteristic of a BiLGFET. A constant backgate voltage V_{BG} is applied while the drain/source voltage V_{DS} is swept from -5V to 5V. The transfer characteristic of a BiLGFET is shown in figure 3b. In-situ CCVD grown BiLGFETs exhibit an ultra-high on/off-current ratio of $1x10^7$ at room temperature which is to our knowledge the highest reported value for in-situ CCVD grown BiLGFETs today. The transfer characteristic is consistent with the output characteristic, displaying a unipolar, p-type device behavior. The required bandgap is partly realized by the applied backgate voltage causing an electrical field of low gate field strength of 1.5 MV/cm (i.e. 0.15V/nm) perpendicular to the layer. In addition to this we assume a large contribution of graphene-to-substrate interaction to the total bandgap of bilayer graphene. Such intensive

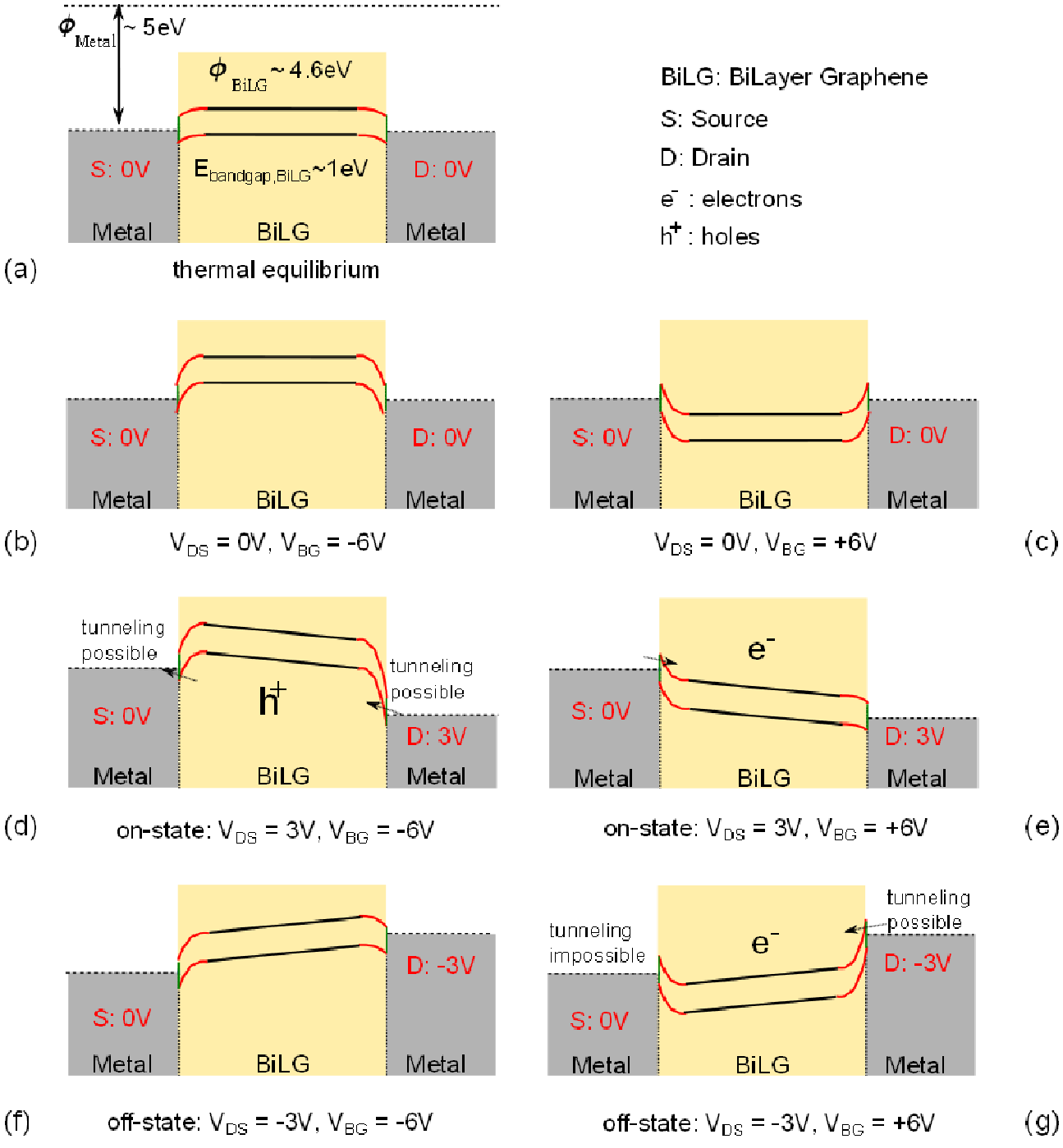

Figure 5. Schematic band diagrams regarding the output characteristic of a bilayer graphene field effect transistor (a) Schematic band diagram for a BiLGFET in thermal equilibrium. (b) Schematic band diagram for a BiLGFET when a constant voltage of V_{BG} = -6V is applied but V_{DS} = 0V. (c) Schematic band diagram for a BiLGFET when a constant voltage of V_{BG} = +6V is applied but V_{DS} = 0V. (d) Schematic band diagram for a BiLGFET while conducting in the on-state, i.e. V_{BG} = -6V at V_{DS} = 3V. (e) Schematic band diagram for a BiLGFET while conducting in the on-state with a lower I_{DS} as in figure 5d, i.e. V_{BG} = +6V at V_{DS} = 3V (f) Schematic band diagram for a BiLGFET when in the off-state, i.e. V_{BG} = -6V at V_{DS} = -3V (g) Schematic band diagram for a BiLGFET when in the off-state, i.e. V_{BG} = +6V at V_{DS} = -3V

interactions may develop during the growth of the bilayer graphene on the silicon dioxide at moderate temperatures under well defined ambient conditions within a CVD chamber [12].

Schematic band diagrams for a BiLGFET are shown in Figure 5 in order to explain the experimental observations of the output characteristic of a BiLGFET. A metal work function of approximately 5eV for nickel is assumed as well as a band gap of approximately 1eV for BiLG, deduced for comparison from carbon nanotubes showing a similar current voltage characteristic [11]. Previous studies [22, 23, 24, 25] reveal that the work function of graphene is in a similar range to that of graphite, ~4.6eV, [26] and depends sensitively on the number of layers [27, 28].

The schematic band diagram for a BiLGFET in thermal equilibrium is shown in figure 5a. Figure 5b shows the schematic band diagram for a BiLGFET when a constant voltage of V_{BG} = -6V is applied but V_{DS} = 0V and figure 5c shows the schematic band diagram for a BiLGFET when a constant voltage of V_{BG} = +6V is applied but V_{DS} = 0V.

For the on-state of a BiLGFET a voltage of V_{DS} = 3V between drain and source is applied as well as a back gate voltage of V_{BG} = +6V and V_{BG} = -6V is applied, as can be seen in figure 5d and 5e, respectively. $I_{DS}(V_{DS} = 3V, V_{BG} = -6V)$ is higher than $I_{DS}(V_{DS} = 3V, V_{BG} = +6V)$ as can be seen in figure 4c. The comparison of figure 5d and 5e shows that in case of $I_{DS}(V_{DS} = 3V, V_{BG} = -6V)$ hole conduction is assumed in case of tunneling through the barriers at the drain and the source contact, while for $I_{DS}(V_{DS} = 3V, V_{BG} = +6V)$ electron conduction is assumed. Caused by the band bending (cf. Fig. 5a) the tunneling of holes as discussed in figure 5d is more likely than the tunneling of electrons as shown in figure 5e.

Figures 5f and 5g are showing the corresponding band diagrams of a BiLGFET in the off-state. In case of V_{DS} = -3V, V_{BG} = -6V neither hole conduction or electron conduction is possible as can be seen in figure 5f. If a voltage of V_{DS} = -3V and V_{BG} = +6V is applied, tunneling for electrons through the drain barrier is possible but tunneling through the source barrier is impossible (cf. Fig. 5g). Hole conduction is also impossible.

In case of an applied backgate voltage of $V_{BG} < -8V$ at V_{DS} = -3V the transistor cannot be switched off (cf. Fig. 4c). In this case the band bending is that intense that the barriers at the source and the drain contact gets thin enough that a hole current flow between source and drain occurs.

Conclusions

Various optical, electrical and structural analyses have been performed on MoLGFETs and BiLGFETs. The combination of structural transmission electron examination with Fourier analysis, Raman spectroscopy as well as extensive electrical characterization of graphene structures on silicon dioxide confirms the suitability of this in-situ CCVD growth process. MoLGFET show the expected characteristic Dirac-point and a typical low on/off-current ratio of 16. In contrast, BiLGFETs exhibit ultra-high on/off-current ratios of 10^7 at room temperature, exceeding previously reported values by several orders of magnitude. We explain the improved device characteristics by a combination of effects, in particular graphene-substrate interactions, hydrogen doping and Schottky-barrier effects at the source/drain contacts as well. With this novel fabrication method hundreds of large scale BiLGFETs are realized simultaneously on one 2'' wafer by in-situ CCVD grown BiLG in a silicon CMOS compatible process. This will allow a simple and low-cost integration of graphene devices for nanoelectronic applications in a hybrid silicon CMOS environment for the first time.

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