Galvanically isolated differential data transmission using capacitive coupling and a modified Manchester algorithm for smart power converters

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***Abstract*— In this paper, a method for encoding and decoding digital data signals using a modified form of the standard Manchester code for the application in galvanically isolated data transmission in smart power electronics is described. The method includes a modified encoder circuit and a matching decoder circuit that is able to rebuild the original clock and data signal without a separate transmission of the clock signal. A capacitive coupling element with a corresponding signal conditioning circuit was placed between the encoder and decoder circuit to achieve a galvanic isolation between the primary side that processes the data signals and the secondary side that is responsible for the processing of power in smart power devices. After a description of basic principles of the transmission of data over a galvanic isolation and the state-of-the-art of Manchester code based data transmission, the encoding and decoding process of the modified Manchester code is elaborated and experimental results are presented.**

Keywords—robust data transmission; harsh environment; Manchester code; signal conditioning; encoding; decoding, capacitive coupling, galvanic isolation, power electronics, battery systems

I. INTRODUCTION

A. Galvanic Isolation

Modern smart power integrated circuits (e.g., isolated gate drive control in power electronic systems) consist of a digital and/or analog control electronic part where signal conditioning is done and a power electronic part containing the driver power stage. The control electronic part utilizes a core voltage than ranges from 1.8V to 5V depending on the utilized technology whereas the power electronics work with voltages of several hundreds of volts. A similar topology also applies to battery monitoring systems in smart battery systems [9] [10].

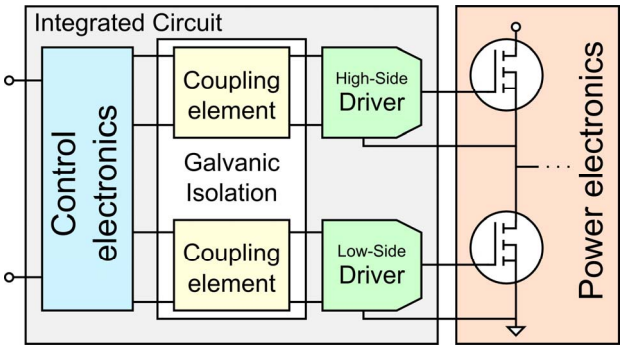

Fig. 1. Smart power converter topology utilizing a galvanic isolation

To enable data transmission between these two parts a galvanically isolated interface has to be applied. Fig. 1 shows an example of an isolated gate driver topology that utilizes this configuration. In this topology a 3.3V logic control electronic block is used to control galvanically isolated driver circuits that are able to drive high-electron-mobility switching elements of the power electronics block which are used to switch voltages of up to 400V at a frequency of up to 5MHz. At a proposed signal rise and fall time of 5ns this topology would ideally work at a slew rate of 80kV/µs. To ensure a stable transmission of this 5MHz switching signal the frequency of the control signal that is transmitted from the control electronics to the driver was increased to a value of 50MHz. To achieve this feat the control electronics as well as the driver circuit were developed as an integrated circuit with an external coupling element used for galvanic isolation. Furthermore the galvanically isolated data (and energy) transmission to the driver circuit enables the reuse of a low-side driver topology for the high-side driver or the design of a multi-level-converter

topology. Possible candidates for the galvanic isolation mechanism necessary for the signal transmission are piezo-coupling, optical coupling, inductive coupling and capacitive coupling [1]. The mechanical coupling method based on piezo crystals was abandoned for this particular application due to the slower signal propagation speed in piezo-ceramic elements compared to direct electrical transmission (e.g., signal transmission over capacitive coupling). Furthermore issues are caused by the assembly technology and the high amount of thermal cycles needed in automotive power electronics [8]. Although optical coupling elements can be used for data transmission they were not chosen because optical couplers are prone to degradation due to diffusion processes in the used materials. The transmission of data over an inductive coupling element was also contemplated but abandoned due to the possible generation of unwanted parasitic oscillations caused by transmitting signals with steep slopes [1]. In this paper a galvanic isolation using a capacitive coupling element was chosen for the signal transmission because of its high frequency range for transmitted signals combined with a high robustness against electromagnetic interferences (EMI).

B. Manchester Code

For the transmission of data signals over a galvanically isolated capacitively coupled bus the Manchester code has proven to be a robust solution [3]. The Manchester code is a synchronous clock encoding method that is in its simplest form generated by using a digital XOR operator on the clock and data signal. Due to this encoding, "high" or "low" values longer than one clock period are avoided because they are encoded into a signal that changes its state in dependence of the clock signal. Thanks to these perpetual transitions it is possible to achieve a robust synchronization at the receiving end. Decoding the Manchester code with a timing- or sampling-based decoding algorithm commonly requires the original clock signal that was used to encode the Manchester code [6]. This is achieved by either including a PLL on the decoder side to rebuild the original clock or by additionally transmitting the original clock signal which would require one or more (depending on single-ended or differential signaling) additional coupling elements. [2]

C. Signal Conditioning

As a capacitive coupling element is not suitable for the transmission of continuous voltage levels and is therefore not able to transmit long periods of logical 1 or 0 signals due to its differentiating behavior. When transmitting a signal over a capacitive isolation barrier the signal appearing on the secondary side of the capacitive coupling element corresponds to rising or falling edges of the voltage signal. This is caused by the change of the voltage dV/dt which degenerates over time (Fig. 2). As soon as the signal threshold level is exceeded, any connected circuit will only trigger once before returning to its natural off state. This behavior is illustrated in Fig. 2. Therefore a signal conditioning circuit that rebuilds the original signal and a data modulation has to be applied to transmit the data signal over the capacitive isolation.

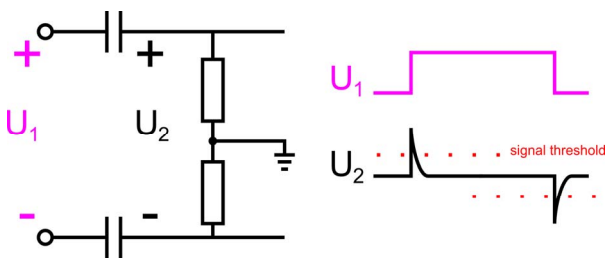

Fig. 2. Capacitively coupled differential signal transmission

II. DATA TRANSMISSION BASED ON MANCHESTER CODE

The proposed modification of the Manchester code changes the encoding process of the standard Manchester code to facilitate the recovery of information coded into the signal as well as rebuilding the clock signal without the use of a PLL which would normally be necessary to rebuild a clock signal for the decoding process. To achieve the proposed functionality of the encoder/decoder pair, it was necessary to modify the standard Manchester signal. In the modified Manchester signal, the first clock period during the change of state of the data signal is marked with a specific state. At a transition from logic 0 to 1 in the data signal the modified Manchester code is kept low for the entire clock period instead of using the XOR encoding method of the standard Manchester code. Analog to this at a transition from 1 to 0 the modified Manchester code is encoded by keeping the signal high for the entire clock period. This modification is only used at transitions in the data signal. Consecutive bits are encoded in the standard Manchester code. For a change of the data signal from logic 0 to logic 1 the modified Manchester signal exhibits a logic 1 state during the first clock period. This is illustrated in Fig. 3. An encoder circuit was developed that was able to detect a change of state of the data signal by comparing the original data signal with a data signal that was delayed by one clock period. This way the developed decoder circuit was able to detect a state change at the beginning of each clock signal period and rebuild the original clock signal by triggering a one shot circuit that can be customized to correspond to the original clock signal frequency. This rebuilt clock signal can then be used to decode the modified Manchester signal and regain the information of the original data signal. The advantage of this proposed encoding algorithm is the possibility of synchronous clock and data reconstruction in the modified decoder circuit. A similar decoding process in which the clock signal is being extracted from a standard Manchester encoded signal and also avoids the use of a PLL was considered. However in that approach the specific state of the encoded Manchester signal described earlier is located at a transition in the middle of a clock period (Fig.3). This causes the clock signal to be out of phase with the encoded data signal on the secondary side and a synchronization of the encoded signal with the beginning of a clock signal period is required in order to enable the correctly timed extraction of the original data signal. This is achieved by shifting either the clock signal or the encoded data signal to the correct phase which requires further complexity in the decoder circuit. In the proposed modified Manchester algorithm this complexity is instead shifted to the encoder circuit on the primary side to produce a modified encoded signal in order to lessen the complexity of the decoder circuit on the secondary side. The proposed decoder circuit is self-synchronizing due to clock and data signal being able to be decoded in the same

phase from the encoded modified Manchester signal. Furthermore the proposed concept exhibits an independence from process variations, temperature and transmission frequency inside a certain frame in which the original clock period does not decrease under the limit of the used one-shot generators pulse length.

A. Encoding process

The encoding process of a standard Manchester coded signal is shown in Fig. 3 in addition to the proposed modified Manchester code.

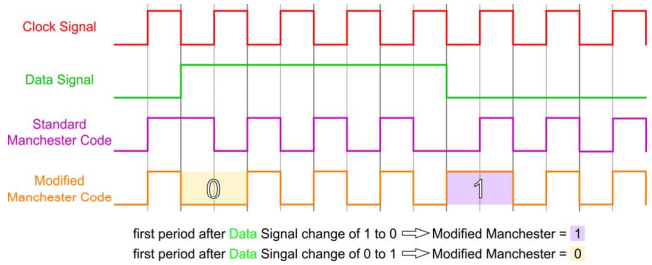

Fig. 3. Standard and modified Manchester code

The encoder used to encode the modified Manchester signal is illustrated in Fig. 4. In this encoder circuit, the original data signal is shifted by one clock period by a D-flip-flop and then further edited by comparing the original data signal (DATA) with the shifted data signal (Q) with an exclusive-OR (XOR) gate. Using the signal from this XOR gate a comparison can be done to check if a change between a logic state (0 to 1, or 1 to 0) has occurred in the last period. The inverted version of the original clock signal is then modified by an AND gate together with the inverted compared signal (X) and used to encode the original data signal in a final XOR gate to achieve the modified Manchester signal on the output of the encoder circuit.

TABLE I. SIGNALS IN MODIFIED MANCHESTER ENCODING

Signal	Origin 1	Operator	Origin 2
Q	DATA	D-flip-flop	CLK
X	DATA	XOR	Q
CLK2	$\overline{X}$;	AND	$\overline{CLK}$;
Modified Manchester	DATA	XOR	CLK2

This modified Manchester signal is then further processed by a circuit that converts the single ended signal to a differential signal using an inverter on one of the lines while keeping the delay between both transmission lines at a minimum. These signals are supplied to the inputs IN+ and IN- of the signal conditioning circuits which includes the capacitive coupling element.

B. Signal conditioning

An adapted version of the signal conditioning circuit described in [4] and [5] was applied to ensure a robust and reliable transmission of signals with minimal delay. This signal conditioning is illustrated in Fig. 5.

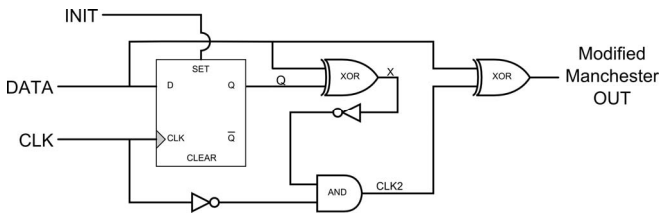

Fig. 4. Modified Manchester encoding circuit

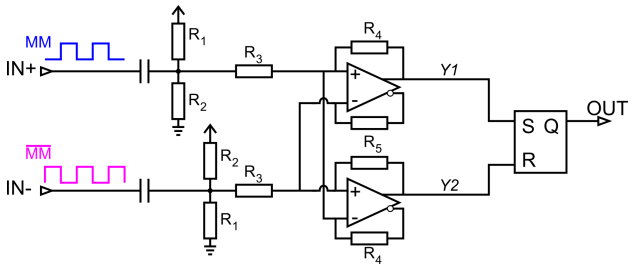

Fig. 5. Signal conditioning circuit

After the coupling elements utilized for the galvanic isolation the inputs to the comparators were outfitted with additional resistors (R1, R2) to the respective supply and ground rails to ensure a fixed reference for secondary side of the transmission lines. The comparators were connected in a positive feedback configuration for both inputs. This was done to control the switching threshold separately for each input and to ensure a well-defined signal state during the complete switching cycle. Both signals are then input to an SR-flip-flop where the top line signal Y1 represents the set signal S and the bottom line signal Y2 represents the reset signal R. At the output of the SR-flip-flop the modified Manchester signal is provided for the following decoder circuit. This signal conditioning circuit ensures a robust transmission of the encoded signals and the output of a clean signal.

C. Decoding process

For the decoding of the modified Manchester signal, a simple D-flip-flop (C) and the clock signal is necessary. As depicted in Fig. 6, the clock signal is extracted by flip-flops A and B in combination with an OR operator. While VDD is connected to the D-inputs, the Modified Manchester Signal and the inverted version of it are connected to the clock input of D-flip-flop A and B respectively. This means that VDD is put to the output Q on every rising edge of the modified Manchester signals and its inverted version. However, an inverted version CLR of the generated clock signal CLK OUT is connected to the clear input of D-flip-flops A and B. This causes the output of a logical zero to the output Q of the D-flip-flops A and B every time the clock signal CLK OUT goes high. This causes the exclusive recognition of state changes at the beginning of the clock period while state changes during the clock period are ignored. The Q outputs of flip-flop A and B are put into an OR gate which forms the preliminary signal CLKX. The first pulse of this signal CLKX initiates the clock signal generation and is inverted to be connected to the CLEAR input of flip-flop A and B. It continuously resets the output of flip-flops A and B after a finished clock pulse which in turn allows the generation of the subsequent clock pulse. To ensure a predetermined clock period length, the CLKX signal path includes a monostable multivibrator circuit which

stretches the preliminary clock pulses to the predetermined length previously defined by the original clock signal CLK supplied to the encoder circuit (Fig. 4). The monostable multivibrator used in the decoder circuit exhibits a topology similar to the topology described in [7]. All signals present in the decoding sequence are illustrated in Fig 7.

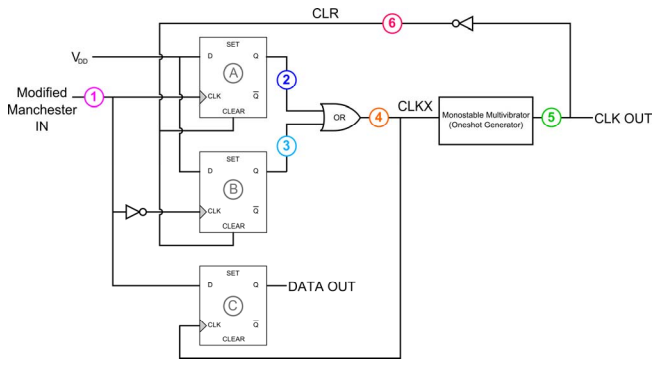

Fig. 6. Modified Manchester decoding circuit

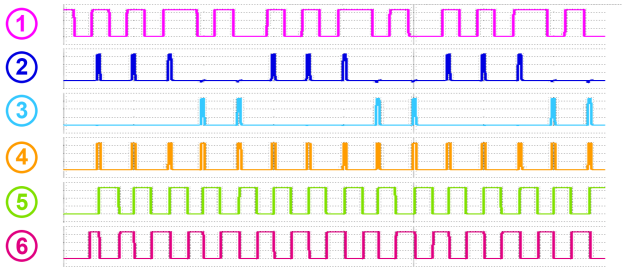

Fig. 7. Simulation of the decoding sequence (1: Modified Manchester Signal, 2:Output Q of flip-flop A, 3:Output Q of flip-flop B, 4: Signal CLK, 5:Signal CLK_OUT, 6: Signal CLR)

III. Simulation Results

The whole Modified Manchester circuit consisting of encoder circuit, signal conditioning and decoder circuit were designed and simulated using the integrated circuit design software Cadence 6.1.5. The encoder was designed to be able to handle a data signal with minimal pulse lengths of 20ns while utilizing a clock frequency of 50MHz which in this configuration corresponds to an effective data rate of 50Mbit/sec. The circuit diagram was created using the cadence schematics XL editor, while the actual IC layout was created by cadence layout editor XL. Both were optimized for robustness and reliability while minimizing the signal transmission delay. Due to the construction of the actual IC layout the transmission process could be simulated in consideration of parasitic resistances and capacitances occurring inside the circuit to guarantee simulation results that are as consistent as possible with measurement results in reality. Fig. 8 shows a simulation of the encoding and decoding sequence of the modified Manchester code. Signal 1 displayed in Fig. 8 represents the data signal (Fig. 4, Signal DATA) that is to be encoded and transmitted over the galvanic isolation. It is input into the encoder circuit (Fig. 4) together with the signal 2 that represents a clock signal (Fig. 4, Signal CLK) with a frequency of 50MHz to generate the modified Manchester signal (Fig. 6, Signal 3). Signal 4 represents the modified Manchester signal after the galvanic isolation and the signal conditioning circuit (Fig. 5, Signal OUT). After the signal conditioning circuit, the modified Manchester signal is then put into the decoder circuit (Fig. 6), the decoder provides the signal 5 that represents the decoded DATA signal (Fig. 6, DATA OUT). The signal 6 displayed in Fig. 8 represents the rebuilt clock signal that is also provided by the decoder circuit (Fig. 6).

IV. Experimental Results

The proposed galvanically isolated data transmission was realized as part of a galvanically isolated driver circuit as an integrated circuit. To accommodate the harsh environments that are commonplace in automotive application a high temperature capable IC technology provided by X-Fab Semiconductors was chosen for the development of the ASIC. This high temperature technology was able to tolerate temperatures in an extended range of -40°C and +175°C. All functional blocks included in the ASIC were designed and layouted to ensure a robust and reliant functionality within the proposed temperature and voltage range. The proposed ASIC was equipped with gold bond wires with a strength of 1.2mil and coupling capacitances of 10p which would be able to tolerate the estimated dV/dt of 80kV/µs and the corresponding occuring current of 80mA without problems. Several functional tests with the modified Manchester code were performed on the processed ASIC with the previously described functional blocks. Fig. 9 shows the measurement of the modified Manchester encoding and decoding process which was performed at a clock frequency of 50MHz. The signal declared as “Modified Manchester Code” in Fig. 9 shows that the encoder was able to perform the proposed encoding algorithm at the given frequency. The measurements of the decoding process circuit were performed under the same conditions at a transmission frequency of 50MHz with coupling capacitances of 10pF. Fig. 9 shows the encoder input signals DATA and CLK together with the signals of the decoder output DATA OUT and CLK OUT. A delay of 40ns was measured between the input signal of the encoder circuit DATA and the output signal of the decoder circuit DATA OUT with a jitter of less than 5ns. These Measurements confirm the proper function of the Modified Manchester encoding and decoding process as well as its viability under realistic conditions.

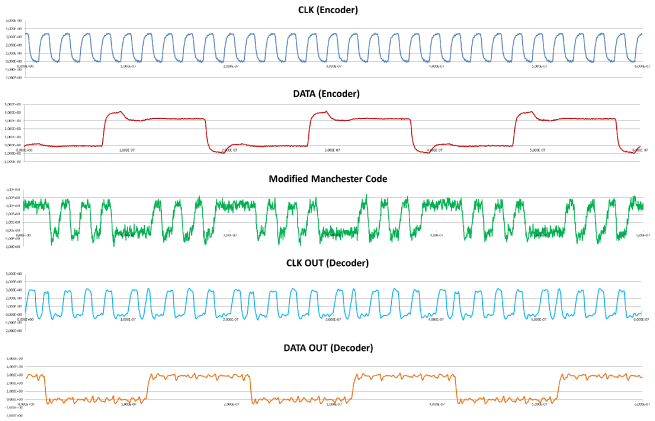

Fig. 8. Measurement of Modified Manchester encoding and decoding

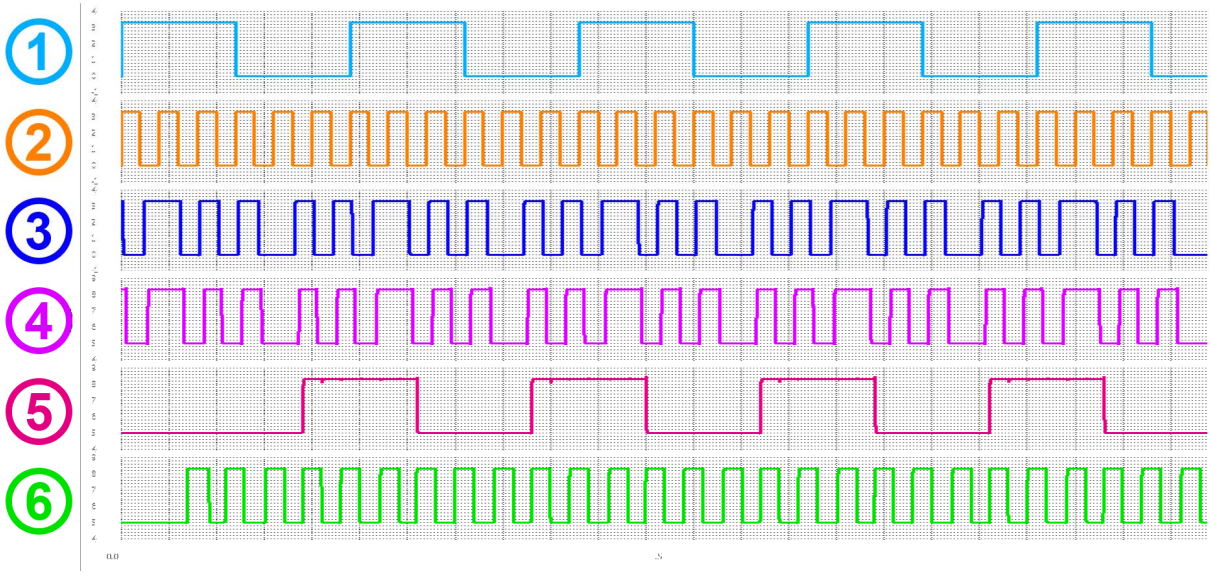

Fig. 9. Simulation of the sequence of encoding, singal conditioning and decoding of the modified Manchester code (1:Data signal 2:Clock, 3:Modified Manchester signal, 4:Modified Manchester Signal after the capacitive coupling element and signal conditioning, 5:decoded data signal, 6:rebuilt clock signal)

V. SUMMARY

The presented data transmission topology consists of the following components: An encoder circuit to generate a modified form of Manchester code which enables the synchronous decoding of data and clock by the decoder circuit from just this one encoded signal. Two galvanically isolating capacitive coupling elements combined with a differential signal conditioning circuit for the transmission of the encoded signal with a high robustness to external influences. Lastly a decoder circuit that is able to decode the modified Manchester code and provide the original data signal as well as a rebuilt clock signal. As confirmed by simulation and experimental results this data transmission topology is able to provide a robust and galvanically isolated high frequency transmission of the encoded data signal. Furthermore no additional coupling elements are needed to transmit the original clock signal that was used to encode the data signal over the galvanic isolation to the decoder circuit. This provides a high reliability at a minimum number of passive coupling elements. The integration of the whole circuit provided a high miniaturization factor in addition to the possibility of processing high frequency signals.

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