Prediction of SRAM Reliability Under Mechanical Stress Induced by Harsh Environments

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***Abstract*—On the example of a 28nm SRAM array, this work presents a novel reliability study which takes into account the effect of externally applied mechanical stress in circuit simulations. This method is able to predict the bit failures caused by the stress via the piezoresistive effect. The stability of each single SRAM cell is simulated using static noise margin. Finally, the whole array's behavior is reproduced by including device parameter variations in Monte-Carlo simulations. The results show good agreement with corresponding experiments in which mechanical stress was introduced into the SRAM array by indentation. This validates the presented simulation method for future use in the design of electronic products, especially for harsh environment applications, where high stress is expected.**

Keywords- *SRAM Stability, SRAM Reliability, Mechanical Stress, Device Simulation, Piezoresistance, SPICE-Simulation, Monte-Carlo Simulation, Static Noise Margin*

I. Introduction

The continuing miniaturization in nanoelectronic circuits makes semiconductor chips available that integrate an ever increasing functionality. Since ensuring the reliability of these complex systems is challenging, primarily consumer electronics (CE) has benefitted from this evolution so far. However, safety-critical applications (automotive, avionics, medical) are nowadays as well in need of high-performance integrated circuits (ICs) of the most advanced technology nodes. Since no longtime data on field performance is available for these nodes, reliability modeling must depend on high-accuracy simulations. It is also forced to include destabilization effects considered marginal in CE application.

Field effect transistors (FETs) are a vital component of ICs, and accounting for their degradation through hot carriers [1] and through the bias-temperature instability [2] has a long tradition. Furthermore, the time-zero variability of the FET parameters due to process variation is a standard aspect of reliability simulations. Whereas the piezoresistive effect has been known for a long time to influence the FET characteristics [3] and has found applications in pressure sensors [4], strain engineering [5] or FET placing strategies near VIAs [6], only recent experiments have demonstrated the impact of the piezoresistive effect on general IC reliability [7–9]: exposing an SRAM array to mechanical stress from nanoindentation modifies the cell's FET characteristics and induces bit failures. This failure mode is in particular relevant for circuits driven in harsh environments where bending or vibration can result in high mechanical stress during circuit operation.

Preventing failures from externally applied stress requires taking into account appropriate piezoresistance models during circuit design. We here present a simulation method that is able to account for this effect and compares well to experimentally measured failures. We start with a general discussion of piezoresistivity and describe how to model it on single-FET level. In the main part of this paper, we apply the method to the analysis of an SRAM array under mechanical stress and verify the simulational results by experimental measurements.

II. Linearised piezoresistivity model

By the piezoresistive effect in silicon, the application of mechanical stress results in a change in conductivity. Its microscopic origin is the crystal lattice deformation under stress, which leads to a change in band structure, and in carrier scattering processes. The local relative change in silicon resistivity ρ is linked to the local stress tensor $\hat{\sigma}$ in six component vector notation as [10]

$$\frac{\Delta\rho_j}{\rho_0} = \sum_k \pi_{jk}\sigma_j. \tag{1}$$

The silicon piezoresistance tensor π consists of three independent components π_{11}, π_{12} and π_{44} representing the ρ change along the direction of each normal component of stress, perpendicular to its direction and due to shear stress, respectively. In this work, only the current, and therefore resistivity, in channel direction is considered. Furthermore, only the three normal stress components are included in the simulations.

III. Piezoresistivity modeling for single FETs

The quadratic model for MOSFET drain current in the saturation region is

$$I_d = \mu K \left(V_{gs} - V_{th}\right)^2, \tag{2}$$

where V_{gs} and V_{th} are the gate-source and the threshold voltage, μ is the carrier mobility and K a constant factor.

While the influence of mechanical stress on V_{th} is not completely certain, most evidence points to no influence [11–13], therefore V_{th} is assumed independent of stress and the

relative change in I_d, here due to stress, becomes equal to the relative change in mobility alone

$$\frac{\Delta I_d}{I_{d0}} = \frac{\Delta\mu}{\mu_0}. \tag{3}$$

The often used approach [11, 14] to include piezoresistivity into the above equation is via the relation $\Delta\mu/\mu_0 = -(\Delta\rho/\rho_0)$, which was also used in earlier published stages of this work. However since the relation between resistitvity and mobility is $\rho = 1/q\mu n$, with the electron charge q and the carrier concentration n, this relation only holds true for very small changes in resistance and is no longer appropriate at the stress levels seen in this work. To include larger changes the following equation is used

$$\frac{\Delta\mu}{\mu_0} = \frac{\mu_s - \mu_0}{\mu_0} = \frac{1/\rho_s - 1/\rho_0}{1/\rho_0}, \tag{4}$$

where μ_s and ρ_s are the mobility and resistivity under mechanical stress. Combining 4 with 1 and 3 yields [15]:

$$\frac{\Delta I_d}{I_{d0}} = \frac{\Delta\mu_j}{\mu} = \frac{1}{\frac{\Delta\rho_j}{\rho}+1} - 1 = \frac{1}{\sum\limits_k \pi_{jk}\sigma_j + 1} - 1. \tag{5}$$

This change in drain current due to stress can now be implemented into a SPICE-simulation.

IV. Piezoresistivity and SRAM stability

A. SRAM static noise margin

Cross-coupling two inverters leads to a circuit with two stable states. Extending it by two access transistors allows reading and writing the SRAM cell state, see Fig. 1. The

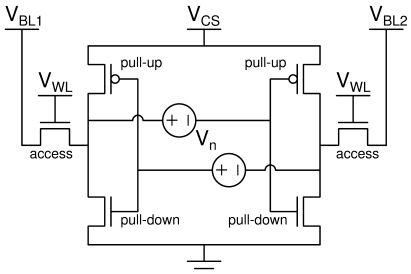

Fig. 1: Schematic of an SRAM cell with noise sources V_n after [16].

stability of this circuit in static consideration is described by the static noise margin (SNM, [16]). Two voltage sources of opposite polarity and identical magnitude V_n within the cross-coupling loop model the electrical noise. The static noise margin is defined as the minimum V_n that removes one of the two cell states, turning the cell into a system with only a single stable state unable to store information. Geometrically, the SNM has an interpretation as the edge length of the maximum square that can be inscribed in *both* lobes of the butterfly curve, which results from combining the two inverter voltage transfer curves as shown in Fig. 2.

During read access, the SRAM cell is particularly prone to a bit flip. Therefore, in this work, cell stability is modeled by the read static noise margin m, defined as the SNM with the bit lines and word line at the same high potential, such that the access FETs are open and the bit line potential destabilizes the cell.

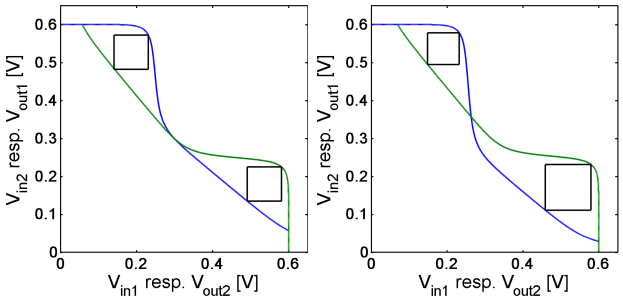

Fig. 2: On the left the butterfly curve of a symmetric SRAM cell is shown, on the right that of an asymmetric one with V_{th} of all transistors randomly varied. Both graphs include a graphical representation of the static noise margin as black squares in the eyes of the curve.

The margin m depends on cell design, voltage conditions, mechanical stress, FET variability and further parameters. We find that the dependence of m on V_{CS} is approximately linear and external mechanical stress adds an offset but does not change the slope of this dependence if all other aforementioned factors remain constant.

Inverting the V_{CS} dependence of m provides an alternative measure for cell read-stability: for given static noise m_{ref}, the voltage $V_{\mathrm{dipR}}(m_{\mathrm{ref}}, \sigma)$ satisfies

$$m(V_{\mathrm{CS}} = V_{\mathrm{dipR}}, \sigma) = m_{\mathrm{ref}}. \tag{6}$$

The quantity V_{dipR} is experimentally determined as the minimum supply voltage V_{CS} for which the bit cell remains stable during a read access, see Fig. 3. Note that during the V_{dipR}

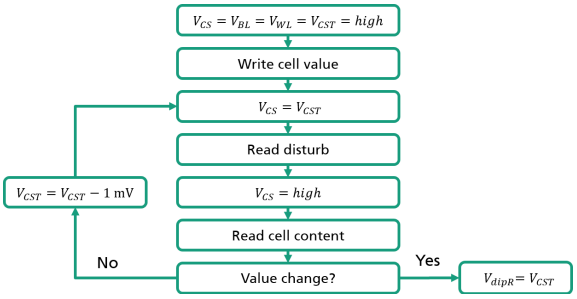

Fig. 3: Measurement procedure for V_{dipR}.

test, the bit and word line potentials remain fixed and are not lowered with V_{CS}.

B. Accounting for doping variability

Accounting for the variability of SRAM cells in the simulation is essential for subsequent comparison to experiments. The V_{th} variability of an SRAM cell's FETs is particulary important and a standard consideration in this regard.

While these V_{th} variations lead to a change in cell characteristics per se, in this work parameters affecting piezoresistivity are more important. The piezoresistive coefficient π is dependent on doping level [10] and so is the variation in V_{th}

[17]. While the local variation in doping level is unknown and not available, it can be roughly estimated using the variability in V_{th} as a proxy. Finally, the variability in π resulting from the one in doping level can be calculated and used in the simulations.

C. Experimental setup

The here described experimental approach [8] allows to examine Chip-package-interaction (CPI) and Chip-board-interaction (CBI) for novel SRAM devices in operation and to detect potential failures of the architecture.

The chips were assembled on a flip chip substrate without a lid and the silicon was thinned down to a minimum of 16 µm at the back side. To enable electrical in-situ measurements, the chip was connected to a socket before, during, and after the indentation with forces of various magnitudes. The here described experimental setup enables a fully reversible process in contrast to a previous study [7].

The experiments consist of two parts each with a distinct electrical measurement procedure. In both of them the mechanical stress is induced by spherical, elastic nanoindentation performed at the backside of the chip. Simultaneous to these indentations, electrical measurements are taken. The first procedure is already described in Sec. IV-A to determine V_{dipR} under stress and thereby ΔV_{dipR} in comparison to its unstressed value. The other procedure is a 50 times repeated read disturb at a fixed voltage V_{CST} but otherwise consists of similar steps as shown in Fig 3.

Fig. 4 shows the resulting bit cell fault matrix with additional background noise for an applied load of 1.3 N. Loading leads to a significant 40% radial increase of the bit cell fault probability at the indentation area (red circle). The process is fully reversible, meaning that the fault disappears upon unloading.

Fig. 4: Bit fault matrix with additional background noise for 1.3 N load. The blue lines indicate an averaging corridor for data representation in a 1D graph further explained in Sec. IV-D

As a last step, finite element method (FEM) simulations of the indentation are conducted using the SRAM layout and the semiconductor stack parameters (exact geometry and material information for each layer) to yield stress/strain fields at the indented area. The model contains the actual chip device with a thinned Si-layer, solder bumps with an underfill layer, a finely layered BEoL structure and the nanoindentation tip used for spherical indentation. The used finite element solver is a deformation-based solver, which means that the deformations are calculated, and then the stress tensor is obtained using the standard constitutive models.

D. Comparison of simulation and experiment

The simulations will be compared to the experimental results in two ways. First the experimental results were converted into a graph showing the change in V_{dipR} along one axis of the SRAM array, arbitrarily defined as x-direction. As can be seen in Fig. 4 the cells whose V_{dipR} lies in the voltage range examined in the experiment are sparsely scattered, making up approx. 1% of the array's cells. Therefore, a ΔV_{dipR} graph for one row of cells is not practical and an 81 cells wide averaging corridor is defined, indicated by the blue lines. A window of 25 cells length is moved along the corridor in one column steps, and the average ΔV_{dipR} of all examined cells located within is determined. The resulting graph is shown in Fig. 5 together with simulation results using the mechanical stress values corresponding to the corridor's central row of cells as input. The simulation results show good agreement with the experiments, differing at most by a factor of 1.25.

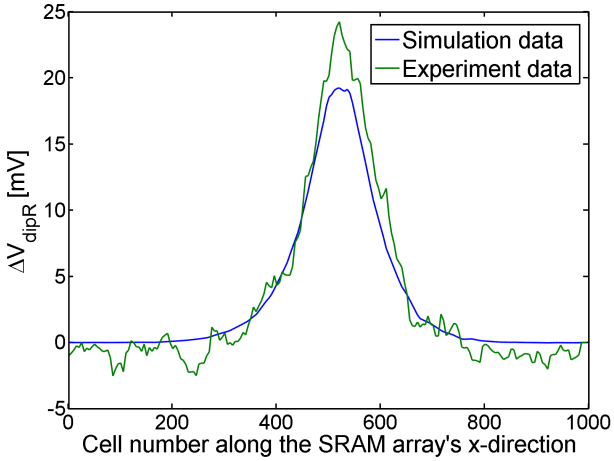

Fig. 5: Comparison of experiment and simulation results showing good agreement. The experimental results are running averages along an 81 cell wide corridor while the simulation used stress values corresponding to the corridor's central row of cells. Results differ by a factor of 1.25 at the peak. The slopes are also well reproduced.

Next, the results of a simulated 2D array of SRAM cells are shown. Here a Monte-Carlo simulation with 100k samples is conducted. The samples were spread evenly on a 2D grid, and a voltage range equal in extend but not absolute value to the experiments was chosen so that it contains the unstressed V_{dipR} of 1% of samples corresponding to the experiment. Because noise levels in the experiment are unknown, only ΔV_{dipR} of the simulations can be compared, not absolute values. The results of the FEM stress simulation are now overlaid on the cell grid and used as input for ΔV_{dipR} simulations. The results of this simulation and a corresponding map of experimental results can be seen in Fig. 6.

The results of the 2D simulation also agree well with the experiments. The cells around the indentation point show a similar average ΔV_{dipR} and the size of the stress affected

regions correlates well. There are minor discrepancies at the most extreme values of ΔV_{dipR} and in the diameter of the stress affected region along the x axis. These differences can both be accounted for by the higher sample size in the experiment compared to the simulation.

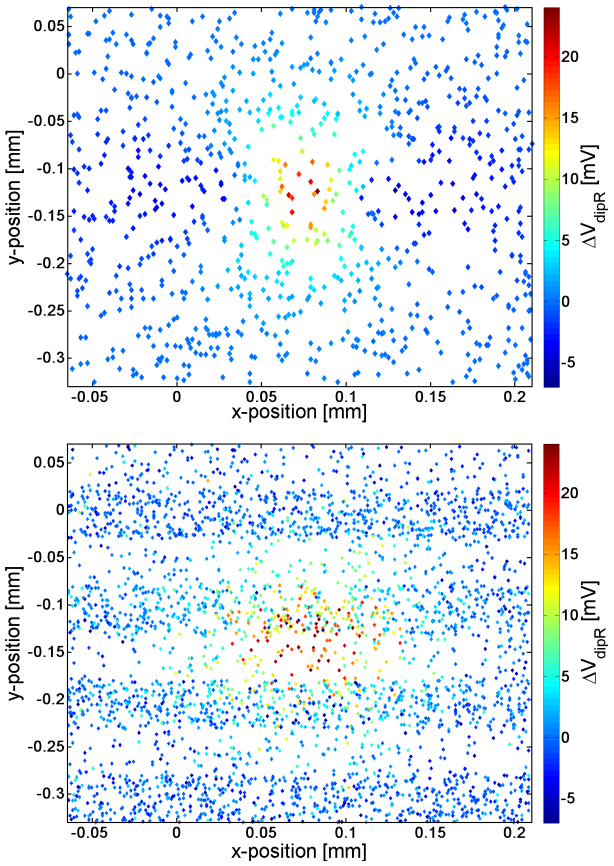

Fig. 6: The 2D Monte-Carlo simulations shown on top and the experiment data shown below are in good agreement: the centers and outline of the group of cells showing stress dependent behavior match well. The stripe structure of the experiment data is due to technology dependent distribution of the SRAM cells in the array.

V. Conclusions

This work describes the simulation of an SRAM array under extrinsic mechanical stress. It starts with the piezoresistivity model, describing the relation between mechanical stress and semiconductor resistivity, which is then integrated in simulations of the FETs of an SRAM cell via mobility change leading to change in drain current. To accurately reproduce the behavior of a full SRAM array, parameter variability of V_{th} was included and the doping level dependent variability of the piezoresistive coefficient π was estimated by way of the, also doping dependent, V_{th} variation. These variabilities lead to varying reactions to mechanical stress and were included via Monte-Carlo simulations. Finally, the results were compared to experimental outcomes and are in good agreement. The described approach is thereby validated for use in the design of electronic components designated for harsh environments, where the occurrence of mechanical stress is expected. Including this method will make such devices more reliable without the need for tedious and costly validation experiments. The method presented in this paper will be expanded, validated for further technologies, and provided as a predictive tool for IC design.

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