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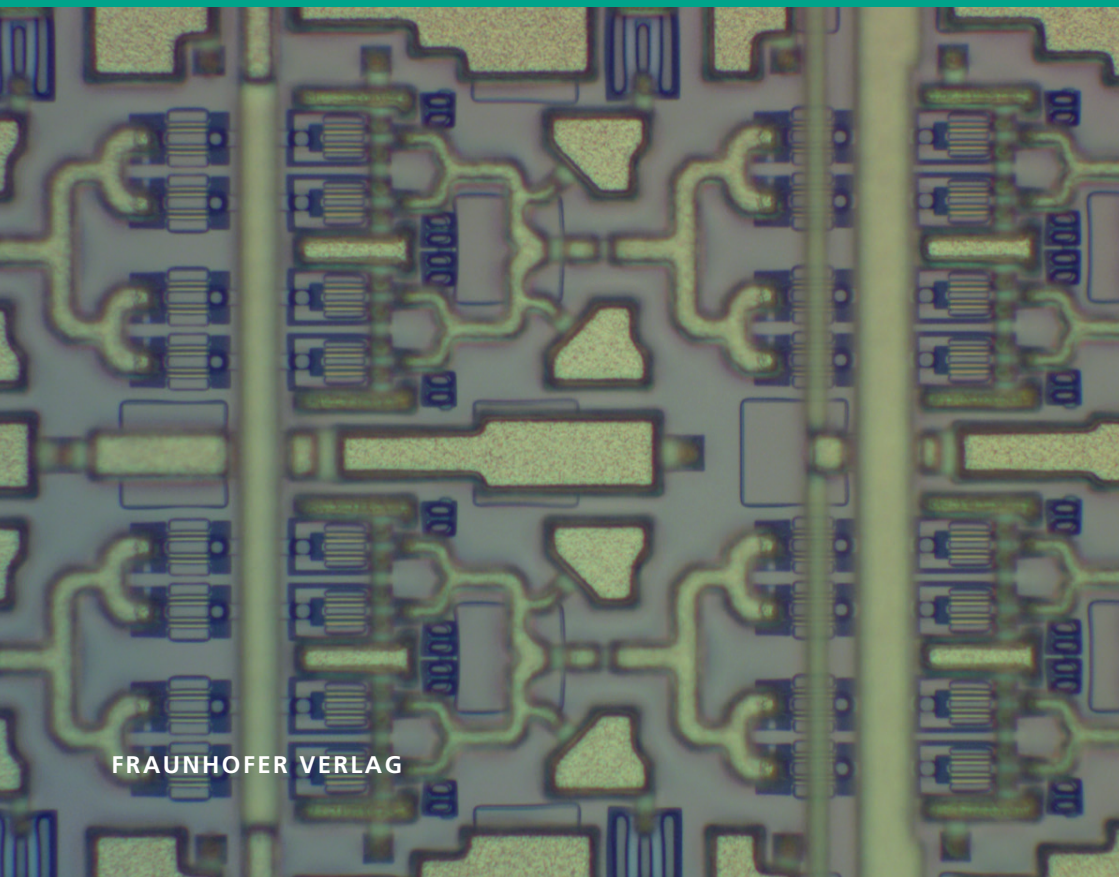
Laurenz John

INTEGRATED SUB-MILLIMETER-WAVE HIGH-POWER AMPLIFIERS IN ADVANCED InGaAs-CHANNEL HEMT TECHNOLOGY



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Contact:
Fraunhofer Institute for
Applied Solid State Physics IAF
Tullastrasse 72
79108 Freiburg
Phone +49 761 5159-0
info@iaf.fraunhofer.de
www.iaf.fraunhofer.de

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Integrated Sub-Millimeter-Wave High-Power Amplifiers in Advanced InGaAs-Channel HEMT Technology

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Kurzfassung

Die vorliegende Arbeit beschreibt die Entwicklung von breitbandigen, monolithisch integrierten Leistungsverstärkern im Frequenzbereich um 300 GHz. Diese Schaltungen sind zentrale Kernkomponenten für den erfolgreichen Aufbau von zukünftigen, hochbitratigen Richtfunkstrecken als auch von innovativen Radarsensoren im unteren THz-Frequenzbereich. Wesentliche Ziele der Arbeit sind die eingehende und umfassende Untersuchung von geeigneten Transistorkonfigurationen und Schaltungskonzepten, die erfolgreiche Realisierung von kompakten Verstärkerzellen für die platzeffiziente Integration in multifunktionalen Frontend-Schaltungen sowie der Aufbau von leistungsstarken Verstärkermodulen mit hoher Linearität.

Auf Transistorebene ist die experimentelle Optimierung der Gate-Drain-Recesslänge für eine Verbesserung der Durchbruchspannung auf über 4 V beschrieben. Diese Entwicklung ermöglicht den Betrieb der Bauelemente mit Spannungen größer als 1,5 V sowie eine Verbesserung der Leistungsdichte auf Werte von über 250 mW/mm. Des Weiteren werden in dieser Arbeit erstmals monolithisch integrierte Strukturen zur Load-Pull-Charakterisierung im Frequenzbereich oberhalb von 200 GHz untersucht, wodurch einzigartige Möglichkeiten zur Modellverifikation ermöglicht und neue Erkenntnisse für den Verstärkerentwurf bei 300 GHz gewonnen werden können.

Zur erfolgreichen Realisierung von ultrakompakten Submillimeterwellen-Verstärkern mit bisher unerreichter Ausgangsleistung, ist ein neuartiger Modellierungsansatz von Mehrfingertransistoren dargestellt. Dieser basiert auf erprobten Modellen von Zweifinger-Transistorfingern, welche in einer EM-simulierten Mehrfingertransistorschale implementiert werden. Die erfolgreiche Anwendung dieser Modellierungsmethode ermöglicht eine deutliche Reduzierung der benötigten Chipfläche und darüber hinaus eine wesentlich verbesserte Beschreibung der Bauelementeigenschaften von Leistungstransistoren mit bis zu acht Transistorfingern.

Für die Entwicklung von innovativen Leistungsverstärkerzellen und verlustarmen Power-Combining-Netzwerken ist die Analyse und Bewertung kompakter Dünnfilm-Verdrahtungsmöglichkeiten beschrieben. Durch die Realisierung neuartiger Vorderseiten-mikrostreifenleitungen mit strukturierter Massefläche wird die Entwicklung sehr hochohmiger Leitungstypen gezeigt, welche die erfolgreiche Realisierung von monolithisch integrierten On-Chip-Combinern mit signifikant verbesserter Effizienz bei THz-Frequenzen ermöglichen.

Basierend auf diesen Arbeiten sowie der eingehenden Analyse von parallelen und seriellen Transistorkonfigurationen, wird die Umsetzung einer neuartigen Verstärkertopologie bei 300 GHz demonstriert. Die Topologie basiert auf der Kombination von Kaskoden-Zellen in den Eingangsstufen und Common-Source-Bauelementen in der Ausgangsstufe. Dies ermöglicht die platzeffiziente Parallelschaltung von 32 Transistorfingern mit einer enormen ausgangsseitigen Gesamtgateweite von 512 µm innerhalb einer sehr kompakten Chip-Breite von lediglich 0,35 mm. Aufbauend auf dieser Verstärkertopologie wird

eine operative Bandbreite von mehr als 50 GHz und eine Rekord-Ausgangsleistung von 24 mW bei 300 GHz erzielt, was eine Verbesserung der bisherigen maximalen Ausgangsleistung der zugrundeliegenden HEMT-Technologie um den Faktor 4 darstellt. Durch die deutliche Verkleinerung der für die Verstärkerzelle benötigten Chipfläche, wird die Ausgangsleistung pro eingesetzter Chipbreite ebenfalls sehr signifikant um einen Faktor von größer als 4 gesteigert. Die gemessene Ausgangsleistung der sehr kompakten Verstärkerzelle is größer als 20 mW von 286 bis 310 GHz, was den weltweiten Stand der Technik in diesem Frequenzbereich definiert.

Durch den erfolgreichen Aufbau der innovativen Submillimeterwellen-Verstärker in Hohlleitermodule wird eine beeindruckende lineare Ausgangsleistung von 6 mW und eine Sättigungsleistung von mehr als 10 mW über eine 3 dB-Bandbreite von 285 bis 335 GHz erzielt. Mit diesen Ergebnissen wird der Stand der Technik für mHEMT-Verstärkermodule um einen Faktor von bis zu 4 verbessert, wodurch eine signifikante Steigerung der verfügbaren Ausgangsleistung für die Realisierung von Kommunikationsanwendungen als auch hochauflösenden Radarsensoren der nächsten Generation erfolgreich demonstriert wird.

Abstract

This work examines the realization of broadband InGaAs mHEMT power amplifiers in the frequency band around 300 GHz. These circuits are developed as key components for the implementation of wireless high-capacity communication systems and innovative radar solutions in the lower THz frequency band. The goal is the in-depth investigation of device configurations and amplifier topologies for the realization of highly-compact power amplifier cells, which are suitable for monolithic integration in multifunctional front-end circuits as well as low-loss packaging into waveguide modules.

With the evaluation of different drain-gate recess lengths, the break-down voltage of the mHEMT devices is improved to values above 4 V. This permits the operation of the transistors at voltage levels exceeding 1.5 V and increases the power density to values larger than 250 mW/mm at device level. Furthermore, monolithic integrated circuits for on-chip load pull are demonstrated for the first time in the frequency range above 200 GHz, providing the unique possibility of model verification and new insight for PA-design considerations in the lower THz range around 300 GHz.

To reduce the size of the PA MMICs and maximize the output power per required chip width, a novel modeling approach for multi-finger transistors is implemented. This approach is solely based on two-finger device models which are included in an EM-simulated multi-finger shell. By using this innovative modeling method, highly-compact devices with up to 8 transistor fingers are realized and accurately described. Thus, the superior model accuracy and bandwidth of the symmetric two-finger transistor is utilized and limitations of previously-used HEMT devices are overcome.

To implement highly-compact power amplifier cells and power-combing networks, thin-film wiring possibilities are analyzed and evaluated. For the first time, thin-film transmission lines with structured ground metal are implemented in a III-V technology at the lower THz-frequency range. These transmission lines are used as key building block for the realization of novel thin-film combiners with improved combining efficiency in comparison to previously-reported THz power combiners.

Based on these investigations as well as the analysis of parallel-connected and series-connected device configurations, the implementation of a novel 300-GHz PA topology is evaluated. This topology is based on the combination of cascode gain stages at the input and common-source devices in the output stage, which enables the successful and chip-space-efficient integration of 32 parallel transistor fingers with a total gate width of 512 µm on an ultra-compact chip width of only 0.35 mm. State-of-the-art output-power performance is achieved with this chip-size-optimized PA topology, demonstrating high bandwidths and a record output power of 24 mW around 300 GHz. Hence, the output-power level of the underlying technology is significantly improved by a factor of 4. Since the PA core is implemented on an even reduced absolute die area, when compared to previously-reported mHEMT PA circuits, the output power per required chip width is also increased by a factor larger than 4. The measured output power of this compact

amplifier cell is in excess of 20 mW over the frequency range from 286 to 310 GHz, advancing the state of the art for solid-state power amplifier MMICs.

Additionally, with the successful packaging into waveguide modules, more than 10 mW saturated output power and state-of-the-art 6-mW linear output power are demonstrated on waveguide level with a 3-dB bandwidth covering the frequencies from 285 to 335 GHz. These results improve the state of the art for mHEMT amplifier modules by a factor of up to 4, successfully demonstrating a significant increase in available output power for the realization of next-generation communication applications and high-resolution radar sensors.

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Contents

Abbreviations and Symbols

Abbreviations

ADS	Advanced Design System
BCB	Benzocyclobutene
BEOL	Back end of line
B2B	Back to back
CB	Common base
CE	Common emitter
CG	Common gate
CI	Confidence interval
CPW	Coplanar waveguide
CS	Common source
CST	Computer Simulation Technology AG
DC	Direct current
DUT	Device under test
ECPW	Elevated coplanar waveguide
EM	Electromagnetic
FEOL	Front end of line
FET	Field-effect transistor
FOM	Figure of merit
GaAs	Gallium Arsenide
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
IC	Integrated circuit
IMN	Input matching network
InGaAs	Indium Gallium Arsenide
InP	Indium Phosphide
ISMN	Interstage matching network
ISS	Impedance standard substrate
LNA	Low-noise amplifier
mHEMT	Metamorphic high-electron-mobility transistor
MAG	Maximum available gain
MIM	Metal-insulator-metal
MMIC	Millimeter-wave integrated circuit
MSG	Maximum stable gain
NiCr	Nickel-Chromium
OMN	Output matching network

P2P	Point-to-point
PA	Power amplifier
PDK	Process design kit
RF	Radio frequency
SEM	Scanning electron microscope
SiGe	Silicon Germanium
SiN	Silicon Nitride
SSPA	Solid-state power amplifier
TFMSL	Thin-film microstrip transmission line
TFR	Thin-film resistor
TGW	Total gate width
TRL	Thru-reflect-line
TSV	Thru-substrate via
UA	Unit amplifier

Symbols

BV_{DSO}	Off-state drain-source breakdown voltage
f_{max}	Maximum frequency of oscillation, power-gain cutoff frequency
f_{op}	Frequency of operation
f_T	Transit frequency, current-gain cutoff frequency
g_{DS}	Output conductance
g_m	Transconductance
h_{21}	Forward current gain
I_D	Drain current
$I_{D,max}$	Drain current in saturation
I_G	Gate current
k	Rollet stability factor
OP_{1dB}	Output power in 1-dB gain compression
OP_{3dB}	Output power in 3-dB gain compression
P_{DC}	DC power
P_{out}	Output power
Q	Quality factor
R_D	Drain resistance
R_S	Source resistance
U	Unitary power gain, Mason gain
V_{DS}	Drain-source voltage
V_G	Gate voltage
V_{th}	Threshold voltage
W_G	Gate width

1 Introduction

"Nothing, I guess". This was the reputed response of Heinrich R. Hertz, the physicist who first demonstrated the existence of electromagnetic waves, when asked about any potential application for his "Hertzian waves". Since Hertz's first proof of James C. Maxwell's theory of electromagnetism in 1886 [7, 45], however, the radio waves have significantly shaped and contributed to our economic and social development since the early 20th century.

While the millimeter-wave (mm-wave) frequency spectrum—covering the frequency range from 30 to 300 GHz—has been attracting radar and wireless-communication applications for decades, the purpose has been mainly for scientific and military usage. In recent years, however, mm-wave technologies have been fostered by commercial applications, such as automotive radar and 5G [9, 47], that go well beyond the traditional niche markets. This trend towards ever-higher frequencies and the increased interest for wireless-system implementation at frequencies up to 300 GHz—even at a commercial level—is driven by the available spectrum, which provides the bandwidths for high-capacity communication and high-resolution radar applications.

With the rapid shift to an always connected society of today's digital world, however, the electromagnetic spectrum has become a valuable and scarce resource, due to the increasing integration of sensing devices and technologies into everyday appliances for systems and applications, such as the Internet of things, machine-to-machine communication, and autonomous vehicles. Driven by new businesses and applications, billions of sensors and actuators are being wirelessly connected and every little piece of the frequency spectrum, up to the upper end of the mm-wave frequency range at 275 GHz, has already been allocated for wireless communication, sensing, and radar applications in most parts of the world [29, 31, 86].

Due to the ever-rising global mobile data traffic—which is growing by almost 50 % every year [19]—engineers, researchers, and spectrum regulators are looking to the sub-millimeter-wave frequency bands around and above 300 GHz [1, 2]. Especially the frequency band around 300 GHz has attracted a lot of attention for the implementation of high-data-rate wireless point-to-point (P2P) links in recent years [16, 22, 40, 95, 104]. Enabled by the high absolute bandwidths, which are available at the THz-frequency range (0.3–3 THz), wireless backhaul links have become feasible with the capability to handle the predicted Tbit/s throughput in the backbone of beyond-5G communication networks, either as an extension or replacement of fiber-optical connections [15, 69, 88].

While the next generations of mobile communication networks are, in addition, discussed as a crucial technology for autonomous vehicles [33], another key enabling technology for future self-driving transportation solutions are millimeter-wave radar sensors [20, 91]—which are already significantly contributing to the road safety of today. As the bandwidth for automotive radar applications is typically below a couple of Gigahertz, broadband millimeter-wave active and passive imaging systems have demonstrated

manifold applications in safety and security, due to their ability to operate in harsh environmental conditions like snow, fog, dust and penetrate materials such as plastic, drywall, and clothing [71, 72]. While broadband W-band radar systems, with a bandwidth of operation exceeding 25 GHz, have demonstrated a resolution close to 7 mm at 80 GHz [83], the high achievable bandwidth, increasing resolution, and shrinking antenna dimensions are a strong motivation to increase the center frequency to the lower terahertz-frequency band around 300 GHz. Broadband radar systems in this frequency range, for instance, have demonstrated imaging solutions with sub-4-mm resolution [14, 74].

One of the key building blocks for most of these wireless communication or imaging systems is the power amplifier in the output stage of the transmitter. Yet, achieving sufficient output-power levels to compensate the rising atmospheric attenuation and free-space path loss [103] is a major challenge when increasing the frequency of operation well above 100 GHz. This is due to the shrinking dimensions of the active devices—which are scaled down in order to achieve the required cutoff frequencies for sub-millimeter-wave operation—reducing the breakdown voltage and available power density on the device level.

1.1 Technologies for 300-GHz Power Amplifiers

With the progressive scaling of junction dimensions and junction thicknesses of active devices, high-bandwidth transistor technologies featuring power-gain cutoff frequencies (f_{max}) above 1 THz have been demonstrated over the last decade [61, 66, 70, 118]. Driven by the growing interest in communication, radar, and imaging applications at frequencies around 300 GHz, even silicon-based CMOS technologies have demonstrated active circuits up to 325 GHz [81, 116]. Up to date, however, the best performance in terms of bandwidth, gain, and output power of 300-GHz stand-alone-amplifiers as well as receive and transmit circuits is enabled and has been demonstrated by III-V high-electron-mobility transistor (HEMT) and heterojunction bipolar transistor (HBT) devices.

When requiring high gain and lowest noise figures—not only considering the power density on device level—the InGaAs-channel HEMT has proven to be the most suitable semiconductor device technology for the development of high-dynamic-range transmit and receive solutions at the lower THz band. Especially InGaAs metamorphic HEMT (mHEMT) devices, which are processed on GaAs wafers, have demonstrated state-of-the-art low-noise amplifiers [113, 110] as well as chipsets for broadband radar [75] and communication [57] applications with state-of-the-art noise figures above 100 GHz. Furthermore, by integrating multiplier, mixing and amplifier circuits on a single die—as shown with the integrated 220–260-GHz InGaAs mHEMT single-chip radar front end in [75]—high complexity on circuit level has been demonstrated with III-V HEMT devices.

While InGaAs mHEMT devices have demonstrated state-of-the-art noise figures at mm-wave and THz frequencies, the generation of high RF-power levels of 10 dBm and more, has proved to be a major challenge. As the bias voltage for safe long-term operation is typically in the range of 1.0 V, the power density is limited on device level. Fig. 1.1 shows the state of the art in terms of measured output power demonstrated by H-band amplifiers, excluding the results of this thesis. This frequency range is dominated by InP-based HBT and HEMT technologies with significantly larger breakdown voltages and,

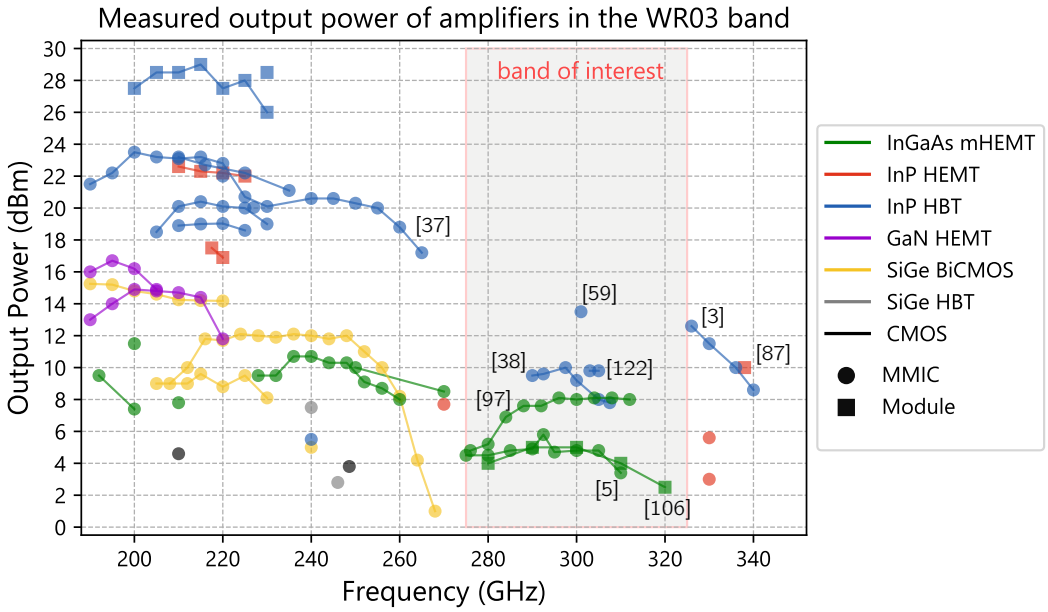


Figure 1.1: State-of-the-art measured output power of solid-state power amplifier MMICs and modules at H-band frequencies, excluding the results of this thesis.

Table 1.1: Most relevant III-V HEMT and HBT technologies for H-Band operation

Technology	f_T (GHz)	f_{max} (GHz)	BV_{off} (V)	V_{bias} (V)	Wiring type	Company/Institute
InP HBT	392	859	> 4.5	2.0	thin-film microstrip line	Teledyne Scientific
InP HEMT	500	1200	> 4	> 1.8	(grounded) coplanar waveguide	Northrop Grumman Corp.
InGaAs mHEMT	>500	>1000	> 3.5	1.0	(grounded) coplanar waveguide	Fraunhofer IAF

therefore, a larger power density on device level, compared to the depicted mHEMT technologies. Hence, the highest output power levels at H-band have been reported for InP HBT and InP HEMT based PA MMICs biased at 1.8–2.2 V [3, 37, 38, 59, 87, 122]. In [37], 17 – 24-dBm output power was reported between 180 – 265 GHz and at a narrow frequency band around 300 GHz, up to 13.5 dBm has been demonstrated in [59], both using a 250-nm InP HBT technology.

A comparison of the three most relevant MMIC technologies for 300-GHz operation is shown in Table 1.1. Important single-device characteristics such as cutoff frequencies, breakdown voltage, and maximum available/stable gain are key indicators for the capability of a semiconductor technology in terms of achievable power gain at a certain frequency on device level. The implementation of chip-size optimized multi-functional MMICs and amplifiers as well as the performance on circuit level, in addition, strongly depend on the wiring possibilities for matching and bias-insertion network design. Hence, the available layer stack including metals and dielectrics for signal routing is another key feature of semiconductor technologies. The most common types of on-chip transmission lines at frequencies above 100 GHz are the coplanar waveguide (CPW) and the thin-film microstrip line (TFMSL). While CPW transmission lines are primarily implemented in two-metal-layer HEMT technologies, the TFMSL environment requires additional dielectric layers on the wafer front side and has been widely used in InP HBT technologies.

Key figures such as the feasible impedance range and attenuation of the transmission lines, however, depend on the exact layer sequence and thickness of the underlying technologies.

While the active-device characteristics as well as wiring possibilities are fundamentally limiting the achievable PA performance for a given technology—the choice of topology and active-device configuration, additionally, significantly impacts the achievable output power on circuit level. The device configuration, in this sense, means the arrangement of active devices in common-source (CS), common-gate (CG), cascode, or stacked configuration, for example—and the circuit topology describes which and how many devices are cascaded or parallelized in a series or parallel power combining concept, respectively. To give more detailed information on the circuit topologies of the 300-GHz PAs of Fig. 1.1, the implemented device configurations are evaluated in the following section.

1.1.1 State of the Art of 300-GHz Power Amplifier Concepts

To put the concepts and measured output-power performance of the state of the art of power amplifiers operating around 300 GHz in the WR03-band into context, a detailed summary is provided in Tab. 1.2. The measured saturated output-power level of the listed amplifiers was already introduced in Fig. 1.1. In addition, Tab. 1.2 gives more details on the implemented circuit topologies as well as key characteristics, such as the implemented transistor periphery in the output stage (total gate width, TGW), chip dimensions, and supply voltages.

Two figure of merits (FOMs) are used to evaluate the output-power performance on circuit level. The first is the measured output power normalized to the implemented device periphery (P_{out}/TGW)—which fundamentally depends on the power density of the underlying technology, as well as the efficiency of the employed combiner topology. This FOM, therefore, can be used to directly compare the performance of amplifiers which are implemented in the same technology and to further asses the employed topology in terms of feasible output power on device level as well as power-combining efficiency. The second FOM is used to evaluate the compactness of the implemented PA cores, by normalizing the measured output power to the used chip width (P_{out}/W). This FOM indicates the efficiency of the implemented PA topologies in terms of how much chip area is required to achieve a certain output power performance. This is especially relevant when considering further parallelization, as well as chip and system integration.

In general, the output-power density (P_{out}/TGW) of vertical HBT and lateral HEMT devices cannot directly be compared, due to their fundamental differences in the respective transistor functionality. However, the results reported for the upper mm-wave frequency range show, that the InP HBT power amplifier circuits benefit from a higher power density on device level—which is, on the other hand, demonstrated over significantly smaller bandwidths around 300 GHz, in comparison to InGaAs-channel HEMT circuits, as can be seen in Tab. 1.2.

All of the listed InP HBT topologies are implemented with the transistor of the last stage being in common-base (CB) configuration. This is due to the fact, that the analysis of 250-nm InP HBT devices in CB and common-emitter (CE) configuration has showed that—when considering the gain performance in large-signal operation—the gain and

Table 1.2: Comparison of PA results and topologies around 300 GHz in the WR03 band.

Frequency♣ (GHz)	**Technology**	**Topology**	**Chip width**♠ (mm)	**TGW** (µm)	$\mathbf{V_{DC}}$★ (V)	$\mathbf{P_{out,sat}}$ (dBm)	$\mathbf{P_{out}/TGW}$‡ (mW/mm)	$\mathbf{P_{out}/W_{chip}}$* (mW/mm)	**Ref**
180–260	250-nm InP HBT	3-stage, cascode, 16-way combined	1.1	384	2.7	20–24	645	225	[37]
290–307.5	250-nm InP HBT	3-stage, cascode, 2-way combined	0.25	32	1.95	7.8–10	312	40	[38]
300–305	250-nm InP HBT	4-stage, common-base, 4-way combined	0.4	40	1.8	9.5–9.8	238	24	[122]
301	250-nm InP HBT	4-stage, cascode, 2-way combined	0.5	96	2.2	13.5	233	45	[59]
326–340	130-nm InP HBT	2-stage, double-stack, 4-way combined	0.7	80	1.8	8.6–12.6	227	25	[3]
338	sub-35-nm InP HEMT	4-stage, common-source, 2-way combined	0.3	160	2.2	11†	79	42	[87]
275–320	35-nm InGaAs mHEMT	3-stage, cascode, 2-way combined	0.4	72	0.9	5–7†	69	13	[106]
270–310	35-nm InGaAs mHEMT	1-stage, triple-stack	0.23	40	3.4	4–6	100	17.3	[5]
270–317	35-nm InGaAs mHEMT	1-stage, triple-stack, 2-way combined	0.5	80	3.0	3–6	50	8	[4]
275–312	35-nm InGaAs mHEMT	5-stage, common-source, 4-way combined	0.48	128	1.2	5–8	49	13	[97]

♣: The frequency range corresponds to the reported large-signal bandwidth.
♠: Required chip width of the PA core including matching networks and the first stage of shunt capacitors in the bias insertion network, without RF/dc-pads.
★: Applied drain-source voltage (V_{DS}) and collector-emitter voltage (V_{CE}) of single HEMT and HBT devices.
‡: Total gate width, device periphery in the output stage.
†: Only packaged results are reported. The depicted results include the reported values minus the specified transition loss.
*: Chip width of the PA core♠.

power density of CE devices significantly decreases above 200 GHz, as reported in [118]. This consequently reduces the usefulness of the CE device configuration for PA circuits at the upper mm-wave frequency band. Therefore, state-of-the-art InP HBT PA circuits below 200 GHz typically use a CE power-amplifier cell [37]. For higher frequencies up to 300 GHz, a cascode topology is mostly implemented in InP HBT PA circuits, using the advantageous large-signal performance of the CB devices [37, 38].

The wiring type of the listed InP HBT PAs is TFMSL—which is used to parallelize up to 16 cascode PA cells in [37]—achieving state-of-the art 13.5-dBm output power around 300 GHz [59]. Looking at the output power per device periphery (P_{out}/TGW) and per required chip width (P_{out}/W), however, the 300-GHz results reported in [38, 59, 122] are significantly inferior to the ones reported up to 260 GHz [37], which have been realized in the same 250-nm InP HBT technology. Thus—considering the higher supply voltage and larger implemented finger width used in [37]—the 300-GHz PAs evidently still provide room for significant improvement in terms of output-power level per required chip width.

When comparing the InP-HBT PA topologies depicted in Tab. 1.2, only [3] claims the implementation of a series-connected topology with a 4-way combined double stack configuration (transistor stacking is discussed in detail in Section 2.2.2). While output-power levels above 10 mW are achieved over a small bandwidth with this topology, the implemented device periphery is significantly larger than the ones reported with the cascode topology in [38]. Therefore, when considering the 227-mW/mm power density per device periphery—which is the lowest of the listed InP HBT results around 300 GHz—it has to be concluded, that the claimed double-stack implementation is not substantiated by the reported measurement results in [3]. Keeping in mind the different combiner losses and

supply voltages listed in Tab. 1.2, the results reported in [3] rather demonstrate a performance level which is comparable to the classical cascode topology—showing no improved output-power performance by implementing the stacked topology around 300 GHz.

In InGaAs-channel HEMT technologies, on the other hand, the cascode configuration has very often been implemented in LNA and PA circuits up to THz frequencies above 400 GHz—due to its large levels of small-signal gain which can be provided in comparison to CS transistors. Yet, in the 300-GHz state of the art shown in Tab. 1.2, only one mHEMT cascode PA topology has been reported with [106]. In contrast, [5] and [4] report on 300-GHz PA circuits based on a triple-stack PA cell and mere CS HEMT amplifiers are described in [97] and [87].

All of the depicted 300-GHz HEMT PAs are implemented in CPW-wiring environment, which typically leads to a larger required chip area for matching network implementation in comparison to compact TFMSL circuits. When comparing the output power per required chip width of the InP HBT as well as InGaAs mHEMT results depicted in Tab. 1.2, the mHEMT results are significantly below 20 mW/mm, in contrast to up to 45 mW/mm for InP-based 300-GHz circuits. This is in large part due to the lower operating voltage—resulting in a lower power density on device level for the mHEMT devices—and in part caused by the CPW-wiring environment, which limits the implementation of compact 300-GHz PA cells.

When considering the results of the triple-stack mHEMT PA circuits reported in [4] in comparison to the cascode performance demonstrated by [106]—as for the stacked-HBT topology in [3]—no improvement in terms of output power per device periphery is shown for the stacked-HEMT topologies. Both the triple-stack circuit in [4] as well as the cascode design in [106] report on a two-way combined PA topology with tandem-X couplers at the same frequency and in the same technology. Therefore—keeping in mind possible power-density variations on device level, since the MMICs were not measured on the same wafer—a direct comparison of the parallelized stacked PA cell in [4] as well as the cascode PA cell in [106] is reasonable. Comparing the measured results, the triple-stack topology achieves significantly lower output-power levels, despite an even larger implemented total gate width (TGW) and higher supply voltage per device than the cascode circuit. Even when considering the slightly higher compression level of the cascode measurement data, no output-power improvements and, therefore, no successful transistor stacking at 300 GHz can be concluded from the data reported in [4][1].

In general, it can be concluded from the results listed in Tab. 1.2, that no superior device configuration in terms of significantly improved large-signal performance can be derived from the small number of different 300-GHz circuits, which were realized in the same InGaAs mHEMT technology. Within the same technology, single-device PA cells (CS for example) as well as cascode and stacked PA cells have demonstrated no clear advantage in terms of output-power performance on circuit level—neither per device periphery nor per required chip width.

[1] The triple stack reported in [5] is excluded in this discussion, due to the large ripple shown in the frequency-sweep measurements in [5], which indicates a large measurement uncertainty. However, since the same triple-stack PA cell was implemented in [4] with significantly inferior large-signal performance, only [4] is used to evaluate the triple-stack performance.

1.2 Goals and Outline of this Work

This work examines the development of broadband solid-state power amplifiers (SSPAs) in Fraunhofer IAF's InGaAs mHEMT technology, covering the frequency band around 300 GHz. Wireless communication and imaging systems based on this HEMT technology have set the state of the art around 300 GHz. By using high-gain and low-noise monolithic front-end chip sets with an excellent bandwidth in the range of 50 GHz, real-time capable 300-GHz P2P links with data rates in excess of 100 Gbit/s and imaging solutions with sub-4-mm resolution have been demonstrated [15, 57, 80]. The available output power, however, has been limited to power levels below 3 mW (5 dBm), using the packaged 300-GHz PA MMIC reported in [106]. To overcome this limitation and increase the operating range of wireless 300-GHz systems, the realization of the first HEMT based 300-GHz power amplifiers with output-power levels larger than 10 mW (10 dBm) is described in this thesis. These power amplifiers are required as key components for the development of next-generation high-performance THz P2P links and the exploration of novel applications for highly-broadband sensing systems at the lower THz frequency band.

The goal is the in-depth investigation of device configurations and topologies for the implementation of amplifiers with high output power. While large bandwidths in the range of 50 GHz are targeted, one of the key design goals is the miniaturization of amplifier circuits and the realization of highly-compact PA cells on the smallest chip size possible. Since power amplifiers typically require a large amount of chip area in comparison to other circuit components, a compact implementation is essential to enable the monolithic integration of multifunctional transmit-receive solutions on a single MMIC. Hence, the in-depth investigation of innovative chip-size-optimized PA cells at the lower THz frequency range around 300-GHz is described in detail in this work. By achieving highly-compact circuit dimensions, the integration as reusable IP blocks in next-generation multi-channel MMICs and THz front ends with high-bandwidth and outstanding dynamic range is made possible. In addition, by reducing the required die area for single-chip front ends, the costs and efforts for processing, handling, as well as packaging of the MMICs can be notably reduced.

The circuit dimensions are, furthermore, of utmost importance when considering the assembly into waveguide modules. A key challenge in the successful packaging of stand-alone amplifier circuits is the suppression of cavity resonances when surrounding the MMIC with a closed cavity and a conductive surface material—as it is typically done in split-block waveguide packaging technologies. The theory tells us that cavity modes can exist and be excited for a width of the cavity that exceeds one half of a free space wavelength [26]. At 300 GHz, this corresponds to a width of 500 µm. Increasing the width of the chip beyond this limit possibly increases the complexity and costs for MMIC packaging if additional measures for cavity-mode suppression are needed. Thus, to ensure the successful packaging of the PA MMICs developed in this work, a maximum chip width of 500 µm was targeted. On this limited chip area, however, DC pads as well as bias-distribution networks also need to be integrated. This requirement limits the width of the PA-core circuit to less than 400-µm. The PA circuits described in the following chapters, therefore, have been designed for a reduced chip width while maximizing the total number of gate fingers in the output stage, and hence, maximizing the achievable output power

at the required width of the integrated circuit. This figure of merit (P_{out}/chip width) was introduced in the previous section and is sought to be maximized, as this FOM indicates the efficiency of the implemented PA topology in terms of how much area is required on the wafer to achieve a certain output-power performance.

With recent developments of the back-end-of-line (BEOL) process of Fraunhofer IAF's InGaAs mHEMT technology—which includes the addition of a third metal layer as well as several additional dielectric layers in the former two-metal-layer BEOL—the implementation of TFMSL wiring has been made possible. Therefore, thin-film wiring and the associated possibilities for the design of innovative chip-size-optimized TFMSL matching and power-combining networks are investigated in depth at the frequency range around 300 GHz in this thesis.

The results which are achieved on circuit level in this work are based on the comprehensive analysis of single transistors and device configurations, their implementation and modeling in chip-size-reduced PA cells, as well as the investigation of novel low-loss thin-film wiring possibilities for compact amplifier and combiner circuits. Fig. 1.2 shows an overview and the graphical structure of this thesis. The approach to improve the 300-GHz PA performance of the underlying InGaAs mHEMT technology on MMIC and module level can be divided into three parts. Each part deals with extensive design-related investigations as well as numerous improvements regarding three different system levels of the PA development: the device level, the MMIC level, and the module level.

The first part—described in Chapter 3—includes detailed investigations on the transistor level, which are related to device-level performance as well as multi-finger-transistor implementation and modeling. In order to increase the breakdown voltage and, furthermore, improve the power density on device level, the length of the drain-gate recess is investigated and optimized experimentally. To maximize the total gate-width, novel multi-finger CS and cascode device layouts are developed, enabled by thin-film feeding structures which permit an accurate in-phase matching and feeding of multiple two-finger devices in parallel. The on-chip large-signal characterization of single devices—which are used for load-target definition and large-signal-model verification—is investigated for the first time at frequencies above 200 GHz, using unique in-situ load-pull MMICs with tunable output-matching networks at 300 GHz.

The PA-circuit design on MMIC level describes the second cornerstone of this thesis, which is covered in Chapter 4. Based on the multi-finger cascode and CS devices with up to eight transistor fingers described in Chapter 3, a highly-compact unit-amplifier (UA) topology is developed with the focus on maximizing the total gate width in the output stage and, hence, increasing the achievable output power on the smallest chip width possible. As the discussion of previously implemented PA circuits in the underlying mHEMT technology in Section 1.1.1 shows, no clearly superior topology can be derived from the prior-realized 300-GHz PAs. Thus, possible device configurations for a suitable 300-GHz PA implementation are evaluated thoroughly and design considerations for achieving an improved 300-GHz output power performance over a wide bandwidth with high linearity is described in detail. To implement several UA cells in parallel, novel TFMSL on-chip power combiners are investigated—including elevated CPW and air-bridge TFMSL environments. This permits the efficient parallelization of several UA cells in the BEOL of this mHEMT technology, by using thin-film wiring. Based on the UA cell and the power

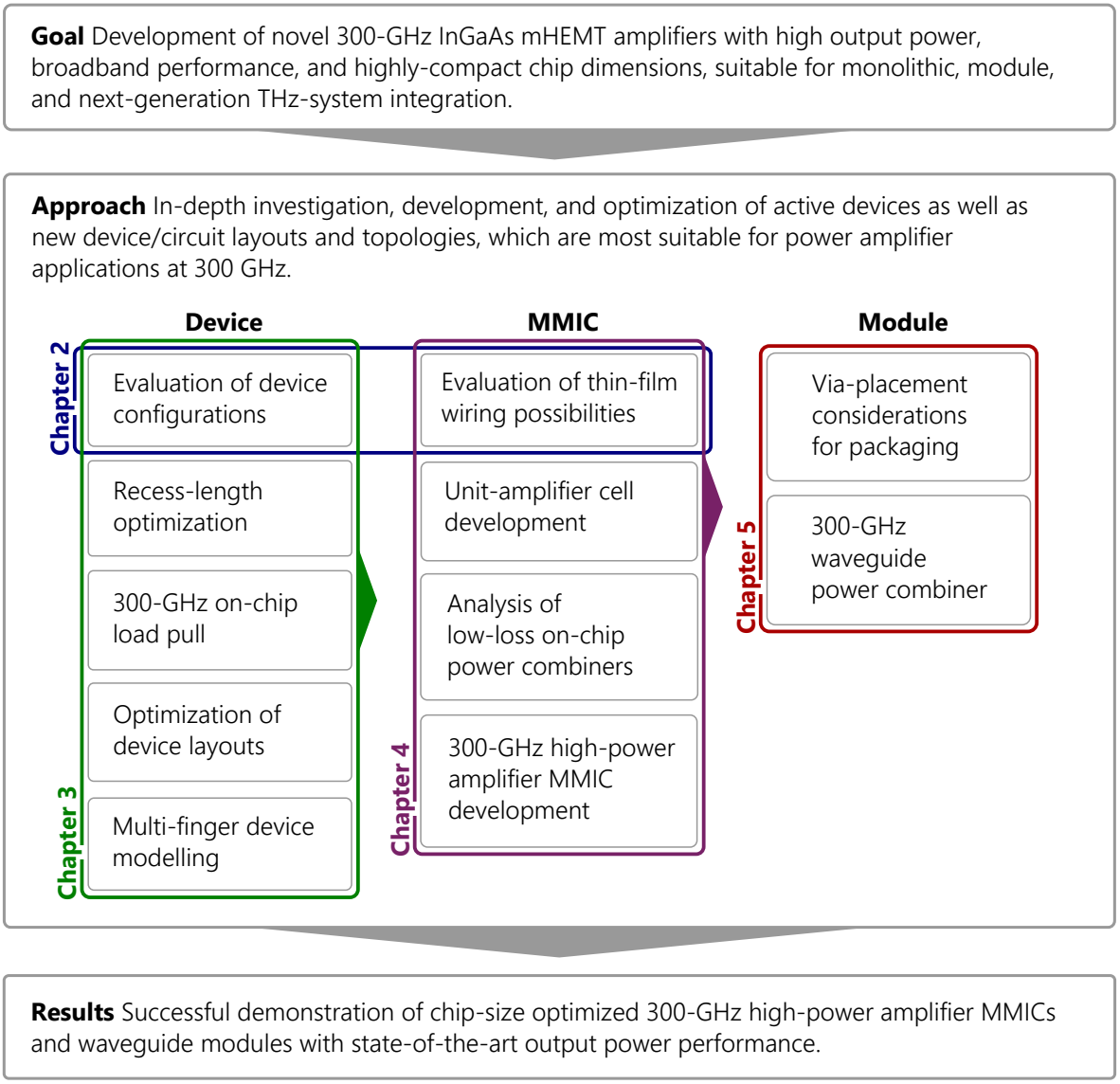


Figure 1.2: Graphical structure of this thesis. Depicted are the goals, approaches, and results. The design approach is categorized in investigations regarding the device level, MMIC level, as well as module level. The Chapters 3 to 5 are structured accordingly. Device configurations and thin-film transmission lines are first introduced in Chapter 2 as key building blocks for the subsequent device and circuit design. A detailed summary and assessment of the key achievements, results, and findings is provided in Chapter 6.

combiners, high-power amplifier MMICs with state-of-the-art output power performance are demonstrated.

The third main topic covered in this thesis is dedicated to the module integration and packaging of 300-GHz PA circuits, which is described in Chapter 5. While through-substrate vias are not needed for TFMSL matching networks to be functional, through-wafer connections are, nonetheless, required for most MMIC-to-waveguide transitions and the suppression of in-package resonances when considering MMIC packaging. Yet, the necessity of vias within the active circuit area of compact TFMSL MMICs strongly depends on the amplifier topology and device layout used. In order to avoid substrate resonances after packaging, the requirements for via placement were investigated and are

described in detail, including design rules for their implementation in TFMSL circuits. To increase the output-power performance on the module level, a low-loss 3-dB waveguide coupler is developed for efficient MMIC parallelization on waveguide level. The measured performance of the packaged PA MMICs is described and discussed in detail in the second part of Chapter 5.

As a basis for the development of multi-finger devices in different device configurations in Chapter 3 and, furthermore, the design of compact PA MMICs discussed in Chapter 4, the IAF-mHEMT MMIC technology is first introduced in Chapter 2. This includes the evaluation of thin-film wiring possibilities in the available BEOL variants—which is required for the feeding of the multi-finger devices, as well as for the design of the compact matching and power combining networks described in this work. In addition, the general PA concepts of parallel-connected as well as series-connected topologies are introduced in Chapter 2 and the corresponding limitations are discussed—this includes, for example, the limitations of stacked-FET topologies at 300-GHz, which are evident from the state-of-the-art evaluation in the previous Section 1.1.1.

A detailed discussion and conclusions of the above-mentioned investigations on device, MMIC, and module level is covered in Chapter 6—which provides a summary of key results, findings, and achievements, which are described in the following chapters.

2 Analysis of Device Configurations and Thin-Film Transmission Lines

A general block diagram of a typical RF power amplifier topology is shown in Fig. 2.1, consisting of multiple active devices in parallel as well as matching networks for impedance transformation and power splitting/combining. Within a given technology, the implemented topology and choice of active-device configuration can significantly impact key figures such as the achievable bandwidth, gain, output power, and circuit dimensions, for example. Furthermore, a certain topology which shows great potential at the lower mm-wave frequency range, possibly provides no significant benefit at the THz-frequency band around 300 GHz. Hence, the choice of a proper topology is a crucial part of the power amplifier design—including the choice of the active-device configuration as well as the selection of the wiring type for the implementation of the passive impedance transformation networks depicted in Fig. 2.1.

The theoretical analysis of RF power amplifier concepts as well as modeling and design procedures to achieve good linearity, high efficiency, or high bandwidth, for example, are well covered in the literature [12, 21, 35, 92]. This chapter's aim is to introduce the underlying InGaAs-channel mHEMT technology and to provide an analysis of the abovementioned two key building blocks for the realization of highly-compact 300-GHz PA circuits: the transistor configuration of the active devices as well as the monolithic transmission lines for the implementation of compact matching networks and low-loss power combiners. The results of these evaluations will be required for the discussion of the modeling and design approach of multi-finger devices and chip-size-optimized PA MMICs described in the following chapters.

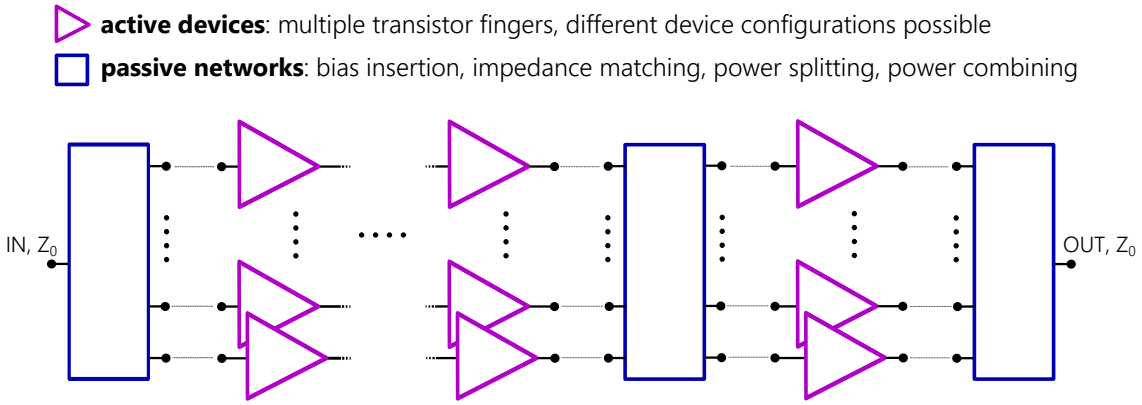


Figure 2.1: General block diagram of an RF power amplifier, consisting of parallel active devices and matching networks. The active device configurations and wiring possibilities for sub-mm-wave PA circuits are discussed in detail in this chapter.

The MMIC fabrication including transistors, capacitors, resistors, and multiple metal layers for interconnections is, in general, divided into two parts. The front-end-of-line (FEOL) part consists of the processing of the active devices, including the epitaxial growth of the heterostructure, mesa etching, and gate processing. The processing of metal and dielectric layers which are used for matching and bias-insertion network design, on the other hand, is generally included in the BEOL part of the fabrication. III-V HEMT and HBT technologies on GaAs and InP substrates, furthermore, typically feature a backside process including wafer thinning and through-substrate-via processing, which is required for packaging and most MMIC-to-waveguide transitions.

In the following section (Section 2.1), the FEOL of the InGaAs-channel mHEMT technology is introduced, including key device figures which are relevant for the achievable PA performance at the lower THz band. In Section 2.2, the basic concepts and limitations of parallel-connected and series-connected devices for 300-GHz power amplifiers are introduced, taking into account the relevant characteristics of the used HEMT technology. The available BEOL variants, along with thin-film transmission lines, are then discussed in detail in Section 2.3.

2.1 Metamorphic High-Electron-Mobility Transistor Technology

Fraunhofer IAF's 35-nm gate-length mHEMT devices are based on an InGaAs/InAlAs double heterostructure with high In-content in the InGaAs channel [65, 64, 66]. Fig. 2.2 shows the simplified cross section of the HEMT devices, which are processed on 100-mm semi-insulating GaAs wafers by molecular beam epitaxy (MBE). To adapt the lattice constant of the GaAs substrate, a ternary grown metamorphic buffer is used, with a linear $In_xAl_{0.48}Ga_{0.52-x}As$ ($x = 0 \rightarrow 0.52$) transition. The electrons are confined in a single $In_{0.8}Ga_{0.2}As$ layer, using $In_{0.52}Al_{0.48}As$ barriers with double-sided δ-doping. The heterostructure is capped with a highly doped $In_{0.53}Ga_{0.47}As$-cap layer for reduced ohmic contact and low source resistance. The corresponding band diagram of this layer sequence is shown in Fig. 2.2 on the right.

Typical device characteristics of a single HEMT are listed in Fig. 2.3 on the right. The mHEMT devices have been developed for MMIC applications up to 800 GHz, featur-

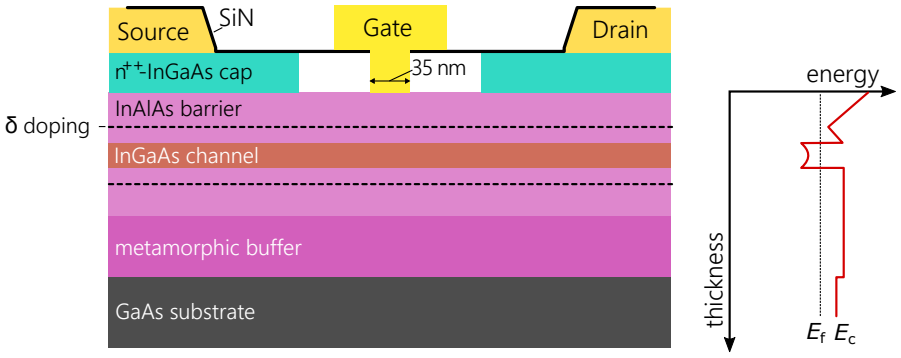
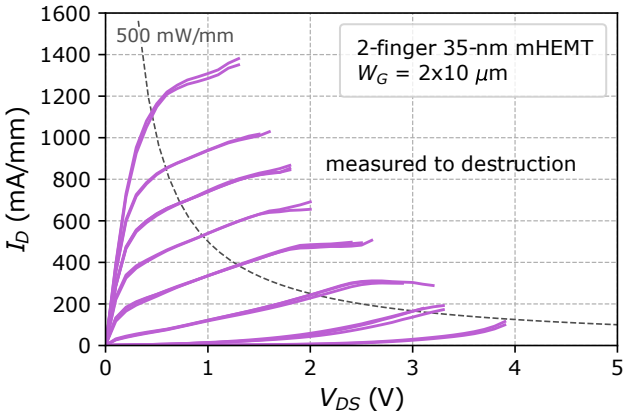


Figure 2.2: Simplified cross section of Fraunhofer IAF's 35-nm gate-length mHEMT and an illustration of the corresponding conduction band edge diagram.



Single device characteristics	
R_{on}	250 Ω·µm
$I_{D,max}$	1300 mA/mm
V_{th}	−0.3 V
BV_{DSO}	> 3.5 V
$g_{m,max}$	2500 mS/mm
f_T	> 500 GHz
f_{max}	> 1000 GHz
$P_{density}$*	150 mW/mm

*: Power density at V_{DS} = 1 V, 400 mA/mm,

Figure 2.3: Output characteristics (left) and typical characteristics (right) of a 35-nm InGaAs-channel mHEMT 2-finger device with 2x10-µm gate width (W_G).

ing a transition frequency f_T and power-gain cutoff frequency f_{max} above 500 GHz and 1000 GHz, respectively. For power-amplifier development, the current and voltage limits are of particular interest. Therefore, the output characteristics of devices which have been measured to destruction by sweeping the drain-source voltage at a constant gate voltage, are depicted on the left in Fig. 2.3. At a knee voltage of 0.6 V, the saturation current $I_{D,max}$ is typically in the range of 1200 to 1300 mA/mm and the off-state drain-source breakdown voltage BV_{DSO} is above 3.5 V. Hence, at a typical bias condition of 1 V and 400 mA/mm for PA applications, the power density on device level is around 120 to 150 mW/mm in load-pull measurements at the lower mm-wave frequency band. Device configurations and PA concepts to increase the output power on MMIC level, are discussed in the following section.

2.2 Concepts and Device Configurations for sub-mm-Wave Power Amplifiers

In general, the maximum output power—which is achievable with a single transistor—is fundamentally limited by the current and voltage limitations of the underlying device technology. In order to increase the output power for a given technology, single devices are connected in series and/or in parallel to increase the output power level by voltage and/or current combining.

2.2.1 Parallel-Connected Power Amplifier Concepts

The most straightforward method to increase the output power in PA circuits on device level is to increase the current swing by maximizing the total gate width. This is done by means of maximizing the single-finger width as well as the number of transistor fingers per device, as depicted in Fig.2.4(a).

Increasing the finger width, however, impacts the achievable gain, bandwidth, and the maximum frequency of operation. This is due to the fact that parasitic device capacitances as well as ohmic losses of the transistor fingers scale with the finger width,

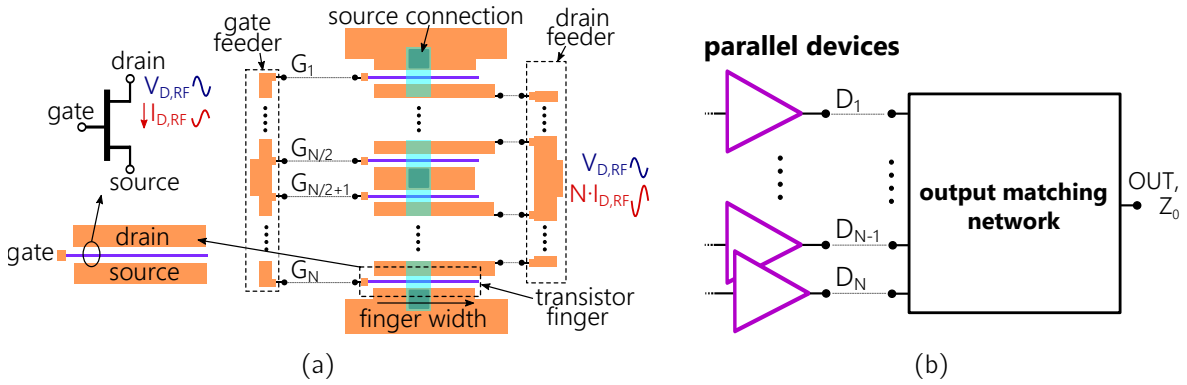


Figure 2.4: Simplified (a) N-finger common-source device and (b) schematic view of the parallel-connected amplifier topology, which is used to increase the output-power performance by combing the current of multiple parallelized devices or circuits.

limiting the extrinsic cutoff frequencies and achievable gain. Furthermore, additional losses and phase imbalances, introduced by the feeding structures of multi-finger devices, can impact the single-device performance in a similar way—limiting the achievable gain, bandwidth and output power on the device level. Especially at sub-mm-wave frequencies, and due to the increasing electrical length of multi-finger feeding structures, this impact cannot be neglected and is evaluated in detail in Section 3.2.1.

To further increase the total gate width in PA circuits and, hence, increase the output power, several multi-finger devices or prematched multi-transistor power cells are parallelized, as illustrated in Fig. 2.1. This N-way parallelization is realized using output-matching and power-combining circuits to match the system impedance Z_0 to the output of the parallelized devices, as shown in Fig. 2.4(b). Assuming ideal and lossless power combining—which is far from being attainable in practice at sub-mm wave frequencies—the output power scales with the number N of parallel devices according to

$$P_{\mathrm{OUT,N}} = N \cdot I_{\mathrm{DS,RF}} \cdot V_{\mathrm{D,RF}}, \tag{2.1}$$

with $V_{\mathrm{DS,RF}}$ and $I_{\mathrm{D,RF}}$ being the RF drain-source voltage and RF drain current, respectively, of the single devices.

By increasing the total gate width and adding up the current on device level, the impedance level—and therefore the optimum load impedance—decreases in accordance to the increasing gate width. Since the ideal load-line resistance decreases by the same number the device capacitances are increasing, the theoretically achievable matching bandwidth is not affected by the increasing impedance-transformation ratio. This is due to the fact, that only the product $R \cdot C$ of the capacitance C and the resistance R of an RC-parallel element is relevant for the achievable matching limit [10, 30]. The achievable insertion loss as well as feasible power combining efficiency, on the other hand, is limited by the larger impedance-transformation ratios which need to be covered by the matching networks [13, 85]. Hence, high-order impedance-transformation networks are required to achieve broadband matching—decreasing the combining efficiency at sub-mm-wave frequencies due to high transmission-line losses—and the chip dimensions of power amplifier circuits tend to get large in comparison to other circuit components. This, however, imposes a major challenge for the assembly of the PA circuit as well

on-chip integration into complex front-end MMICs. Since compact chip dimensions are a key parameter of the developed PA cells in this work, the implementation of chip-size-optimized multi-finger devices is described in Chapter 3.

2.2.2 Series-Connected Power Amplifier Concepts

In contrast to the parallel-connected current-combing PA topology, the stacking of multiple transistors in a series-connected device configuration potentially provides benefits in terms of gain, reduced chip size as well as higher output-impedance levels [101]. The simplified schematic of the stacked-FET topology with N in series-connected devices is shown in Fig. 2.5. The depicted voltage and current swings indicate the general behavior in the stacked-FET configuration—yet both phase and amplitude are not to scale.

The input signal is applied to the lowest device in common-source configuration, acting as a current source for the N-1 stacked devices in common-gate configuration. By adding up the drain-source voltages of the N in series connected FETs, the output-voltage swing—and, hence, the output power—is increased. In order to realize an increased voltage swing, the voltages need to be added and swing in phase. To achieve this, the depicted voltage swing at the gates of the common-gate devices needs to be implemented. This can be achieved by careful selection of the passive gate impedances $Z_{G,2}$ to $Z_{G,N}$, as well as possible impedance transformation networks in-between the stacked devices, which are not depicted in Fig. 2.5.

As mentioned above, a significant benefit of the increased output-voltage swing is the higher output and load impedance, reducing the effort for impedance matching and permitting more efficient broadband output matching. Furthermore, by stacking the devices in series, the chip width is only increased by the layout dimensions of the required impedance matching networks at the gates of the CG devices. Hence, by combining multiple devices in a series-connected topology, compact and chip-size-efficient power gain becomes feasible.

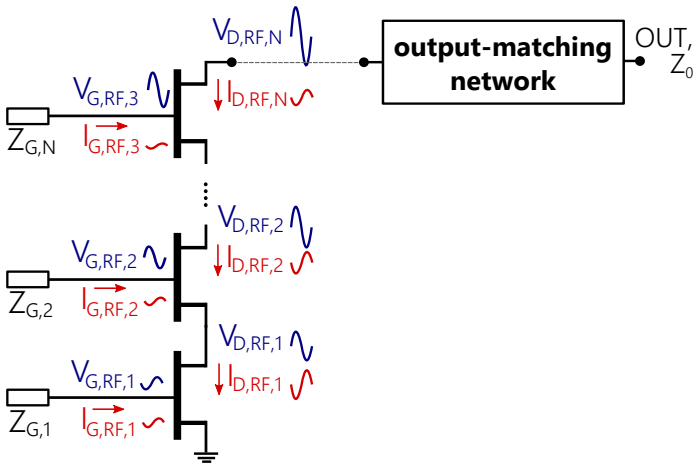


Figure 2.5: Simplified schematic of N in-series connected transistors, a topology which is used to increase the output-power performance by voltage combining. The depicted voltage and current swings indicate the general behavior—both phase and amplitude are not to scale.

Yet, the maximum number of devices which can be stacked to increase the output-power level is limited—as described with the prospects and limitations of stacked-FET approaches in [114, 115]. Since the current gain of the CG devices is smaller than unity and the RF gate current of each stage is contributing to the respective source current, the output current swing of an N-stacked FET is reduced with each additional CG device:

$$I_{\mathrm{D,RF,N}} < I_{\mathrm{D,RF,N-1}}. \tag{2.2}$$

Furthermore, with the dependency of the current gain on the transit frequency f_{T} as well as the frequency of operation f_{op}, the maximum achievable output power with N stacked devices is given in [115] by

$$P_{\mathrm{OUT,N}} = N \cdot V_{\mathrm{DS,RF,1}} \cdot I_{\mathrm{D,RF,1}} \left(\frac{f_{\mathrm{T}}}{f_{\mathrm{op}} + f_{\mathrm{T}}} \right)^{N-1}. \tag{2.3}$$

Due to the linear voltage-related growth and the exponential current-related decrease of the output power, in dependency on N, an optimum number of N_{max} stacked devices for maximum output-power performance exists and can be calculated from (2.3). This maximum number of stacked devices is given by

$$N_{\mathrm{max}} = \left(In \left(1 + \frac{f_{\mathrm{op}}}{f_{\mathrm{T}}} \right) \right)^{-1}. \tag{2.4}$$

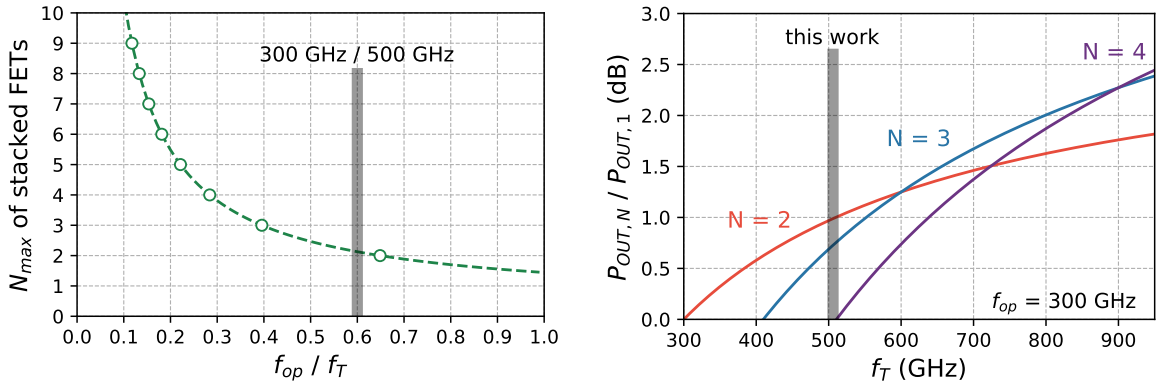
The optimum number of stacked devices is, therefore, dependent on the ratio of the frequency of operation f_{op} to the current-gain cutoff frequency f_{T} of the corresponding semiconductor technology. This dependency of N_{max} versus f_{op} normalized to f_{T}, is depicted in Fig. 2.6(a).

Due to the described current limitation, the stacking of multiple devices is only beneficial at frequencies well below the current-gain cutoff frequency. To stack at least two devices for slightly improved large-signal performance in a cascode configuration, e.g., the frequency of operation needs to be below approximately three-fourths of the underlying technology's f_{T}. For the operation of two stacked transistors around 300 GHz, this would require an f_{T} larger than 400 GHz. With the f_{T} of 500 GHz, this requirement is satisfied for the 35-nm mHEMT technology used in this work.

The additional output power gained from device stacking can be calculated from (2.3). The N-stack output power, normalized by the achievable output power of a common-source device $P_{\mathrm{OUT,1}}$, is then given by

$$\frac{P_{\mathrm{OUT,N}}}{P_{\mathrm{OUT,1}}} = N \left(\frac{f_{\mathrm{T}}}{f_{\mathrm{op}} + f_{\mathrm{T}}} \right)^{N-1}. \tag{2.5}$$

This theoretically-achievable additional output power is plotted for the frequency of operation of 300 GHz in Fig. 2.6(b). Depicted is the output-power improvement for two, three, and four stacked devices in dB, which is plotted versus the required current cutoff frequency f_{T}. This plot shows, however, that in order to gain at least 1-dB additional output power from two stacked devices at 300 GHz, f_{T} needs to be above 500 GHz. Furthermore, to significantly improve the performance with the implementation of a third stacked device, f_{T} should be larger than 800 GHz for 300-GHz operation.



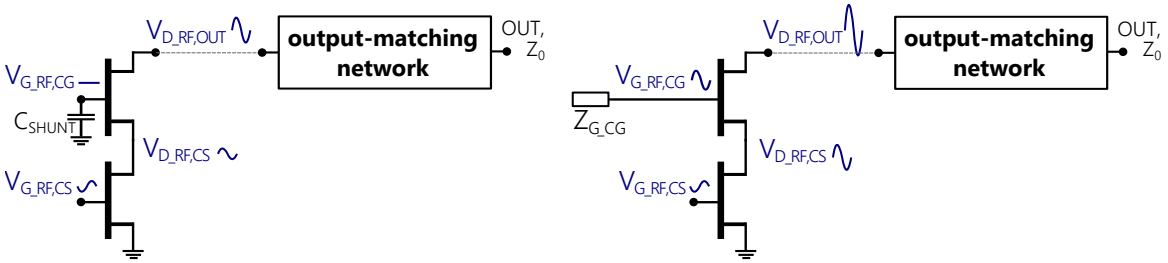
(a) (b)

Figure 2.6: (a) Limit of the optimum number N of stacked devices for maximum achievable output power versus the frequency of operation f_{op} normalized to the transit frequency f_T [115] and (b) output-power improvement for N-stacked devices operating at 300 GHz, dependent on the current-gain cutoff frequency f_T (2.5).

Up to date, only a small number of sub-35-nm InGaAs-channel HEMT technologies have reported f_T values above 600 GHz [58, 63], with the highest current-gain cutoff frequency being reported for a 20-nm InGaAs mHEMT technology with $f_T = 660$ GHz [63]. This, however, is only achieved by progressive device scaling, which leads to a significant reduction of the breakdown voltage—reducing the power density on device level. Hence, the advantages of compact implementation and increased output-power performance of stacked-FET PA cells are very limited at sub-mm-wave frequencies. For the development of 300-GHz PA MMICs in the underlying mHEMT technology, this implies that the optimum number of stacked devices is limited to a maximum of two. With a third stacked device, the output-power performance at 300-GHz is, in theory, even decreasing in this mHEMT technology. This explains the limited performance of the triple-stack-PA results discussed in the state-of-the-art results of the previous chapter.

Cascodes in Classical and Double-Stack Configuration Since the optimum number of stacked devices for improved output-power performance is limited to two transistors in cascode configuration, the difference between the classical cascode and two stacked transistors is discussed here. This will be required for the cascode-design considerations evaluated in Section 3.3.

For the classical cascode configuration, two transistors are cascaded—a CS device followed by a CG transistor, as depicted in Fig. 2.7(a). The gate of the CG transistor is either directly connected to ground in the case of an AC-coupled cascode approach [38] or RF-shorted by implementing a large parallel capacitor C_{SHUNT}. As a result of this, the gate potential $V_{G\_RF,CG}$ is constant over time, as depicted in Fig. 2.7(a). The gate-source voltage swing at the CG device is, therefore, determined by the voltage swing $V_{D\_RF,CS}$ at the drain of the CS device. Hence, since the CS device is acting as current source for the CG device, the voltage gain of the CS device is approximately unity which in consequence reduces the Miller effect—and, therefore, the input capacitance—drastically. As a result of this, improved output-to-input isolation, broadband matching and superior maximum-



(a) "Classical" cascode (b) Double-stack cascode

Figure 2.7: Simplified schematics of the cascode configuration. (a) Shows the "classical" cascode with RF-short at the CG gate terminal. The double-stack cascode, which provides an increased output-voltage swing, is depicted in (b).

stable gain can be achieved—which are the well-known key characteristics of the classical small-signal cascode [89].

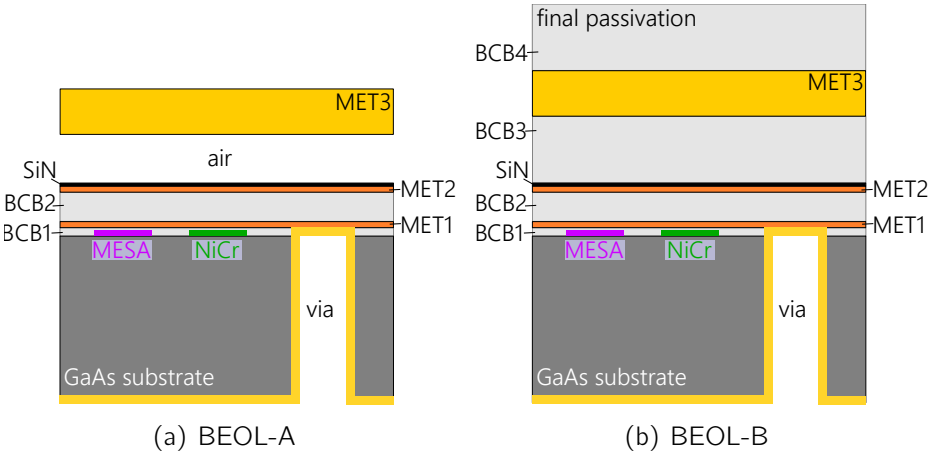
Yet, since the gate potential of the CG device is shorted for the RF signal, only the CG device contributes to the output-voltage swing. The RF-shorted gate-potential at the CG device, on the other hand, can lead to large voltage swings in saturation, causing soft compression and device degradation. Therefore, in order to safely increase the output-power level of the PA cell in cascode configuration, the drain-source voltage of both the CS and the CG device have to be stacked and swing in phase, as described above.

By introducing the voltage swings at the gate of the CG transistor as well as at the drain of the CS device, which are depicted in Fig. 2.7(b), the voltage gain of the CS input transistor is increased. This typically reduces the output-to-input isolation of the stacked cascode, which is consequently limiting the maximum-stable gain of this transistor configuration. Hence, trade-off design decisions between achievable gain, output power, stability, and higher impedance levels for broadband matching need to be made. The main design parameters in sub-mm-wave cascode design, therefore, include the implementation of the CG-gate matching network $Z_{G,CG}$ as well as a possible impedance-matching network between the cascaded devices, which is not depicted in Fig. 2.7. These considerations are used and required as a basis for the comparison of multi-finger devices in common-source and cascode configuration in Section 3.3.

2.3 Thin-Film Transmission Lines for Compact sub-mm-Wave Power Amplifiers

In the frame of this work, two different BEOL variants have been used for integrated-circuit (IC) design. The reason for this is, that—over this period of time—the three-metal-layer BEOL with top-metal layer in air-bridge technology was developed to a fully-passivated BEOL variant, including additional BCB layers. The cross-section and available layers of both front-side-process variants are shown in Fig. 2.8(a) and Fig. 2.8(b), respectively.

Both BEOL variants include 50-Ω/□ NiCr thin film resistors and an 80-nm-thick SiN layer used for on-wafer metal–insulator–metal (MIM) capacitors. Three metal layers (MET1-MET3) are available for the design of compact matching networks with thin-



(a) BEOL-A (b) BEOL-B

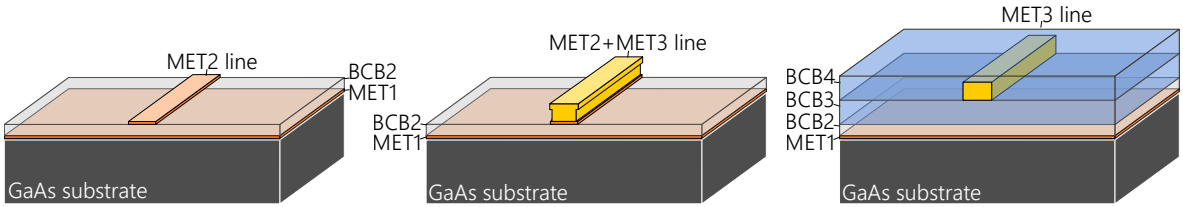
Figure 2.8: Simplified schematic cross-section (not to scale) of the three-metal-layer InGaAs mHEMT IC thin-film wiring environments on GaAs substrate. (a) Air-bridge technology and (b) BCB technology.

film-microstrip-line interconnects on the wafer front side. The electron beam evaporated Au-based first and second metal layers are defined in a lift-off process, while MET3 is a 2.7-µm-thick plated Au layer.

The air-bridge technology variant—which is shown in Fig. 2.8(a)—was originally developed from a two-metal-layer technology variant with top-metal layer in air-bridge technology. This air-bridge technology variant will hereafter be referenced as *BEOL-A* variant. The layer-stack depicted in Fig. 2.8(b)—hereafter referred to as *BEOL-B* variant—includes two additional BCB layers. BCB3 was introduced to enable the implementation of thin-film transmission lines with increased substrate height of the BCB dielectric, and the BCB4 layer is implemented as the final passivation layer.

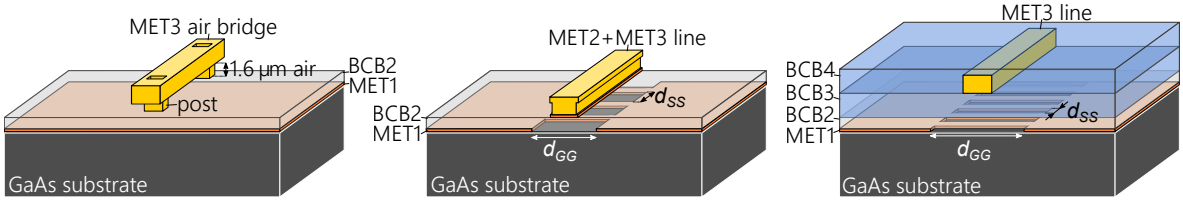
To suppress substrate modes, the wafers are thinned down to 50 µm, through-substrate vias are dry etched and the wafers are Au plated on the back side. Using the available front-side layers and back-side process, CPW as well as TFMSL interconnections can be implemented in this mHEMT technology. Since the underlying three-metal-layer BEOL was developed from a two-metal-layer technology variant with air-bridge top-metal layer, previously realized 300-GHz circuits and combiners in this technology have been mostly implemented in CPW-wiring environment—as discussed in Section 1.1.1. The relevance of a compact PA design regarding the feasibility of packaging into waveguide modules, on-chip integration, as well as efficient power combining, was also introduced in the previous chapter. In order to realize a compact PA core, independent of backside processing and the substrate height, therefore, compact multi-finger devices and 300-GHz PA cells have been developed and are discussed in Chapter 3 and Chapter 4, using TFMSL interconnections for the matching networks.

A general advantage of TFMSL wiring is the small required chip area for the implementation of matching and impedance transformation networks. This is typically due to their small width and bend dimensions in the range of a few micrometers, which enables a compact matching network implementation and the accurate in-phase matching of in-close-proximity parallelized devices—reducing the required chip width of parallelized components significantly, when compared to circuits in CPW-wiring environment. These



(a) MET2 TFMSL (b) MET2MET3 TFMSL (c) MET3 TFMSL

Figure 2.9: TFMSL interconnections which are typically used in Fraunhofer IAF's three-metal-layer BEOL processes including the top metal layer with and without air-bridge technology.



(a) Air-bridge TFMSL (b) Elevated MET2MET3 CPW (c) Elevated MET3 CPW

Figure 2.10: Thin-film (a) air-bridge as well as (b, c) elevated CPW transmission lines, which permit the implementation of low-loss high-impedance transmission lines with the design parameters d_{gg} and d_{ss} (d_{gg}: ground-to-ground spacing, d_{ss}: MET1-strip spacing).

advantages of using thin BCB layers for TFMSL wiring has been described for GaAs pHEMT [50] and InP HEMT [117, 36] technologies as well as this InGaAs mHEMT technology [56, 75, 74] for a wide range of compact circuit topologies.

Fig. 2.9 and Fig. 2.10 show the cross section of six different thin-film transmission lines, which have been used for the wiring in the matching and power combining networks described in this work. The TFMSL interconnections depicted in Fig. 2.9(a) (*MET2 TFMSL*, *MET2MET3 TFMSL* and *MET3 TFMSL*) can be clustered in the category of "traditional thin-film wiring", since these interconnections have been widely used for the design of compact MMICs in this InGaAs mHEMT technology for a wide variety of applications from 0 to 600 GHz [75, 51, 52]. Furthermore, the depicted layer sequences correspond with the classical microstrip line —including the conducting strip separated from the closed ground plane by a dielectric layer—which makes them very comparable to TFMSL interconnections in InP HBT technologies [118].

The main drawback of the traditional TFMSL interconnections in the underlying BEOL-A technology is the limited impedance range and high insertion loss, as discussed in the following sections. In order to decrease the insertion loss and realize thin-film transmission lines with high characteristic line impedances—which is necessary for the required impedance transformation in most 50-Ω power combining concepts—the three transmission lines shown in Fig. 2.10 were investigated to increase the combining efficiency of the power combiners in Section 4.3. As these thin-film transmission lines are a crucial building block for the implementation of the PA design—their dimensions, properties as well as limitations were analyzed in simulation using the 3D electromagnetic (EM) simulation tool CST Microwave Studio. Since the thin-film lines with structured ground plane cannot be evaluated by simply calculating the corresponding port modes in CST, the transmission line parameters—such as the effective line impedance Z_{line}

or the propagation constant γ—have been calculated from the simulated S-parameters according to [27] from

$$Z_{\text{line}}{}^2 = Z_0^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} \tag{2.6}$$

and

$$e^{-\gamma x_{\text{line}}} = \left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \sqrt{\frac{(1+S_{11}^2 - S_{21}^2)^2 - (2S_{11})^2}{(2S_{21})^2}} \right)^{-1} \tag{2.7}$$

with Z_0 being the reference impedance of 50 Ω and x_{line} the length of the transmission lines, respectively.

The equations (2.6) and (2.7), furthermore, permit the determination of the Telegrapher's equation [27] and parameters such as the quality factor of the transmission lines, for example. The quality factor Q of a transmission is defined as

$$Q = \frac{\beta}{2\alpha} \tag{2.8}$$

where α is the attenuation constant and β is the phase constant of the propagation constant γ [85]. This unit-less figure of merit is also used to evaluate the high-impedance transmission lines discussed in the following sections.

2.3.1 Traditional Thin-Film Wiring

The transmission lines shown in Fig.2.9(a) and Fig.2.9(b) have been typically used in the technology variant including the top-metal layer in air-bridge technology (*BEOL-A*). MET1 is implemented as substrate-shielding DC and RF ground and the TFMSL signal line is routed in MET2, using the 1.4-µm-thick BCB layer (BCB2) between MET1 and MET2 as dielectric substrate. MET3 can additionally be used to increase the conductor thickness of the signal line in order to reduce the losses and increase the current carrying capability, as depicted in Fig. 2.9(b) (*MET2MET3 TFMSL*). *MET2 TFMSL* and *MET2MET3 TFMSL* interconnections can also be used in the *BEOL-B* technology variant. The additional BCB layers, however, need to be considered in simulation.

Yet, realizing high-impedance as well as low-loss transmission lines is an issue for the TFMSL interconnections depicted in Fig.2.9(a) and Fig.2.9(b). Due to the low thickness of the BCB2 layer, the required width of a 50-Ω transmission line is only 3.5 µm for the *MET2 TFMSL* and 2.7 µm including the MET3 layer, respectively (Fig. 2.11(a)). The insertion loss of a quarter-wavelength transmission line is, as a result of the narrow line width, in the range of 0.6 dB to 0.8 dB around 300 GHz—which significantly reduces the efficiency of power combining networks in such a wiring environment, as can be seen in Fig. 2.11(b). Furthermore, the feasible impedance range of the MET3-reinforced TFMSL is limited by the 2.5-µm minimum-width design rule for MET3, which limits the maximum feasible line impedance to 53 Ω for the *BEOL-A* variant. This, however, has been a critical issue within the *BEOL-A* technology variant due to the fact, that high-impedance 71-Ω transmission lines are required for the impedance transformation in combiners such as the Wilkinson combiner.

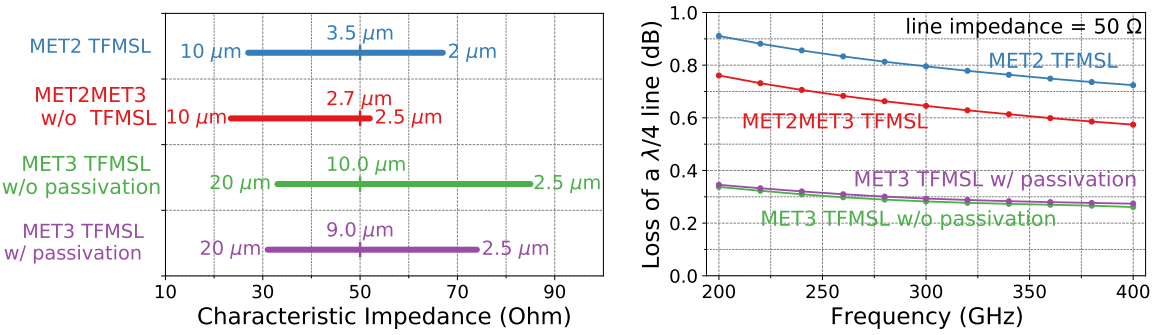
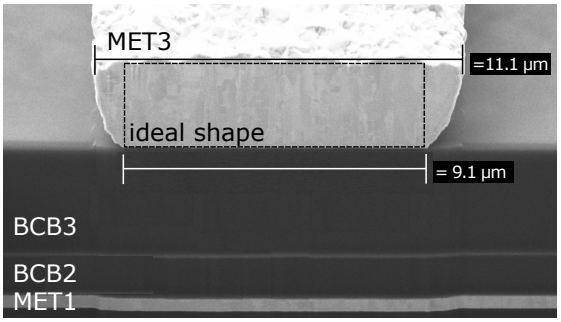


Figure 2.11: (a) Simulated feasible impedance range of the transmission lines depicted in Fig. 2.9. The line width, which is required for the minimum impedance, the maximum impedance as well as a 50-Ω line impedance, is also shown in µm. (b) Loss of the thin-film transmission lines depicted in Fig. 2.9 for a length of $\lambda/4$. The loss is normalized to a quarter wavelength at the respective frequencies. The line impedance of each transmission line is 50 Ω.

The issue of the limited impedance range for TFMSL interconnections was recently addressed with the introduction of the additional BCB layers in the *BEOL-B* variant. By using MET3 for *MET3 TFMSL* interconnections (Fig. 2.9(c)), high-impedance thin-film lines with characteristic impedance well above 70 Ω are feasible—reducing the loss of a $\lambda/4$-line to 0.3 dB around 300 GHz, as can be seen in Fig. 2.11(b).

The impact of the final passivation BCB layer on the feasible impedance range of the *MET3 TFMSL* can bee seen in Fig. 2.11(a). By implementing the final passivation—which is required as scratch-protection layer to improve the mechanical protection for the subsequent handling of the fabricated circuitry—the impedance range is again limited to approximately 74 Ohm. The shape of the MET3 signal line which is considered here, is the perfect rectangular-model shape depicted in Fig. 2.9(c). Yet in reality, the galvanically-grown top-metal layer has a trapezoid-like shape, as depicted with the MET3-TFMSL scanning electron microscope (SEM) cross section shown in Fig. 2.12. While the bottom width of the 9-µm-wide MET3 line is approximately true to size, the width dimension at the top increases by around 1.0 µm at both sides, reducing the characteristic impedance significantly. The impact of this trapezoidal shape is especially relevant at



MET3 shape	Impedance of MET3 Thin-Film Microstrip Line			
	without final passivation		including final passivation	
	width: 2.5 µm	width: 10 µm	width: 2.5 µm	width: 8 µm
ideal	86.5 Ω	50.0 Ω	75.9 Ω	51.7 Ω
real	79.6 Ω	48.3 Ω	69.9 Ω	49.8 Ω
ideal shape W=W+2*0.4 µm	80.1 Ω	48.4 Ω	70.2 Ω	50.1 Ω

Figure 2.12: Scanning-electron- microscope image of a 9-µm-wide MET3-TFMSL cross section without final passivation (left). The impact of the non-ideal MET3 shape on the line impedance of 2.5-µm-wide high-impedance lines as well as 50-Ω lines is depicted on the right, in comparison to the ideal rectangular shape.

very narrow widths of the transmission line and, furthermore, when the final passivation is used to cover the signal line with BCB.

On the right-hand side of Fig. 2.12, the impact on the *MET3 TFMSL* impedance is summarized, when considering the real MET3 shape in simulation. For a 9–10-µm-wide MET3 line with characteristic impedance in the range of 50 Ω, the impedance deviation is below 2 Ω and, thus, can almost be neglected on circuit level. In general, the impact of the galvanic top-metal shape can be taken into account in simulation with good accuracy by using the ideal rectangular shape and increasing the width by 0.4 µm at each side. For the implementation of high-impedance MET3 lines, however, the line-width deviation is significantly more critical, due to the larger impact in relative terms. By stressing the 2.5-µm minimum-width design rule of MET3 to the limit, only an approximately 70-Ω line impedance can be realized within the design rules when using the final passivation. Since the exact dimensions of the MET3 layer can, furthermore, vary by a few hundred nanometers between different runs, the overall spread on circuit level can be impacted by narrow-width high-impedance MET3 lines.

To address these above-discussed limitations of the *BEOL-A* thin-film transmission lines as well as the *MET3 TFMSL*, air-bridge thin-film wiring as well as elevated CPW wiring has been investigated to implement low-loss and high-impedance thin-film transmission lines for TFMSL power combiners at 300 GHz.

2.3.2 Air-Bridge Thin-Film Wiring

In order to increased the impedance range and reduce the insertion loss of the thin-film transmission lines in the *BEOL-A* variant, the air-bridge transmission line depicted in

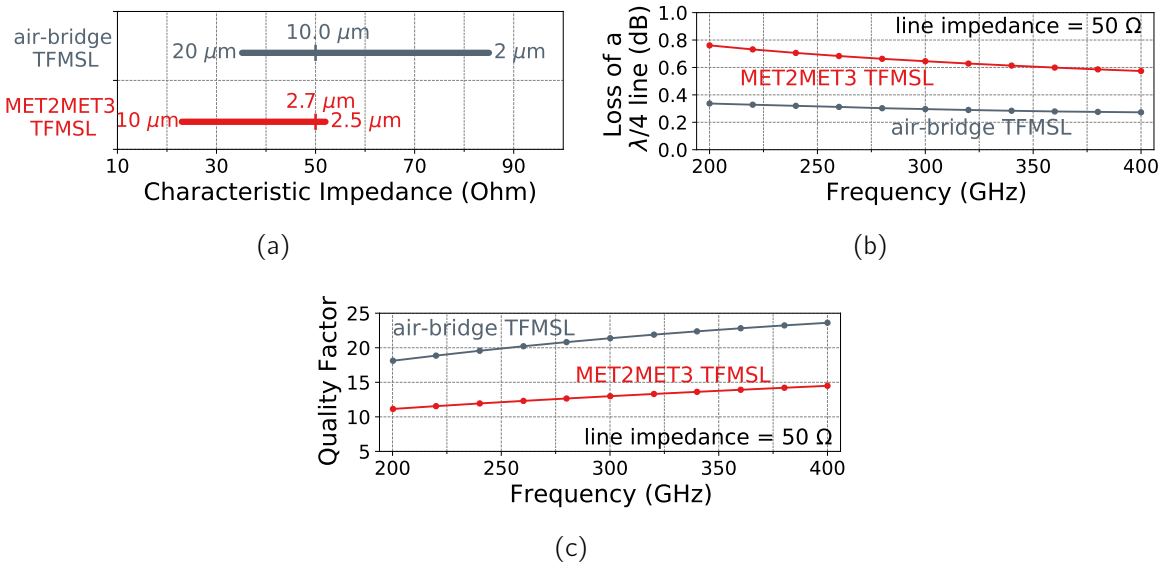


Figure 2.13: (a) Simulated feasible impedance range of the *air-bridge TFMSL* depicted in Fig. 2.10(a). The line width, which is required for the minimum impedance, the maximum impedance as well as a 50-Ω line impedance, is also shown in µm. (b) Loss of the *air-bridge TFMSL* for a length of $\lambda/4$. The loss is normalized to a quarter wavelength at the respective frequencies. The line impedance is 50 Ω. (c) Quality factor of the transmission lines.

Fig. 2.10(a) has been investigated. By using the additional 1.6-µm "air-substrate", the substrate height of this *air-bridge TFMSL* is increased and, hence, high-impedance transmission lines with low insertion loss are feasible. The number of posts, which are required to hold up the air-bridge, is strongly dependent on the routing of the transmission line. The simulated data depicted in Fig. 2.13 is, therefore, considering an ideal transmission line without any posts.

Air-bridge transmission lines have been previously reported in two-metal-layer BEOL technologies [46, 107, 109, 25], typically requiring an opening in the MET1 ground plane for the posts of the air-bridge interconnection. Since the posts of the *air-bridge TFMSL* depicted in Fig. 2.10(a) are set on top of the BCB2 layer, the impact of the posts is strongly diminished and not considered in this section. The simulated insertion loss of this quarter-wavelength 50-Ω *air-bridge TFMSL* is 0.3 dB at 300 GHz—reducing the loss significantly in comparison to the traditional TFMSLs in the *BEOL-A* technology variant (*MET2* and *MET2MET3 TFMSL*s in Fig. 2.9). This improvement is also seen in the quality factor Q of the *air-bridge TFMSL*, which is improved by approximately 40 % from 13 to 21 at 300 GHz (Fig. 2.13(c)). The loss and impedance range of the air-bridge thin-film line is very similar to the *MET3 TFMSL* discussed in the previous section. The implementation of this thin-film transmission line in 300-GHz Wilkinson combiners is, therefore, investigated in Section 4.3.

2.3.3 Thin-Film Transmission Lines with Structured Ground Metal

By removing the MET1 ground plane underneath the thin-film signal line—as depicted in Fig. 2.10(b) and Fig. 2.10(c), respectively—elevated coplanar waveguides (ECPWs) with increased distance between RF ground and TFMSL signal line are realized, permitting the implementation of interconnections with line impedances well above 70 Ω. Similar elevated CPW transmission lines have been studied for GaAs and silicon substrates in [96, 46, 48], providing higher wave-impedances and lower attenuation compared with conventional CPWs.

Fig. 2.14 shows the simplified top view of the investigated thin-film transmission lines with structured ground plane. In order to permit the implementation of bends, while preventing odd-mode propagation and improve the shielding of the GaAs substrate, the two CPW ground planes are connected using 1-µm-wide MET1 strips. The ground-

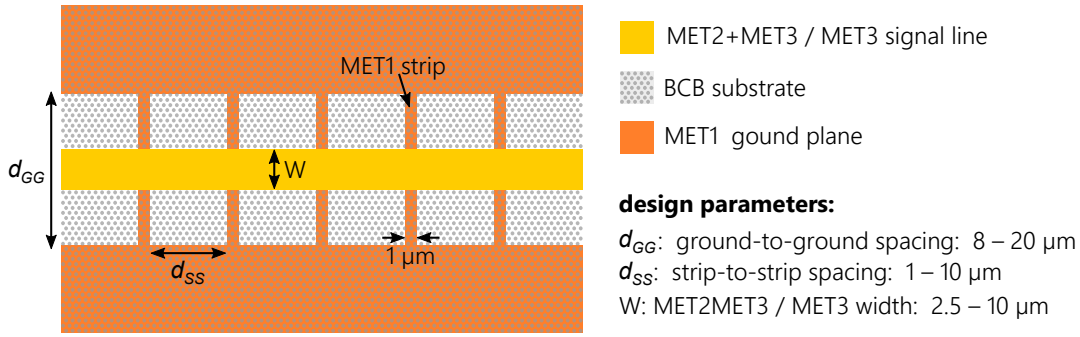


Figure 2.14: Top view of the of the elevated-CPW thin-film line. The signal line is either realized with MET3-reinforced MET2 (MET2 + MET3) or only in MET3. The MET3 signal line is only possible with the additional BCB layers of the *BEOL-B* variant.

to-ground spacing d_{GG} as well as the distance d_{SS} between the MET1 strips, however, strongly impact transmission line characteristics such as the line impedance, electrical length and attenuation. For example, by reducing the strip spacing d_{SS}, the periodic structure of a slow-wave CPW transmission line [99] is realized—which is a well known concept in silicon-based CMOS and SiGe technologies [17, 18, 60], to shrink electrically-long transmission-line elements as well as reduce the attenuation by shielding the lossy Si substrate.

The two design parameters d_{GG} and d_{SS} are, therefore, considered in the following for the implementation of the in Fig. 2.10(b) and Fig. 2.10(b) depicted ECPW thin-film lines.

MET2MET3 Elevated Coplanar Waveguide Fig. 2.15(a) shows the simulated impedance range of the *MET2MET3 ECPW* (Fig. 2.10(b)) for strip-to-strip spacing (d_{SS}) values of 1 µm, 3 µm, 6 µm and 10 µm. The width of the signal line is swept from the design-rule minimum of 2.5 µm to a maximum of 10 µm—and the impedance-range results are depicted for a discrete ground-to-ground spacing (d_{GG}) of 8 µm, 14 µm and 20 µm. The impedance range of the classical *MET2MET3 TFMSL* are also given as reference benchmark.

While the in Fig. 2.15(a) depicted *MET2MET3-TFMSL* impedance range with closed MET1 ground plane is limited to 53 Ω at the upper end, high-impedance thin-film lines in the impedance-range around 80 Ω are feasible with a strip-spacing of 10 µm and ground-to-ground spacing larger than 14 µm. For d_{SS} values larger than 10 µm, the line impedance approximately corresponds to the impedance of the ideal elevated CPW line without any ground-to-ground connections. Yet by reducing the strip spacing d_{SS}, the upper limit of the impedance range is lowered as well.

The simulated attenuation of a 50-Ω *MET2MET3 ECPW* transmission line for d_{SS} = 1–10 µm and d_{GG} = 8–20 µm is shown in Fig. 2.15(b). In comparison to the 0.65-dB loss of a *MET2MET3 TFMSL*, the depicted ECPW loss can be reduced to the range of 0.22–0.3 dB by implementing a ground-to-ground spacing larger than 10 µm and choosing a strip-spacing above 3 µm. These results show, that high-impedance transmission lines can be implemented with significantly reduced attenuation in the *BEOL-A* variant, by opening the MET1 ground plane.

However, even though the electrical length of the transmission line is slightly reduced when decreasing the spacing between the MET1 strips towards a slow-wave-structured ground plane, the best performance in terms of low losses for efficient power combining is achieved with an ideal elevated CPW—as can be seen in Fig. 2.15(b) and Fig. 2.15(c), respectively. This is, furthermore, shown with the quality factor depicted in Fig. 2.15(d), which significantly decreases when reducing the strip spacing and—as a result of this—notably increasing the number of MET1 strips. The increased attenuation and lower quality factor for low d_{SS} values is due to the eddy-current loss on the grounded shields [18], which are implemented with the MET1 strips. As a result of this—even though the phase constant β is increasing—the quality factor and, hence, the loss per wave length is dominated by the increasing attenuation, caused by the grounded shields. This subject of increased eddy-current loss on slow wave transmission lines with grounded shields is

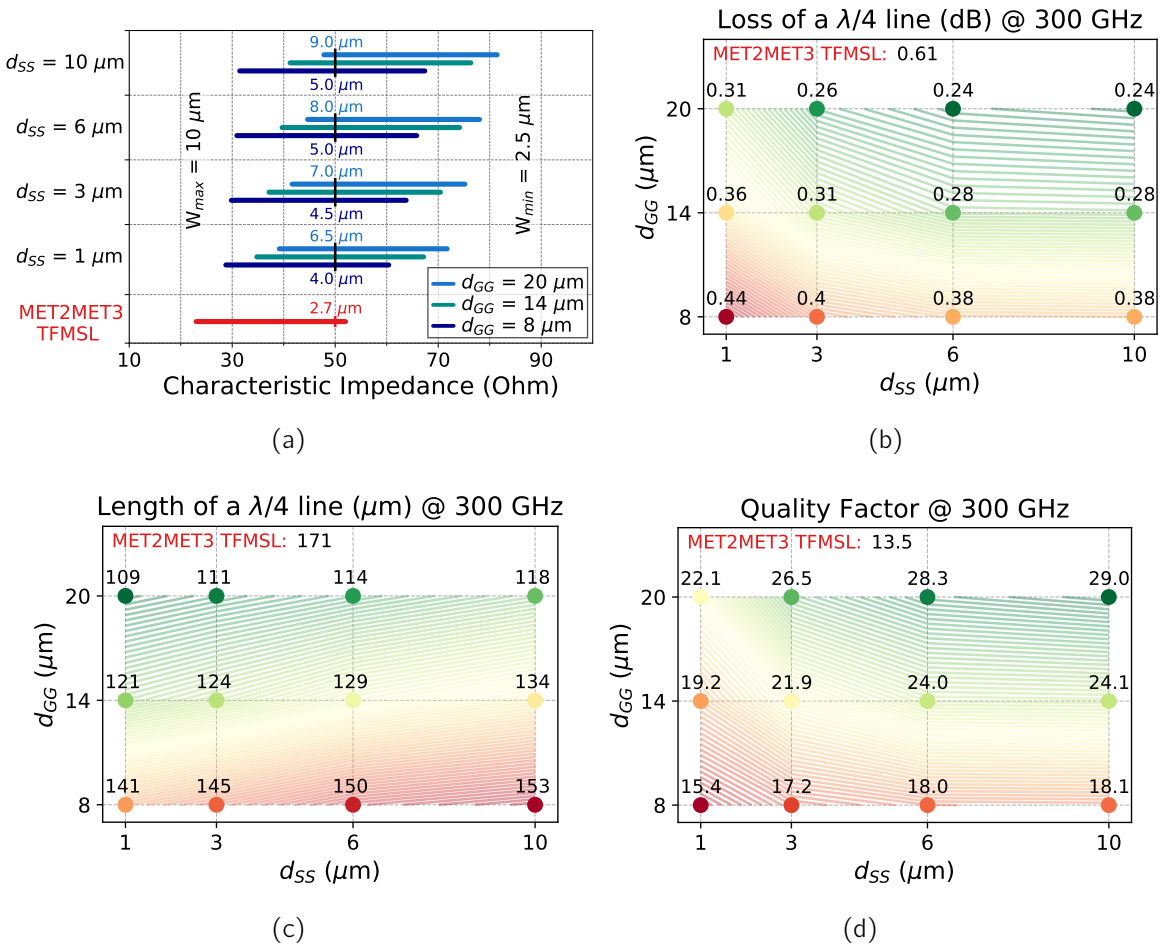


Figure 2.15: (a) Simulated feasible impedance range of the elevated MET2MET3 CPW transmission line depicted in Fig. 2.10(b). (b) Loss of the ECPW line for a length of $\lambda/4$. The loss is normalized to a quarter wavelength at the respective frequencies. (c) Length of quarter-wave-length long elevated MET2MET3 CPW transmission line depicted in Fig. 2.10(c). (d) Quality factor Q of the elevated MET2MET3 CPW transmission lines. The effective line impedance of each transmission line is 50 Ω. The colors in (b)–(d) are coded with the depicted discrete values of the corresponding transmission-line parameters.

a well known issue in CMOS technologies and is, furthermore, the reason why floating shields with inferior slow-wave feature are often preferred over the grounded shields [18].

Hence, as a result of the data discussed above, requirements such as substrate shielding, physical dimensions, as well as losses need to be considered when choosing the values of d_{SS} and d_{GG}. For the implementation in combiner networks, however, larger d_{SS} and d_{GG} values are to be preferred to achieve the best combining efficiency. More details on the ECPW characteristics are shown in Appendix B.

MET3 Elevated Coplanar Waveguide Since the quarter-wavelength 0.3-dB loss of the *MET3 TFMSL* depicted in Fig. 2.9(c) is very acceptable for 300-GHz operation, the main motivation to investigate the *MET3 ECPW* was the reduced upper impedance-range limit of the thin-film line including the scratch protection. Fig. 2.16 shows the simulated impedance range, attenuation, length of a $\lambda/4$ line, as well as the quality

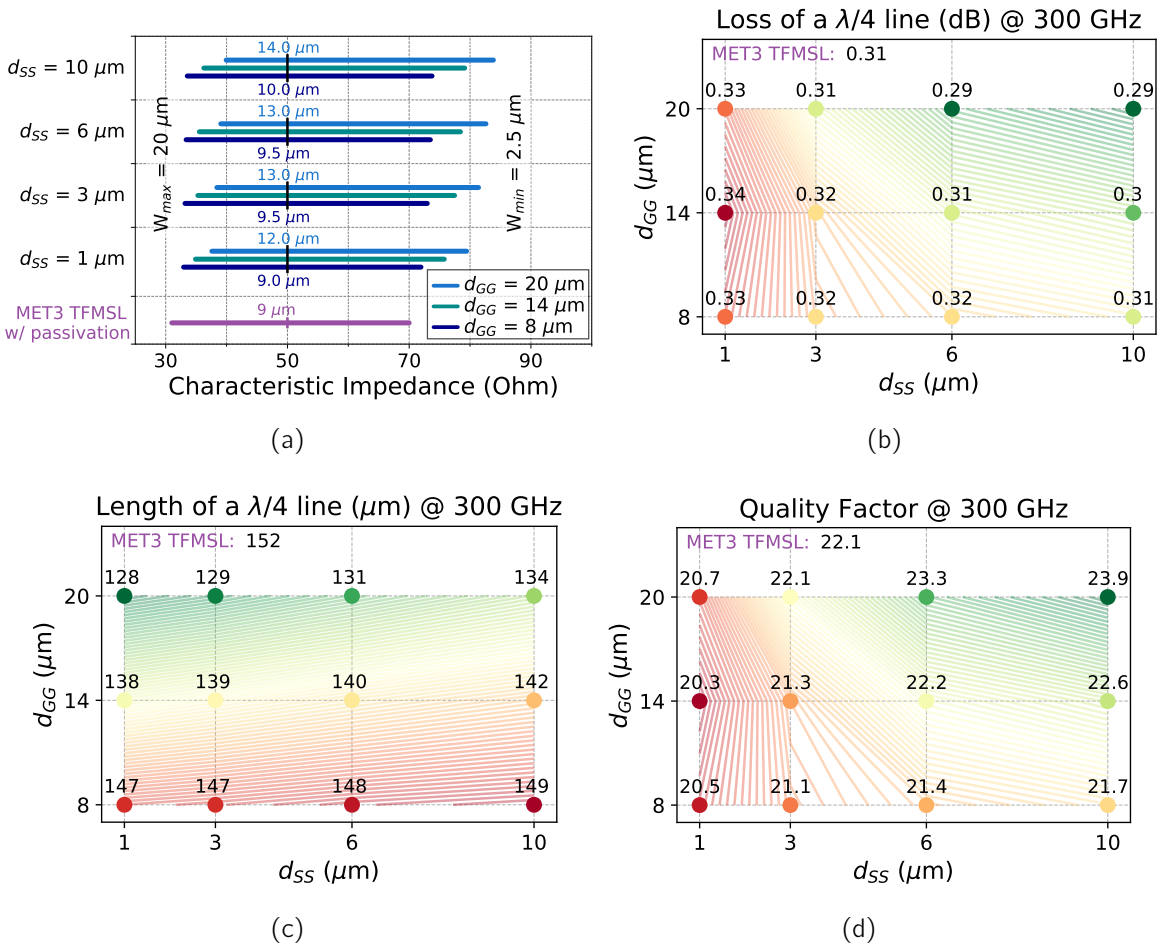


Figure 2.16: (a) Simulated feasible impedance range of the elevated MET3 CPW transmission line depicted in Fig. 2.10(c). (b) Loss of the ECPW line for a length of $\lambda/4$. The loss is normalized to a quarter wavelength at 300 GHz. (c) Length of quarter-wave-length long elevated MET3 CPW transmission line depicted in Fig. 2.10(c). (d) Qualitiy factor Q of the elevated MET3 CPW transmission lines. The effective line impedance of each transmission line is 50 Ω. The colors in (b)–(d) are coded with the depicted discrete values of the corresponding transmission-line parameters.

factor of the *MET3 ECPW* with the same MET1-opening dimensions as discussed in the previous paragraph (d_{SS} = 1 µm, 3 µm, 6 µm, 10 µm and d_{GG} = 8 µm, 14 µm, 20 µm). The corresponding figures of the classical *MET3 TFMSL* are also given as reference benchmark. The depicted line widths in Fig. 2.16(a) are those of the corresponding layout implementations—the real MET3 shape is then considered in simulation by sizing the width of the MET3 signal line by 0.4 µm at both sides.

As can be seen in Fig. 2.16(a), for strip-spacing d_{SS} values above 10 µm and a ground-to-ground distance larger than approximately 10 µm, a characteristic impedance level well above 80 Ω is feasible with the *MET3 ECPW*. Even for d_{SS} = 1 µm, a maximum line impedance of 80 Ω is feasible with d_{GG} = 20 µm. When looking at the loss introduced by a quarter-wavelength 50-Ω ECPW, only slight improvements are observed for a ground-to-ground spacing up to 20 µm and d_{SS} values above 3 µm. In order to significantly reduce the attenuation, a ground-to-ground spacing above 20 µm would be required, which is

not considered due to the large required layout dimensions, which would contradict the targeted implementation of compact PA cells.

Furthermore, due to the above discussed increased attenuation of the grounded shields of the slow-wave structures, the loss per wave length is even slightly increased for $d_{SS} = 1\,\mu m$. The same trend, is also seen in the decreased quality factor of the simulated slow-wave lines—despite the reduced electrical length depicted in Fig. 2.16(c). The main advantage of the *MET3 ECPW* is, therefore, that even for very small slots in MET1—for example in the case of $d_{SS} = 1\,\mu m$—low loss at increased upper impedance range is possible. Hence, high-impedance transmission lines, including the final passivation for scratch protection, with good substrate shielding are feasible without reducing the signal-line width down to the the design-rule limit. This is especially relevant when considering a certain spread of the MET3 signal-line width, to improve the robustness of compact TFMSL on-chip combiners.

Thin-film Wilkinson combiners, which have been implemented with the here discussed ECPW TFMSLs in the *BEOL-A* and *BEOL-B* variants are discussed in detail in Section 4.3.

2.4 Discussion and Conclusion on Chapter 2

This chapter introduces the underlying 35-nm InGaAs-channel HEMT technology and describes the in-depth analysis of two key components for the development of highly-compact 300-GHz PA MMICs in this mHEMT technology: the active devices including possible configurations for the implementation in PA circuits as well as thin-film transmission lines for the realization of the matching and power-combining networks. The analysis of these two topics is required as a basis for the PA-design considerations described in the following chapters.

The comprehensive evaluation of the state of the art of previously reported 300-GHz power amplifiers in Chapter 1 has shown, that the successful stacking of several active devices was not conclusively demonstrated in prior publications which claim the implementation of stacked PA topologies. Hence, the theoretical evaluation of the series-connected device configuration is discussed here, and the respective benefits as well as limitations for the implementation at 300-GHz are evaluated. The theoretically achievable output-power improvement of N-stacked transistors at the sub-mm-wave frequency range around 300 GHz is analyzed for the first time, considering the f_T limitations of cascaded CG devices described in [114]. From this analysis it was found, that a double-stack theoretically permits an improved 300-GHz output-power performance in comparison to single CS devices. The expected improvement, however, is only in the range of 1 dB. Furthermore, the stacking of three devices does not yield any further increased output-power performance. Considering the challenges in stacked PA design at sub-mm-wave frequencies—which is strongly limited by large-signal-model deviations—the relevance of the stacked-FET topology for the implementation of broadband PAs with high linearity in real-world systems and scenarios around 300 GHz, therefore, is concluded to be strongly diminished. This is a significant result for the PA design and topology considerations discussed in the following chapters.

The second part of this chapter is dedicated to the extensive analysis of monolithic transmission lines. For the implementation of compact 300-GHz PA cells and efficient power combiners, thin-film wiring possibilities have been investigated in the two available BEOL variants of the underlying technology—including the BEOL with top-metal layer in air-bridge technology (*BEOL-A*) as well as the recently developed variant featuring additional BCB layers (*BEOL-B*). A key challenge for the realization of low-loss thin-film combiners is the utilization of high-impedance transmission lines, which are required for the impedance transformation in most 50-Ω power-combining concepts. Thus, to enable low-loss and high-impedance transmission lines, novel thin-film wiring possibilities with structured ground metal are analyzed for the first time in a III-V technology at the lower THz frequency band. The analysis of elevated CPW interconnections and the possibility of implementing slow-wave transmission lines by reducing the spacing of the grounded-shield stripes shows, that a trade-off decision between loss per wavelength and reduced physical length needs to be made. When using the *BEOL-A* variant, the elevated CPW transmission lines permit upper impedance-range limits well above 70 Ω, which is not possible with the prior used thin-film lines in this technology variant. At the same time, the attenuation at 300-GHz is significantly reduced. For the *BEOL-B* variant, on the other hand, the main advantage of elevated CPW and slow-wave thin-film wiring is the possibility of realizing high-impedance transmission lines with increased signal-line width, despite using the final passivation for scratch protection. Hence, by implementing the structured MET1 ground plane, the impact of the galvanically-grown MET3 shape as well as potential width variations on the characteristics of high-impedance MET3 lines can be reduced. The implementation of novel low-loss 300-GHz thin-film Wilkinson combiners based on these transmission lines are investigated in Section 4.3 as a crucial building block of the highly-compact PA circuits developed in this thesis.

3 Analysis of InGaAs mHEMT Devices for Broadband 300-GHz Power Amplifiers

Means to increase the output power on chip level, by voltage and current combining of multiple devices or PA cells, are described in the previous Chapter 2. On device level, this is done by parallelizing several transistor fingers in multi-finger transistor configurations, which are further integrated in parallel-connected as well as series-connected topologies. When increasing the frequency of operation to the lower THz frequency band, however, the electrical dimensions of multi-finger-device elements such as the feeding structures, for example, significantly increase in size—even if they are implemented close to the design-rule minimum. Therefore, the practical implementation and modeling of multi-finger devices for compact THz PA circuits is discussed for the underlying InGaAs-channel HEMT technology in the following sections. Layout limitations of devices with multiple transistor fingers in common-source as well as cascode configuration are evaluated. Further, a modeling approach based on two-finger process-design-kit (PDK) device models without feeding structures and a fully EM simulated multi-finger shell is described. To improve the performance on the device level, single devices with different recess lengths—and the associated impact on key device figures such as possibly increased voltage handling capabilities—were evaluated and are first described in the following section.

3.1 Recess Optimization for Increased Breakdown Voltage

The process sequence of the 35-nm InGaAs mHEMT fabrication is shown in Fig. 3.1 on the left. A wet-chemical mesa etch process is used for device isolation and an electron-beam evaporated GeAu layer is deposited for the ohmic contacts. The 35-nm gate foot length is defined by inductively-coupled plasma etching of the depicted SiN layer and the gate recess is etched subsequently, by removing the cap layer. The opening in the SiN layer then acts as a shadow mask for the gate-foot metalization.

Using this process sequence, the length of the gate recess is defined by the etching duration of the cap layer. Yet, the recess length between gate and source as well as gate and drain, respectively, have a strong impact on key device figures such as noise performance and breakdown characteristics. An undersized recess length, for example, degrades the breakdown voltage of the devices whereas an oversized recess increases the source resistance, which limits the noise figure and bandwidth [102]. However, due

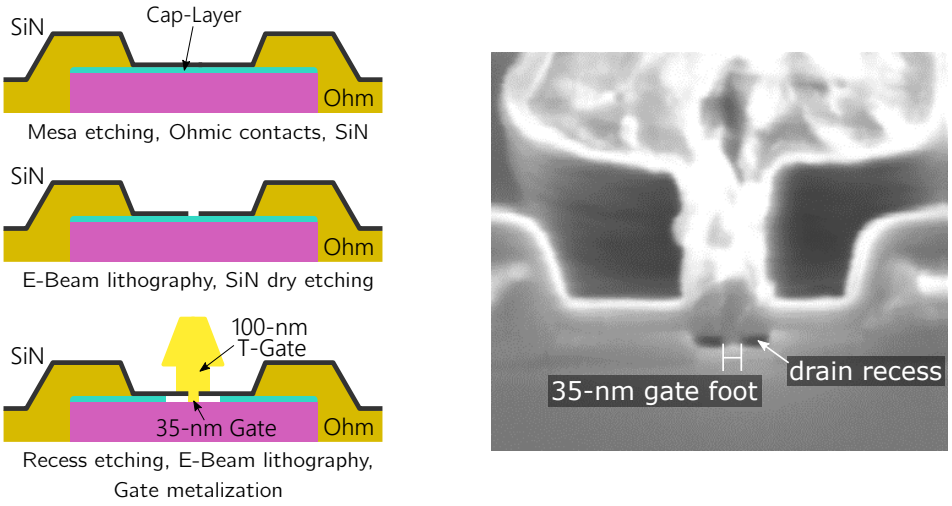


Figure 3.1: (left) Process sequence of the planar 35-nm InGaAs mHEMT fabrication and (right) SEM image of the fabricated T-gate cross section.

to the above described process sequence—which defines both the length of the source recess as well as the drain recess in a single etching step—the transistor finger is perfectly symmetric and, therefore, drain recess and source recess cannot be optimized separately.

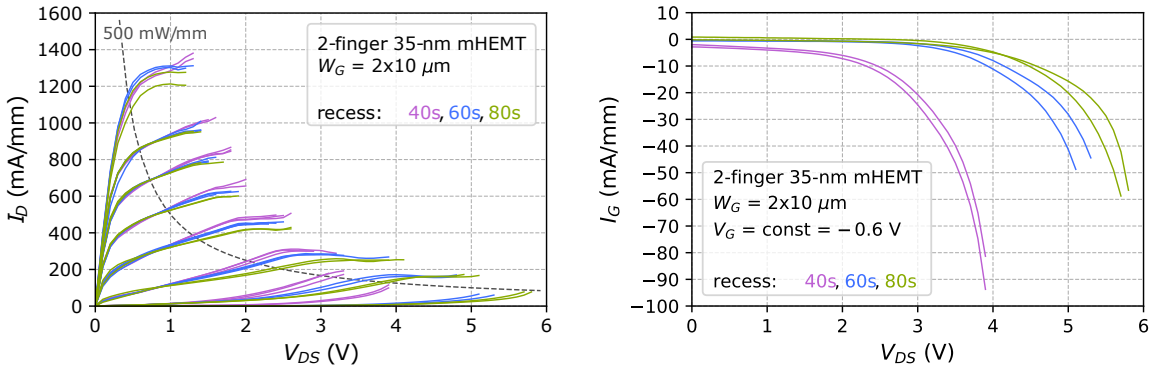
Hence, the possibility of increasing the recess length, to improve the breakdown voltage of the mHEMT devices, was investigated experimentally. Starting with the standard etching duration of 40 seconds, longer etching times of 60 seconds as well as 80 seconds were processed and evaluated. Since the etching time can only be varied between different wafers using the above described process sequence, batch processing with up to 8 wafers was done, including a wafer split for the recess processing over the course of several runs. Therefore, device spread needs to be considered for the underlying research-level technology when comparing the results of the three recess-length variants, which could not be processed and measured on the same die but only on different wafers.

3.1.1 Evaluation of Recess-Length Impact on DC and Small-Signal Device Figures

To evaluate the impact of the performed recess etching time, breakdown measurements of single HEMT devices were done. Furthermore, in order to provide a well-founded basis to asses the device performance of the different recess variants, key device parameters have been extracted from DC and RF wafer-mapping measurements.

DC Performance Characterization and Evaluation The measured I-V characteristics of CS mHEMT devices with 40-s, 60-s and 80-s recess variants are depicted in Fig. 3.2. Each measurement curve represents a single device which was measured to destruction, by sweeping the drain-source voltage at constant gate voltages from zero up to device burnout.

At drain currents above approximately 400 mA/mm, a very similar breakdown behavior at V_{DS} values in the range of 1.2–2 V can be observed for all three recess variants (Fig. 3.2(a)). In this I-V region, the breakdown is dominated and limited by the poor



(a) (b)

Figure 3.2: Measured I-V DC-burnout curves of 35-nm mHEMT devices width different recess lengths. (a) Shows the measured output characteristics I_D vs. V_{DS} and (b) shows the corresponding gate currents I_G vs. V_{DS} for $V_G = const = -0.6\,V$.

thermal conductivity of the metamorphic buffer. Due to the high-thermally-resistive ternary layers that are associated with the transitional buffer grading between the GaAs substrate and the transistors' epitaxial layers, the operating range of V_{DS} is limited for high current densities—independent of the investigated recess lengths. For lower drain-current densities, on the other hand, significantly improved output conductance g_{DS} and off-state breakdown behavior is observed when increasing the recess-etching time from 40 s to 60 s and 80 s, respectively.

Fig. 3.2(b) shows the respective burnout gate currents for the three recess variants, measured at a constant gate voltage (V_G) of −0.6 V. By defining a maximum gate-current density as breakdown parameter, the off-state breakdown behavior of the measured samples can be compared. For a gate current of $I_G = -10$ mA/mm, e.g., approximately 2.4 V drain-source voltage is applied to the devices with 40 s recess. The 60-s variants, on the other hand, shows significant improved breakdown behavior with $V_{DS} = 4$ V off-state breakdown voltage for this −10-mA/mm gate-current limit. This corresponds to an off-state breakdown improvement of 1.6 V. By further increasing the recess-etching time to 80 s, the breakdown is only slightly increased by approximately 0.5 V.

Judging from the I-V burnout curves depicted in Fig. 3.2, improved performance in terms of off-state breakdown, is observed. To further assess the impact of the recess-length variation on the device performance, additional key DC device figures have been evaluated. These figures include the saturation current $I_{D,max}$, the drain resistance R_D (which is equal to the source resistance R_s for the symmetric HEMT device), the maximum transconductance $g_{m,max}$, as well as the output conductance g_{DS}, which are displayed in Fig. 3.3. To account for device spread—which is essential since device measurements of different wafers and runs are compared—the mapping data of at least 8-wafers and 144 single-finger devices per wafer have been considered for each recess variant in Fig. 3.3. Since no normal distribution can be assumed for the measured device parameters and the underlying distribution is not known, the 95-% confidence interval (95-% CI) for the median is used to compare the three recess variants, rather than the median. The 95-% CI describes the range for the median at a confidence of 95 % and,

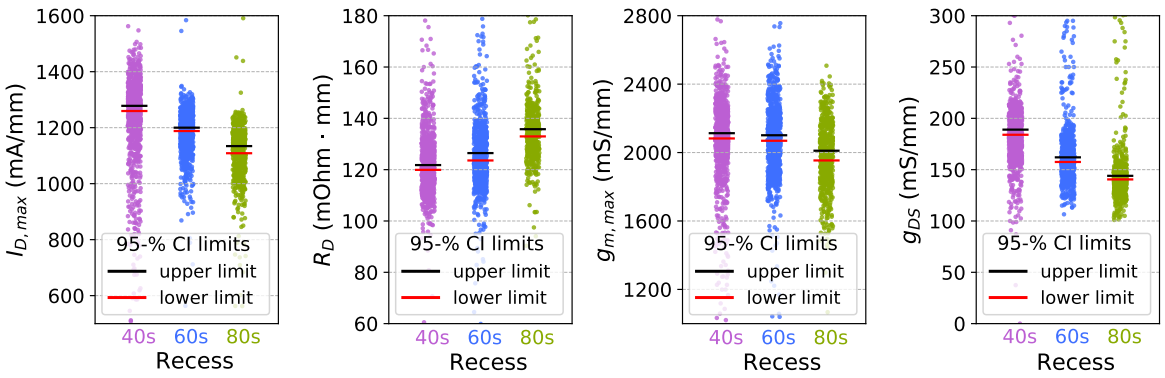


Figure 3.3: Measured DC characteristics of the 40-s, 60-s, and 80-s recess variants at $V_{DS} = 0.8\,V$: (a) maximum drain current $I_{D,max}$, (b) drain resistance R_D, (c) the maximum transconductance $g_{m,max}$, and (d) the output conductance g_{DS}.

hence, permits the statistical evaluation of the limited number of samples without knowing the underlying distribution [94]. The limits for the confidence intervals are calculated according to [119].

When evaluating the DC parameters depicted in Fig. 3.3, a decline of approximately 80 mA/mm is observed when increasing the etching time from 40 s to 60 s and from 60 s to 80 s, respectively. This decreasing drain current is mainly caused by the higher R_D (as well as R_s), which is slightly increased for the 60-s recess and significantly larger for the 80-s variant, with $R_{D,80} > 130\,mOhm \cdot mm$. The $g_{m,max}$ values, on the other hand, stay constant around 2100 mS/mm for the 40-s and 60-s recess, while a clear drop below 2000 mS/mm can be seen for the etching time of 80 s. As already shown in the I-V output characteristics depicted in Fig. 3.2(a), notably improved g_{DS} values are achieved with the longer recess variants. Hence, especially for the 60-s variant, a significant improvement in terms of intrinsic gain $g_{m,max}/g_{DS}$ is achieved, which is increased by a factor of approximately 1.2 in comparison to the 40-s recess. Yet, due to the lower $g_{m,max}$ values, this figure of merit only improves by a factor below 1.1 when further increasing the etching time to 80 s.

Small-Signal Performance Characterization and Evaluation The small-signal parameter S_{21} at 40 GHz, transit frequency f_T, as well as $g_{m,max,RF}$ and $g_{DS,RF}$—which have been calculated from the mapping data of at least 8-wafers and 37 two-finger devices per wafer—are depicted in Fig. 3.4. The measurement data of standard 2x10-µm CPW transistors at 40 GHz is used here, since at this frequency, accurate results and device-parameter extraction are ensured. Furthermore, the 40-GHz data is sufficient to evaluate the small-signal performance of the different recess variants without the impact of the on-wafer measurement setup, which would need to be considered at higher mm-wave frequencies. Due to the smaller number of samples in comparison to the Fig.-3.3 DC data, the 95-% CIs are less confined for the measured RF data. Only for the $g_{DS,RF}$ values, a clear improvement can be seen for the longer-recess variants, with $g_{DS,RF}$ values below 90 mS/mm. The other device parameters show mostly overlapping limits for the confidence levels of 95 %.

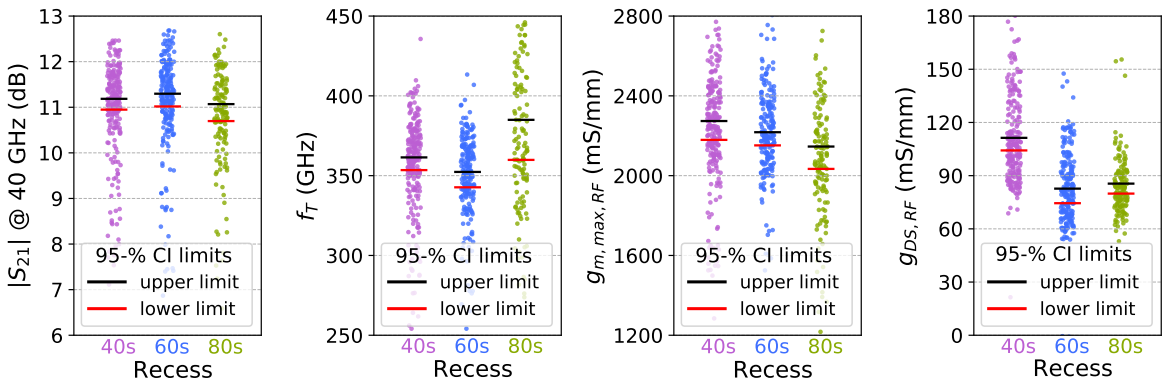


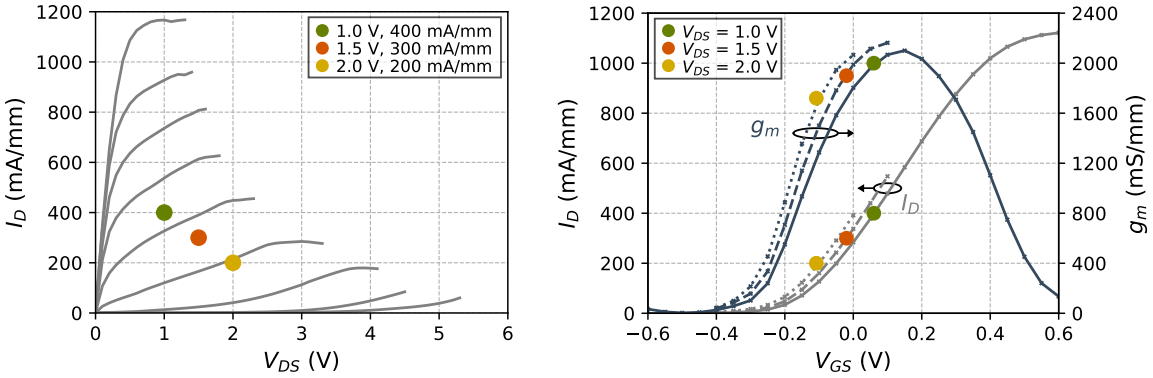
Figure 3.4: Measured RF characteristics of the 40-s, 60-s, and 80-s recess variants: (a) small-signal gain $|S_{21}|$ at 40 GHz, (b) transit frequency f_T, (c) maximum RF transconductance $g_{m,max,RF}$, and (d) RF output conductance $g_{DS,RF}$.

The measured small-signal gain S_{21}, for example, shows now clear trend for the three recess variants. The same observation was made for measurement results on circuit level (not shown here), which are additionally impacted by the spread of the passive matching elements during the BEOL processing and, therefore, cannot be used to evaluate the three HEMT variants. For all recess variants, the f_T values of the 95-% CI are in the range of 340 to 380 GHz. The depicted $g_{m,max,RF}$ data indicate, however, a similar trend as for the DC values in Fig. 3.3. While most of the 95-% confidence interval of the 60-s $g_{m,max,RF}$ is within the corresponding 40-s CI, the range of the 80-s CI is observed to be at lower values.

Conclusions Based on the measurement data discussed above, the 60-s recess variant was chosen as the new standard for the recess processing of the underlying 35-nm mHEMT technology. When compared to the prior-standard 40-s recess length, significant improvement in terms of breakdown voltage and output conductance g_{DS} are observed. Further key device figures such as $I_{D,max}$, R_D, and $g_{m,max}$ are either not affected or only slightly deteriorated. The 80-s recess variant, on the other hand, provides only moderate breakdown improvements with significantly increased R_D as well as further decreased $I_{D,max}$ and $g_{m,max}$ values, when compared to the 60-s recess.

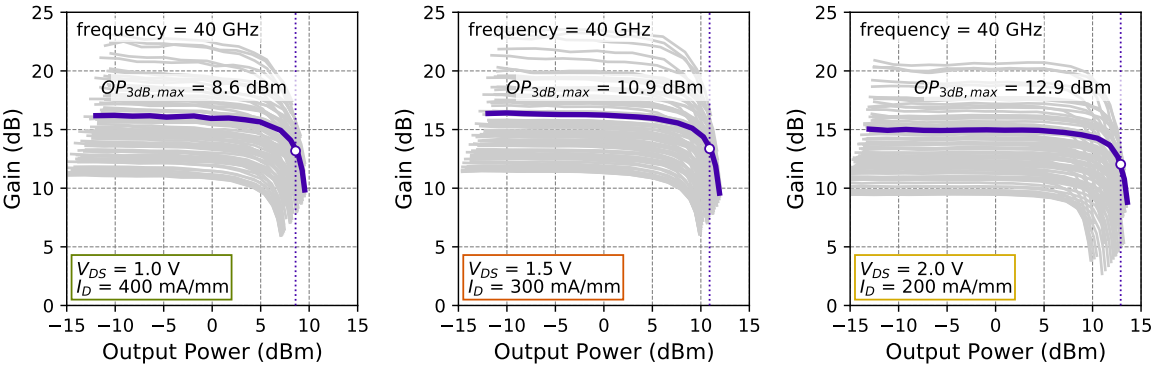
3.1.2 Large-Signal Performance Characterization and Considerations

The main motivation for the investigation of the above discussed recess-length variants is the possibility of increasing the voltage-handling capabilities and, hence, the power density on the device level. Fig. 3.5(a) shows the output characteristics of a 60-s recess device with typical DC-bias conditions in the range of 1.0 to 2.0 V. For operation at $V_{DS} = 1$ V, a DC-bias point around 300 to 400 mA/mm is typically chosen for PA applications at the upper mm-wave frequency band, providing high intrinsic gain for broadband amplifier implementations. However, while the 60-s recess length permits the operation at drain-source-voltages of up to 2.5 V, the mHEMT devices need to be biased at significantly



(a) (b)

Figure 3.5: (a) Measured output characteristics for the 60-s recess variant and (b) transfer characteristics of the HEMT device in the corresponding bias points of 1.0-V, 1.5-V and 2.0-V V_{DS}.



(a) (b) (c)

Figure 3.6: Measured gain versus output power at 40 GHz of a 2-finger device with 2x30-µm gate width for V_{DS} in the range of 1.0 to 2.0 V. The curves depicted in grey color represent the results of a load-pull measurement, the optimum-load data for maximum output power in 3-dB gain compression is highlighted. The data in (a), (b) and (c) corresponds to the bias condition displayed in the lower-left corners of the respective figures.

lower I_D values, in order to avoid thermal breakdown at high current densities. The respective bias conditions up to 2 V are highlighted in Fig. 3.5(a). Fig. 3.5(b) displays the corresponding transfer and g_m characteristics at 1.0 V, 1.5 V and 2.0 V drain-source voltage, respectively.

To evaluate the large-signal performance at increased voltage levels, load-pull measurements were performed using an active 40-GHz load-pull setup. This 40-GHz system was used for device characterization at the beginning of this work, due to the lack of available active load-pull systems at higher frequencies. However, since the power density of the underlying mHEMT devices is typically independent of the operating frequency, the 40-GHz results can be applied to the lower THz band around 300-GHz. The measured gain characteristics of a 2-finger mHEMT with 30-µm finger width are plotted versus the

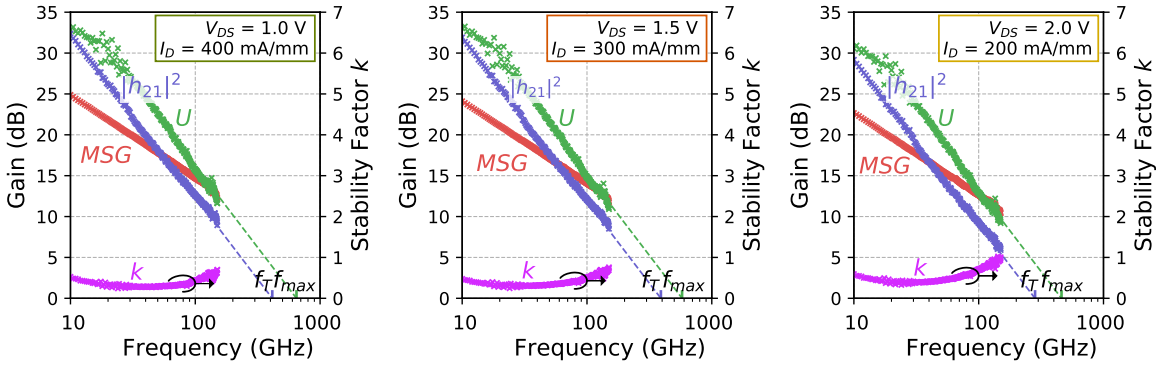


Figure 3.7: Measured forward current gain h_{21}, unitary power gain U and maximum stable gain MSG as a function of the frequency. f_T and f_{max} are defined where h_{21} and U reach unity, respectively. The data in (a), (b) and (c) corresponds to the bias condition displayed in the upper-right corner of the respective figures.The measured gain characteristics correspond to a 2-finger device with 2x30-µm gate width.

measured output power in Fig. 3.6. At 1 V and 400 mA/mm, a maximum of 8.6-dBm output power was measured at 3-dB gain-compression (OP_{3dB}). This corresponds to a power density of 121 mW/mm at the device level. By increasing the voltage to 1.5 V at 300 mA/mm, the measured OP_{3dB} is improved by 2.3 dB to 10.9 dBm or 205 mW/mm, respectively. This significant improvement of 70 % is achieved due to the fact, that at $V_{DS} = 1.0$ V the device is biased close to the knee voltage of approximately 0.4 V. Hence, increasing V_{DS} by only 500 mV results in a significantly larger maximum voltage swing, improving the power density by more than two-thirds. By further increasing V_{DS} to the value of 2.0 V, a maximum OP_{3dB} of 12.9 dBm is achieved (325 mW/mm). This corresponds to an OP_{3dB} improvement of almost 170 %, by doubling the voltage from 1 V to 2 V.

While a significant improvement in terms of 40-GHz output-power performance is achieved by increasing the DC voltage to 2.0 V, the gain-level is almost 2 dB lower in comparison to the 1.0-V biasing condition. This is due to the reduced intrinsic gain at the lower 200-mA/mm current level, as can be seen in Fig. 3.5(b). To illustrate the impact of the reduced current-handling capabilities at higher supply-voltage levels on key device characteristics for sub-mm-wave operation, Fig. 3.7 shows the gain figures h_{21} (forward current gain), U (unitary power gain) and MSG (maximum stable gain) for a 2x30-µm transistor, measured up to 150-GHz. The 1.0-V, 1.5-V, and 2.0-V DC bias corresponds to the highlighted biasing conditions in the Fig.-3.5(a) output characteristics. The respective cutoff frequencies f_T and f_{max} are defined where h_{21} and U reach unity, respectively, and are summarized together with the large-signal results in Tab. 3.1. As the MSG for frequencies below the k-point—which is the point where the stability factor k is equal to 1—does not depend on the transistor's finger width, the MSG at 300 GHz in Tab. 3.1 is calculated by extrapolation of the measured 30-GHz MSG with a slope of –10 dB/decade, which is the characteristic MSG drop off over frequency.

Table 3.1: Overview of the device performance at different bias conditions.

	Bias Condition		
	$\mathbf{V}_{DS}$ = 1.0 V $\mathbf{I}_{D}$ = 400 mA/mm	$\mathbf{V}_{DS}$ = 1.5 V $\mathbf{I}_{D}$ = 300 mA/mm	$\mathbf{V}_{DS}$ = 2.0 V $\mathbf{I}_{D}$ = 200 mA/mm
$\mathbf{OP}_{3dB,max}$ (dBm)	8.6	10.9	12.9
$\mathbf{OP}_{3dB,max}$ (mW/mm)	121	205	325
PAE @ OP_{max} (%)	34	36	40
$\mathbf{f}_{T}$ (GHz)	414	391	283
$\mathbf{f}_{max}$ (GHz)	647	578	461
MSG @ 30 GHz (dB)	20.0	19.3	17.9
MSG @ 300 GHz (dB)	10.0	9.3	7.9

Discussion Looking at the device characteristics listed in Tab. 3.1, significantly improved large-signal figures, e.g. power density on device level, is achieved when increasing V_{DS} to voltage levels above 1.0 V. Yet, reduced cutoff frequencies as well as available gain at 300 GHz need to be accounted for when increasing V_{DS} above roughly 1.2 V. As f_T decreases below 300 GHz for $V_{DS} = 2.0$ V at $I_D = 200$ mA/mm, especially the large-signal benefit of the double-stack-cascode configuration is affected, since no improved output-power performance can be expected when operating the HEMT devices around f_T, as discussed in Section 2.2.2. While the lower available bandwidth can be compensated by decreasing the finger width, the reduced *MSG* significantly impacts the PA implementation at the lower sub-mm-wave frequency range. Especially, when considering PA topologies with increasing transistor size in the output stages, the reduced gain needs to be accounted for in order to avoid soft compression due to high losses in the interstage matching networks (ISMNs) and large driving ratios in the cascaded stages. 300-GHz large-signal results in different bias conditions on circuit level are discussed in detail for the compact PA MMICs developed in Section 4.2.2.

As a result of the figures discussed above, and in order to take full advantage of the increased breakdown voltage, the current-handling capability of the HEMT devices at higher voltage levels needs to be improved. A promising solution to increase the on-state breakdown voltage at high current densities is the implementation of InGaAs-channel HEMT devices on Silicon substrate [62, 112], which is motivated by the results discussed above and currently being developed at Fraunhofer IAF. By transferring the HEMT-epi layers to a Si carrier substrate, the development of InGaAs-channel HEMTs on insulator are investigated—without the limitations of the high-thermally-resistive ternary layers associated with the transitional buffer grading.

3.2 Evaluation and Modeling of Multi-Finger Devices

The state of the art of solid-state power amplifiers at frequencies around 300 GHz is introduced in detail in Section 1.1.1. As discussed in this introduction, most of the HEMT

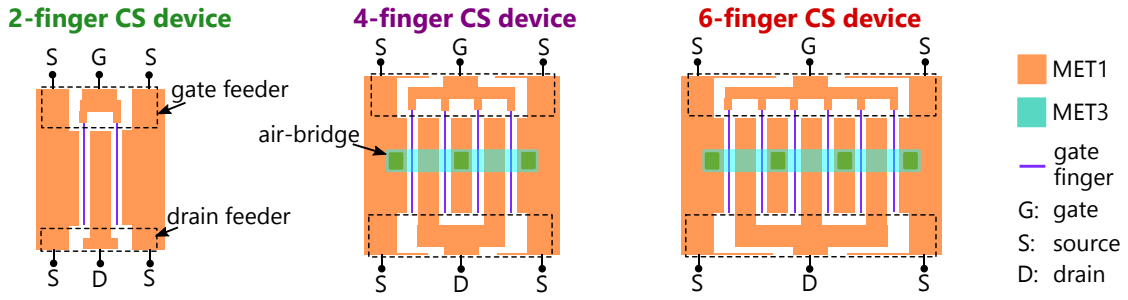


Figure 3.8: Simplified PDK layouts of transistors in CS configuration with two, four and six transistor fingers. The wiring environment is coplanar waveguide.

based PA circuits, on GaAs as well as on InP substrates, which have been reported at frequencies above 100 GHz, are implemented using CPW transmission lines for wiring. The main reason for the usage of CPW wiring is the limited number of metal layers for signal routing, which is two for most HEMT technologies, including a top-metal layer in air-bridge technology.

Due to their good characteristics in terms of transmission line loss [73], CPW interconnections are typically preferred for the design of HEMT-based LNA circuits, in order to achieve the best noise performance possible [113, 110]. In power-amplifier circuits, however, where multiple devices are parallelized in order to increase the output power, the rather bulky dimensions of CPW transmission lines are limiting the implementation possibilities of compact matching networks and, hence, the realization of compact chip dimensions. TFMSL wiring on the other hand—which is discussed in detail in Section 2.3 for the underlying mHEMT technology—permits the implementation of chip-size optimized circuits and is implemented in the power amplifiers of this work.

As a result of the still young history of the three-metal-layer BEOL of this mHEMT technology, up to date, most circuits have been implemented with CPW interconnections. Hence, the active device models have been extracted and are available in CPW environment. In order to maximize the output power in PA circuits, the total gate width is increased. This is done by using devices with multiple transistor fingers, as depicted with the simplified layout of CS devices with two, four and six transistor fingers in Fig. 3.8. This idea of parallel current combining is discussed in Section 2.2.1.

In the most simple case of only two transistor fingers, the general device layout consists of only two parts: the 2-finger transistor structure—including a single drain finger, two gate fingers and two source fingers—as well as the gate and drain CPW feeding structures. When increasing the number of transistor fingers, the feeding structures at gate and drain increase in size as well as complexity. Furthermore, additional air-bridge elements are required to implement the ground connection of the middle source finger(s), as depicted in Fig. 3.8. As the frequency of operation is increased, the electrical length of these source-connecting lines as well as the feeding structures grows, significantly impacting the device performance. In addition to that, the higher complexity of multi-finger devices is impacting both the achievable RF performance—in terms of maximum bandwidth, for example—as well as the effort which is required for transistor modeling.

The transistor models used to model this work's multi-finger devices are based on a multi-port modeling approach with an electrical equivalent circuit model of the extrinsic

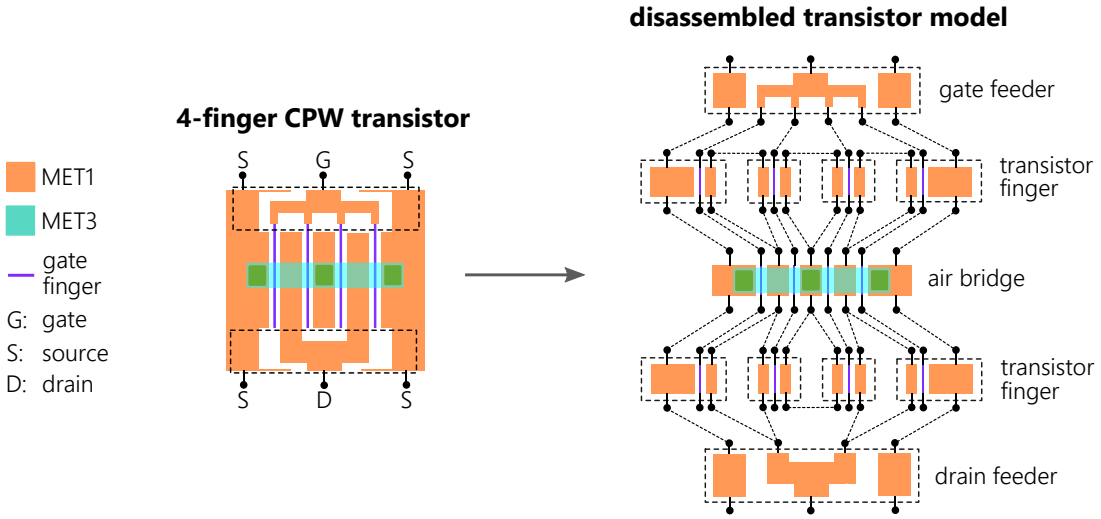


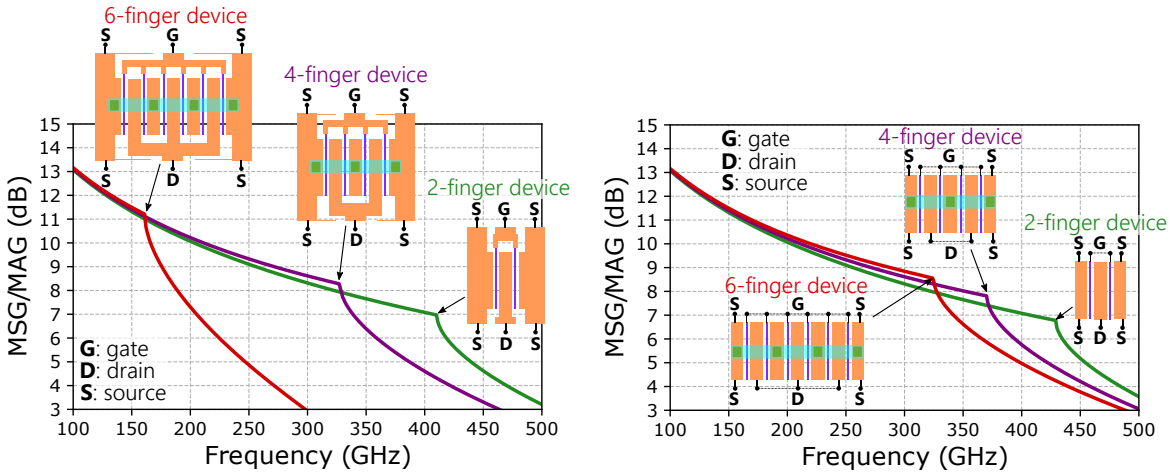
Figure 3.9: Schema for the disassembled planar 4-finger HEMT structure, separated into individual multi-port elements. Ports are symbolized with dots. Connections between different ports are shown with dotted lines [78].

transistor shell, which is based on the actual structure and layout of the transistor [78]. As an example, Fig. 3.9 shows the planar CPW structure of a 4-finger CS device, which is composed of feeding and finger structures as well as the air bridge to connect the source fingers. The depicted feeding and finger structures are separated by optimizing the fit of the equivalent circuit parameters to up to 330-GHz measured and 3D-EM simulated transistor structures with different gate widths and number of transistor fingers, as described in [78]. Hence, the impact of the increased complexity and each layout element can be evaluated in simulation—which has been done for the available multi-finger models depicted in Fig. 3.8, in order to permit the best choice for device selection and the design of compact sub-mm-wave PA circuits.

3.2.1 Impact of Feeding Structures and Layout Complexity

The impact of the more complex layout of CPW-multi-finger devices on the high-frequency performance is depicted in Fig. 3.10, which shows the simulated maximum stable gain (MSG) and maximum available gain (MAG) of 2-finger, 4-finger and 6-finger devices in a typical CPW environment. The frequency range of the depicted plots is centered around the devices' k-points, where the stability factor k is equal to 1. Fig. 3.10(a) shows the MSG/MAG characteristics of the devices including the gate and drain feeding structures, while in Fig. 3.10(b), ideal loss-less feeding structures with zero electrical length are considered—which corresponds to shorted gate and drain fingers as depicted in Fig. 3.10(b).

The lower k-point of devices including the feeding structures in Fig. 3.10(a) occurs because of the additional losses introduced by gate and drain feeders. Due to larger feeding structures, the shift to lower frequencies is more significant for the device with four and six transistor fingers. For the 2-finger and 4-finger transistors, a shift to lower frequencies of approximately 20 GHz and 50 GHz is observed, respectively. With six transistor fingers, on the other hand, a significant bandwidth reduction of more than



(a) w/ feeding structures (b) w/o feeding structures

Figure 3.10: Comparison of simulated MSG/MAG and k-point of 2-finger, 4-finger and 6-finger CS devices with 20-µm finger width in CPW environment. (a) Shows the results including the impact of the gate and drain feeding structure and (b) shows the optimal behavior without the impact of the lossy feeders.

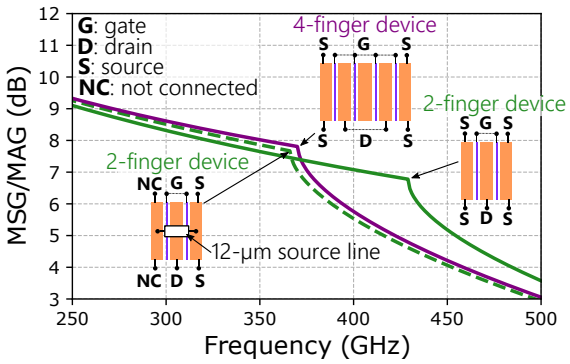


Figure 3.11: Simulated MSG/MAG values of 4-finger and 2-finger devices excluding the gate and drain feeding structures.

100 GHz is caused by the losses and phase imbalance introduced by the gate and drain feeding structures.

When comparing the devices without feeders in Fig. 3.10(b), a frequency shift of 60 GHz is observed between 2-finger and 4-finger transistors—and additional 45 GHz for the 6-finger device. This is due to the asymmetrical layout of the multi-finger CS devices in CPW environment, which requires air-bridges to connect the source fingers in the middle, introducing asymmetrical losses and source degeneration. A similar behavior, as for the 4-finger transistor, is observed when a source line with the length of the air-bridge is added between source and ground connection to one of the source fingers of the ideal 2-finger transistor without feeding structures—which is depicted with the dashed line in Fig. 3.11. Especially at sub-mm-wave frequencies, the impact of the air bridges increases due to their increasing electrical length in comparison to the device layout dimensions, which cannot be significantly reduced within the design rules. This impact of the source-air-bridge can be reduced by maximizing the number of parallel air bridges.

As a result of the decreasing achievable bandwidth of transistors with four and more transistor fingers in the standard CPW layout depicted in Fig. 3.8, their usefulness for PA circuits around 300 GHz is strongly diminished. Another key factor which needs to be considered—but is hard to quantify—is the accuracy of active device models with more than two transistor fingers. Due to the increasing challenges for on-wafer measurements at the upper mm-wave frequencies, the accuracy is reduced by factors such as RF-probe coupling, the influence of the RF pads and the calibration accuracy, for example. Therefore, the frequency range below 110 GHz is typically given more weight during parameter extraction. As a result of this, the overall accuracy of the available multi-finger models is reduced due to their additional layout complexity when increasing the number of gate fingers—which needs to be described correctly—in comparison to the most simple device layout of the symmetric 2-finger device.

To illustrate the impact and challenge of inferior simulation accuracy, when using the available multi-finger device models for 300-GHz PA design, Fig. 3.12 shows the comparison of two 4-finger cascode singe-stage cells. The cascode depicted in Fig 3.12(a) was implemented using two parallel CS and CG 2-finger devices. The cascode cell shown in Fig 3.12(c), on the other hand, was designed using two parallel 2-finger CS devices and a single 4-finger CG device—implementing the same total gate width. The corresponding

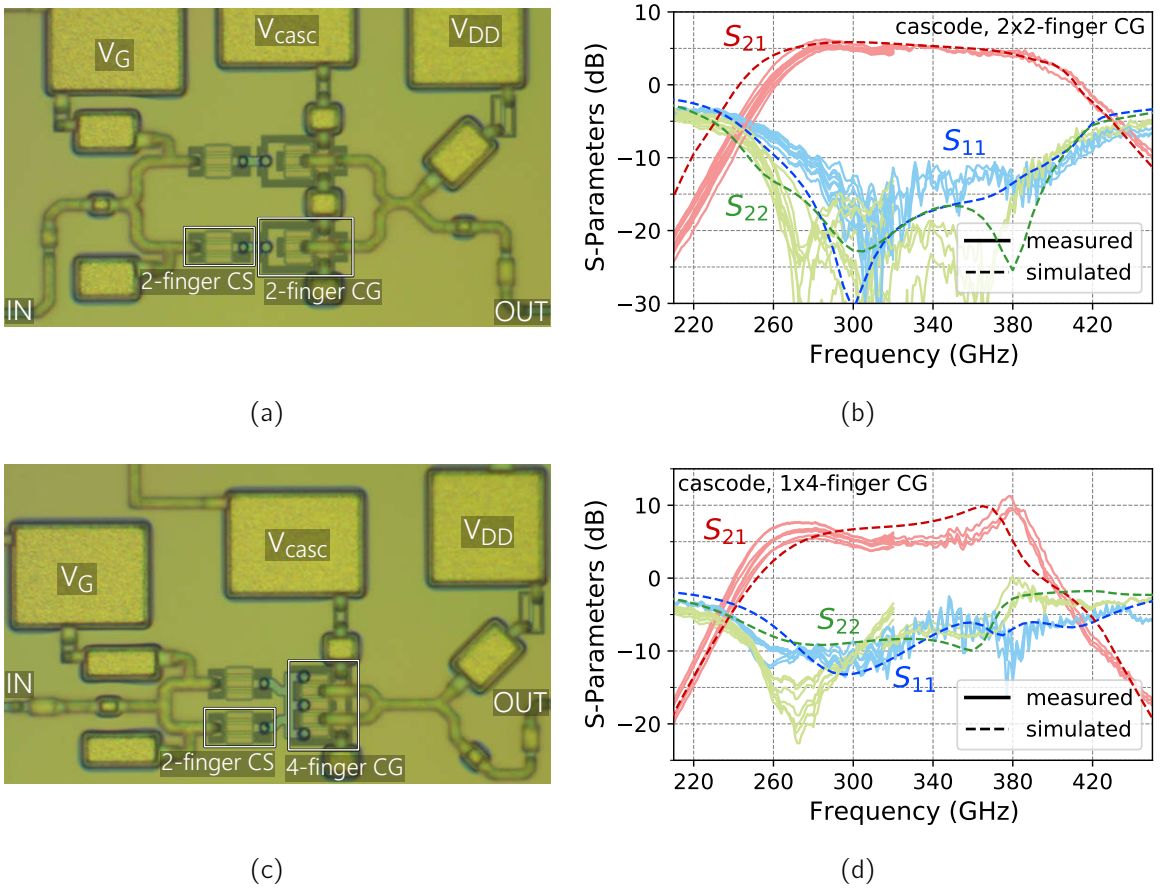


Figure 3.12: Chip photographs, and measured S-parameters of pre-matched 4-finger cascode cells. (a,b) The 4-finger cell is implemented with two parallel 2-finger CS and CG devices. (c,d) A 4-finger CG device from the PDK is used in the 4-finger cascode cell.

measured and simulated S-parameters of both cascode cells are depicted in Fig 3.12(b) and Fig 3.12(d), respectively.

While the simulation results of the cascode cell using only 2-finger devices fit to the measurement results to an excellent extend (Fig 3.12(b)), the results including the 4-finger CG device show significant deviations (Fig 3.12(d)). One could argue, that the general measured behavior is described with the 4-finger CG model in Fig 3.12(d). Yet, considering the increasing complexity of larger PA circuits—where a multitude of devices needs to be accurately modeled in cascaded as well as parallel configuration—the design uncertainty observed for the relatively simple single-stage multi-finger design in Fig 3.12(d) can lead to design failure and increased number of required design cycles. Hence, only 2-finger device models are used in this work. The modeling approach, which was used to simulated the 4-finger cascode cells depicted in Fig. 3.12, is described in detail in the following section.

3.2.2 Modeling of Compact Multi-Finger Devices

The superior performance, in terms of bandwidth and achievable gain at sub-mm-wave frequencies, of the most simple and symmetric two finger device is discussed above. As a result of this and when considering the superior accuracy of the active device models, a multi-finger modeling approach only based on 2-finger models is implemented. Since thin-film wiring is chosen for the development of compact PA cells—as described in Chapter 2—the gate and drain feeding structures of TFMSL multi-finger devices can be realized in one of the metal layers above MET1, providing a closed MET1 ground plane around the active devices, as depicted with the 4-finger TFMSL device layout in Fig. 3.13. Hence, no additional air-bridges are required and the ground connection of the middle source finger(s) is realized in the ground-plane metal MET1.

Due to the closed MET1 ground plane, multi-finger devices can be described and simulated by parallel 2-finger-transistor models in close proximity. With this approach, the 4-finger device in TFMSL environment depicted on the right in Fig. 3.13, is modeled using two parallelized 2-finger device models without gate and drain feeders. The feeding structures of the 2-finger devices are included in the EM-simulated multi-finger transistor shell and can be optimized as a part of the matching network design. Fig. 3.14 shows the planar structure of the underlying 2-finger CPW CS devices, which is composed of

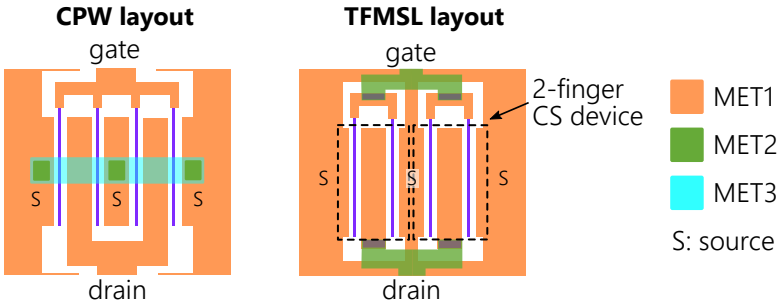


Figure 3.13: Layout of 4-finger common-source devices in CPW and TFMSL environment. Due to the closed MET1-ground plane, no air-bridge is required for the source connection in the TFMSL layout.

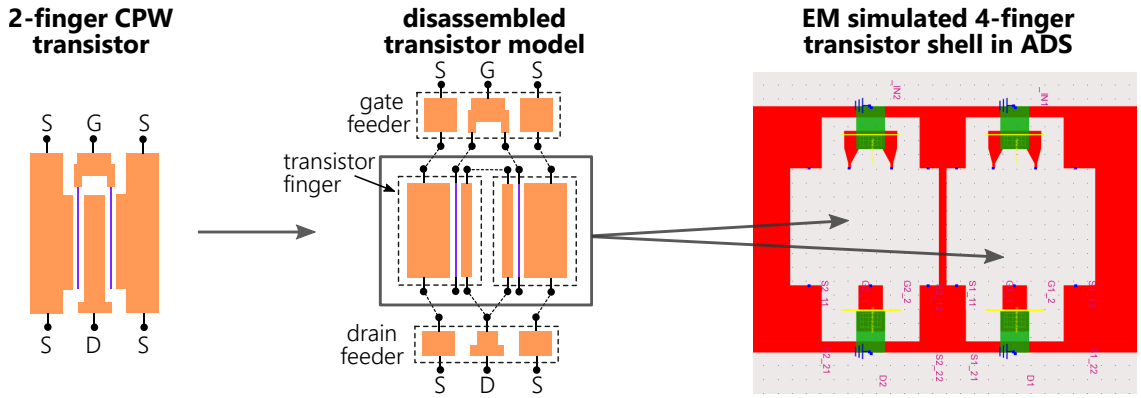
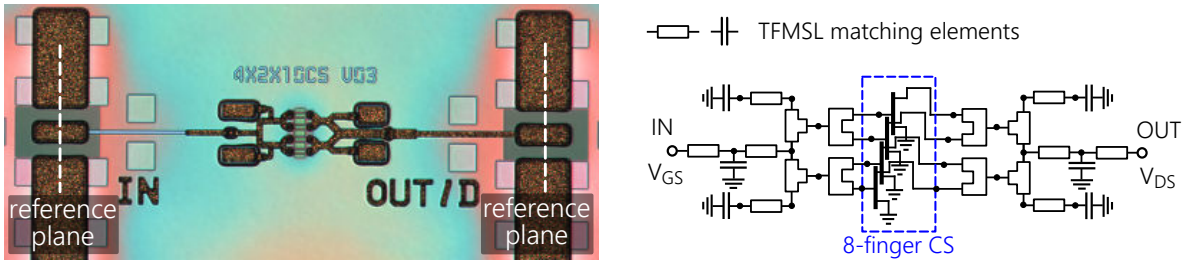


Figure 3.14: Multi-port transistor model: planar structure of a 2-finger CPW device (left), disassembled 2-finger structure including feeding and finger elements (middle), EM simulated 4-finger shell with feeding structures in ADS (right).

feeding and finger structures. Only the 2-finger transistor model without gate and drain feeding structures is used from the PDK, embedded into an EM-simulated multi-finger transistor shell. Hence, accurate in-phase feeding of multi-finger devices with more than four transistor fingers is possible, enabling a "power-bar-like" device implementation.

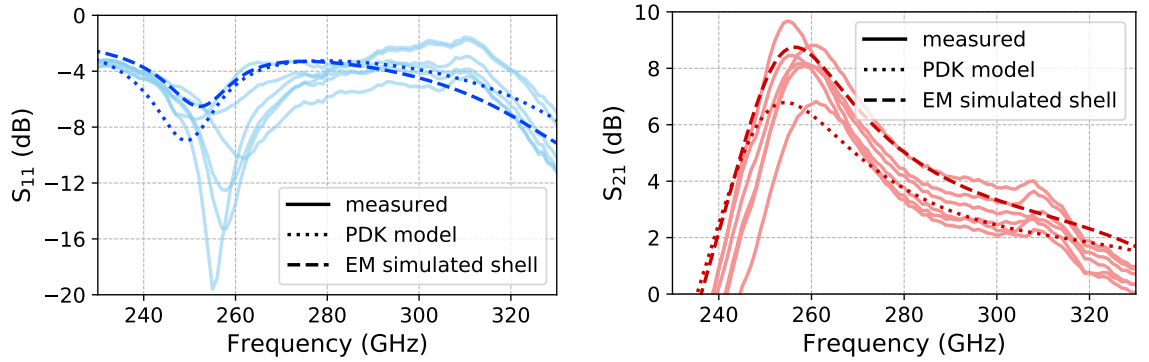
The chip photograph and schematic of a pre-matched 8-finger CS cell, which was used to verify the above described modeling approach, is depicted in Fig. 3.15. The corresponding S-parameters of the 8-finger CS cell are shown in Fig. 3.16. Depicted are the on-wafer measurement results of 10 average-performing cells of a 37-cell mapping, in order to account for RF-probe placement uncertainties as well as device spread over the wafer. Two simulation results are compared, using in both cases the same models and same reference planes for the input and output matching networks. The dotted lines in Fig. 3.16 represent the simulation using the standard 2-finger CPW model from the PDK to model the 8-finger CS transistor. The simulation based on an EM-simulated 8-finger shell and four 2-finger device models without feeding structures, is depicted with dashed lines.

While both simulations show similar performance in terms of S_{11} and S_{12} figures—which fit quite well to the measurements—the EM-simulated multi-finger shell provides an improved accuracy for the S_{21} and S_{22} S-parameters. This is mainly due to larger changes in the layout of the TFMSL drain-feeding structures, in comparison to the standard CPW layout. Fig. 3.17 shows the corresponding layout as well as reference planes of the multi-finger transistor shell. The transistor shell is simulated using ADS Momentum, including a *MET2MET3 TFMSL* at each input and output port. The inner reference plane is set to the MESA edge, where the 2-finger CS PDK structures are connected to the multi-finger shell. A total of seven ports are defined per 2-finger device, including connections to four source fingers, two gate fingers and a single drain finger. At this inner reference plane, the zero-length calibration is used in Momentum. The four input and output ports are defined at the outer edge of the *MET2MET3 TFMSL*. The implemented feed type of the TFMSL ports in Momentum is TML and the reference plane is shifted to the MET1 feeding structures, as depicted in Fig. 3.17. This way, the TFMSL feeding structures are simulated as a part of the matching network design, enabling an accurate implementation of matching elements into the feeding structures.

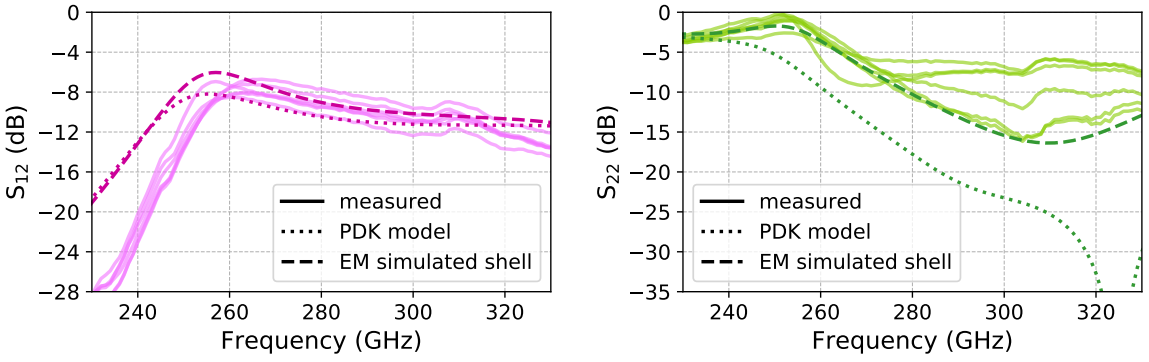


(a) (b)

Figure 3.15: (a) Chip photograph and (b) schematic of a 300-GHz pre-matched 8-finger CS test circuit.



(a) (b)



(c) (d)

Figure 3.16: Measured and simulated S-parameters of the pre-matched 8-finger common-source cell depicted in Fig. 3.15. The dotted lines represent the simulation using four parallel 2-finger PDK transistor models in CPW environment. The dashed lines represent the simulation using this work's multi-port modeling approach.

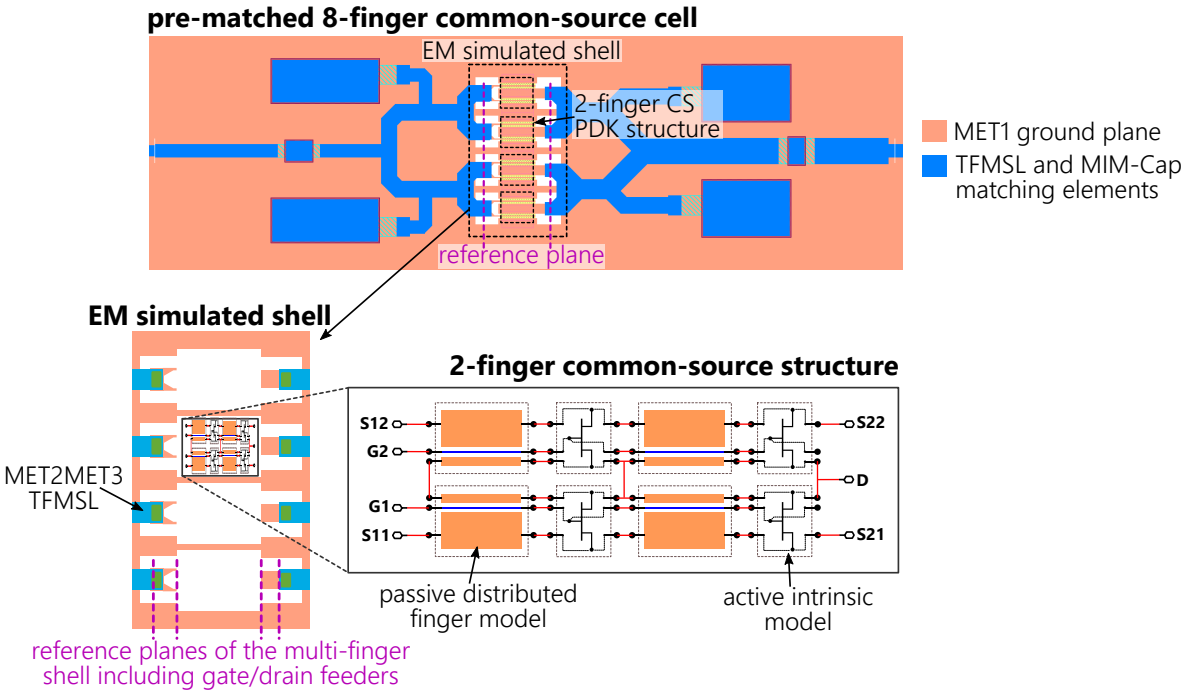
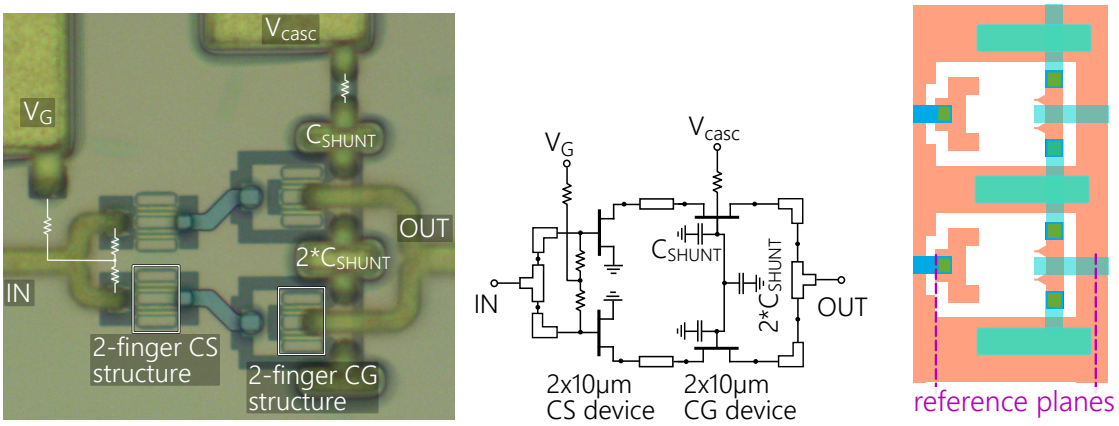


Figure 3.17: Layout and modeling approach of the pre-matched 8-finger common-source cell depicted in Fig. 3.15. The 8-finger CS transistor is modeled using a EM-simulated shell including a total of 36 ports—8 input/output ports and 7 ports for each parallel 2-finger device. Each 2-finger transistor is modeled using a symmetric 2-finger device model without feeding structures from the PDK, including two intrinsic device models per finger.

By using Momentum EM/circuit co-simulation in ADS for the development of multi-finger transistor shells, time-efficient optimization and simulation of multi-port models with more than 30 ports is possible. Implementing this modeling approach, compact multi-finger transistor cells are described with good accuracy. Further benefits are, that only a single active device model is required to describe a multitude of different multi-finger devices, which offers maximum flexibility to the designer as well as reduces the effort for multi-finger modeling significantly. Hence, only a small number of test structures needs to be fabricated and characterized, in order to provide an accurate 2-finger model in the PDK. Based on this, devices with a larger number of transistor fingers can be developed as a part of the design process for applications where larger power levels are required. This is demonstrated for more complex device layouts with the development of chip-size optimized cascode cells in the following.

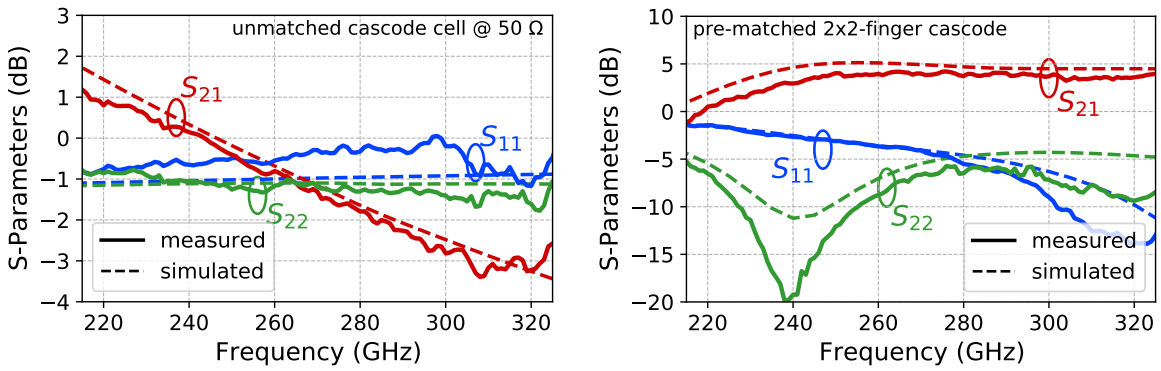
3.2.3 Development of Compact Multi-Finger Cascode Devices

To verify the design and modeling approach of using multiple parallel 2-finger devices for multi-finger cascode devices, the cascode cell depicted in Fig. 3.18(a) was developed and characterized, based on the 4-finger cascode cell discussed previously in Section 3.2.1 and shown in Fig 3.12(a). Two 2-finger CS and CG devices are parallelized in this 4-finger cascode cell, using the standard CPW layout of the CG device from the PDK. The impedance-matching network at the gate of the CG devices primarily consists of the MIM capacitors C_{SHUNT} at both sides of the CG devices, as depicted in Fig. 3.18(b).



(a) Chip photo (b) Schematic (c) EM CG shell

Figure 3.18: (a) Chip photograph, (b) equivalent circuit, and (c) EM-simulated CG shell of the 4x10-µm cascode PA cell with feeding structures. The layout of the 2-finger devices is the standard layout from the PDK.



(a) (b)

Figure 3.19: Measured and simulated S-parameters of the 4x10-µm cascode PA cell with four transistor fingers: (a) without pre-matching and (b) matched to 50 Ω.

Hence, both CG devices share a common MIM capacitor. The design considerations for the shunt capacitors at the gate of the CG devices are discussed in detail in the following section.

The parallel devices are simulated in Momentum including the feeding structures in the EM-simulated 4-finger shell. The CS devices are simulated as described in the previous subsection. For the 4-finger CG shell, the parallel MIM capacitors are included in the simulation model, as depicted with the Momentum model shown in Fig. 3.18(c). On-wafer measurements of the unmatched cascode cell in Fig. 3.18 as well as a 50-Ω input-out matched variant (not depicted in Fig. 3.18) are plotted in Fig. 3.19, showing a good agreement between measurement and simulation. A four-stage 300-GHz amplifier MMIC [52], which was developed based on this 4-finger cascode cell, is described in detail in Section 4.2.1.

Chip-Width Optimized Multi-Finger Cascode Cells In order to reduce the chip width of the 4-finger cascode cell discussed above—which permits to increase the number of parallel 2-finger devices for a specific chip width—a width-optimized 2-finger CG device layout was developed. Fig. 3.20 shows the layout of the standard 2-finger CG device layout from the PDK on the left, in comparison to the width-optimized layout variant on the right. The main changes include a reduction of the source and drain-finger width as well as a reduced spacing between the source fingers and the MET1 ground. The layout of the transistor fingers including the drain-to-source spacing, on the other hand, was kept the same.

In order to implement the width-reduced finger structure described above, the layer sequence of the gate and drain feeding structure was changed. For the standard layout variant, the gate feeder is implemented in MET1 and connected to MET3 lines at the upper and lower side—forming the depicted vertical gate bus. The drain connection is implemented as MET3 line which is crossing the MET1 gate feeder, connecting the drain finger to the drain TFMSL. Due to the depicted minimum-width and minimum-spacing design rules for the MET1 and MET3 layers—which are almost at the design rule limit for the depicted layout implementation—the layout width could not be significantly reduced without changing the layer sequence. Therefore, the width-optimized variant is implemented with the depicted non-stop MET3 gate bus and extended MET1 drain finger, permitting an overall width reduction of almost 40 % from 24 µm to 15 µm.

Based on the width-optimized CG device layout depicted in Fig. 3.20, the 4-finger and 8-finger cascode cells shown in Fig. 3.21 and Fig. 3.22 have been implemented. To further reduce the chip width of the cascode cells, shunt capacitors are implemented at only one side of each 2-finger CG device. The 2-µm-wide MET1 stripes between the parallelized CG devices in Fig. 3.21 is required to provide a closed MET ground plane and ensure the symmetry of the 2-finger device structures. This is necessary to implement the simulation approach of only using symmetric 2-finger models as described above.

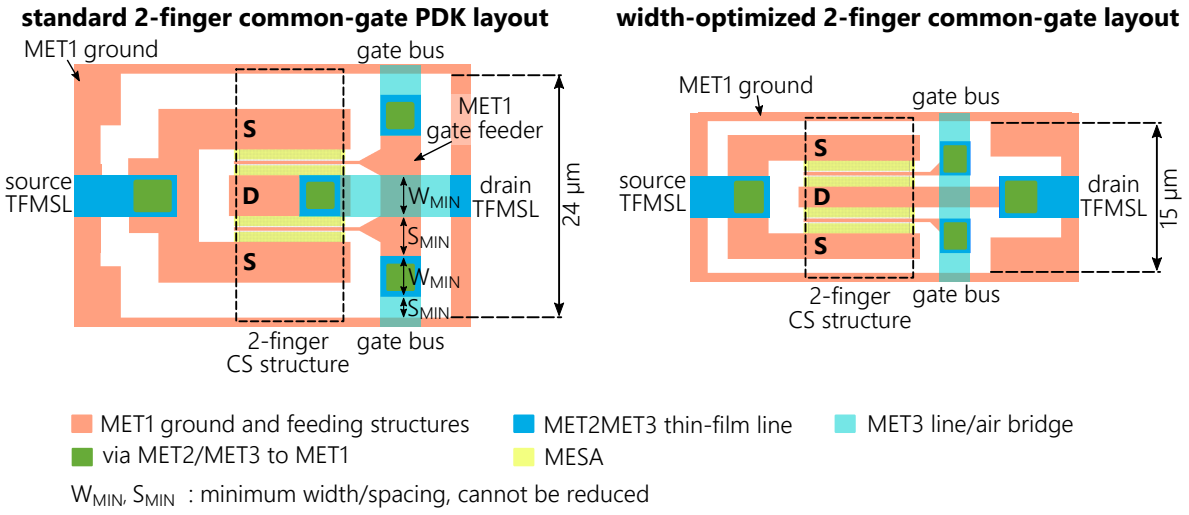


Figure 3.20: Layout of 2-finger CG devices. The standard 2-finger CG layout from the PDK is depicted on the left. A width optimized layout variant is shown on the right.

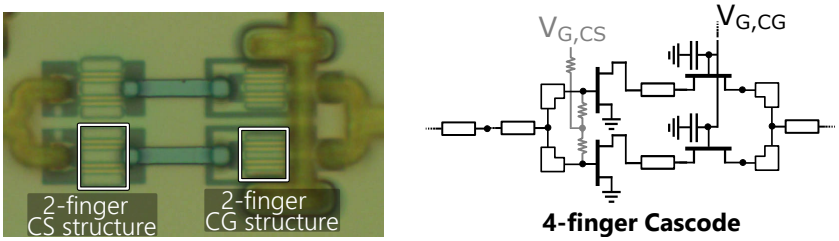


Figure 3.21: Chip photograph and equivalent circuit of a 4-finger cascode cell with feeding structures, implemented with the width-optimized CG-device layout depicted in Fig. 3.20.

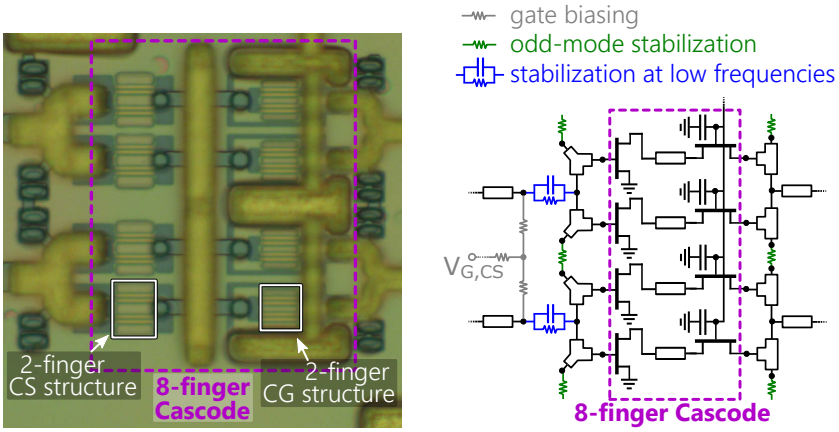
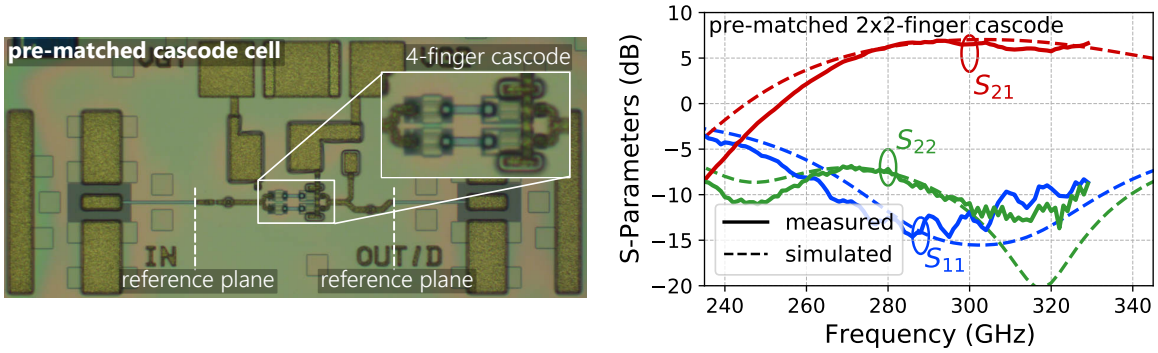


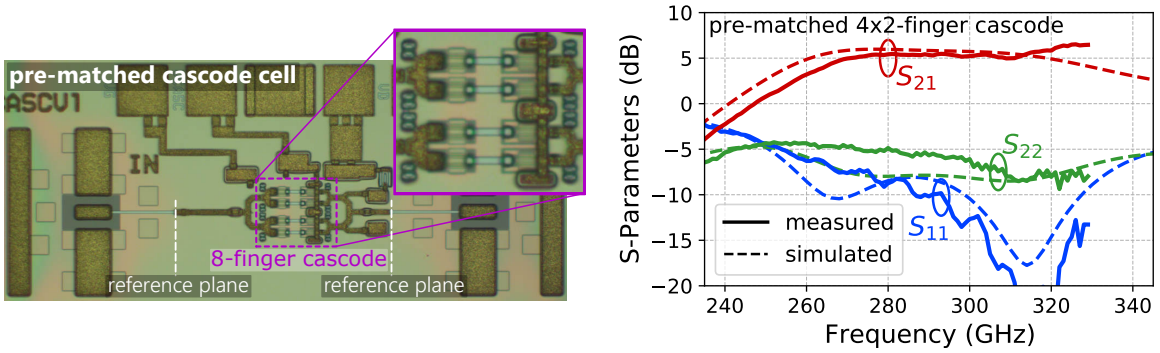
Figure 3.22: Chip photograph and equivalent circuit of an 8-finger cascode cell with feeding structures, implemented with the width-optimized CG-device layout depicted in Fig. 3.20.



(a) (b)

Figure 3.23: (a) Chip photograph, and (b) measured and simulated S-parameters of a pre-matched 4-finger cascode, based on the cascode cell shown in Fig. 3.21.

By embedding the two finger CS and CG models in the fully EM-simulated 8-finger cascode shell, stabilization elements can be implemented in the multi-finger transistor shell, as depicted in Fig. 3.22. The chip photographs of pre-matched 4-finger and 8-finger cascode cells including on-wafer measurement results are depicted in Fig. 3.23 and Fig. 3.24, respectively. The measured small-signal gain of the compact cascode devices is in the range of 5 to 7 dB. Good agreement between measurement and simulation is achieved, despite major changes to the layout of the CG devices. This, however, demonstrates the



(a) (b)

Figure 3.24: (a) Chip photograph, and (b) S-parameters of the pre-matched 8-finger cascode cell, based on the cascode cell shown in Fig. 3.22.

advantages of the implemented modeling approach—providing maximum flexibility for the development of compact multi-finger devices during the design process, customized for the requirements of specific circuit implementations.

3.3 Comparison of Device Configurations

The modeling of multi-finger CS and cascode devices is discussed in the previous section. The figures which have been considered in the discussion up to now, however, are only small-signal characteristics like gain and bandwidth, respectively. This section is, therefore, dedicated to the evaluation of the large-signal performance of the multi-finger devices discussed above. The takeaways of this evaluation were applied in the PA circuit design described in Chapter 4.

The motivation for the development of the above described compact cascode cells is the reduction of the required chip width and, hence, an increased output power per total chip width. Yet, as can be seen from the chip photographs in Fig.3.25, the chip width required for the 8-finger cascode implementation is almost doubled in comparison to the 8-finger common-source device. This leads to the conclusion, that the cascode configuration needs to deliver almost twice as much output power as a CS transistor, in order to achieve the same output-power level per required chip width for a given number and width of transistor fingers. The output power considered here is referenced to the device level, not considering the required impedance transformation as well as losses in the power-combining network.

As discussed in Section 2.2, devices in cascode configuration can provide larger levels of small-signal gain in comparison to CS transistors. Under large-signal condition, on the other hand, both the CS and the CG transistor must contribute to the output voltage swing, in order to prevent soft compression and increase the output-power level. In order to identify the appropriate geometry of the cascode cells for large-signal operation, two design parameters are considered: the size of the shunt capacitors C_{SHUNT} at the CG transistor and the length L_{MSL} of the TFMSL interconnection between the CS and the CG device. These parameters can be varied—at least in a certain range—without increasing the required width of the cascode-cell layout.

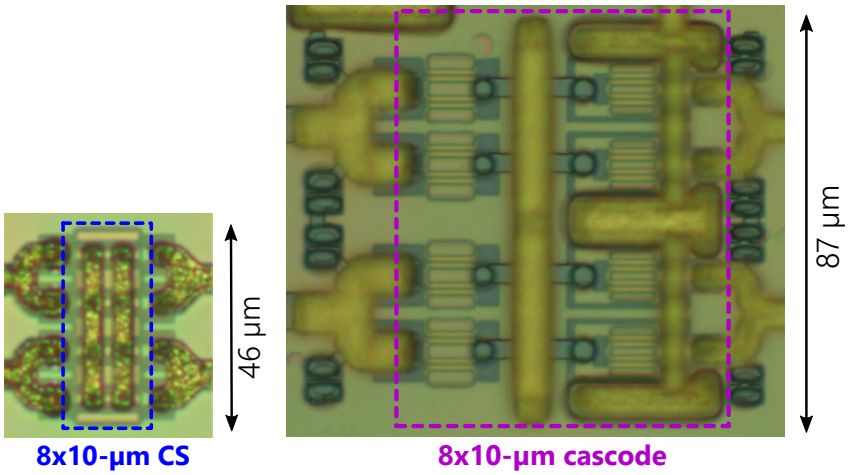


Figure 3.25: Chip photographs of (a) an 8-finger common-source device and (b) an 8-finger cascode device. The cascode is implemented with the width-optimized CG-device layout. The required chip width of the cascode cell is almost doubled in comparison to the CS cell.

Since the output power on device level scales with the number of transistor fingers—and, therefore, the relative output-power level is not dependent on the absolute number of gate fingers—only 2-finger devices are considered in the following. The finger width, which is used in this discussion, is 10 µm and the benchmarks to measure the cascode performance is the 7-dB MSG as well as the 4.5-dBm OP_{3dB} 3-dB gain compression power of a CS device with 10-µm finger width.

Fig. 3.26 shows the simulated MSG/MAG and stability factor of a 2x10-µm cascode for different values of the considered design values L_{MSL} and C_{SHUNT}. For shunt-capacitor values larger than 200 fF, the cascode is only conditionally stable around 300 GHz and the MSG is independent of the length L_{MSL}, at least in the considered range of up to 40 µm. In this case, the MSG of the cascode at 300 GHz is 15 dB, compared to the 7-dB MSG of a CS transistor. For $C_{SHUNT} < 200$ fF, the cascode is unconditionally stable

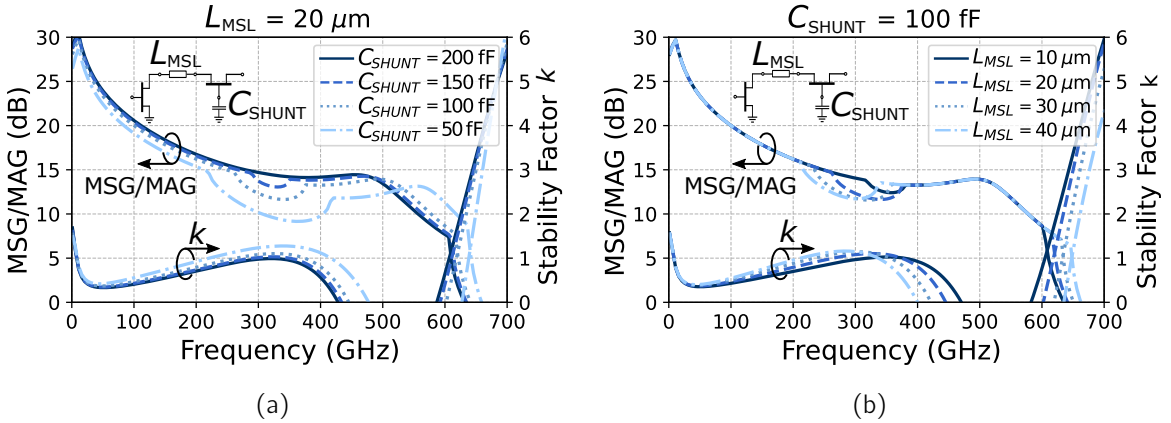
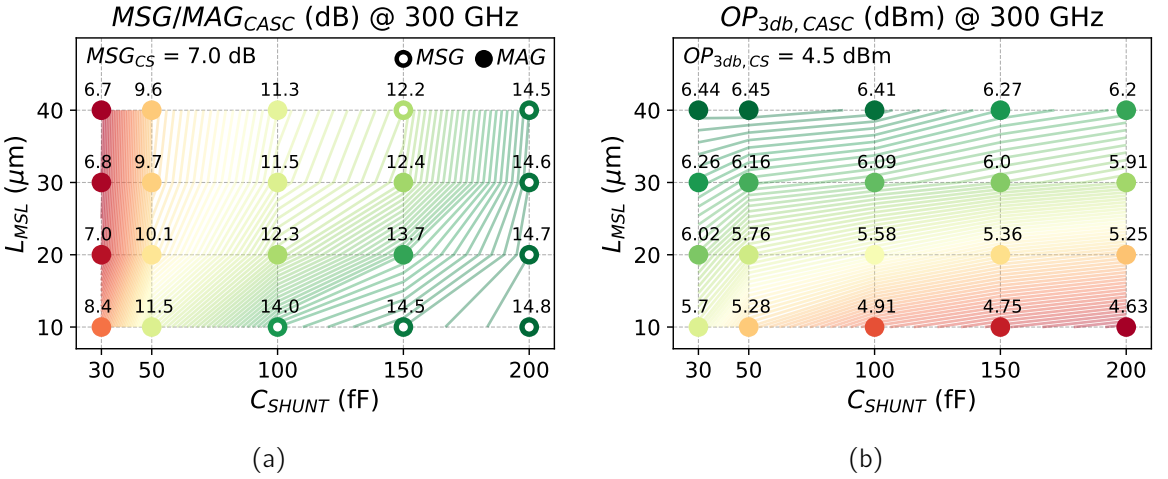


Figure 3.26: Simulated MSG/MAG and stability factor k of a 2-finger cascode with 10-µm finger width: (a) for different C_{SHUNT} values at $L_{MSL} = 20$ µm, and (b) for different L_{MSL} values at $C_{SHUNT} = 100$ fF.



(a) (b)

Figure 3.27: (a) Simulated MSG/MAG and (b) simulated OP_{3dB} 3-dB gain compression output power of a 2-finger cascode with 10-µm finger width for different values of C_{SHUNT} and L_{MSL} at 300 GHz. The colors in (a) and (b) are coded with the depicted discrete values of the corresponding gain and output-power levels.

over a certain frequency band around 300 GHz, depending on the values of L_{MSL} and C_{SHUNT}.

The maximum stable and available gain at 300 GHz can also be seen in Fig. 3.27, which shows the simulated MSG/MAG values as well as the OP_{3dB} 3-dB gain compression power for a 2x10-µm cascode at 300 GHz. The length of the microstrip line L_{MSL} is swept from 10–40 µm, and the range of C_{SHUNT} is 30–200 fF. For large values of C_{SHUNT} and a short interconnection between the CS and CG device ($L_{MSL} = 10$ µm), the achieved output power performance of 4.63 dBm is found to be not significantly improved compared to a 2x10-µm CS single device, which delivers a maximum OP_{3dB} of 4.5 dBm at 300 GHz. However, by optimizing the values of C_{SHUNT} and L_{MSL} within the considered range, the output power can be increased by 1.8 dB ($OP_{3dB} = 6.44$ dBm) in simulation—at a significantly reduced gain level.

The below-2-dB improvement of the simulated output power performance, on the other hand, complies with the prospects and limitations of stacked HEMT devices described in Section 2.2. This theoretical discussion of stacked HEMT devices suggests, that due to the below-unity current gain of the CG devices, the achievable output-power improvement of the double-stack configuration is limited to around 1 dB for an f_T value around 500 GHz. Since the available and in this simulation considered large-signal model assumes an f_T above 600 GHz, the slightly higher simulated output-power improvement of the stacked cascode is reasonable. Despite the unrealistically high cutoff frequency assumed here, the limited improved large-signal performance is observed. By doubling the DC supply voltage of the cascode and, hence, doubling the DC power consumption P_{DC}, the output power is only increased by a factor of 1.5 in simulation.

Based on these simulation results, Tab. 3.2 gives a summary and comparison of the 8-finger common-source and cascode devices depicted in Fig. 3.25. This comparison includes the L_{MSL} and C_{SHUNT} values of the maximum-gain as well as maximum-output-power cases of the cascode configuration. While there are some better trade-off choices

Table 3.2: Comparison of multi-finger cascode and common-source device performance at 300 GHz

	Type of device configuration		
	8x10-µm CS	**8x10-µm cascode** max-gain case: $C_{SHUNT} = 200\,fF$, $L_{MSL} = 10\,\mu m$	**8x10-µm cascode** max-P_{OUT} case: $C_{SHUNT} = 30\,fF$, $L_{MSL} = 40\,\mu m$
MSG/MAG (dB)	7.0 (MSG)	14.8 (MSG)	6.7 (MAG)
OP$_{3dB}$ (dBm)	10.5	10.6	12.4
Chip width (µm)	46	87	87
OP$_{3dB}$ per Chip width (mW/mm)	244	132	200
P$_{DC}$ (mW)	32	64	64

than the listed maximum-gain case—possibly providing both large gain levels as well as improved output-power performance—the output power per required chip width is in any case inferior for the cascode, when compared to the CS device. Even though improved power levels are achieved in simulation for the cascode, the chip width is almost doubled in comparison to the multi-finger CS device, limiting the usefulness in compact PA cells. It further needs to be noticed, that the data depicted in Fig 3.27 is considering the cascode performance only at 300 GHz. For the implementation of broadband cascode PA cells, the design parameters C_{SHUNT} and L_{MSL} and their impact need to be considered over the full frequency band of interest.

3.4 On-Chip Load Pull for Large-Signal Characterization of Devices at THz Frequencies

In order to reduce the number of needed design cycles and thus the time as well as the costs for developing complex MMICs, accurate simulation models of active circuit components are required. However, since the impact of the on-wafer measurement setup on the measurement result increases at the upper mm-wave frequency band—due to RF-probe coupling, for instance—the accuracy of single device measurements is limited. Hence, the intrinsic model extraction is typically performed at frequencies below 150 GHz [78, 118] and extrapolated for higher frequencies. To evaluate the active device models at frequencies well above this frequency range where the extraction was done, pre-matched single devices can be used to accurately verify the small-signal behavior at different bias conditions [42]. Load-dependent large-signal device characterization, on the other hand, is a major obstacle in the development and validation process of large-signal transistor models for mm-wave and sub-mm-wave frequency applications.

In Section 3.1, a 40-GHz load-pull system is used to evaluate the large-signal performance of mHEMT devices at different biasing conditions. Such active—but also passive—load-pull [84, 105] is typically used at the lower mm-wave frequency regime for large-signal device characterization and model verification. The magnitude of the load reflection coefficient ($|\Gamma_L|$) of the optimum load impedances for maximum gain, power, and efficiency of sub-mm-wave devices, however, is typically greater than 0.6, assuming a 50-Ω reference impedance. Due to the high losses of RF probes at frequencies beyond 100 GHz, these required reflection factors are not feasible with off-chip passive load tuners. Therefore, active load-pull systems have been introduced recently, which are

theoretically able to permit load-pull characterization at sub-mm-wave frequencies [23]. Yet, the limited availability of high-power amplifiers to realize the required $|\Gamma_L|$ values around 300 GHz, for instance, is still a major issue.

The required sub-mm-wave load-pull impedances, on the other hand, can be realized on chip with a tunable passive matching circuit. Using tunable impedance matching networks for the in-situ characterization of source and load mismatch with regard to the noise figure and maximum output power of single transistors has been demonstrated at the mm-wave frequency range below 200 GHz [11, 24, 43]. When further increasing the frequency of operation to the upper mm-wave frequency band around 300 GHz, the limited available input power on RF-probe level becomes an issue even for the realization of passive on-chip load pull. The available input drive at 300 GHz is typically limited to values below 0 dBm, for example. This is not enough to characterize a single device with 3 to 5 dBm output power in large-signal operation, when considering the additional losses of the RF pads and the feeding lines. Therefore, additional circuit elements such as integrated amplification stages are required to compensate for the limited input power. The realization of such an on-chip load-pull MMIC was investigated in this thesis [54], with the intend to further provide means for the evaluation of the underlying mHEMT technology under large-signal conditions around 300 GHz. The topology and characterization of the 300-GHz load-pull circuit and its subcomponents is described in the following sections.

3.4.1 On-Chip Load-Pull Circuit Topology

The block diagram of the circuit topology which was investigated for on-chip load-pull measurements is shown in Fig. 3.28. The corresponding chip photograph of the realized MMIC is shown in Fig. 3.29. An important requirement for this characterization approach to work is an accurate on-wafer calibration, which is necessary to characterize the depicted subcircuits. This is required for the later de-embedding of the output matching network. In order to ensure the accuracy of the performed measurements, advanced reference calibration methods with 150-µm port extension are used [98]—and the reference plane is set to the input and output of the port extension of the investigated circuits, as shown in Fig.3.29.

The input of the DUT is matched to 50 Ω (IMN) for small-signal operation, and a variable load impedance is presented to the output of the DUT, realized with a tunable output matching network (OMN). The limited available input power is a major issue

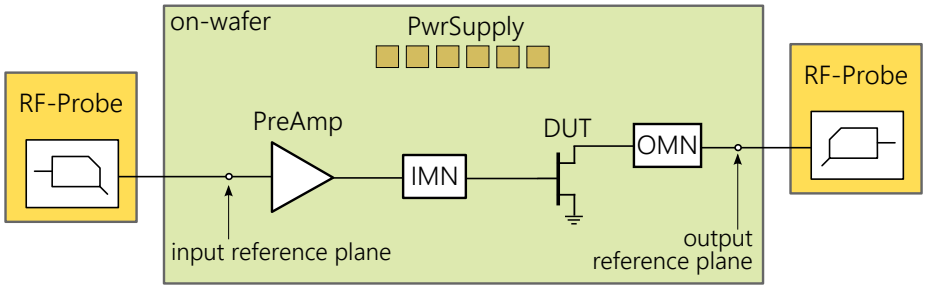


Figure 3.28: Block diagram of the integrated circuit topology for on-chip load-pull characterization.

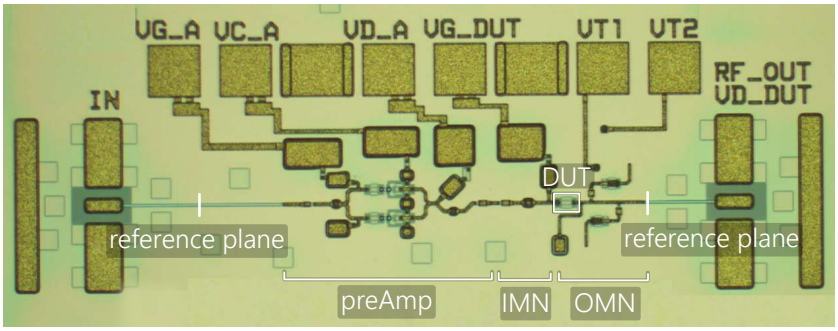


Figure 3.29: Chip photograph of a 2x15-µm prematched DUT with tunable output matching network and integrated preamplifier. The required chip area is 1200 µm x 400 µm.

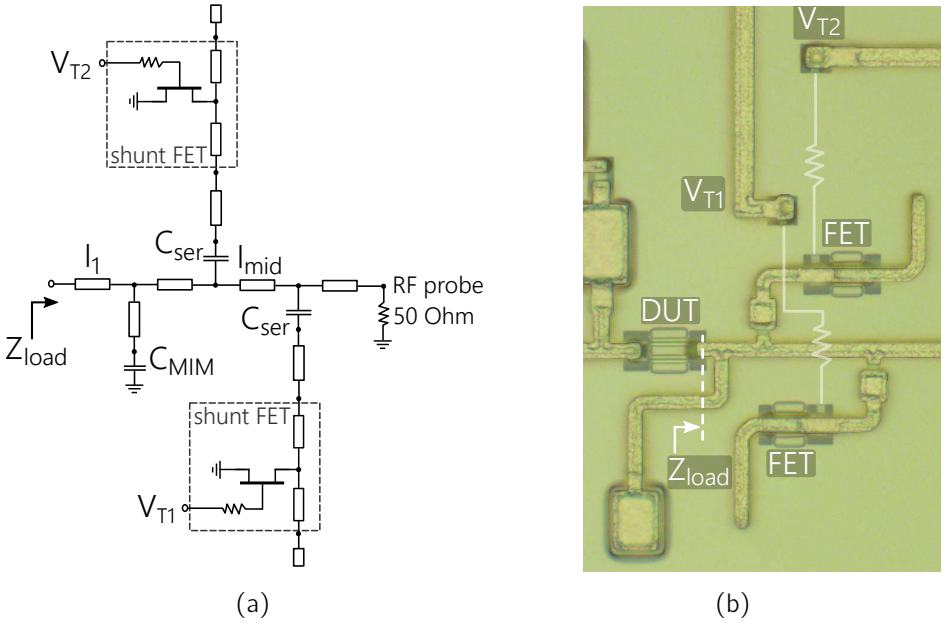


Figure 3.30: (a) Schematic of the tunable output matching network with two shunt-FET stubs and one capacitively terminated stub. (b) Chip photograph of the OMN with 2x12-µm DUT.

for large-signal characterization of single devices and amplifier circuits at sub-mm-wave frequencies, as described above. The available scalar setup for large-signal measurements provides up to −2 dBm input power at RF-probe level around 300 GHz. Hence, in order to increase the power level at the input of the device under test (DUT), a broadband preamplifier with sufficient output power was designed and integrated. The design approach for this amplifier cell is described in detail in the Section 3.2.

The schematic of the implemented output matching network and the chip photograph of a 2x12 µm DUT with the tunable matching network are shown in Fig. 3.30(a) and Fig. 3.30(b), respectively. Two open-circuit stubs with shunt-FETs are used to realize a tunable load impedance. This circuit topology was chosen based on extensive simulations, considering the achievable tuning range as well as the required linear behavior of the network. The simulated load impedances of a single-stub network, with a 2x10-µm shunt FET and 5-µm wide T-junction, is shown in Fig. 3.31(a). The drain potential of the shunt FET is floating, while the tuning voltage V_T is swept from below threshold up to voltages above $g_{m,max}$. At tuning voltages below pinch-off, the capacitive behavior

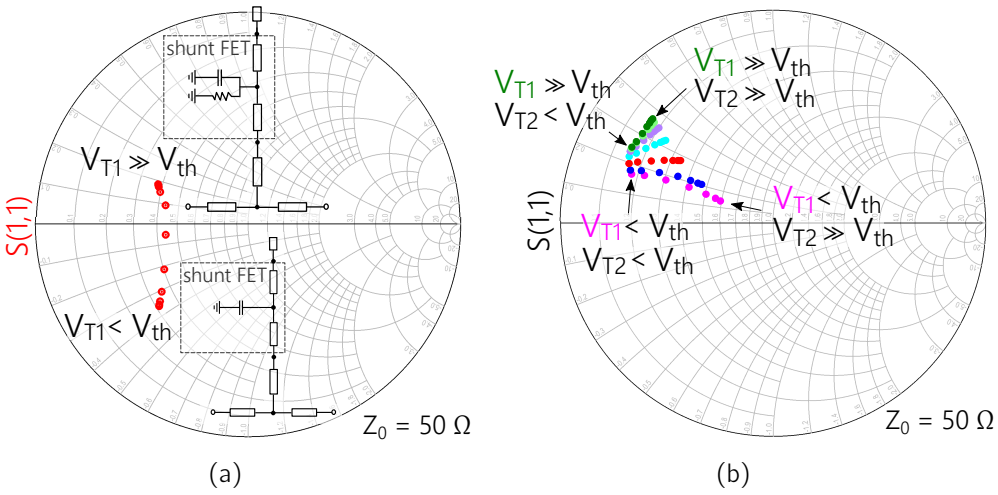


Figure 3.31: (a) Simulated S_{11} of a single tunable open-circuit stub with 2x10-µm shunt-FET. (b) Simulated two-dimensional load impedance range of the tunable OMN.

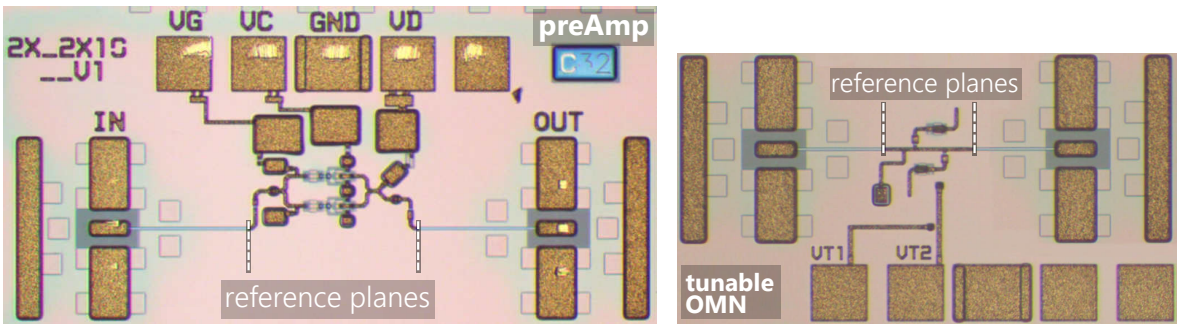
of the open-circuit stub is dependent on the length of the microstrip lines and the width of the shunt FET, which is increasing the capacitance and electrical length of the stub. The inductive behavior of a resistively terminated stub is observed for highly conductive states of the shunt FET ($V_T \gg V_{th}$), dependent on the on-state resistance of the shunt FET and the electrical length of the microstrip line between T-junction and shunt FET.

The simulated load impedances of the full output matching network with two of the described tunable open-circuit stubs are shown in Fig. 3.31(b). The electrical length of the microstrip line between the two tunable stubs (l_{mid}) defines the phase shift, which enables the two-dimensional load tuning with two control voltages. The capacitively terminated stub, depicted in Fig. 3.30, is used to realize the required inductive load impedances at 300 GHz in the upper left segment of the Smith chart. By varying the length l_1 of the line at the output of the DUT, the phase of the tunable impedance range can be adjusted. Since the drain supply voltage of the DUT is applied with the RF-probe, the series capacitors C_{SER} are implemented to decouple the drain bias voltage of the shunt FETs from the DUT.

3.4.2 On-Chip Load-Pull Characterization

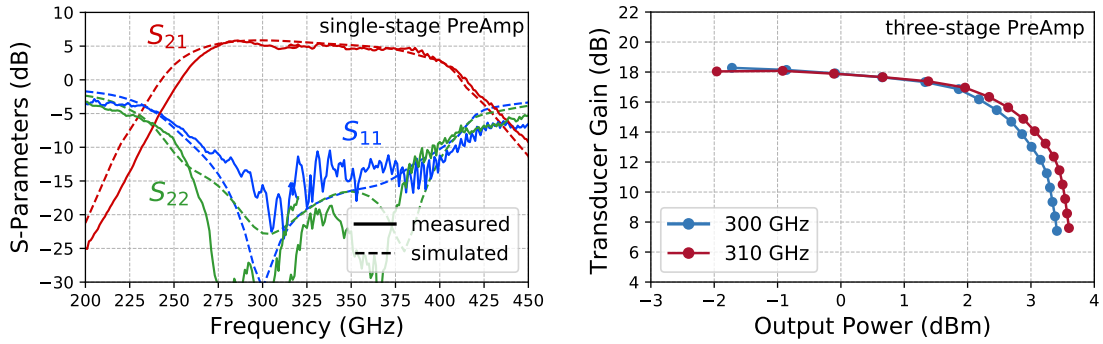
In order to determine the delivered output power of the DUT at a given load impedance, the tunable OMN in Fig. 3.29 needs to be characterized and de-embedded. Furthermore, it must be ensured that the integrated preamplifier does not impact the overall power measurements—in terms of gain compression, for example.

Fig. 3.32(a) shows the chip photograph of the integrated cascode cell for on-wafer characterization, integrating two parallel 2-finger cascode devices with 10-µm finger width. The measured S-parameters of the preamplifier are depicted in Fig. 3.33(a), featuring better than 12-dB input and output return loss and 5-dB small-signal gain over the frequency band of 275 to 380 GHz. Power-sweep measurements of a three-cascode-stage circuit variant are shown in Fig. 3.33(b), depicting the measured transducer gain vs. measured output power at 300 and 310 GHz. This three-stage version was used for



(a) (b)

Figure 3.32: Chip photographs of (a) the cascode preamplifier cell and (b) the tunable OMN for on-wafer characterization.



(a) (b)

Figure 3.33: (a) Measured S-parameters of the cascode amplifier cell depicted in Fig. 3.32(a). (b) Measured gain vs. output power of a three-stage amplifier version of the preamplifier cascode cell depicted in Fig. 3.32(a).

the large-signal characterization due to the limited available input power and in order to ensure enough gain to drive the amplifier into saturation. The measured OP_{1dB} of the three-stage cascode cell is at 2 dBm, showing the required good linearity for integration as linear preamplifier and delivering input-power levels up to the range of 1 dBm at DUT level.

The load impedance presented to the DUT and the losses in the OMN at low power levels can be determined and de-embedded with the measured S-parameter data of the OMN. By performing additional large-signal measurements of the tunable OMN, the linearity of the OMN can be verified, which is important to ensure that the losses in the OMN are independent of the power level. In addition to the preamplifier, test circuits with only the described tunable OMN have been fabricated and characterized at 300 GHz. The chip photograph of the tunable OMN for on-wafer characterization is depicted in Fig. 3.32(b) and the measured tunable load-impedance range of the OMN at 300 GHz is shown in Fig. 3.34(a). The tuning voltages are swept from -0.6 V to 0.9 V with a 0.3-V step size.

On-wafer scalar power measurements of the tunable OMN have been carried out for the highlighted load impedances in Fig. 3.34(a), up to the maximum available source power of -3 dBm. The whole setup was calibrated to the probe-tip of the RF probes

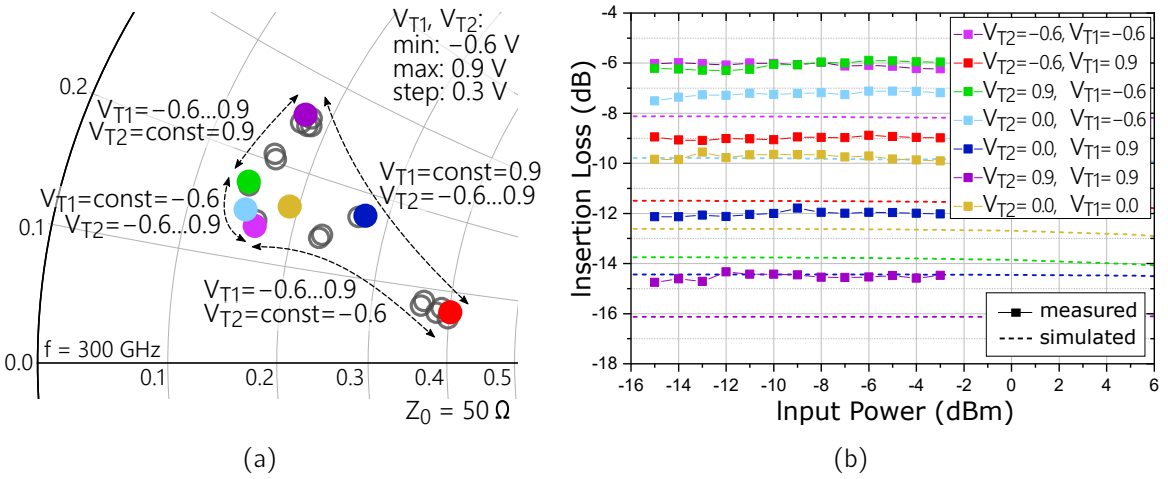


Figure 3.34: Measurement results at 300 GHz of the tunable OMN depicted in Fig. 3.32(b): (a) measured load-impedance range and (b) scalar measurement of the insertion loss vs. input power.

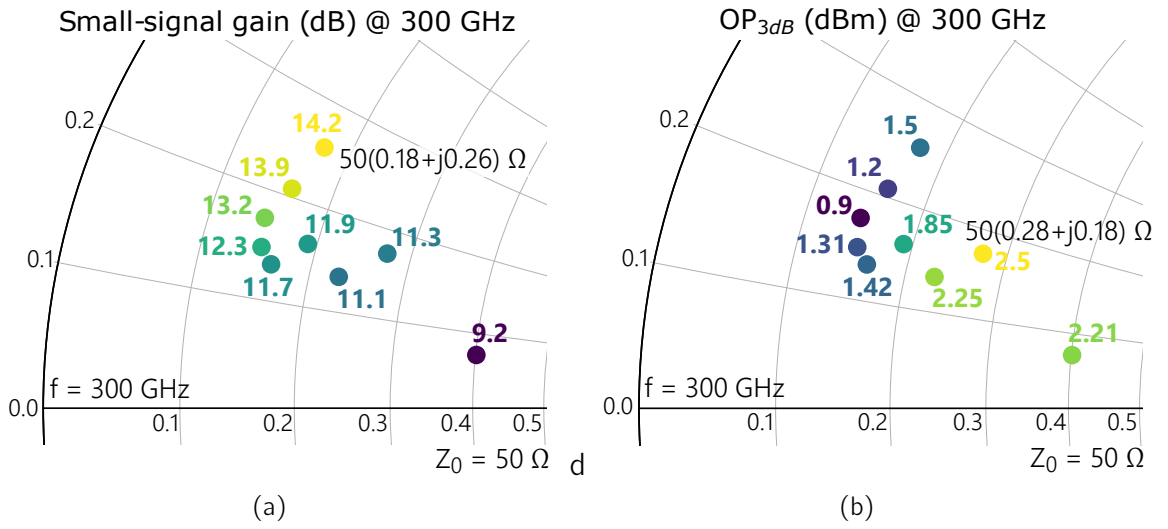


Figure 3.35: (a) Measured 300-GHz small-signal gain after de-embedding to DUT level. (b) Measured 300-GHz OP_{3dB} after de-embedding to DUT level.

performing a thru-reflect-line (TRL) calibration, using an impedance standard substrate (ISS). The port extension of the RF-pads is then de-embedded in a later processing step, in order to adjust the reference plane of the power measurement to the S-parameter measurements.

The results of the measured power sweeps are depicted in Fig. 3.34(b), showing a good linearity above −10 dBm input power. Due to the high losses of the tunable OMN and hence low output-power level, the accuracy of the power measurement at lower input power is limited by the accuracy of the power meter. Further, mismatch errors of the scalar power measurements have to be taken into account [8]. Due to the limited available source power, the linearity of the OMN could only be verified up to an input-power level of −3 dBm. Simulation results, however, show a good linearity up to power levels exceeding 5 dBm, as depicted in Fig 3.34(b). Since the fabricated active devices do

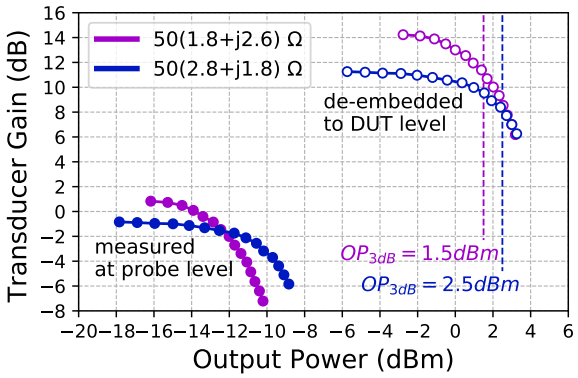


Figure 3.36: Measured 300-GHz transducer gain vs. measured output power before and after OMN de-embedding. Depicted are the results for the two load impedances for maximum SS gain $50 \cdot (1.8 + j2.6)\,\Omega$ and maximum $OP_{3\mathrm{dB}}$ $50 \cdot (2.8 + j1.8)\,\Omega$.

not perfectly match the simulation model, an offset between the measured and simulated power sweep results is observed due to mismatch errors at the corresponding bias points of the shunt-FETs. Based on the good agreement of the power measurement with the performed S-parameter measurements and the simulated linearity at input-power levels above -3 dBm, the OMN is presumed to be linear and is de-embedded with the measured S-parameter data in the following.

The power measurements of the full on-chip load-pull MMIC depicted in Fig. 3.29, including a 2x15-µm DUT, have been carried out at 1-V drain-source voltage and 450 mA/mm. The measured small-signal gain (preamplifier + DUT) as well as the delivered output power of the 2x15-µm DUT, measured at 3-dB gain compression, is shown in Fig. 3.35 for the impedance range depicted in Fig. 3.34(a). A maximum gain of 14.2 dB was measured for a 50·(0.18+j0.26)-Ω load impedance—while at 3-dB gain compression, a maximum output power of 2.5 dBm was measured into a 50·(0.28+j0.18)-Ω load impedance. The corresponding transducer gain vs. output power curves—before and after de-embedding the OMN losses—are depicted for the maximum-SS-gain and maximum-$OP_{3\mathrm{dB}}$ load impedances in Fig. 3.36.

Discussion To compare these results with the simulation, the de-embedded $OP_{3\mathrm{dB}}$-contour points shown in Fig. 3.34(a) are plotted in Fig. 3.37 against the $OP_{3\mathrm{dB}}$ contours of the available large-signal transistor model. To account for the scalar measurement setup, the ADS load-pull simulation was conducted using a CST model of the DUT input-matching network and a 50-Ω input source impedance. The power gain, which is considered in the calculation of the depicted $OP_{3\mathrm{dB}}$ contours, is the transducer power gain.

The simulated load impedance for maximum output power at 3-dB gain compression is $50 \cdot (0.32 + j32)\,\Omega$, which is not within the tuning range of the measured output matching network. Judging from the measured $OP_{3\mathrm{dB}}$ points depicted in Fig. 3.37, the optimum load-impedance needs to be assumed at the high-impedance load range which is observed in simulation. The absolute measured power level is approximately 2 to 3 dB below the simulated values, which is a known issue of the available large-signal models. Assuming a simple parallel R-C equivalent circuit for the output of the DUT, the corre-

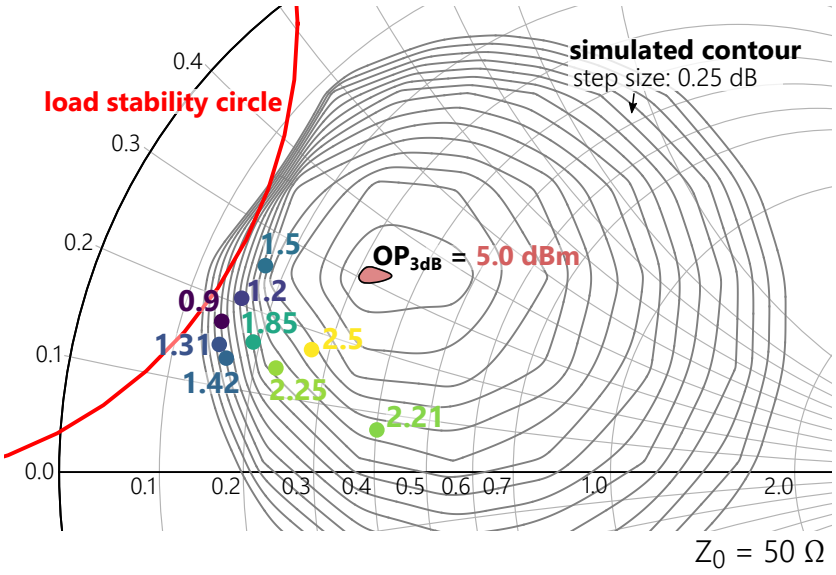


Figure 3.37: Measured OP_{3dB}-contour points in comparison to simulation at 300 GHz. The ADS load-pull simulation was conducted using a CST model of the DUT input-matching network and a 50-Ω input source impedance. The power gain, which is considered in the calculation of the depicted OP_{3dB} contours is the transducer power gain.

sponding simulated Cripps load is $R_{opt} = 32\,\Omega$. This corresponds to a normalized load impedance of $R_{opt,mm} = 0.96\,\Omega \cdot mm$. A similar Cripps load of $R_{opt,mm} = 1.125\,\Omega \cdot mm$ was measured in the very comparable 50-nm gate-length mHEMT technology used in [115]. The maximum gain was measured for a 50·(0.18+j0.26)-Ω load impedance, which corresponds to the impedance range close to the simulated load stability circle. Due to the narrow output-power contours in this impedance range, the impact of measurement uncertainties—caused by the RF-probe placement, for example—is particularly high.

The measurement results shown above demonstrate, that on-chip load pull is feasible at THz frequencies with the implemented circuit topology. Based on these results—considering the simulation and measurement data depicted in Fig. 3.37 as well as the discussion above—the load targets of the PA MMICs described in Chapter 4 have been chosen. Yet, to verify the simulation on a quantitative level, the measured data needs to be extracted and averaged of multiple cells, which was not done here. The tunable load impedance range can be increased by combining the measurement results of multiple tunable OMNs with overlapping impedance locus into a single power contour plot, which can also be used to verify the results at the overlapping impedance range. Furthermore, due to the large bandwidth of the integrated preamplifier, a broadband characterization of the DUT around 300 GHz is feasible.

Hence, the described approach can be used as straight-forward input for circuit design, at frequencies where no load-pull system is available. The best accuracy, however, can only be provided by active load-pull setups, which have shown significant process in recent years [23]. The main bottleneck at 300 GHz, is up to date the lack of broadband high-power amplifiers with sufficient output-power levels significantly above 10 dBm. The implementation in THz measurement equipment is, therefore, a major application of the developed power amplifiers described in the following.

3.5 Discussion and Conclusion on Chapter 3

As a major part of the development of chip-size optimized 300-GHz PA circuits, single-device characteristics as well as the modeling, simulation, and characterization of transistors with up to 8 transistor fingers have been investigated and evaluated.

To increase the power-density on device level, extended-recess transistors and their corresponding DC, RF, and large-signal characteristics have been evaluated experimentally. By increasing the etching duration of the recess-processing step from 40 s to 60 s, the off-state breakdown voltage at 10 mA/mm gate current is increased from 2.4 V to 4.0 V. Since the 60-s recess showed only moderately deteriorated key device figures such as $I_{D,max}$ and R_D by significantly improved intrinsic gain $g_{m,max}/g_{DS}$ values, this variant was chosen as new standard for the IAF-mHEMT technology, improving the intrinsic gain by a factor of 1.2. For the further increased 80-s recess, on the other hand, only slightly improved breakdown behavior by notably decreased saturation current and drain resistance was observed. With the improved breakdown voltage of the 60-s variant, the operation of the mHEMT devices at 2-V drain-source voltage yields a significant improvement of the power density from 150 mW/mm to 380 mW/mm, in comparison to the 1-V biasing condition. Yet, in order to operate the mHEMTs at increased voltage levels, the biasing condition needs to be adapted to lower drain currents. As a result of this, the bandwidth and maximum gain was found to be reduced due to reduced g_m values. This finding is important to be considered in PA design when increasing the frequency of operation to the lower THz frequency range.

Multi-finger transistors are a crucial building block for the realization of compact amplifiers with high output power. By increasing the frequency of operation towards the lower THz band around 300-GHz, the electrical size of the available multi-finger CPW device layouts and their feeding structures also increases. This significantly reduces the achievable bandwidth, as shown with the analysis and comparison of devices with two, four and six transistor fingers. It is shown, that the best performance in terms of bandwidth and modeling accuracy is only achievable with the most simple two finger transistor. To benefit from the superior device performance of 2-finger transistors and overcome the abovementioned limitations—which are introduced by the increasing complexity of classical multi-finger HEMT layouts—a novel simulation approach for multi-finger PA cells based on highly parallelized 2-finger devices is proposed. Using this innovative approach, only the PDK model for the finger structure of the transistor is required and the multi-finger transistor shell is simulated and optimized as a part of the matching network design. As a result of this, a unique flexibility during the design process is enabled. Furthermore, substantial improvement in terms of modeling accuracy of chip-size-optimized CS and cascode cells with up to 8 transistor fingers around 300 GHz is demonstrated. Thus, the accurate description of complex multi-finger cascode devices in TFMSL environment is realized, which has not been possible with the prior used multi-finger PDK elements. At the same time, the number of active device models which need to be provided in the PDK is minimized, reducing the required effort for model extraction significantly.

The developed cascode cells have been optimized with the intent to minimize the chip width, which is essential to allow further parallelization on circuit level. To maximize the achievable output power on the smallest chip size possible, the cascode and CS performance was analyzed considering the required chip width of the corresponding multi-

finger PA cells. This evaluation shows that when considering the achievable output power and the required chip area for the two device configurations, the CS devices demonstrate superior performance in terms of P_{out} per chip width. Furthermore, the gain benefit of the stacked cascode is strongly diminished, while doubling the DC power consumption. The only slightly improved output power of the cascode device corresponds to the results of the theoretical analysis of stacked HEMT devices and their dependency on the current-gain, which is described in Section 2.2. As a result of this, CS devices should be preferred over cascode devices when requiring linear output-power performance at 300 GHz, which is a key finding for the implementation of chip-size-optimized PA cells.

To realize the load-dependent large-signal characterization of the mHEMT devices, on-chip load pull at 300 GHz was investigated, using tunable output matching networks. Based on an innovative in-situ load-pull MMIC with tunable OMN, the two-dimensional load tuning and large-signal characterization has been demonstrated for the first time at frequencies above 200 GHz—providing the unique possibility of model verification and valuable insight for PA-design considerations at the lower THz band. Using the results of this investigation in conjunction with extensive load-pull simulations, trade-off load targets have been defined for the design of the developed amplifier circuits.

These device-level-related design approaches and considerations serve as the important basis for the implementation of highly-compact 300-GHz PA circuits with state-of-the-art performance. The successful development of those amplifiers, which are based on a novel PA topology and the above discussed investigations and findings, is described in detail in the following chapter.

4 Development of Compact 300-GHz Power Amplifier MMICs

As introduced in the previous chapters, the goal of this work is not only to develop high-power amplifiers around 300 GHz, but also to minimize the required chip size to enable module and system integration. This chapter describes the development of chip-width optimized PA circuits, which are based on the multi-finger cascode and common-source devices described in Chapter 3. The design of a compact unit-amplifier (UA) cell as well as on-chip power combiners is discussed. These form the building blocks of the developed 300-GHz high-power amplifier MMICs.

4.1 Circuit-Simulation Approach

The PA design process which was used in this work is summarized in a simplified flow chart in Fig. 4.1. This design procedure was employed for the design of several chip-width optimized 300-GHz PA circuits and can be divided into four major parts:

(1) Simulation and modeling of active devices.

(2) Simulation and modeling of passive TFMSL components.

(3) Matching network design.

(4) Implementation and simulation of the full PA MMIC.

These parts, however, cannot be entirely separated from each other and, in many cases, require several optimization cycles, repeating prior design steps.

Simulation of Active Devices To implement the PA circuits at the smallest chip width possible, a "power-bar-like" design approach was targeted. Hence, a large number of two-finger devices is implemented in close proximity, using the multi-finger simulation approach described in Section 3.2. After the number and width of the transistor fingers is chosen, the corresponding multi-finger transistor shell is simulated. The layout implementation of the multi-finger shell can be later adjusted as a part of the matching network design—e.g. to include circuit elements for matching or stabilization within the feeding structures—when required. The finger width is first chosen based on the predicted bandwidth in single-device small-signal simulations. The exact finger width can be adjusted as a part of the design process—which requires to redo this part of the design procedure. Within the PA circuits described in this chapter, a finger width of 10 to 16 µm was chosen with the intent to permit the broadband operation up to an upper frequency limit of 330 to 350 GHz.

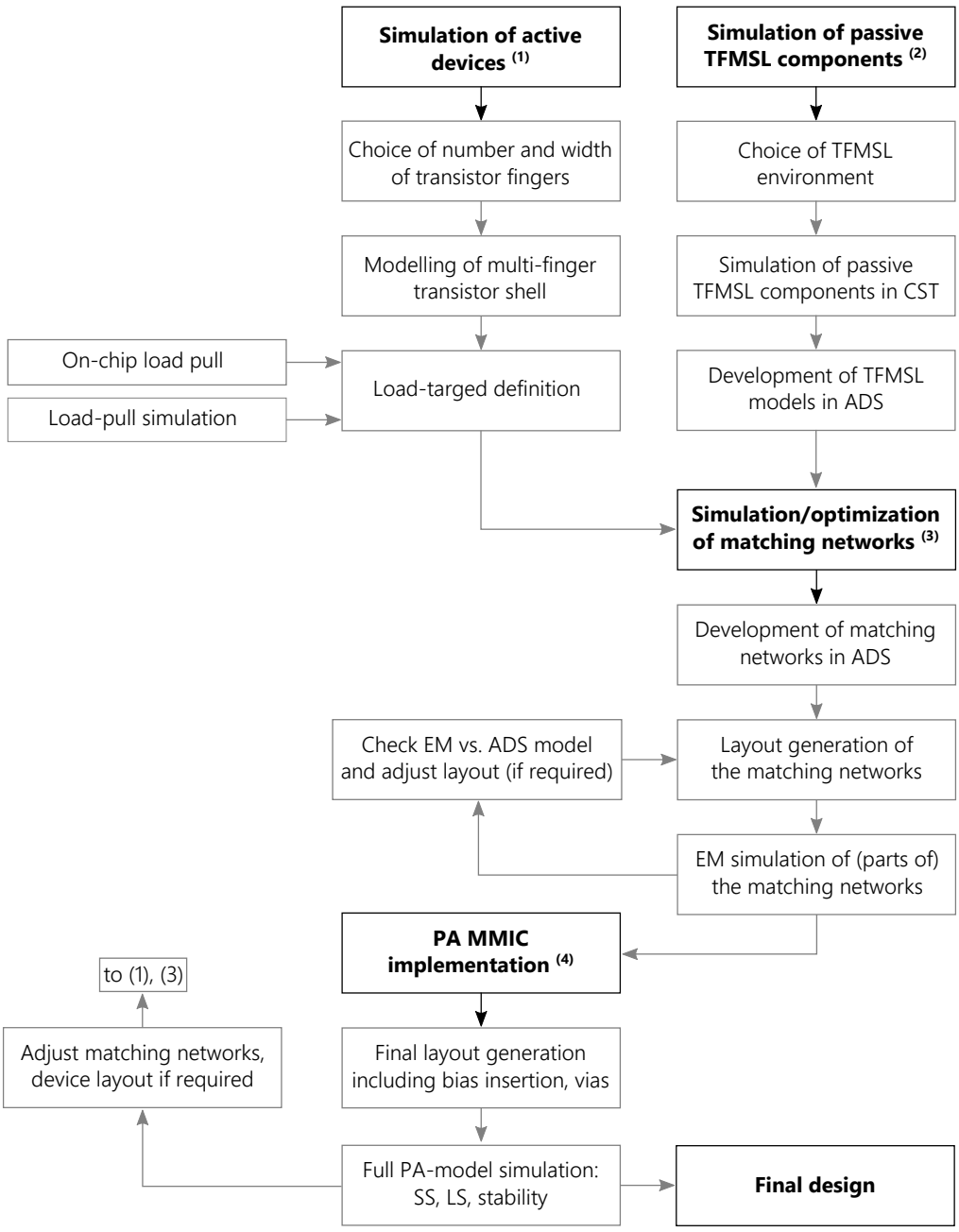


Figure 4.1: Flow chart of the procedure for simulating and modeling active and passive components within the PA-design process.

In the next step, the load targets are defined over the frequency band of interest, in order to ensure the targeted large-signal performance and frequency range. The load targets of the implemented cascode stages were defined in large-signal load-pull simulations. For the CS devices, on the other hand, gain-power trade-off load impedances were defined considering large-signal load-pull simulations as well as the in-situ load-pull measurement data described in Section 3.4.

Simulation of Passive TFMSL Components 3D EM simulators are widely used in IC design at mm-wave and sub-mm-wave frequencies, in order to accurately describe the

passive matching networks and ensure first-pass design success. To develop and optimize a matching or filter network in reasonable time, however, scalable and accurate PDK models of passive elements like transmission lines, T-junctions, bends and capacitors are required for time efficient schematic simulations. Therefore, simple ADS TFMSL-component models have been implemented for the 300-GHz PA design.

In the first step, the wiring environment for the design is chosen and the required TFMSL elements—this includes transmission lines, T-junctions, as well as parallel and series capacitors—are simulated in CST for different geometrical shapes. At this point, the accuracy of these 3D EM models is assumed to be nearly perfect, which is typically the case due to the simplicity of the test structures. In the next step, the TFMSL components are modeled in ADS using the "MLIN" model from the "TLines-Microstrip" library. For each TFMSL environment—e.g. *MET2 TFMSL*, *MET2MET3 TFMSL*, and *MET3 TFMSL*, which are described in Section 2.3—the substrate parameters of an "MSUB" substrate model are fitted to the 3D EM simulation data and are verified for the required transmission-line shapes.

Based on these substrate models, T-junctions and other transmission-line components can then be modeled using the microstrip-line elements from the "TLines-Microstrip" library. TFMSL capacitors are modeled using two transmission lines (*MET2MET3 TFMSL*) with a lumped series/parallel capacitor in between the lines. The width and combined length of the two transmission lines corresponds to the capacitor's actual layout dimensions and the value of the lumped capacitor is calculated with the 0.8-fF/µm^2 capacitance per area of the SiN layer. The model implementation of these simple TFMSL-MIM-cap models for schematic simulations are shown in more detail in the Appendix C.

Simulation and Optimization of Matching Networks The matching networks have been developed based on the prior defined input and load impedances, using the TFSML models for the first schematic implementation in ADS. This network is then, part by part, implemented in the layout and simulated in Momentum and CST. In this design step, the matching networks for multi-finger devices with up to 8 transistor fingers have been developed. Since a "power-bar-like" design is targeted, the width of the matching networks must not exceed the required chip area of the active devices. This needs to be considered during the layout implementation of the matching circuits and leads to several cycles of layout and network optimization. This is required due to coupling between densely-routed TFMSL elements [74], for example, which needs to be compensated. Hence, both the electrical behavior of the networks as well as the limited available chip area for their implementation needs to be considered here.

PA MMIC Implementation Based on the stand-alone layout implementations of the input, output and interstage matching networks—as well as the active device layouts—the full PA MMIC can be implemented. This, for example, requires the implementation of the bias-insertion network as well as through-substrate vias. The operation of the fully-EM-simulated PA implementation is then verified under small-signal and large-signal operation and the stability is checked.

At this point, several of the prior design steps need to be repeated, in order to iteratively optimize the design. This includes the implementation of circuit elements for stabilization and biasing within the feeders of the multi-finger device layouts—which requires the re-simulation of the multi-finger transistor shell. This offers great flexibility for optimization during the design process. Furthermore, a re-routing of the matching networks is typically required in order to implement the bias-insertion networks at the limited given chip area—which leads to at least one additional cycle of the matching network simulation and optimization step.

The implementation of the bias-insertion network—which is discussed in detail in the following sections—is one of the most crucial steps during the design process of a chip-size optimized PA cell. Due to the high current required at the drain supply, the drain voltage is usually applied via RF-shorted stubs. The corresponding stubs have been implemented in the interstage and output matching networks of the developed PA MMICs during the matching network design. Since the space for bias insertion is very limited in the PA circuits of this work, the implementation of an RF-shorted stub for gate-voltage insertion was omitted and the gate-voltage is applied via the NiCr layer, which is routed below the MET1 ground plane. Due to the low gate current density—which is usually well below 1 mA/mm—the resistors in the gate biasing can be in the magnitude of several kilo-Ohms. This proved to be especially beneficial for the stability of the compact PA circuits, since any feedback loop via the gate-bias network is sufficiently damped. During the matching network simulation, the gate-bias network can be simply considered by implementing a shorted high-ohmic resistor in simulation.

Due to the closed MET1 ground plane, the TFMSL matching networks can be developed with a simplified layer stack, which does not consider the material or height of the semiconductor substrate. Yet, one of the important findings of this work is, that the implementation of vias nevertheless needs to be considered during the design process of the PA MMIC—since resonances in the substrate potentially do effect the operation of the fully processed TFMSL circuits. Therefore—dependent on the circuit topology—the via placement needs to be considered during the design process. This issue is described in detail in Section 5.1.

4.2 Development of a Compact 300-GHz PA Topology

Based on the design procedure discussed in the previous section, a chip-size optimized unit amplifier cell has been implemented, described in Section 4.2.2. As a part of this design process and to reduce the required chip width of the compact unit cell, the multi-finger device models based on closely parallelized two-finger devices have been developed, which have been described in Section 3.2. The result of this circuit optimization is not only the employed multi-finger-device modeling approach—but also several 300-GHz PA circuits, which were implemented during the device-layout and circuit optimization process.

4.2.1 300-GHz Cascode Amplifier Circuits

To validate the multi-finger transistor-modeling approach within multi-stage 300-GHz PA circuits, several TFMSL cascode PA cells have been implemented—integrating cascode cells with four and eight transistor fingers, respectively. The corresponding layout implementations as well as measurement results are discussed and evaluated in detail in the following subsections.

4-Finger-Cascode Topology The chip photograph of a four-stage cascode PA MMIC—which was implemented in the *BEOL-A* variant including MET3 in air-bridge technology—is depicted in Fig. 4.2 [52]. This cascode PA circuit is referred to as *CPA1* in the following. Each gain stage consists of the cascode cell shown in Fig. 3.18, integrating four parallel transistor fingers with a finger width of 10 µm. This 4-finger cascode cell was parallelized four times, implementing a total gate width of 160 µm in each gain stage. The corresponding block diagram of the PA circuit is shown in Fig. 4.3.

The upper two and lower two cascode PA cells of the input and output stages are simultaneously matched to 25 Ω (IMN, OMN), and two-way $\lambda/4$ power combiners/splitters with 50-Ω line impedance are used to transform the parallel 25 Ω to the 50-Ω system impedance. To optimize the bandwidth and reduce losses, a non-50-Ω interstage matching network (ISMN) is used to match the input of the cascode PA cells directly to the output of the preceding stage, without first translating to 50 Ω.

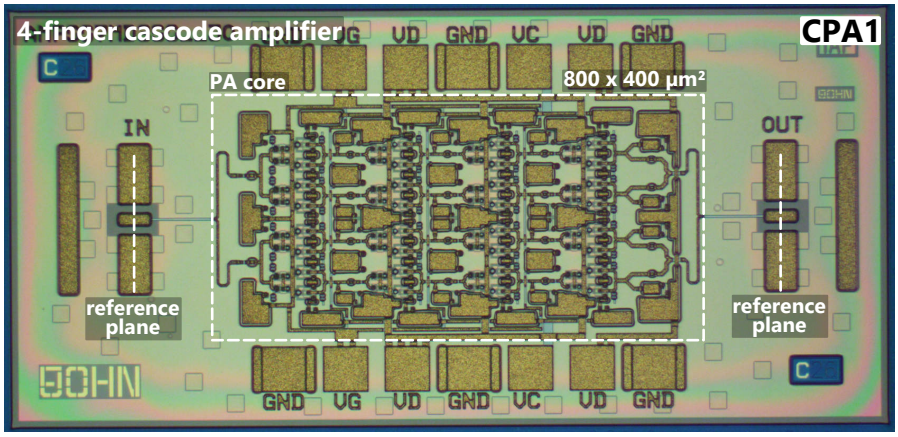


Figure 4.2: Chip photograph of the fabricated PA MMIC *CPA1*, which is based on 4-finger cascode cells [52]. The chip dimensions are 0.75 x 1.5 mm². The required chip area of the 4-stage PA core with eight 2x10 µm cascodes in parallel is 0.4 x 0.8 mm².

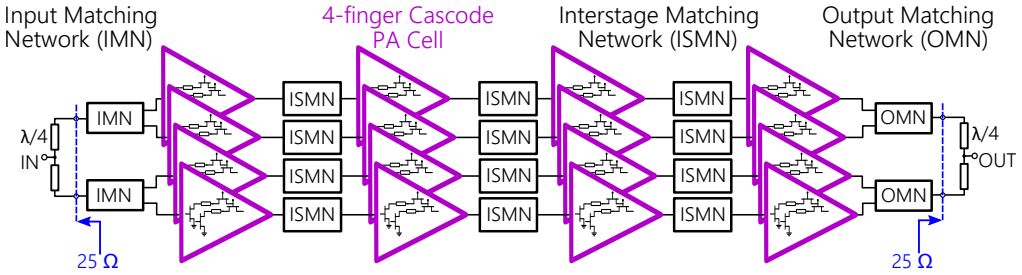


Figure 4.3: Block diagram of the 4-stage power amplifier MMIC *CPA1* (Fig. 4.2). The transistor-finger width in each stage is 10 µm.

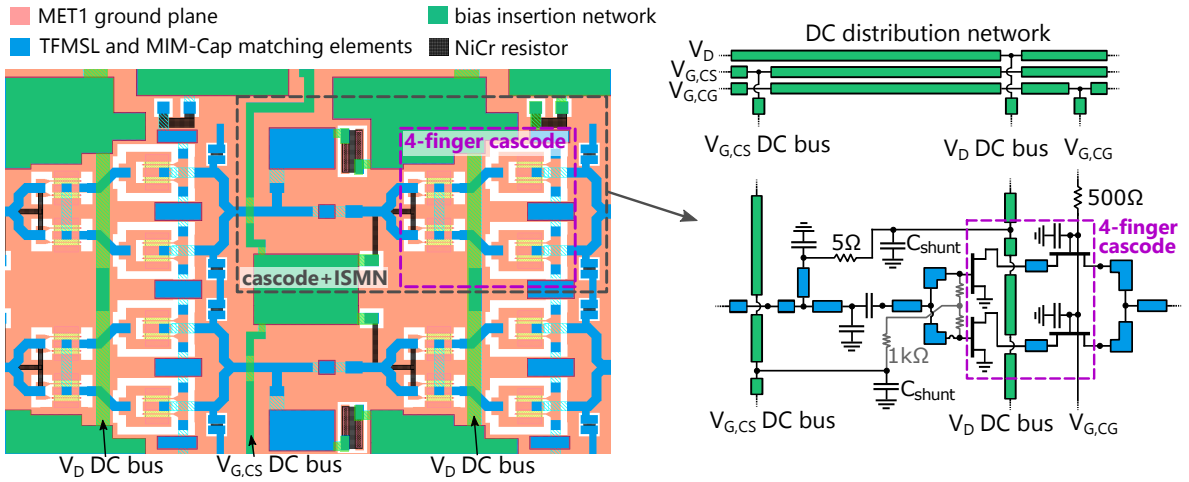
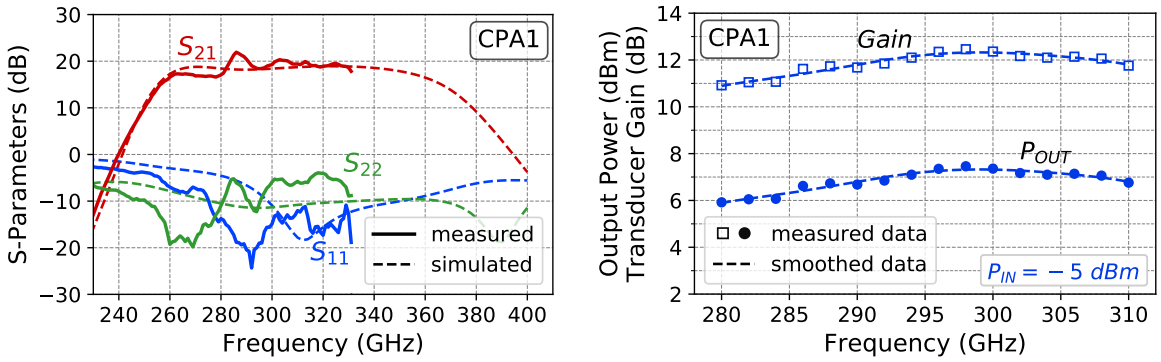


Figure 4.4: Close-up view of the layout and detailed schematic of the 4-finger cascode cell including TFMSL and and MIM-capacitor elements of the interstage matching and bias-insertion networks of *CPA1*.

On the left in Fig. 4.4, a close-up view of the four-stage PA circuit's layout is depicted, including two parallel and cascaded cascode cells as well as the corresponding interstage matching networks. RF-relevant TFMSL and MIM-capacitor elements of the matching networks are highlighted in blue color, and layout elements of the bias-insertion network are depicted in green color. The detailed schematic of a single 4-finger cascode including the interstage matching and bias-insertion network is shown in Fig. 4.4 on the right.

The matching networks are implemented using the *MET2MET3 TFMSL* interconnection, introduced and discussed in Section 2.3. To minimize the required chip width of the PA core, by employing a "power-bar-like" design, the 4-finger cascode cells are parallelized as close as possible, sharing a common shunt capacitor with the adjacent cascode cell(s). This, in turn, limits the chip area for both the interstage matching as well as bias-insertion networks, which must not exceed the width of the cascode cell. As a result of that, the space for the implementation of stubs for bias insertion is limited and the gate-bias voltage is applied via the NiCr layer which is routed below MET1 and directly connected to the gate feeders of the CS devices. The value of the gate-bias resistor is in the range of 1 kΩ, decoupling the gate-bias insertion from the RF path. The drain-bias voltage is fed to the drain of the CG devices via the depicted RF-shorted stub, which is implemented as parallel inductance in the interstage matching network, as can be seen in Fig. 4.4.

To distribute the bias voltages between the cascaded gain stages, a horizontal three-line DC distribution network is implemented at the top and bottom side of the PA core. The bias distribution to the parallelized cascode cells is realized using a vertical *DC bus* for the CS-gate and CG-drain voltages ($V_{G,CS}$, V_D), respectively. Since the gate current of the mHEMT devices is typically below 1 mA per 1-mm gate width, the gate current can be handled by a MET2 thin-film line and, therefore, the $V_{G,CS}$ *DC bus* is implemented as *MET2 TFMSL* in order to reduce coupling with the RF lines. To prevent any significant voltage drop across the V_D *DC bus*, the drain-voltage distribution is completely implemented in MET3. The $V_{G,CS}$ *DC bus* is crossing the ISMN while the V_D *DC bus* is crossing the cascode cell—both crossings are implemented as air bridge. The third bias



(a) (b)

Figure 4.5: (a) Measured S-parameters of the 4-stage power amplifier MMIC *CPA1*. (b) Measured output power and gain versus frequency of *CPA1* at −5 dBm input power.

voltage, $V_{G,CG}$, is fed to the outer cascode cell and distributed via the parallel-connected CG shunt capacitors and gate feeders.

Since both bias insertion and broadband matching is realized with the cascode cell plus ISMN depicted in Fig. 4.4, the parallel implementation of multiple cascodes on minimized chip size is feasible by mirroring and parallelizing this PA cell. The required chip area of the PA core is $0.4 \times 0.8\,\text{mm}^2$—including all active devices, matching networks, and the second stage of shunt capacitors in the bias-insertion network. Using the *MET2MET3 TFMSL* interconnection for the $\lambda/4$ transformation at the output, the introduced insertion loss is in the range of 0.6 to 0.8 dB, while providing no isolation between upper and lower half of the PA core. In order to reduce phase imbalance and suppress odd-mode oscillation between the parallel cascode cells, 5-Ω shunt resistors are connected to the gate feeders of the input stage and the drain feeders of each gain stage (Fig. 3.18).

Fig. 4.5 (a) shows the S-parameters of the 4-stage cascode PA circuit—showing a good agreement between measurement and simulation for the measured H-band frequency range up to 335 GHz. Over the 285–335 GHz band, 13–19-dB small-signal gain was measured. The gain drop for the 265–285 GHz frequencies and observed overshoot at 290 GHz indicate stability issues, which are caused by the limited isolation of the on-wafer measurement setup. The measured transducer gain and output power at a constant input power of –5 dBm are depicted in Fig 4.5 (b). The measured output power of this 4-stage MMIC is between 5.2 and 7.6 dBm over the 280–310-GHz frequency range, measured at about 7-dB gain compression.

Therefore, using the proposed design approach based on highly parallelized 2-finger devices for the densely routed 300-GHz MMIC described here, first-pass design success was achieved—featuring broadband gain and output-power performance. With a required chip width of 400 µm for the PA core, further chip-size reduction was nonetheless required to permit on-chip and system integration as well as further on-chip parallelization.

8-Finger-Cascode Topology The layout of the 4-finger-cascode cell, which is used in the above-described four-stage PA circuit, is based on the standard 2-finger-device layout provided in the PDK. Since the four parallel cascode cells in the above design are already

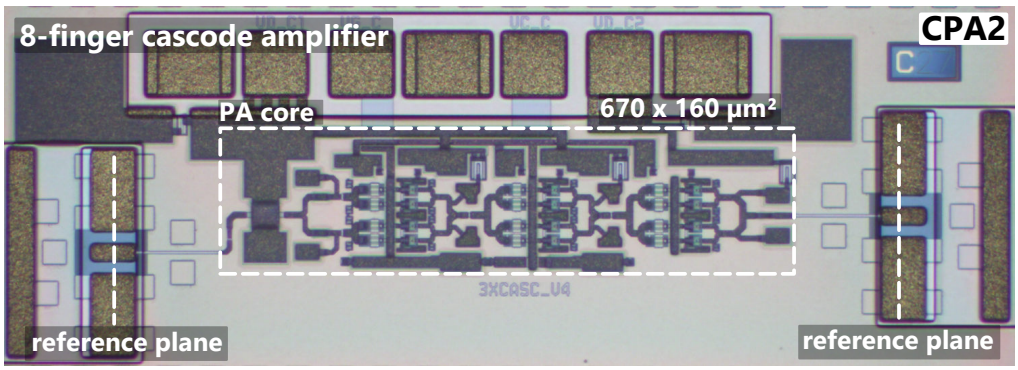


Figure 4.6: Chip photograph of the fabricated 8-finger cascode PA MMIC *CPA2*. The chip dimensions are $0.35 \times 1.2\,\mathrm{mm}^2$. The required chip area of the 3-stage PA core with four 2x10 µm cascodes in parallel is $0.16 \times 0.67\,\mathrm{mm}^2$.

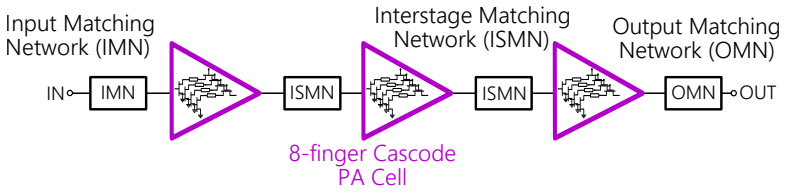


Figure 4.7: Block diagram of the 3-stage power amplifier MMIC *CPA2*. The transistor-finger width in each stage is 10 µm.

parallelized as close as possible, a significant reduction of the PA core's required chip width—and, hence, an increased output power per chip width—could only be achieved by reducing the width of the multi-finger cascode layout.

The layout optimization and development of an 8-finger cascode cell, which permits a cascode-cell-width reduction by almost 40 %, is described in Section 3.2.3 in detail. The chip photograph of a three-stage cascode PA MMIC *CPA2*, which was developed based on this chip-size optimized cascode-device layout, is depicted in Fig. 4.6. The corresponding block diagram is shown in Fig. 4.7. Each gain stage consists of the cascode cell shown in Fig. 3.22—integrating four two-finger devices with 10-µm finger width in parallel, resulting in a total gate width of 80-µm. The required chip area of the PA core is $0.16 \times 0.67\,\mathrm{mm}^2$, including all active devices, matching networks and the second stage of shunt capacitors in the bias-insertion network. This three-stage amplifier was not developed as stand-alone PA circuit, but rather as chip-size optimized PA cell which allows straight forward parallelization or integration as reusable IP block.

On the left in Fig. 4.8, the layout's close-up view of two cascaded 8-finger cascodes is shown—including the interstage matching network depicted in blue color and layout elements of the bias-insertion network highlighted in green. The depicted PA core was optimized for a compact chip size in order to maximize the total gate width on the smallest chip width possible. And as for the 4-finger cascode circuit described above, the interstage matching networks depicted in blue are, therefore, designed for a minimized chip width which must not exceed the width of the parallelized active devices. This permits the parallelization of the compact PA cell at the smallest chip area possible. The gate bias is applied using the NiCr layer, which is routed below the MET1 ground plane. This gate-feeding resistor is directly connected to the gate feeders of the single devices.

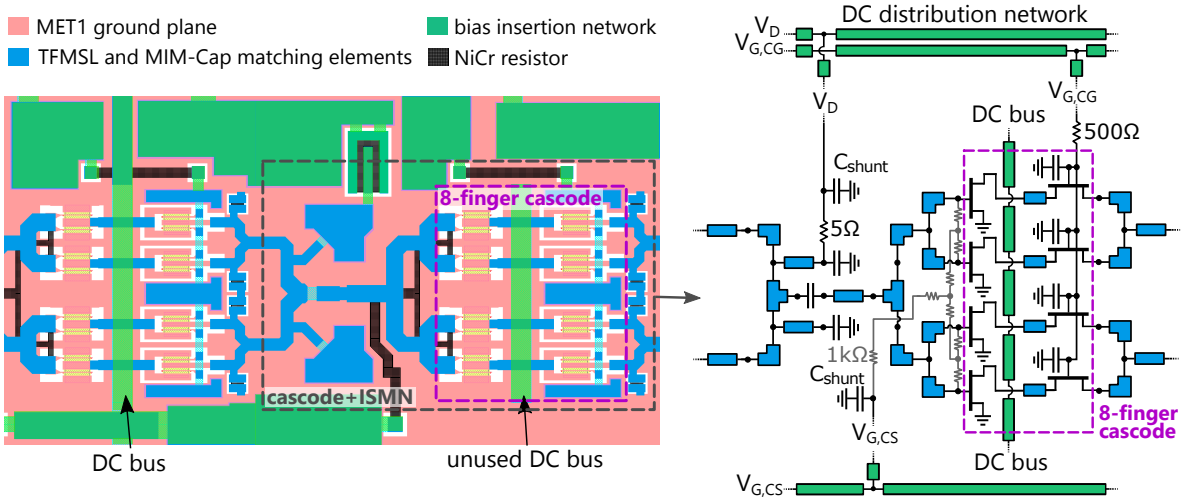
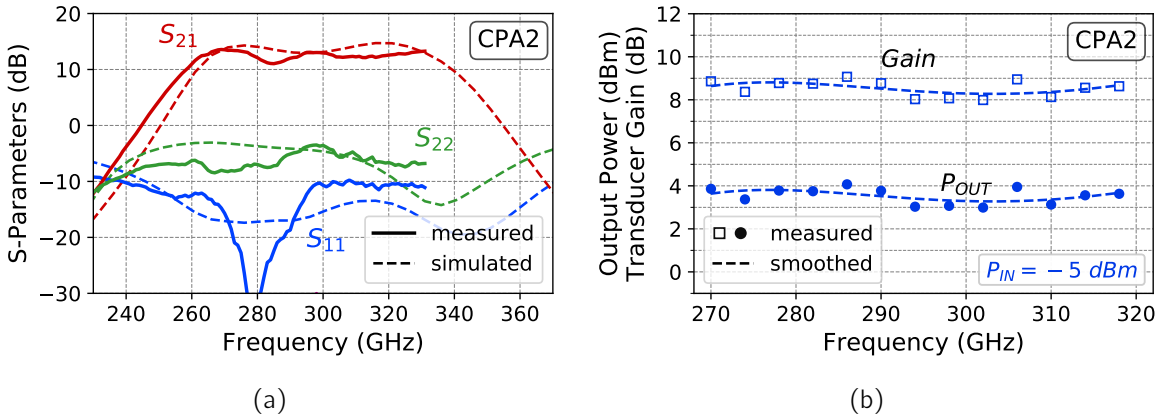


Figure 4.8: Close-up view of the layout and detailed schematic of the 8-finger cascode cell including TFMSL and MIM-capacitor elements of the interstage matching and bias-insertion networks of *CPA2*.



(a) (b)

Figure 4.9: (a) Measured S-parameters of the three-stage 8-finger-cascode MMIC *CPA2*. (b) Measured output power and gain versus frequency of *CPA2* at −5 dBm input power.

The CS-gate voltage $V_{G,CS}$ is applied to the gate-feeding resistor from the lower side of the PA core, while both the CG-drain and the CG-gate voltage (V_D, $V_{G,CG}$) are applied from the upper side. Therefore, a two-line DC distribution network is required at the upper side of the PA core to distribute the bias voltages $V_{G,CG}$ and V_D between the cascaded gain stages—and a single line is used for $V_{G,CS}$ at the lower side. To feed the supply voltages from the upper to the lower side of the PA core, a vertical *DC bus* is implemented in the cascode cell by default. The MMIC depicted in Fig. 4.6 only uses one $V_{G,CS}$ *DC bus* to feed the $V_{G,CS}$ *DC line* at the lower side of the PA core. The unused *DC buses* are not connected to the bias-insertion network in this three-stage MMIC, but only used in the PA circuits of the following sections, where supply voltages need to be fed to multiple PA cells in parallel.

The measured S-parameters as well as saturated gain and output power of the three-stage cascode amplifier are depicted in Fig 4.9. The measured small-signal gain is around 13 dB over the 260–335-GHz frequency band, providing 4–5-dB gain per stage. At 5-dB gain compression, the saturated output power is approximately 4 dBm over a measured 50-GHz large-signal bandwidth from 270 to 320 GHz.

Table 4.1: Comparison of the cascode PA MMIC results of *CPA1* and *CPA2*.

	Type of device configuration in the output stage	
	4x4x10-µm cascode, CPA1 8 two-finger devices in parallel	**8x10-µm cascode, CPA2** 4 two-finger devices in parallel
Chip area of PA core (mm x mm)	0.8 x 0.4	0.67 x 0.16
Output device periphery (µm)	160	80
Average saturated output power (dBm)	6.8	3.7
Output power per total gate width (mW/mm)	29.9	29.3
Output power per PA-core width (mW/mm)	12	14.7

Comparison of Cascode Circuits A summary of the output-power performance of the 8-finger cascode amplifier circuit *CPA2*—in comparison to the previously discussed PA circuit *CPA1* based on 4-finger cascode devices, which were parallelized four times—is given in Tab. 4.1. Considering the average saturated output power normalized to the total gate width in the output stage, both PA circuits achieve similar power densities in the range of 30 mW/mm. Since the number of gate fingers is doubled in the output stage of the 4-finger cascode PA circuit *CPA1*, the 6.8-dBm average output power level is approximately doubled in comparison to the 8-finger cascode PA cell *CPA2*. When considering the output power per required chip width of the PA core, on the other hand, the optimized 8-finger cascode permits an improvement of almost 20 %—keeping in mind device spread between different runs as well as the larger power combining-network, which is integrated in the design based on 4-finger cascode cells.

4.2.2 Chip-size Optimized 300-GHz Unit Amplifier

The compact PA cell which is based on an 8-finger cascode cell and is discussed in the previous section was designed for a minimized chip width and, therefore, both the parallel 2-finger devices as well as the matching networks leave almost no room for a further chip-width reduction. In order to increase the output power without increasing the required chip width, several possibilities can be considered.

Since the finger width of 10 µm—which is used in the designs discussed above—is not the maximum for 300-GHz operation, one option is to increase the finger width and thus the total gate width in the output stage. How much the finger width can be increased, however, is dependent on the frequency range and bandwidth which need to be covered.

The concept of transistor stacking has been introduced in the previous chapters as another possibility to increase the output power. But the benefits of stacking more than two HEMT devices in the underlying technology at the frequency band around 300 GHz is limited even in theory, as discussed in Section 2.2.2. Therefore, stacking of more than two HEMT devices—which is basically the cascode configuration—is not considered here. In Section 3.3 it is shown, that the benchmark output power per required chip width of a common-source transistor cannot be achieved with the stacked cascode configuration. As a result of that, CS devices are implemented in the output stage of the compact unit-amplifier described in the following.

Unit-Amplifier Topology Fig. 4.10 shows the chip photograph of a compact chip-size optimized unit amplifier cell with five gain stages. This unit PA circuit is referred to

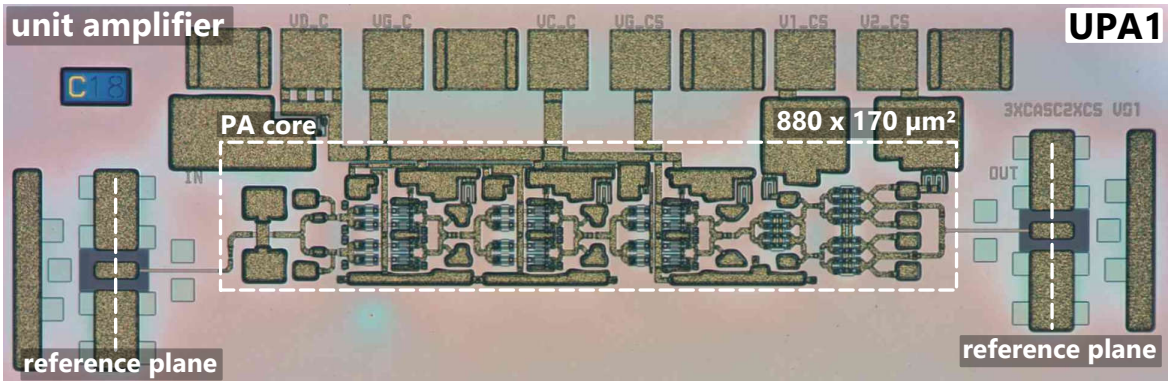


Figure 4.10: Chip photograph of the fabricated unit amplifier MMIC *UPA1*. The required chip area of the 5-stage PA core with 8-finger cascode and CS PA cells is $0.17 \times 0.88\,\mathrm{mm}^2$. The amplifier uses a CS output stage with two $8 \times 16\,\mu$m-finger-width devices in parallel. The gate width of the three cascode stages is $8 \times 10\,\mu$m.

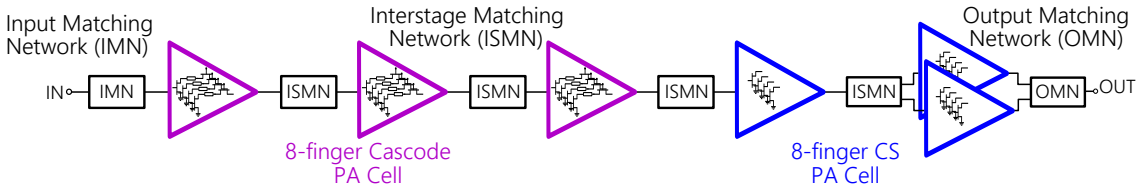


Figure 4.11: Block diagram of the *UPA1* MMIC depicted in Fig. 4.10. The detailed schematic of the five-stage unit amplifier is shown in Fig. 4.12. The transistor-finger width in each cascode and CS stage is 10 µm and 16 µm, respectively.

as *UPA1* in the following. The corresponding block diagram with three cascode stages at the input and two CS output stages is depicted in Fig 4.11. The minimum required width of a cascode is limited by the size of the shunt capacitors at the CG devices, as discussed in Section 3.2.3. In comparison, two parallel 8-finger CS transistors require approximately the same chip width as an 8-finger cascode cell as can be seen in the chip photograph of *UPA1* in Fig. 4.10. For this reason, the CS output stage permits doubling the number of gate fingers in the output stage, compared to a cascode device. Since the cascode cannot provide the same level of output power as a CS device with twice the number of gate fingers, while providing enough gain, the depicted *UPA1* topology was implemented.

As a result of the analysis in Section 3.3, multi-finger cascode devices are only implemented in the input stages, providing high gain over the 280–350-GHz frequency band. It is important to note, that the Section-3.3 discussion only shows the exemplary cascode performance under large-signal operation at 300 GHz. In order to meet the given output power and linearity objectives not only in a narrow frequency range, the dependency of the large-signal performance on the cascode geometry has to be considered over the full frequency band of interest.

The finger width of the cascode devices in the gain stages is 10 µm. For this finger width, the capacitance of C_{SHUNT} is chosen to be 100 fF and the length of the interconnection between the CS and CG device (L_{MSL}) is 20 µm. This way, the cascode is unconditionally stable with around 12-dB MAG over the 280–350-GHz frequency band—as shown in Fig. 3.26—representing a good trade-off between high gain and output-power

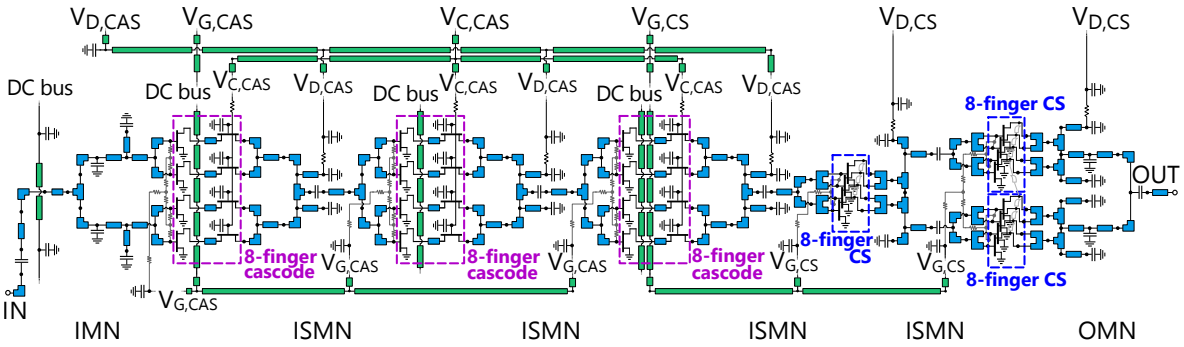


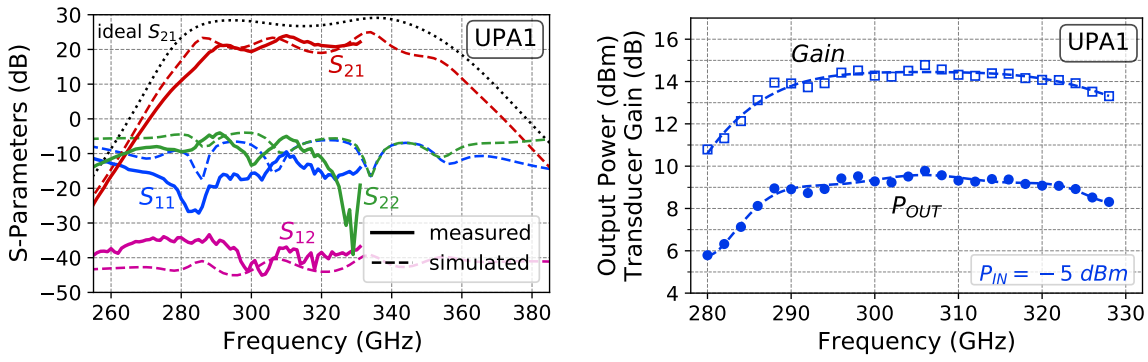
Figure 4.12: Simplified schematic of the five-stage UA cell *UPA1*. A close-up view of the 8-finger cascode devices is depicted in Fig. 3.22, including the gate biasing as well as stabilization elements.

performance. Smaller C_{SHUNT} values would reduce the gain significantly, limiting the gain benefit of the cascode. With a longer transmission line L_{MSL} the cascode is only conditionally stable at 350 GHz and a constant output-power performance cannot be achieved over the full frequency band of interest in simulation. A larger finger width could be implemented in the cascode stages for the frequency of operation around 300 GHz. Since this is not required to sufficiently drive the CS devices in simulation, the 10-µm finger width was chosen.

The 8-finger CS-transistors in the last two stages were implemented with 16 µm finger width. The driving ratio in the output stages is, therefore, 1:2. This means, that the power loss in the interstage matching network as well as the power splitting needs to be covered by the gain of the output stage, which requires at least a gain level in the range of 4 to 5 dB on device level. The simulated 300-GHz MSG of the CS devices is 7 dB at $V_{DS} = 1.0\,\mathrm{V}$, which leaves enough room for trade offs in load-target definition. Yet, when increasing the drain-source voltage at reduced drain-current levels, the resulting reduced gain and cutoff frequencies need to be considered—as discussed in Section 3.1. According to single device simulations and considering the required MSG bandwidth of up to 350 GHz, a finger width around 20-µm could be implemented to increase the output power by approximately 1 dB. However, in order to relax the requirements on the yield and spread of the mHEMT devices, the 16-µm finger width was chosen.

The layout implementation of the cascode stages is identical to the 8-finger cascode amplifier described in the previous section. A detailed schematic of the five-stage UA is depicted in Fig. 4.12, including the bias-insertion network highlighted in green color. The gate voltages from both the cascode as well as the CS devices ($V_{\mathrm{G,CAS}}$, $V_{\mathrm{G,CS}}$) are fed from the lower side of the UA cell to the matching networks, using two DC buses crossing the cascode cells. To permit further parallelization, the feed through of the supply voltages $V_{\mathrm{C,CAS}}$, $V_{\mathrm{D,CAS}}$ and $V_{\mathrm{D,CS}}$—which are fed to the matching networks from the upper side of the UA—is possible via the implemented but unused remaining three DC buses.

The chip area of the UA core is $0.17 \times 0.88\,\mathrm{mm}^2$, including all matching networks as well as the bias-insertion and bias-distribution networks. Hence, this is the chip size which needs to be considered for further integration as PA IP block, for example, not considering the bias insertion to the MMIC.



(a) (b)

Figure 4.13: (a) Measured and simulated S-parameters of the 5-stage unit amplifier MMIC *UPA1*. The dotted line shows the ideal simulated S_{21}, without considering the limited isolation of the measurement system. The dashed lines represent the simulation results considering the poor isolation between input and output. (b) CW measured transducer gain and output power of the UA MMIC between 280–328 GHz, measured with 2-GHz step size at −5-dBm input power.

Measurement Results and Discussion The measured S-parameters of the UA are depicted in Fig. 4.13(a). The unit amplifier was designed for the 280–350-GHz frequency range, showing a measured small-signal gain ripple of around 5 dB. This periodic gain ripple is mainly caused by the poor isolation of the on-wafer measurement setup. Since the UA's measured S_{12} is only around –40 dB, the depicted periodic gain variation at gain levels above 20 dB can be observed. By including a simple model for the RF-probe overcoupling, a similar behavior is observed for the simulated S-parameters in Fig. 4.13(a).

Fig. 4.13(b) shows the measured transducer gain and output power versus frequency for CW operation of the UA. The frequency was swept from 280–328 GHz with 2-GHz step size at –5-dBm available source power. The CS devices in the output stages were biased with 1.3-V drain-source voltage at 400 mA/mm. The drain-supply voltage of the cascode stages is around 2.4 V ($V_{DS} \approx 1.2$ V) at 400 mA/mm. The UA's saturated output power in this biasing condition is in the range of 8 dBm to 9.7 dBm over the 285–328-GHz frequency range, measured at about 6-dB gain compression. The large-signal gain at this –5-dBm input-power level is around 14–15 dB.

The possibility of increasing the power density on device level of the mHEMT devices with extended gate-drain recess, by operating the transistors at higher drain-source voltages, was discussed in Section 3.1. At 40 GHz, a 2.4-dB OP_{3dB} improvement was measured when increasing V_{DS} from 1.0 V to 1.5 V. To illustrate the benefit of increased supply voltages on the UA's large-signal performance at 300 GHz, Fig. 4.14 shows the measured gain vs. output power characteristics at different bias conditions. By increasing $V_{D,CASC}$ from 1.8 to 2.2 V and $V_{D,CS}$ from 0.9 to 1.3 V, respectively, both the linear (OP_{1dB}) as well as saturated output power is significantly improved. To further increase the output-power performance by increasing the drain-source voltage, a higher load impedance would be required, in order to benefit from the larger voltage swing. This can be seen in Fig. 4.14, which shows no significant improvement in terms of output-power level when further increasing $V_{D,CS}$.

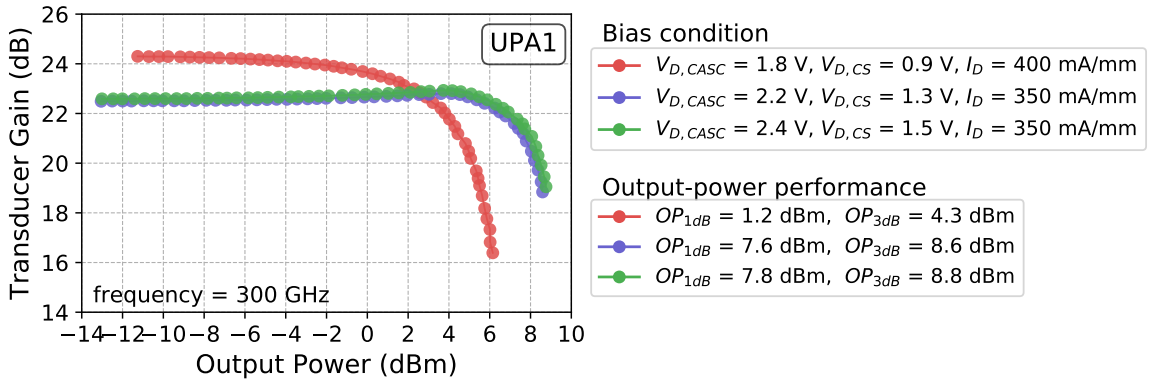


Figure 4.14: Measured *UPA1* large-signal gain versus output power at 300 GHz for different bias conditions. For operating conditions at increased drain-source voltages, the current is reduced as discussed in Section 3.1.2.

Based on the data depicted in Fig. 4.14, an OP_{3dB} improvement of more than 4 dB is observed when increasing the supply voltage to 1.3 V. Furthermore, the compression behavior of the PA circuit is significantly affected. The tremendous OP_{1dB} improvement from below 2 dBm to above 7 dBm is in large part caused by the different biasing condition of the stacked-cascode stages. By not shorting the gate of the CG device with a large MIM capacitor, the cascode is designed for improved large-signal performance, as discussed in Section 3.3. The small-signal as well as large-signal behavior, however, significantly depend on the capacitive voltage divider of $C_{SHUNT,CG}$ with the voltage dependent gate-drain capacitance C_{gd} of the CG transistor. For the cascode devices implemented in this UA cell—as can be seen in Fig. 4.14—the optimum linear behavior is achieved at $V_{D,CASC}$ values in the range of 2.2–2.4 V.

To compare the results of the UA cell *UPA1* with CS transistors in the output stages to the stand-alone 8-finger cascode PA circuit *CPA2*, which is described in the previous section, Tab. 4.2 shows a summary of both PA cells in the same bias conditions. On circuit level, both MMICs show a similar saturated output-power performance in terms of measured output power per total gate width—which is in the range of 30 mW/mm. Compared to the stand-alone 8-finger cascode PA cell *CPA2*, the measured *UPA1* output-power level per required PA core width of 48 mW/mm is notably improved by a factor of four. This improvement is due to the larger transistor-finger width of the CS devices in combination with the very compact implementation of two 8-finger CS devices in the output stage, which do not require significantly more chip area than the single 8-finger

Table 4.2: Comparison of the 300-GHz cascode PA cell *CPA2* and the unit PA cell *UPA1*

	Type of device configuration in the output stage	
	8x10-µm cascode, CPA2 4 two-finger devices in parallel	**2x8x16-µm CS, UPA1** 8 two-finger devices in parallel
Chip area of PA core (mm x mm)	0.67 x 0.16	0.88 x 0.17
Output device periphery (µm)	80	256
Average saturated output power (dBm)	3.7	9.1
Output power per total gate width (mW/mm)	29.9	31
Output power per PA-core width (mW/mm)	12	48

cascode devices in the input stages. Hence, a total gate width of 256 µm is implemented on an ultra-compact chip width of only 0.17 mm, including all required networks for bias insertion and distribution.

4.3 300-GHz Thin-Film Wilkinson Power Combiners

To further increase the output power, by parallelizing the compact UA cell described in the previous section, on-chip power combiners are used. Since the prior state of the art of existing HEMT based PA circuits is mostly implemented in substrate-guided CPW wiring environment, the previously integrated power combiners are also using the semiconductor substrate as dielectric for the combiner implementation.

In this section, the implementation possibilities of TFMSL Wilkinson power combiners are described, which are providing the necessary isolation in order to prevent odd-mode oscillation and load detuning between the parallelized UA cells. This kind of power combiner realized with TFMSL interconnections has been widely used in InP HBT SSPA MMICs at frequencies around 240 GHz as well as 300 GHz [37, 59, 38], providing high levels of output power at the respective frequencies. As shown in the discussion of different thin-film transmission lines in Section 2.3, the minimum loss of a $\lambda/4$ transmission line in the BEOL of the underlying HEMT technology is in the range of 0.3–0.4 dB at 300 GHz—dependent on the type of the TFMSL interconnection. When comparing these values to the reported insertion loss of 300-GHz CPW couplers and combiners—which is typically above 0.8 dB [4, 6, 87]—TFMSL combiners like the Wilkinson combiner appear as a valid option for low-loss 300-GHz power combining.

E. J. Wilkinson introduced the idea of his power divider in 1960 [121]. Originally introduced as non-planar n-way combiner, its two-way version has been implemented in planar IC technologies with great success for decades. Fig. 4.15 shows the schematic of the two-way Wilkinson divider/combiner, which provides in the ideal case more than 20-dB isolation and return loss over a fractional bandwidth of 40 %.

In the case of a 50-Ω system impedance, a characteristic impedance of approximately 71 Ω is required for the $\lambda/4$ lines of the Wilkinson combiner. This line impedance can be implemented in a low-loss *MET3 TFMSL* interconnection, when using the 4.6-µm BCB substrate in the *BEOL-B* technology variant. Realizing the 71-Ω line impedance, while simultaneously achieving a low insertion loss is an issue for the TFMSL interconnections which are typically implemented in the *BEOL-A* variant including the air-bridge top-metal layer, as discussed in Section 2.3. Therefore, the elevated CPW and air-bridge TFMSL—which permit the low-loss implementation of 71-Ohm transmission lines—are used for the design of Wilkinson power combiners in this technology variant.

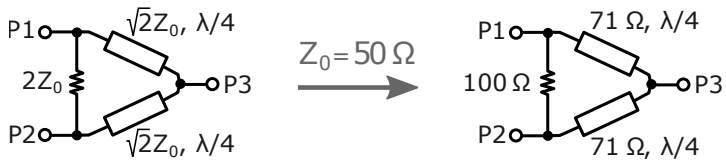
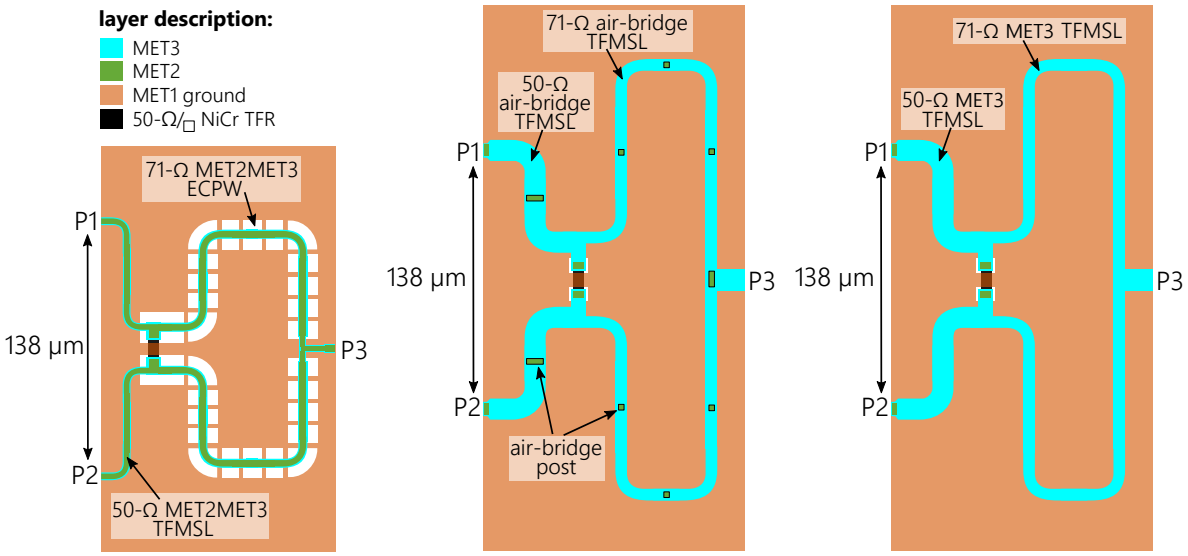


Figure 4.15: Schematic of the 3-dB Wilkinson power divider/combiner for an arbitrary system impedance Z_0 (left) as well as for an system impedance of 50 Ω (right).



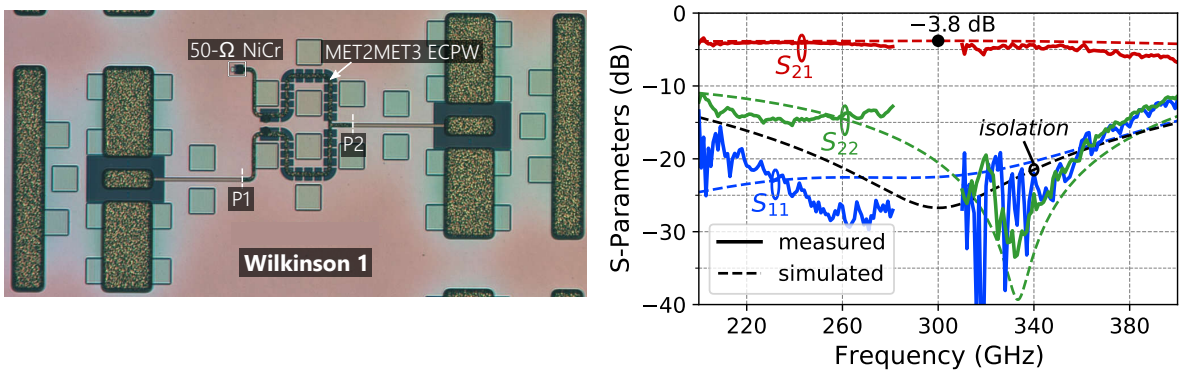
(a) Wilkinson 1 (b) Wilkinson 2 (c) Wilkinson 3

Figure 4.16: Layouts of three Wilkinson power combiners *Wilkinson 1*–*Wilkinson 3*, realized with (a) elevated CPW and (b) air-bridge TFMSL as well as (c) *MET3 TFMSL*.

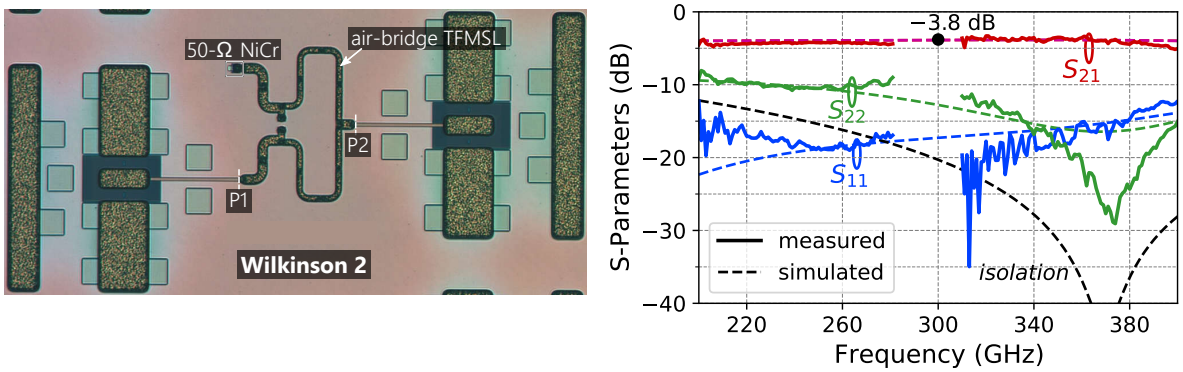
Fig. 4.16 shows the layouts of three Wilkinson combiner variants, implemented in *MET2MET3 ECPW*, *air-bridge TFMSL* as well as *MET3 TFMSL* interconnections. The combiners include 50-Ω TFMSL port extensions of approximately 70-µm length at port 1 and port 2, which are required to parallelize the unit amplifier cell described in the previous section with an output-port distance of 138 µm. Since the transmission-line properties of the air-bridge TFMSL and the *MET3 TFMSL* are very comparable, the layout of *Wilkinson 2* and *Wilkinson 3* are very similar—distinguishing primarily in the additional air-bridge posts in the *Wilkinson 2* design.

S-parameter characteristics of the three 2:1 Wilkinson variants are summarized in Fig. 4.17. To verify the reflection parameters (S_{11}, S_{22}) and transmission parameter (S_{21}) by on-wafer measurements around 300 GHz, the depicted two-port thru-line structures were fabricated. The combiner's isolation is only shown in simulation. The thru-line measurement verifies the 0.8-dB insertion loss of the Wilkinson combiners in the *BEOL-A* variant (Fig. 4.17(a), Fig. 4.17(b)), while the insertion loss of the MET3 Wilkinson combiner (Fig. 4.17(c)) is slightly below the simulated 0.7-dB insertion loss. The input return loss of the combiners is better than 15 dB over the 200–360-GHz frequency range, while only *Wilkinson 1* shows an output return loss above 15 dB around 300 GHz. The simulated isolation is better than 15 dB for frequencies above 260 GHz.

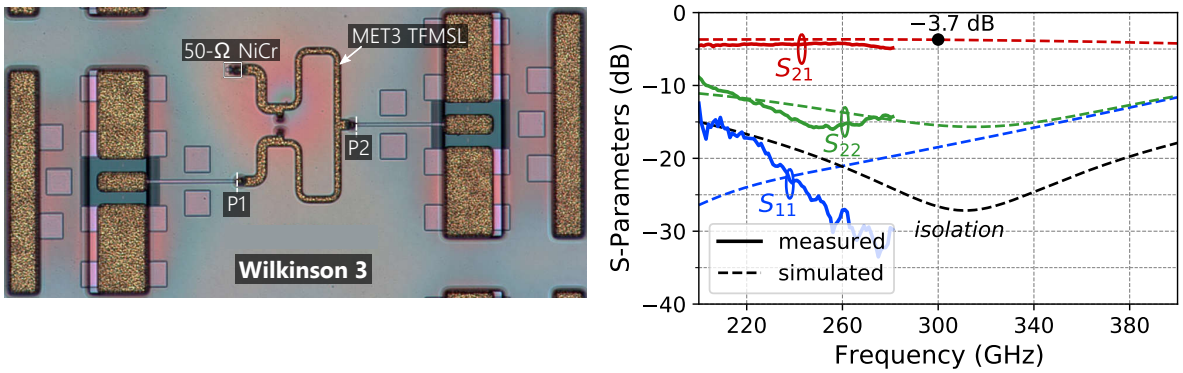
The test structure of the *Wilkinson 3* combiner was only characterized up to 280 GHz and, thus, no measurement data is available for the Y-band frequency range above 310 GHz. Yet, since the measured and simulated Y-band results of *Wilkinson 1* and *Wilkinson 2* are in agreement to a very good extend, a similar behavior is expected for the *Wilkinson 3* combiner. The measurement results depicted in Fig. 4.17, furthermore, demonstrate the functionality of the 300-GHz thin-film Wilkinson combiners and verify



(a)



(b)



(c)

Figure 4.17: (left) Chip photographs and (right) simulated and measured S-parameters of the three Wilkinson combiner variants *Wilkinson 1*–*Wilkinson 3* in thru configuration.

the high-impedance air-bridge and ECPW transmission lines implemented in *Wilkinson 1* and *Wilkinson 2*. For system (on chip) integration, however, the targeted combiner's input and output return loss should be above 15 dB—preferably even above 20 dB—in the frequency band of interest. Therefore, possibilities and limitations to improve the performance of the thin-film Wilkinson combiners have been investigated and are discussed in the following.

4.3.1 Layout Considerations for 300-GHz Thin-Film Wilkinson Power Combiners

As discussed above, the ideal two-way Wilkinson combiner consists of two quarter-wavelength transmission lines as well as an isolation resistor. The layout implementation of these components significantly impacts the combiner's performance, as can be seen from the data shown in Fig. 4.17. Since the loss per quarter-wave length slightly decreases for the implemented thin-film interconnections when increasing the frequency of operation, as discussed in Section 2.3, the combining efficiency can potentially be increased. The increasing electrical dimensions of the isolation resistor and its connection to the thin-film lines, on the other hand, are limiting the achievable performance at the lower THz band above 300 GHz. Hence, the impact of the layout implementation of the resistor and transmission lines of the Wilkinson combiner was investigated for the underlying three-metal-layer BEOL. For the optimization of the Wilkinson layouts discussed here, the *BEOL-B* variant is considered. Yet, the discussed findings also apply for the *BEOL-A* technology variant.

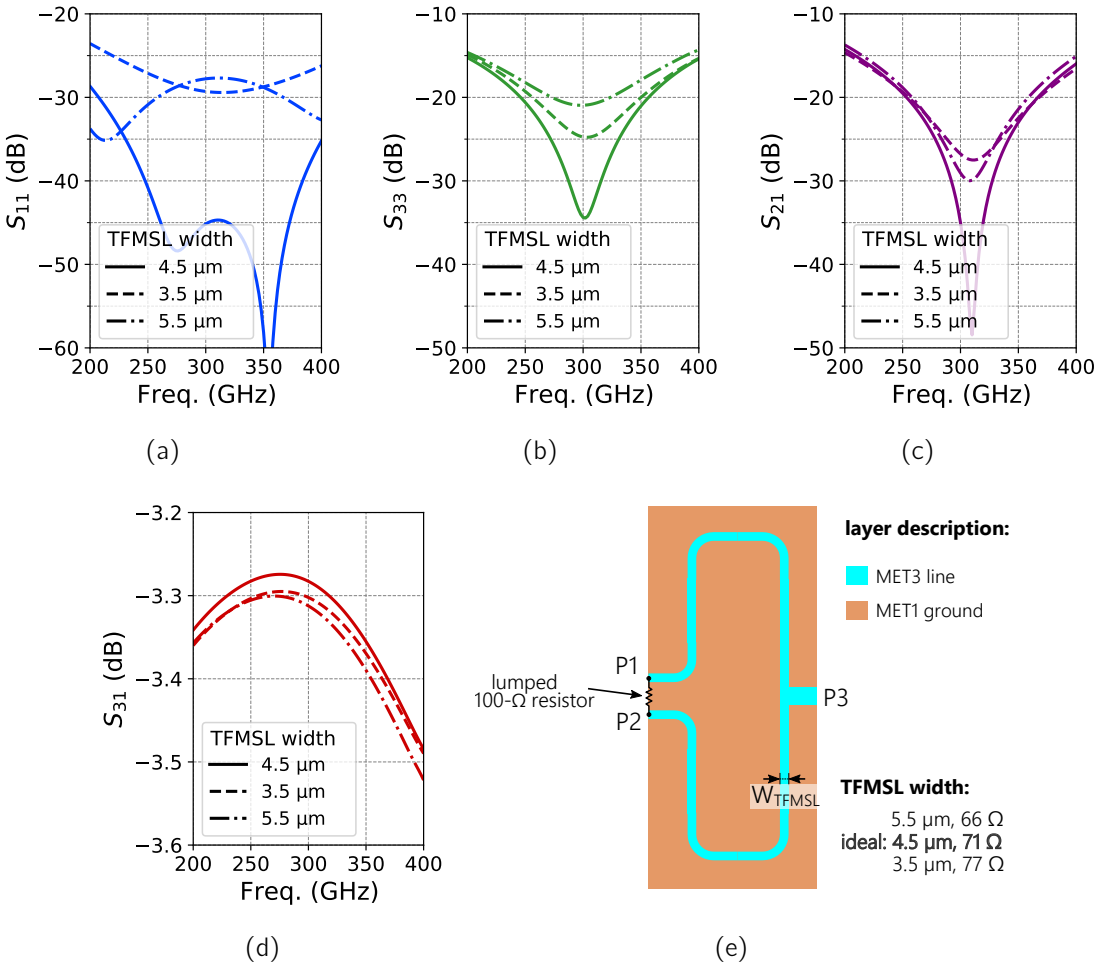


Figure 4.18: Simulated S-parameters of a MET3 TFMSL Wilkinson combiner with lumped isolation resistor. The solid lines represent the ideal case and the dashed and dash-dotted lines represent a worst-case line-width uncertainty of ±1 µm.

Impact of Transmission-Line Imperfections When using the *BEOL-B* variant, as discussed in Section 2.3, the 71-Ω transmission line should be implemented in elevated CPW or slow-wave TFMSL when using the final passivation for scratch protection. This way, the width of the thin-film line can be increased and the impact of width uncertainties of the *MET3 TFMSL* are decreased. When not using the BCB4 layer for final passivation, the *MET3 TFMSL* can be used with a very similar performance.

To evaluate the impact of a non-71-Ω impedance on the Wilkinson performance, the layout without isolation resistor depicted in Fig. 4.18(e) was simulated in CST. A lumped 100-Ω resistor was added in ADS to isolate the imperfections caused by the transmission line. The width of the 71-Ω TFMSL is 4.5 µm, as depicted in Fig. 4.18. This line width already includes the non-ideal MET3 shape, which was discussed in Section 2.3. To account for width uncertainties of the galvanic MET3 layer, transmission line widths in the range of 3.5 µm to 5.5 µm are considered, which corresponds to an impedance range of 66 to 77 Ω. This range covers the approximated worst-case spread of ±1 µm, which is considered here.

The simulated S-parameters of the *MET3-TFMSL* Wilkinson designed for 300-GHz operation with lumped resistor are depicted in Figs. 4.18(a)–4.18(d). In simulation, return loss as well as P1-to-P2 isolation is at least 25 dB over a 50-GHz bandwidth and at least 20 dB over a 100-GHz bandwidth around 300-GHz, respectively. The corresponding insertion loss is within 0.35 dB for 200–350-GHz frequencies. For the worst-case estimation of a 66-Ω line impedance, only the output return loss is significantly affected—providing, however, still at least 20-dB matching over the 275–325-GHz frequency band. For the *MET3 ECPW*, the width dependency is even improved. Hence, the *MET3 ECPW* as well as *MET3 TFMSL* permit the low-loss implementation of thin-film combiners, not limiting the combiners performance outside of the 0.3-dB insertion loss for the quarter-wave impedance transformation.

Impact of Isolation-Resistor Implementation When not assuming an ideal lumped resistor, as it is done above, the combiner results can be significantly deteriorated, even in simulation. To evaluate the impact of the layout implementation of the isolation resistor, the three layout variants R_{iso1}, R_{iso2} and R_{iso3} depicted in Fig. 4.19 have been investigated. The key differences between the three layout variants are the length L_{R} and width W_{R} of the 100-Ω isolation resistor as well as the length L_{stub} of the MET3 line, which is connecting the NiCr thin-film resistor (TFR) to the parallel 71-Ω lines of the combiner.

The R_{iso1} layout variant is requiring the largest chip area while featuring the most relaxed spacing between the *MET3-TFMSL* layout elements, using a 12-µm-long connection to the resistor (L_{stub}) and a 10x5-µm^2 100-Ω resistor. This layout variant has been implemented in the first-generation air-bridge and *MET3 TFMSL* Wilkinsons depicted in Fig. 4.17 and discussed above. R_{iso3} represents an optimized layout variant with both a small NiCr area as well as a short connection to the TFR. The resistor width W_{R} is set to the design-rule limit of 1.5 µm, resulting in the resistor length L_{R} of 3 µm. Since 3 µm is the minimum-spacing limit for the MET3 layer, the MET3 spacing is relaxed to 5 µm to account for the slight expansion of the galvanic top-metal layer. The parallel *MET3-TFMSL* lines are then directly routed next to the MET3-to-TFR via connection.

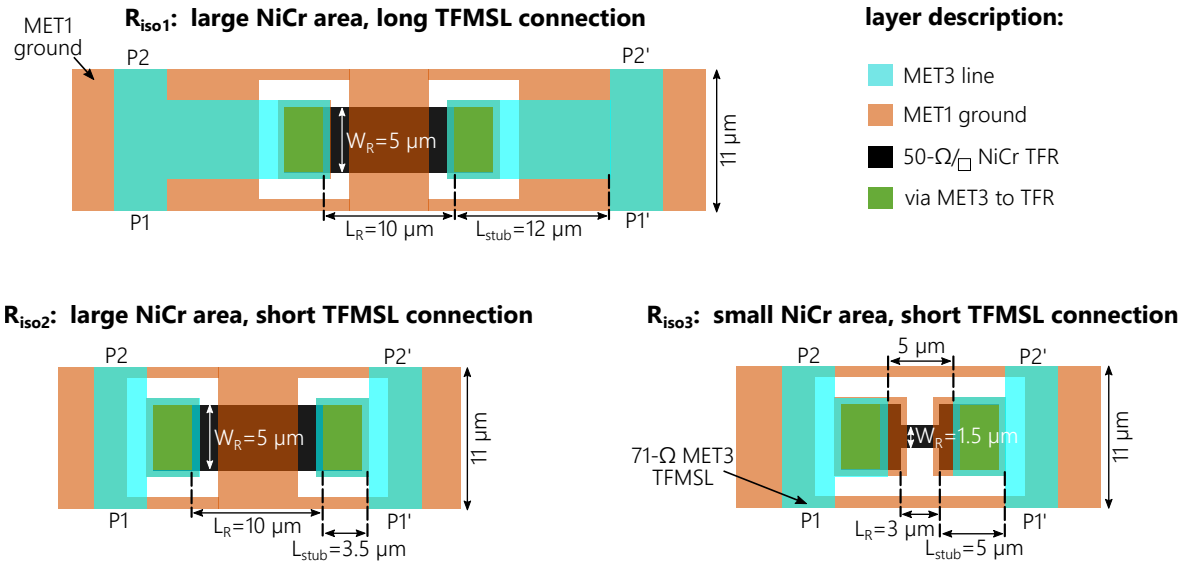


Figure 4.19: Three different isolation-resistor layout variants R_{iso1}–R_{iso3}. The main differences between the layout variants is the TFR area of the 100-kΩ isolation resistor (L_R, W_R) as well as the length L_{stub} of the connecting lines.

The R_{iso2} layout variant, on the other hand, includes the larger NiCr area of R_{iso1} and the short connection of R_{iso3}, to illustrate the impact of the corresponding layout elements.

The simulated S-parameters of the different isolation-resistor layout variants are summarized in Fig. 4.20. The depicted data represents the case of even-mode excitation—which corresponds to a simultaneous excitation—at the ports P1–P1' and also P2–P2', with a virtual open at the plane of symmetry. Hence, half of the TFR and its connecting MET3 line is acting as a lossy open-circuit stub. The parasitic impact of this stub on the S_{11} parameter can be seen in Fig. 4.20(a) and Fig. 4.20(b), respectively, which show the S_{11} magnitude and complex impedance range for the 200–400-GHz frequency band. The magnitude of the corresponding simulated S_{21} parameter is shown in Fig. 4.20(c). Due to the long connection to the TFR layer, the achievable matching and insertion loss for the R_{iso1} layout variant is strongly limited by the parallel capacitance of the lossy open-circuit stub. Hence, the corresponding return loss is only slightly above 10 dB at 400 GHz. The same behavior can be seen for the first-generation Wilkinson combiners depicted in Fig. 4.17, which use the R_{iso1} layout variant. The insertion loss of this layout variant is increasing to up to 0.8 dB at 400 GHz, strongly limiting its usability at the lower THz band around 300 GHz and above.

By reducing the length L_{stub} in the R_{iso2} layout, the parasitic parallel capacitance is reduced, as can be seen in Fig. 4.20(b), permitting improved matching and reduced losses. Further improvement is achieved, by minimizing the physical dimensions of the TFR to the design-rule minimum in the R_{iso3} layout, as described above. Using this layout implementation, a 20-dB match is achieved up to almost 400 GHz, reducing the introduced losses to less than 0.2 dB in simulation. The simulation results of the R_{iso3} layout excluding the TFR layout are also shown for reference, demonstrating how little of benefit a further TFR-size reduction would be.

To improve the matching at frequencies above 400 GHz, the parallel capacitance, which is introduced by the resistor and it's connection, needs to be compensated. This

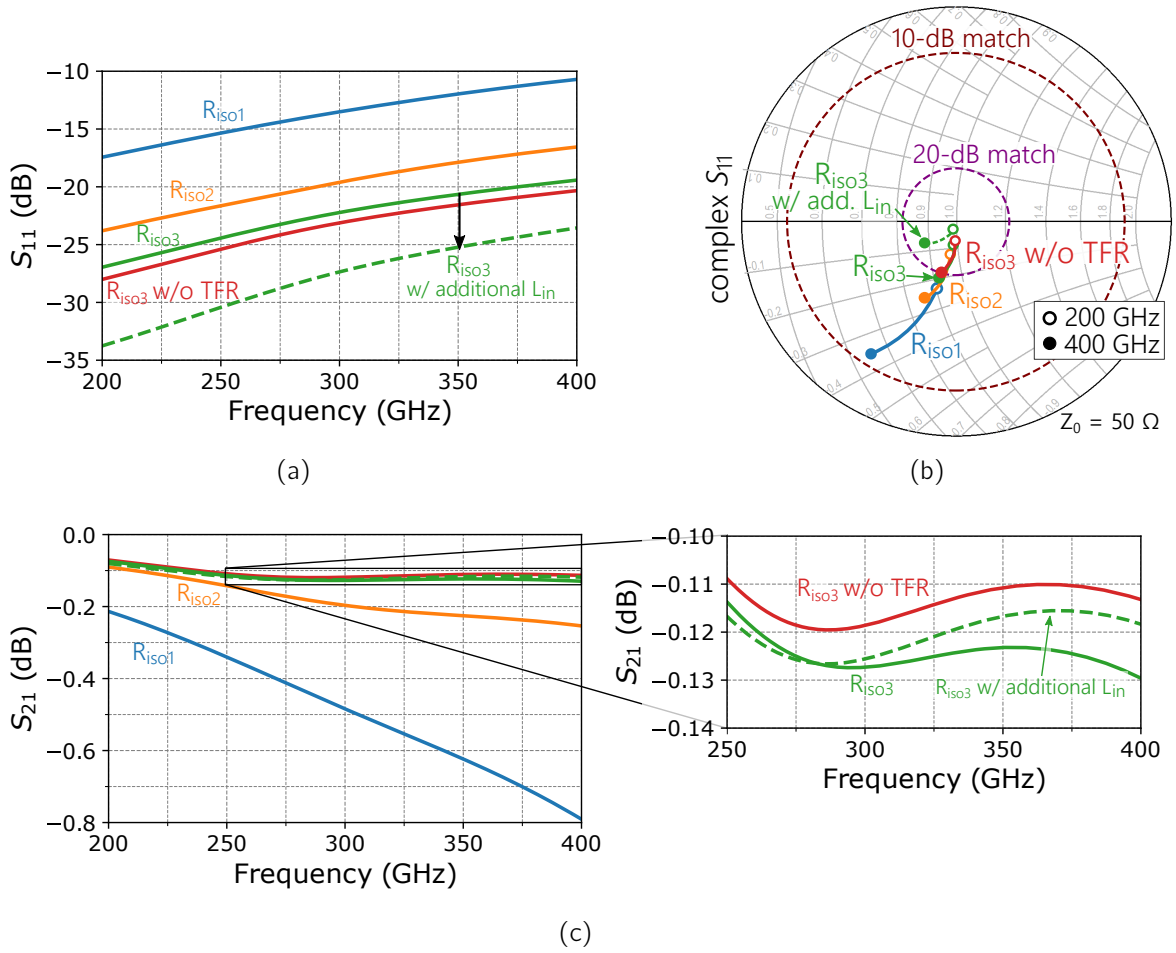


Figure 4.20: Simulated S-parameters of the three isolation-resistor variants, depicted in Fig. 4.19. R_{iso3} is additionally simulated without the NiCr layer (labeled as R_{iso3} w/o TFR) as well as including an additional 12-µm-long MET3 71-Ω TFMSL at the input ports (labeled as R_{iso3} w/ additional L_{in}). (a) and (c) show the magnitude of S_{11} and S_{21}, respectively. A close-up view of the complex input reflection coefficient (S_{11}) in the Smith chart is depicted in (b).

can be done by extending the high-impedance TFMSL at the input ports P1 and P1'—the corresponding simulation results are depicted in Figs. 4.20(a) and 4.20(b). By using the series inductance of an additional 12-µm-long 71-Ω TFMSL, the matching is significantly improved, permitting the implementation in combiner structures up to frequencies well above 400 GHz.

Optimized Thin-Film Wilkinson Combiners Using the optimized R_{iso3} layout variant described above, almost ideal Wilkinson-combiner performance can be achieved at 300 GHz. Fig. 4.21(b) shows the layout and simulated S-parameters of the optimized thin-film Wilkinson combiner. The transmission line can either be *MET3 TFMSL* without BCB4 or ECPW/slow-wave MET3 line including BCB4, showing similar performance in simulation. By implementing the R_{iso3} layout, 25-dB input matching is achieved up to 400 GHz. The P1-to-P2 isolation (S_{21}) as well as the output return loss S_{33} are better than 20 dB over a 100-GHz bandwidth around 300 GHz—which correspond to the ideal results depicted in Fig. 4.18, with lumped isolation resistor. Hence, the feasible 2-to-1

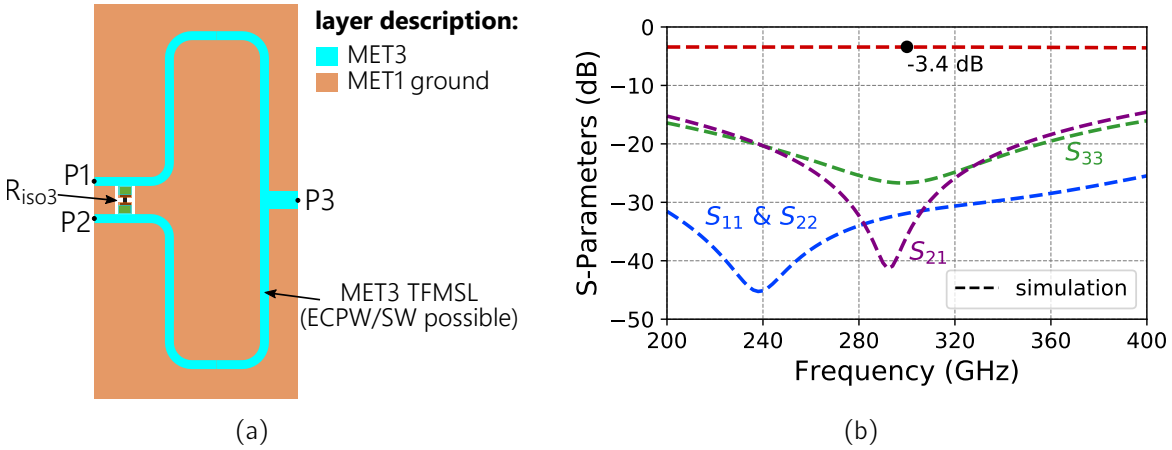


Figure 4.21: (a) Layout and (b) simulated S-parameters of an optimized 300-GHz TFMSL Wilkinson combiner, including the R_{iso3} layout variant with 12-µm-long high-impedance lines at the input ports P1 and P2. The transmission line can either be *MET3 TFMSL* without BCB4 or ECPW/slow-wave MET3 line including BCB4. Both show similar performance in simulation.

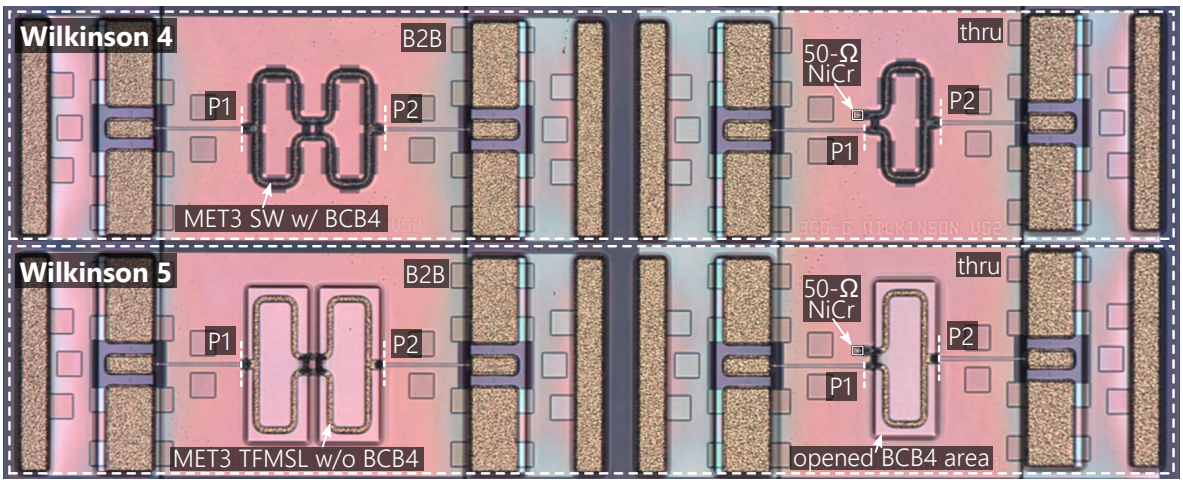
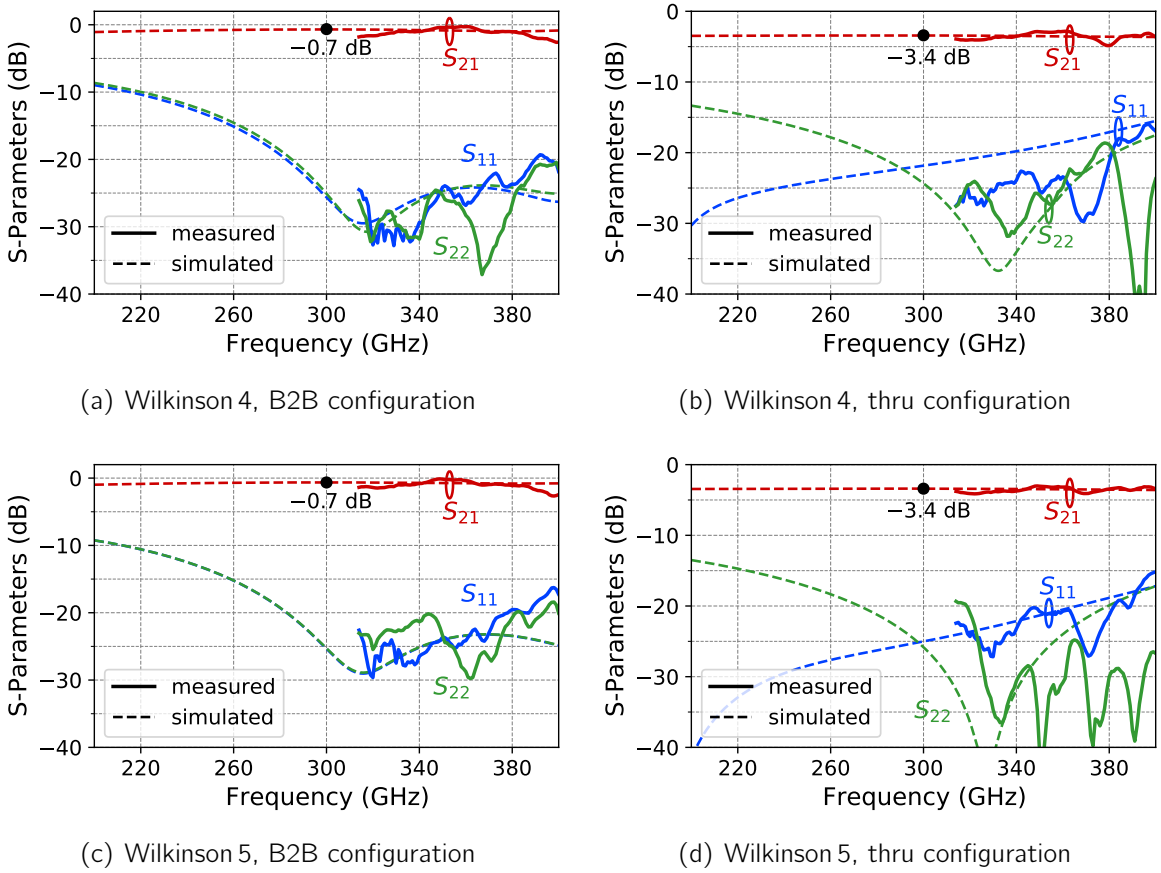


Figure 4.22: Chip photograph of thin-film Wilkinson test structures for on-wafer characterization. *Wilkinson 4* (top) is implemented with slow-wave *MET3 ECPW* including BCB4 and *Wilkinson 5* (bottom) is implemented with *MET3 TFMSL* without final passivation.

power-combining efficiency, which can be achieved with the 0.4-dB insertion loss around 300 GHz, is above 90 % with η=0.93.

To confirm the combiner performance by on-wafer measurements, the Wilkinson test field depicted in Fig. 4.22 was fabricated and characterized. The test structures include two different Wilkinson-combiner implementations, shown in back-to-back (B2B) configuration on the left as well as for through measurements on the right. *Wilkinson 4*—which is depicted on the top—is implemented with MET3 slow-wave transmission lines with 20-µm ground-to-ground spacing and 1-µm stripe-to-stripe spacing, as described in Section 2.3.3, and *Wilkinson 5* is using the *MET3 TFMSL* without the final passivation BCB4. Apart from the different TFMSL environments—which is used for the 71-Ω quarter-wavelength transformation—both combiners are implemented with the optimized isolation resistor described above.



(a) Wilkinson 4, B2B configuration

(b) Wilkinson 4, thru configuration

(c) Wilkinson 5, B2B configuration

(d) Wilkinson 5, thru configuration

Figure 4.23: Measured and simulated S-parameters of the Wilkinson test structures depicted in Fig. 4.22.

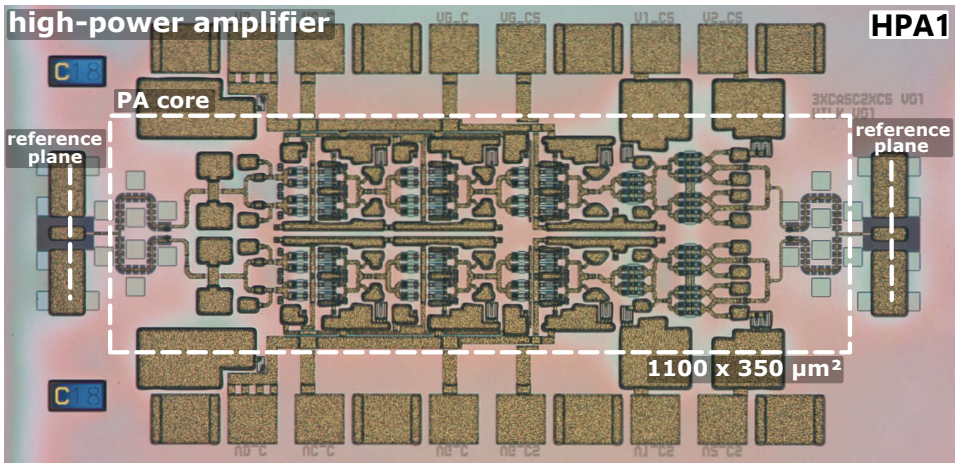
The simulated and measured S-parameters of the Wilkinson test structures are depicted in Fig. 4.23, showing a very similar performance in terms of insertion loss and return loss for both combiner variants. Broadband matching is achieved, demonstrating return-loss figures above 20 dB over the measured Y-band frequency range from 315 to at least 380 GHz. The simulated single-combiner insertion loss—which corresponds to the absolute S_{21} values of the through configurations (Fig. 4.23(a), Fig. 4.23(c)) minus approximately 3 dB—is better than 0.6 dB over the frequency band from 200 to 400 GHz, with a minimum of 0.4-dB at 300 GHz. Based on the depicted measurement results—which are in overall agreement with the simulation to a very good extend—this 300-GHz insertion-loss range of 0.4 to 0.5 dB is achieved in measurement, verifying the simulated stand-alone-combiner S-parameters depicted in Fig. 4.21(b).

The S-parameter data depicted in Fig. 4.23 demonstrate, furthermore, that a very similar performance is achievable with the slow-wave *MET3 ECPW* as well as the *MET3 TFMSL* when considering their implementation in power combining networks. This corresponds to the TFMSL data discussed in Section 2.3.3. While the electrical length of the slow-wave *MET3 ECPW* is increased—as can be seen with the reduced length of the quarter-wavelength ECPW lines in Fig. 4.22 (top)—its main advantage is the feasibility of high-impedance transmission lines including the top-BCB layer for scratch protection and final passivation. This is at least true in combining networks, where the physical dimensions of the transmission lines are not relevant.

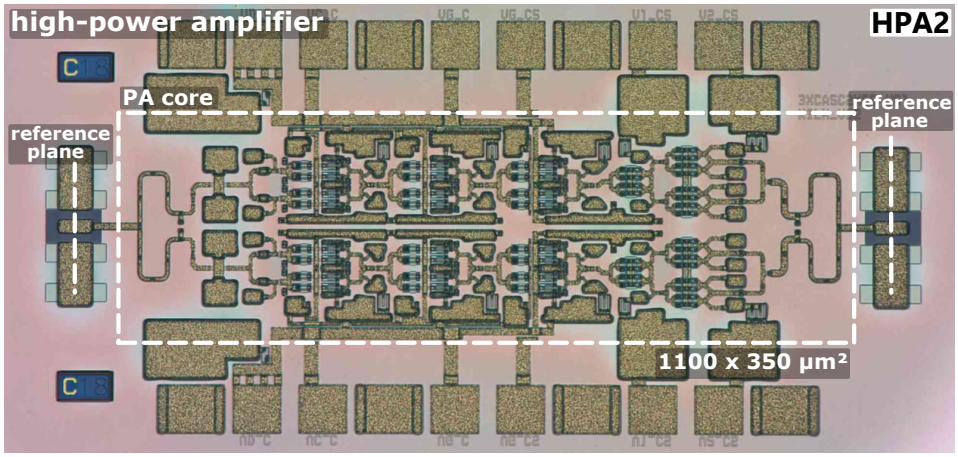
4.4 300-GHz High-Power Amplifier MMICs

Based on the compact UA cell *UPA1* discussed in Section 4.2.2 as well as the Wilkinson power combiners of Section 4.3, high-power amplifier MMICs have been developed and fabricated. The two PA circuits *HPA1* and *HPA2*, which have been designed and processed in the *BEOL-A* technology variant, are depicted in Fig. 4.24. Since the air-bridge BEOL was used for these PA MMICs, the Wilkinson combiners *Wilkinson 1* and *Wilkinson 2* of Section 4.3—which have been developed for the air-bridge top-metal layer variant—were implemented. *HPA1* is using *Wilkinson 1* to parallelize the UA core, and *HPA2* was implemented using *Wilkinson 2*. Both PA cores require a total chip area of approximately $0.35 \times 1.1\,\mathrm{mm}^2$, including all matching networks and the first stage of shunt capacitors in the bias insertion network and excluding RF/DC-pads.

The total gate-width in the output stage, which is implemented with this topology on only 0.35-mm required chip width, is 512 µm. As discussed in Section 4.2.2, vertical DC-bus interconnections have been implemented in the five-stage UA cell, to distribute the

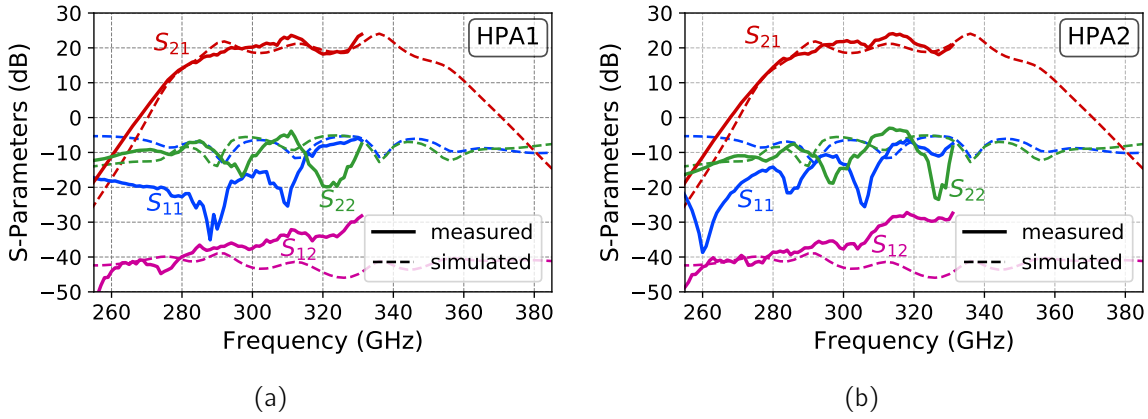


(a)



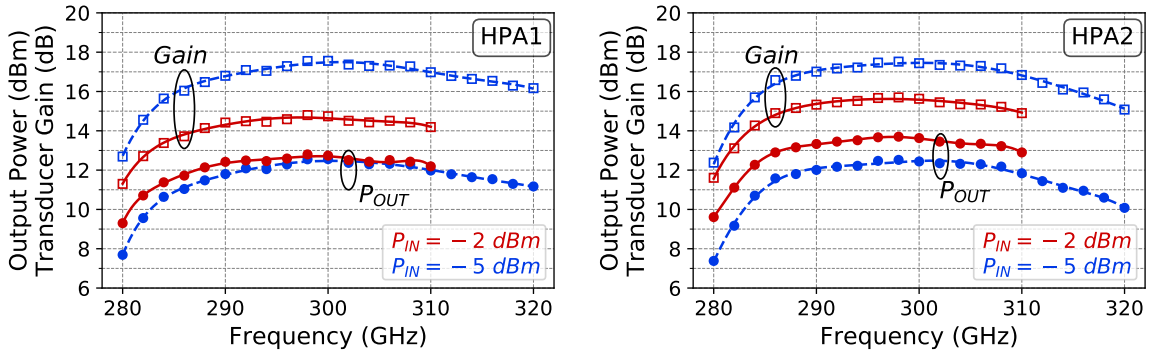
(b)

Figure 4.24: Chip photographs of the fabricated PA MMICs *HPA1* and *HPA2*. The required chip area of the 5-stage PA core is $0.35 \times 1.1\,\mathrm{mm}^2$. These amplifiers use the Wikinson power combiners shown in Fig. 4.17 to parallelize the UA cell depicted in Fig. 4.10.



(a) (b)

Figure 4.25: Measured and simulated S-parameters of the 5-stage MMICs *HPA1* and *HPA2*. The simulation includes a simple model to account for the poor on-wafer isolation between input and output.



(a) (b)

Figure 4.26: CW measured transducer gain and output power of the (a) *HPA1* and (b) *HPA2* MMIC between 280 and 328 GHz with 2-GHz step size at −5-dBm and −2-dBm input power.

bias voltages across the parallelized UA cells. The *HPA1* and *HPA2* MMICs discussed here do not use this feature—but the bias of the parallel UA cells is separated and supplied from both sides using two DC pads. Single-side biasing of 300-GHz high-power amplifier MMICs, which have been developed based on these PA cells, is demonstrated with the packaged PA circuits in Section 5.2.

Measurement Results The measured S-parameters of *HPA1* and *HPA2* are depicted in Fig. 4.25. Both amplifiers achieve a measured small-signal gain around 20 to 25 dB for the frequency range above 290 GHz. The observed gain ripple is mainly due to the poor isolation of the on-wafer measurement setup.

The measured transducer gain and output power of *HPA1* and *HPA2* are shown in Figs.4.26(a) and 4.26(b), respectively—measured at a constant input power versus frequency. Depicted are the results at –5-dBm as well as at –2-dBm input power. The CS devices in the output stages of *HPA1* and *HPA2* were biased with 1.3 V drain-source

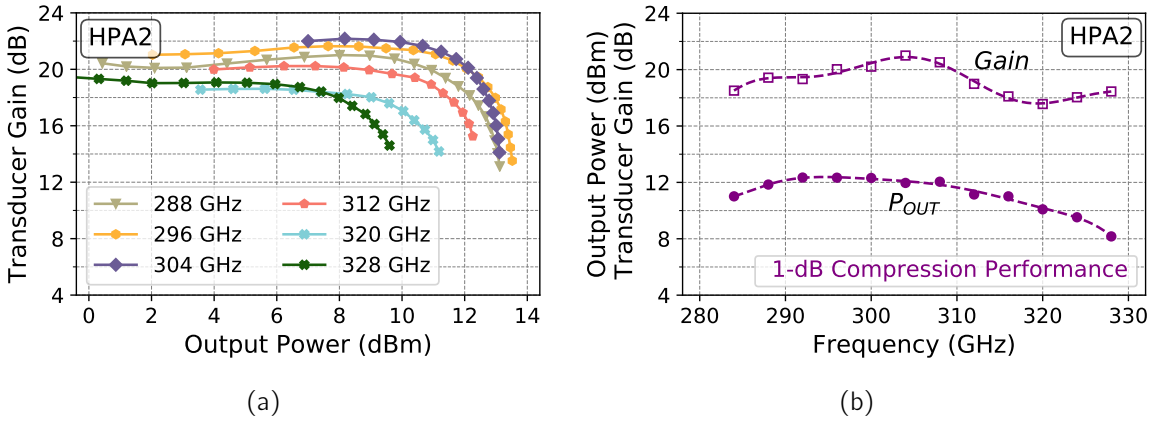


Figure 4.27: (a) Measured transducer gain vs. measured output power of *HPA2* between 284 and 328 GHz with 8-GHz step size and (b) CW measured transducer gain and output power at 1-dB gain compression of the *HPA2* MMIC versus frequency.

voltage and the cascode cells with 2.4 V, resulting in a V_{DS} of 1.2 V per device. Hence, the overall DC-power (P_{DC}) consumption is approximately 1.1 W.

The measured maximum output power level of PA1 is 12.9 dBm, measured at 300 GHz. *HPA2* achieves up to 13.7 dBm measured output power around 300 GHz and at least 13 dBm over the 286–310-GHz frequency range. Both the UA and the high-power amplifier MMICs have been measured on the same wafer. Despite the additional combiner loss, the measured output power level of *HPA1* and *HPA2* is increased by more than 3 dB. This is in large part due to the 100-µm long *MET2 TFMSL* port extension between the RF-pads and the input/output of the UA core *UPA1*, as depicted in Fig. 4.10. This port extension is introducing additional losses of approximately 0.8–1.0 dB at the output which are included in the *UPA1* measurement data.

To understand the enhanced output power performance of the *HPA2* MMIC, in contrast to the *HPA1* MMIC, multiple factors such as minor layout differences and device spread need to be considered. The combiners of both MMICs show a very similar performance in terms of measured and simulated insertion loss around 300 GHz—the connection to the RF pad, however, differs for both PA MMICs. While the *HPA2*-combiner's output is directly connected to the RF pad using a low-loss MET3 air-bridge, this output-port connection is implemented in a lossy *MET2MET3 TFMSL* for the *HPA1* MMIC. Additionally, since the two Wilkinson combiners do not show a perfect 50-Ω load to the parallelized UA cells, the load at device level in the output stage differs on a small scale between the amplifiers *UPA1*, *HPA1*, and *HPA2*.

Fig. 4.27(b) shows the measured transducer gain versus output power for CS operation of *HPA2*. The frequency was swept from 284 to 328 GHz with 2-GHz step size. Alongside high output-power levels above 13 dBm, the power amplifier also shows a good linearity and compression behavior. The measured OP_{1dB} 1-dB gain compression power of *HPA2* is above 10 dBm over the 284–316-GHz frequency band, achieving a maximum OP_{1dB} of 12 dBm at 20-dB gain around 300 GHz, as shown in Fig. 4.27(b).

4.5 Discussion and Conclusion on Chapter 4

This chapter describes the design and implementation of broadband 300-GHz PA MMICs, based on a compact unit amplifier cell and loss-optimized thin-film Wilkinson combiners. As a result of the device-level-related considerations discussed in Chapter 3, a unique "power-bar-like" topology was developed, based on chip-size-optimized 8-finger cascode and common-source devices. Due to their superior output-power performance—when considering the chip width which is required for the implementation of the multi-finger devices—CS devices have been implemented in the output stages and cascode gain cells in the input stages of the unit-amplifier cell (*UPA1*). This innovative topology significantly improved the output power per chip width by a factor of 4 in comparison to stand-alone cascode circuits (*CPA2*). The multi-finger devices were modeled and simulated using highly parallelized two-finger devices in close proximity, which allows for a broadband matching while maximizing the total gate width on the smallest chip size possible.

To enable efficient on-chip power combining at 300 GHz, novel thin-film Wilkinson combiners have been investigated and implemented. High-impedance air-bridge TFMSL and ECPW interconnections were successfully implemented for usage in the *BEOL-A* technology variant and layout considerations as well as limitations of the thin-film combiners were investigated. The isolation-resistor implementation was identified and optimized as the most crucial layout element—demonstrating 300-GHz combiners with 0.4 to 0.5-dB insertion-loss, which is an significant improvement of at least 0.4 dB in comparison to prior published CPW combiners and couplers in this technology [4, 6, 87]. A detailed summary and comparison of on-chip power combiners in the 300-GHz band are given in Appendix A.3.

With the developed modeling and design approach, a total output gate width of 512 µm is implemented on an ultra-compact chip width of only 0.35 mm, demonstrating high integration density and allowing further monolithic on-chip and module integration. The achieved output-power levels of more than 13 dBm around 300 GHz are in detail compared to the state of the art in the following paragraph.

Comparison to the State of the Art Fig. 4.28 shows an overview of state-of-the-art power amplifier MMICs and modules covering the 270–350-GHz frequency range. The depicted results include this work's published PA MMIC results [52, 55, 56] in comparison to other SSPA circuits in InGaAs mHEMT technology, a selection of InP HBT MMICs as well as two InP HEMT based modules. The packaged results in [40, 87, 106] include the loss of the MMIC to waveguide transition, which is typically around 1 dB and is not subtracted in this discussion. A detailed summary of the depicted amplifiers in tabular form, including additional PA figures such as the DC-power consumption as well as power-added efficiency (PAE), is given in Appendix A.1.

When considering the absolute measured output-power level, which is depicted in Fig.4.28(a), the *HPA1* and *HPA2* MMICs [55] achieve state-of-the-art output-power performance. A record peak output power of 24 mW (13.8 dBm) is demonstrated at the lower THz band for solid-state amplifiers. Furthermore, for the first time, more than 20 mW (13 dBm) of output power are achieved over an outstanding bandwidth of 25 GHz

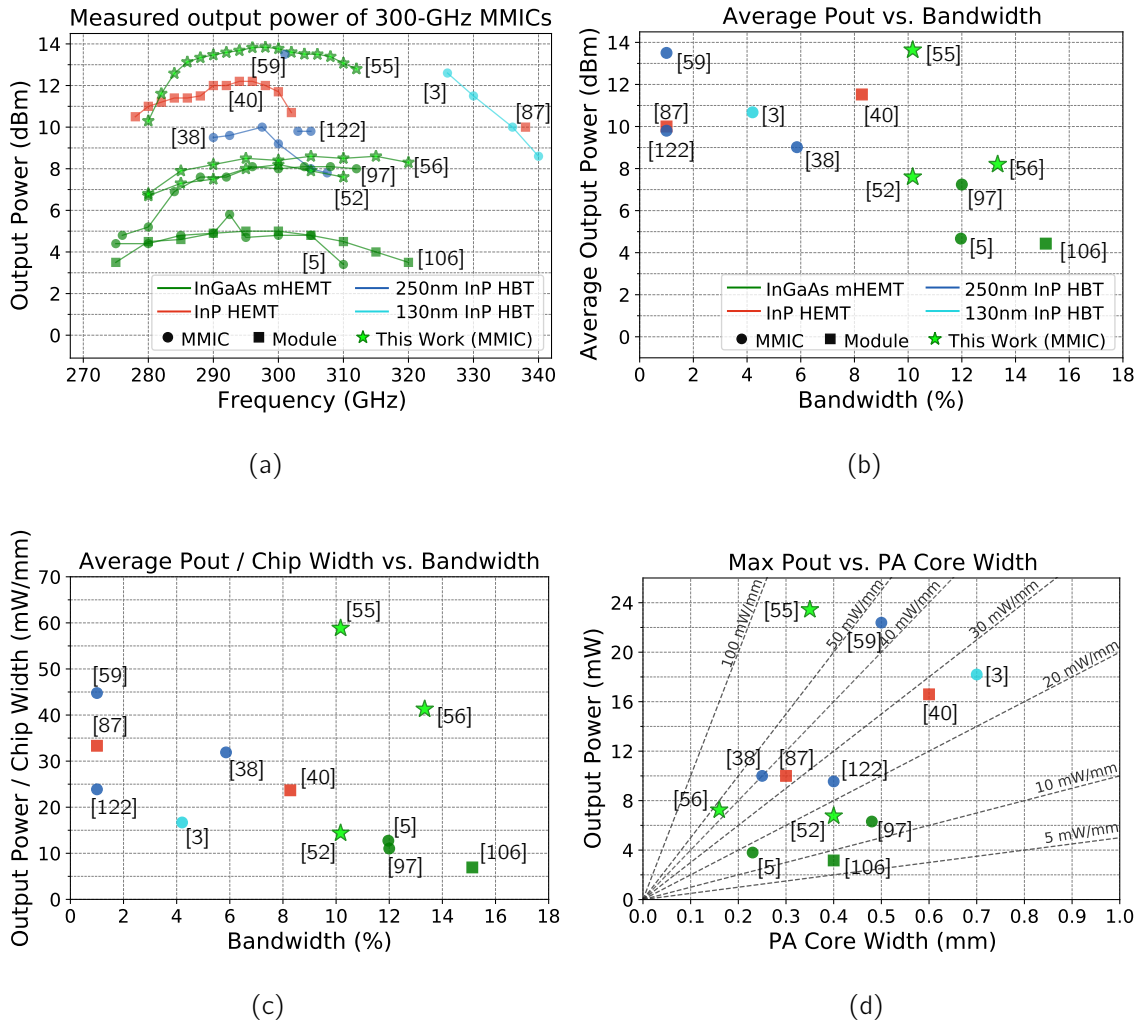


Figure 4.28: Comparison of state-of-the-art power amplifiers around 300 GHz. The measured (average) output power versus frequency and bandwidth is depicted in (a) and (b), respectively—while (c) and (d) take the required chip width of the PA cores into account, considering the chip-width efficiency of the depicted PA results.

around 300 GHz. In comparison, InP HBT SSPAs have demonstrated up to 13.5 dBm in [59], measured at only a single frequency of 301 GHz and biased at a significantly higher single-device voltage of 2.2 V.

This general trend of superior bandwidth of InGaAs mHEMT PA circuits is also depicted in Fig. 4.28(b), which shows the average measured output power versus the corresponding fractional bandwidth. While InP-HBT PA results have demonstrated output-power performance above 10 dBm, the demonstrated bandwidth is significantly below 10 %. This work's high-power amplifier circuits, on the other hand, demonstrate broadband large-signal performance at significantly increased output power levels in [55]. In comparison to the prior state of the art in the underlying mHEMT technology [5, 97, 106], the demonstrated output-power level is notably improved by 6 to 9 dB—which corresponds to a tremendous improvement by a factor of 4 to 8. The output-power level in excess of 10 dBm was measured over a bandwidth exceeding 40 GHz—reporting for the

first time more than 10 mW at THz frequencies in a HEMT based technology at the time of publication [55].

The objective of achieving high output power over a large bandwidth at a narrow chip width was stressed as a major design goal for the developed multi-finger devices and power amplifier topology, respectively. To evaluate this improvement, Fig. 4.28(c) shows the average output power normalized to the required chip width of the PA circuits. This work's outstanding output power per required chip width on MMIC level of almost 60 mW/mm is the only reported result with more than 50 mW/mm. Compared to previously published power amplifiers in the same mHEMT technology [5, 97, 106], the output power per chip width is increased by a factor larger than 4. This improvement can be attributed to the novel topology and modeling approach developed in this thesis, which enables a massive parallelization of gate fingers at the smallest chip size possible. While each of the prior realized cascode [5, 106] and common-source [97] topologies were implemented with a total of 8 transistor fingers in the output stage—requiring a chip width of 0.22 to 0.48 mm—*HPA1* and *HPA2* include 32 parallel transistor fingers with a total gate width of 512 µm on only 0.35-mm PA-core width.

Hence, enabled by the extensive investigations regarding the device level, the configuration of the active devices, and the thin-film wiring possibilities which are discussed in Chapter 2 and Chapter 3, broadband state-of-the-art performance around 300-GHz is demonstrated with the developed PA MMICs. At the same time, the PA core dimensions are significantly reduced in comparison to other 10–13-dBm power amplifier circuits [3, 40, 59]. These highly-compact chip dimensions are a key feature for the success of the assembly, which is described in the following chapter.

5 300-GHz Power Amplifier Waveguide Modules

To reduce packaging losses and achieve the best in-package performance out of mm-wave and sub-mm-wave amplifiers, waveguide packages are typically used for stand-alone amplifier circuits. The packaging technology used for the assembly of the developed power amplifier MMICs into waveguide modules, is Fraunhofer IAF's split-block packaging technology. MMIC to WR-3.4 waveguide transitions were used, which comprise an E-field-probe based waveguide transition, as described in [111]. This packaging technology has been successfully implemented with external quartz transitions as well as integrate transitions on GaAs substrate in low-noise and power amplifiers up to 600 GHz [108] and is described in detail in Appendix D.

The power amplifier circuits of the previous chapter were developed for on-wafer characterization only. Hence, most of the discussed results have been measured before back-side processing and wafer thinning, in order to reduce the required time of the design cycles. This chapter describes the results of the packaged 300-GHz power amplifiers (Section 5.2). In order to realize the packaging of the compact PA MMICs, the backside process including wafer thinning and through-substrate vias (TSVs) is required. Therefore, requirements for the implementation of through-substrate connections in compact 300-GHz TFMSL PA cells was investigated [53] and is described in the following.

5.1 Considerations for Via Placement in Compact THz MMICs

A backside process, including wafer thinning and TSVs, is typically required in III-V IC technologies to suppress unwanted substrate modes when using substrate-based microstrip and grounded coplanar interconnects [44, 118] Since the developed power amplifiers are implemented with miniaturized thin-film microstrip lines including a closed MET1 ground plane on the wafer front side—which only needs to be opened around active devices and NiCr resistors—through-wafer connections are actually not required for the functionality of these backside-free TFMSL matching networks, when only considering the on-wafer performance. However, TSVs are nonetheless required for the implemented MMIC to waveguide transition. This requirement is discussed in detail in Appendix D. Furthermore, when considering MMIC packaging, a via cage is typically required at the die edge to suppress in-package resonances within the cavity of the waveguide module.

Since the dimensions of TSVs are typically in the same order of magnitude as the substrate height—which is 50 µm in the underlying technology for usage around 300 GHz—the via dimensions, in relative terms, increase in size in comparison to the shrinking device

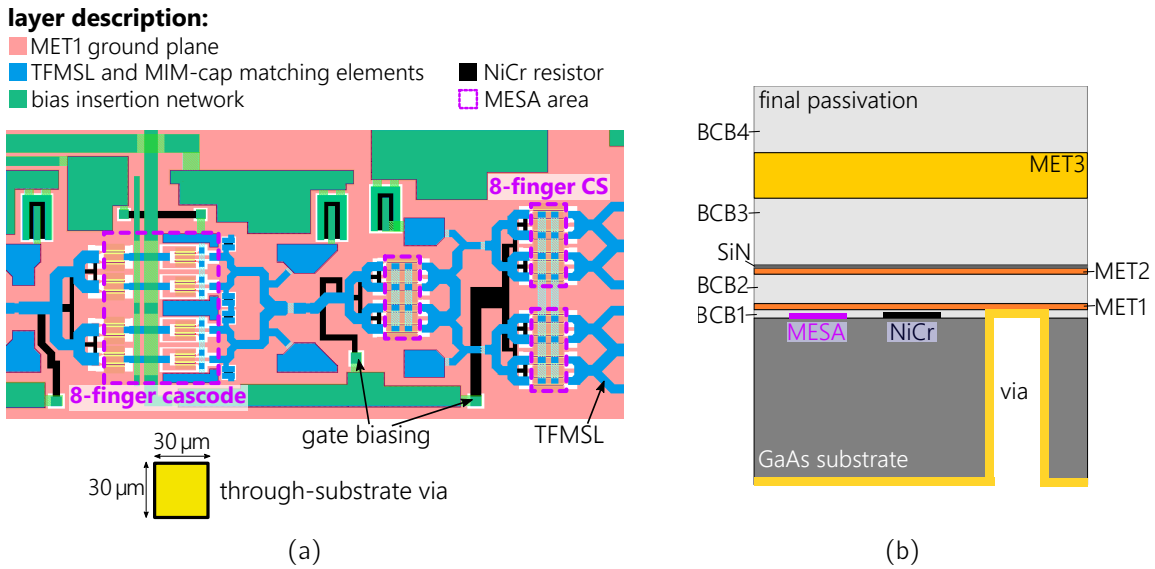
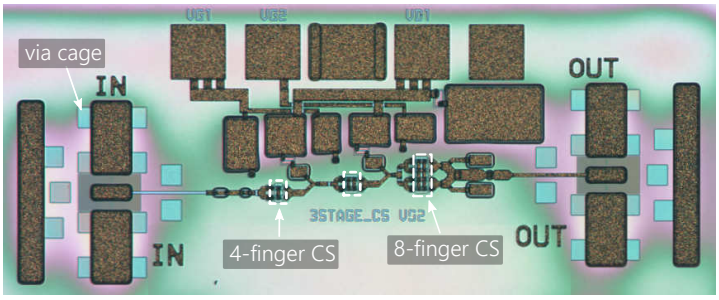


Figure 5.1: (a) Layout of an 8-finger cascode stage and two CS stages. (b) Simplified schematic cross-section (not to scale) of the InGaAs mHEMT IC thin-film wiring environment on GaAs substrate.

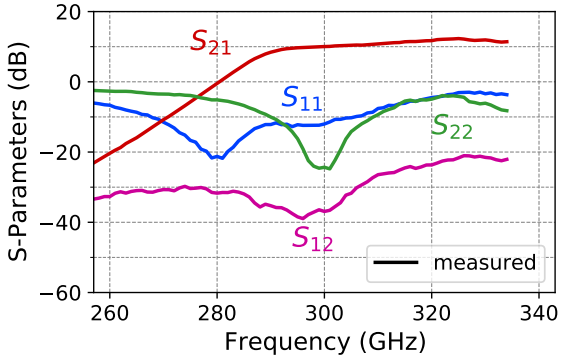
and matching network dimensions at frequencies around and above 300 GHz. Hence, the chip area in which vias can be implemented becomes limited between closely cascaded and parallelized devices.

This limited chip area for via placement can be seen in Fig. 5.1(a)—which shows a close-up view of the unit-amplifier cell *UPA1* developed in Section 4.2.2, including the last 8-finger cascode stage and the two common-source output stages. NiCr thin-film resistors, which are implemented in the bias-insertion network, are depicted in black color and matching elements like TFMSL interconnections and MIM capacitors, which are relevant for the RF signal, are shown in blue color. The 30x30-µm^2 chip area which would be required for a through-substrate connection is shown below the layout. The dimensions of the devices, networks and TSV are true to scale. Furthermore, the most relevant design-rule limitations for via implementation can be derived from the BEOL layer stack shown in Fig. 5.1(b). Since MET1 is required as etch stop during the TSV processing, an overlap with the MESA or any NiCr thin-film resistors must be avoided, which limits the via-implementation possibilities for such compact circuit topologies with high device density. By applying the gate bias via the NiCr layer—which was routed in the depicted tree structure in order to ensure symmetrical voltage distribution—the limited space between the active multi-finger devices is further decreased.

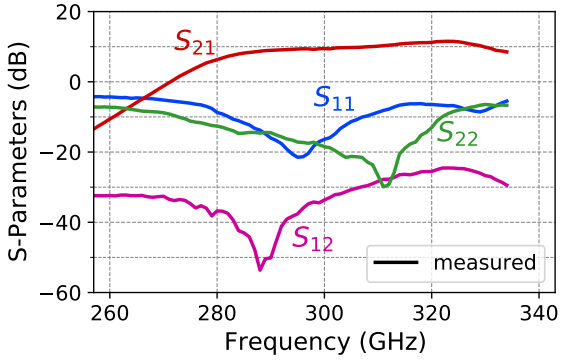
Therefore, due to the limited space for via implementation in the developed PA circuits with high device density, the vias cannot be simply implemented once the design process of the amplifiers has been finished. Whether vias need to be implemented within the active circuit of TFMSL circuits was found to be dependent on the implemented circuit topology and device configuration. Fig.5.2(a), for example, shows the chip photograph of a three-stage 300-GHz amplifier circuit, implemented with multi-finger devices in CS configuration. There are no vias within the active circuit area—only the whole chip die (which is not depicted here) as well as the RF pads are surrounded by a via cage. Thus,



(a) Chip photograph



(b) Thick wafer



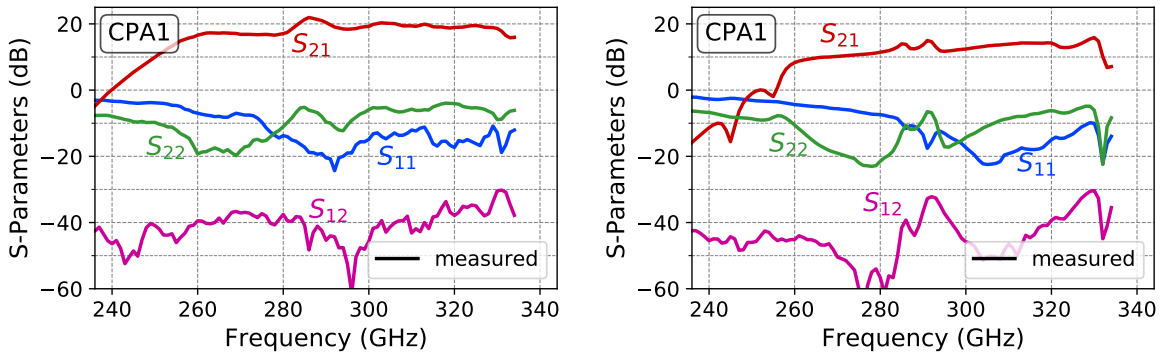
(c) After backside processing

Figure 5.2: (a) Chip photograph and (b, c) measured S-parameters of a three-stage 300-GHz CS amplifier MMIC without TSVs within the active circuit area. The S-parameters were measured on an (b) unthinned wafer, as well as (c) after backside processing.

after the back-side processing, the RF signal can only be coupled into the GaAs substrate at the MET1 opening around the active devices.

The S-parameter characteristics of the three-stage amplifier before and after backside processing are shown in Figs.5.2(b) and 5.2(c), respectively. On-wafer measurements of TFMSL circuits on unthinned wafers—which do not include any TSVs—typically show the ideal circuit behavior with good accuracy, since any RF-power which is coupled into the substrate, is dissipated in the "infinitely" wide substrate. Both the thick-wafer as well as the thinned-wafer measurements, however, show a flat gain response and show no indication of substrate resonances.

Based on these results—as well as several other CS and cascode thin-film-circuit results at lower frequencies [51, 75], which indicate, that no vias are required within the active circuit area of TFMSL circuits in this technology—no vias had been implemented in the compact amplifier cells discussed in Chapter 4. This can be seen in the chip photographs shown in Chapter 4, which only include the via cage around the RF pads as well as the die edge. For these multi-finger cascode topologies, resonant behavior was observed after wafer thinning. This is shown in Fig. 5.3, which depicts the S-parameter characteristics of the four-stage cascode PA circuit *CPA1* described in Section 4.2.1. The thin-wafer measurements show a significantly different behavior, compared to the thick-wafer measurements, showing decreased small-signal gain as well as dips and peaks in the measured small-signal response.



(a) Thick-wafer

(b) After backside processing

Figure 5.3: S-parameters of the four-stage cascode PA MMIC *CPA1* discussed in Section 4.2.1, which have been measured (a) before and (b) after wafer thinning and backside processing.

Since these results indicate topology dependent via-placement requirements, different via-placement scenarios were investigated experimentally, in order to define the requirements for via placement within the IC design process of compact TFMSL PA cells. Furthermore, a simulation model was developed, which permits to consider the via placement as a part of the design process described in Section 4.1.

5.1.1 Experimental Investigation of Via Placement

Fig. 5.4 shows the chip photographs of a 4-stage PA cell [56], consisting of three cascode devices and one CS stage. In order to experimentally investigate the impact of inter-device coupling and resonances in the GaAs substrate, three different via-placement scenarios (VS1–VS3) were considered:

(1) VS1: there are no vias at all underneath the PA core, only around the RF pads and at the die edge, as depicted with the vias highlighted in blue in Fig. 5.4.

(2) VS2: in addition to the VS1 snenario, vias are placed as close as possible to the active devices but not within the interstage matching networks, forming the depicted via cage with vias highlighted in red in Fig. 5.4 (b).

(3) VS3: the vias highlighted in yellow in Fig. 5.4 (b) are added between the active devices, in addition to the vias of VS2.

In each scenario, the whole MMIC as well as the RF pads within the MMIC are surrounded by a via cage, with the result that RF power can only be coupled into the GaAs substrate at the MET1 opening around the active devices. The on-wafer measured S-parameters of the 4-stage PA MMIC before backside processing (thick wafer), as well as for the three via-placement scenarios described above, are shown in Fig. 5.5. In the case of the unthinned-wafer measurement, the small-signal gain is around 20 dB over the 280–350-GHz frequency range, showing a flat gain response. The ripple at the upper H-band frequencies around 320 GHz is mainly caused by the poor isolation of the on-wafer

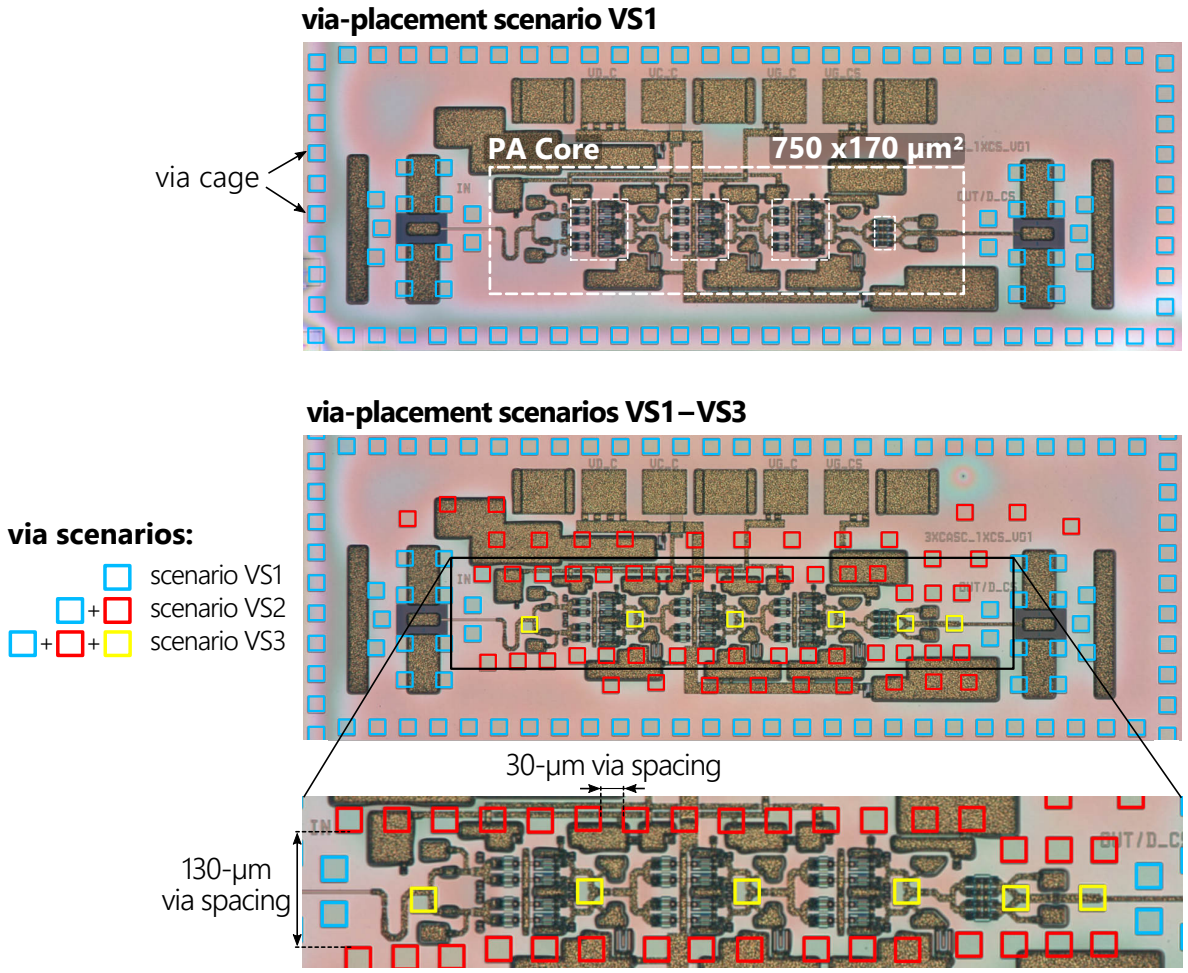
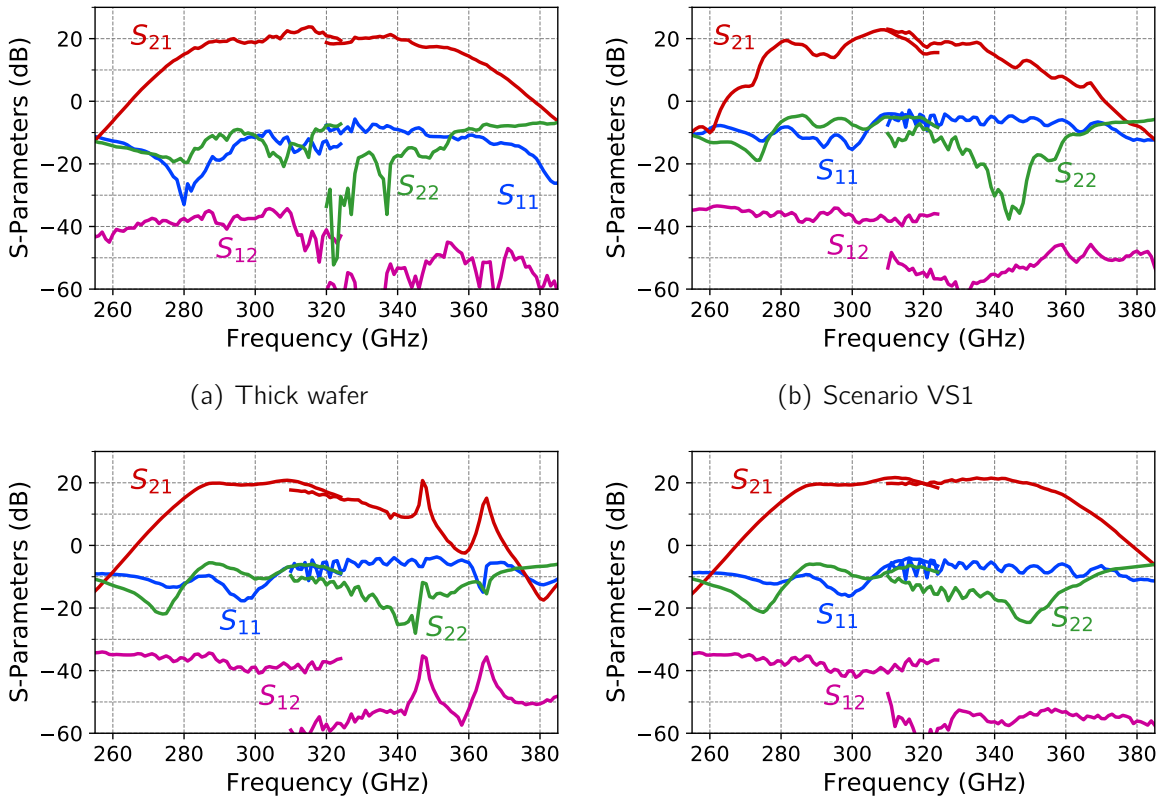


Figure 5.4: Chip photographs of the compact 4-stage PA MMICs with three different via placement scenarios: (1) via scenario VS1 with a via cage at the die edge and around the RF pads (vias highlighted in blue), (2) via scenario VS2 uses additional vias around the PA core (vias highlighted in blue + red), and (3) via scenario VS3 includes additional vias between the active devices (vias highlighted in blue + red + yellow).

measurement setup. In case of the thick-wafer measurements, the same S-parameter characteristics were measured independent of the different via implementation.

When comparing the on-wafer measurement results of the three different via-placement scenarios after back-side processing, a strong dependency of the gain flatness on the via placement is observed—indicating resonant inter-device coupling through the GaAs substrate for the scenarios VS1 and VS2. While the via cage highlighted in red in Fig. 5.4 (VS2, 30-µm via-to-via spacing) sufficiently suppresses the resonances observed in Fig. 5.5 (b) up to 320 GHz, the additional TSVs between the active devices (highlighted in yellow) are still required to avoid resonances at higher frequencies.

As depicted in Fig. 5.5 (c), the measured S_{21} magnitude of VS2 decreases at frequencies around 320 GHz, showing resonances above 340 GHz. The VS3 measurements, on the other hand, show the same flat gain response as the unthinned measured S-parameters, providing a flat 20-dB small-signal gain over the 280–350-GHz frequency range.



(a) Thick wafer (b) Scenario VS1

(c) Scenario VS2 (d) Scenario VS3

Figure 5.5: Measured S-parameters of the 4-stage PA MMICs depicted in Fig. 5.4: (a) measured before backside processing, (b) VS1, (c) VS2 and (d) VS3.

The spacing between the VS2 vias (red vias in Fig. 5.4) is limited to 120–130 µm by the width of the 8-finger cascode devices—forming a GaAs-loaded waveguide underneath the TFMSL PA core. The lower cutoff frequency of a loaded rectangular waveguide is given in [85] and can be calculated by

$$f_c = \frac{c_0}{2a\sqrt{\epsilon_r}}. \tag{5.1}$$

With the speed of light $c_0 = 2.998x10^8$ m/s, the dielectric constant of GaAs $\epsilon_{r,GaAs} = 12.9$ and the width of the loaded waveguide $a = 120$–130 µm, the cutoff frequency for the TE_{10} mode is in the range of 321 GHz to 348 GHz. This frequency range corresponds to the lower end of the frequency range with resonant behavior, which is observed for the cascode PA MMIC without TSVs between the active devices (VS2). These results, furthermore, stress the necessity of the VS3 vias, which are required to suppress through-substrate coupling between the cascaded active devices and avoid the resonances observed in Fig. 5.5(c).

The results discussed here show, that the implementation of vias is necessary to avoid substrate resonances and inter-device coupling, which is most crucial in TFMSL circuits using cascode devices. The resonances observed in the cascode circuits are mainly due

to the larger MET1 ground-plane opening, which is required for common-gate devices, in comparison to common-source transistors.

5.1.2 Simulation of Via Placement in TFMSL Circuits

As shown in the last section, the TSV placement significantly impacts TFMSL circuits after back-side processing, dependent on the implemented topology and device configuration. In order to simulate different via-placement scenarios for the four-stage cascode MMIC depicted in Fig. 5.4 and reproduce the measurement results shown in Fig. 5.5, a simplified model of the cascode MMIC was implemented in CST Microwave Studio.

To evaluate the via-placement requirements for different device and circuit topologies, the whole MMIC—including the matching networks as well as the GaAs substrate, TSVs, and backside metalization—is simulated using a simplified finger model for the active devices, as depicted in Fig. 5.6. The MESA as well as the gate fingers are not considered in this CST model. Only the MET1 source and drain fingers and feeding structures are included, which are the main source of the excited substrate modes. For both the CS and CG devices in Fig. 5.6, the drain fingers are extended and connected to the gate feeders in the case of the CS devices, and to the source feeders for the CG devices. This prevents the excitation of spurious resonances between the transistor fingers in the simulation, so that the resonances caused by substrate modes can be isolated.

In order to reduce the simulation time and effort, the whole DC-bias insertion network, which is not relevant for the propagation of the RF signal, is omitted. The two waveguide ports at the input and output are defined at the port extension of the RF pads, in order to prevent false artifacts in the simulation, caused by the RF-pad simulation.

Fig. 5.7 shows the simulated S-parameters of the 4-stage MMIC CST model depicted in Fig. 5.6. As for the measured small-signal characteristics shown in Fig.5.5, the same four via-placement scenarios (thick wafer, VS1–3) are investigated in simulation. In comparison to the measurement results (Fig. 5.5), the simulated S-parameters (Fig. 5.7) show the same resonant behavior for the four different scenarios, at least from a quantitative point of view. The thick-wafer simulation shows the expected ideal behavior of the

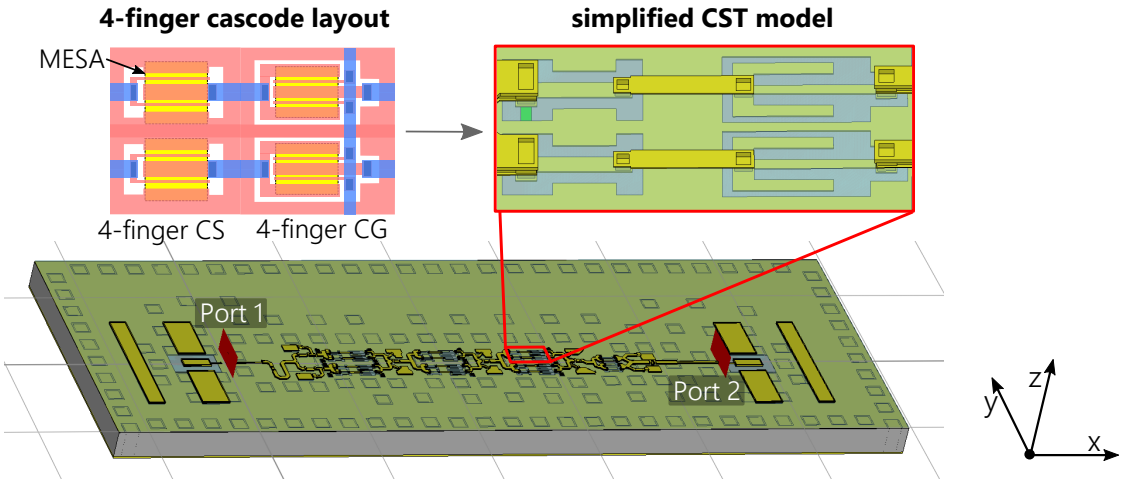
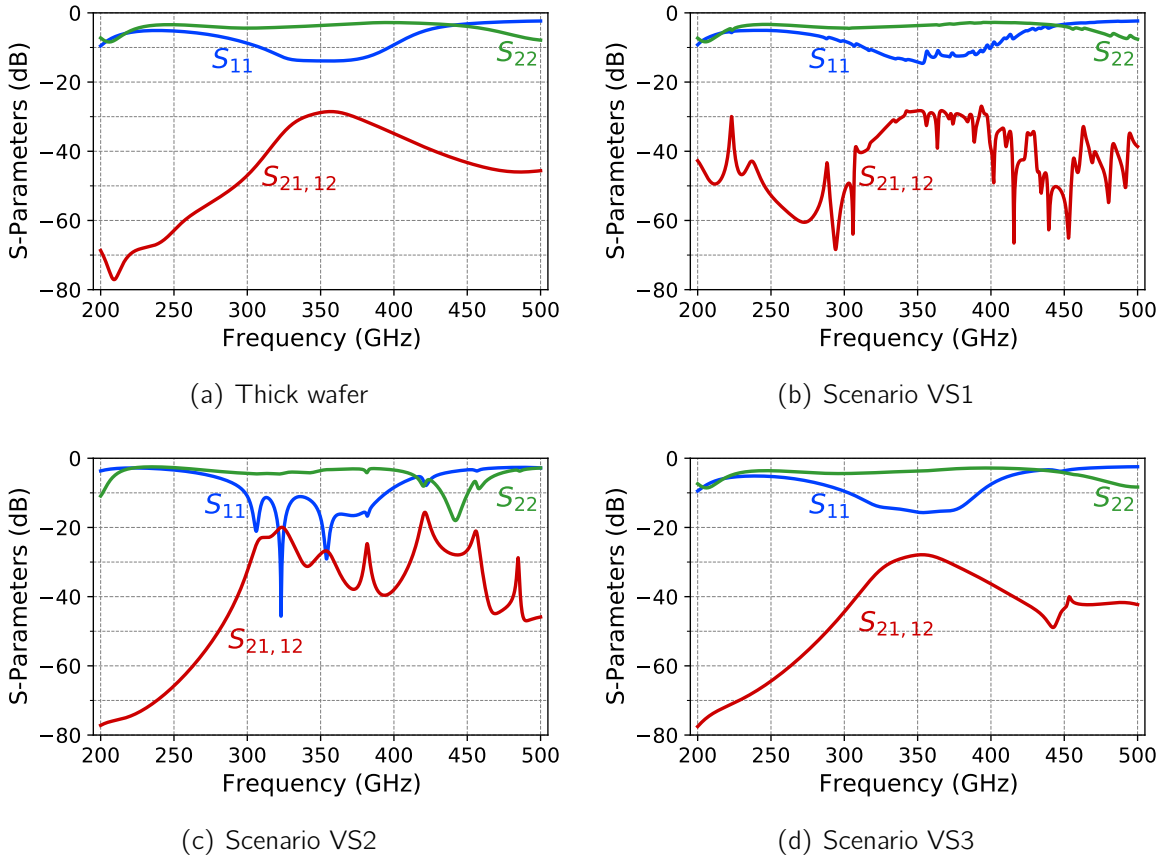


Figure 5.6: Screenshot of the simplified CST simulation model of the 4-stage PA MMIC depicted in Fig. 5.4. The basic 4-finger cascode layout is shown in the top left-hand side for reference.



(a) Thick wafer

(b) Scenario VS1

(c) Scenario VS2

(d) Scenario VS3

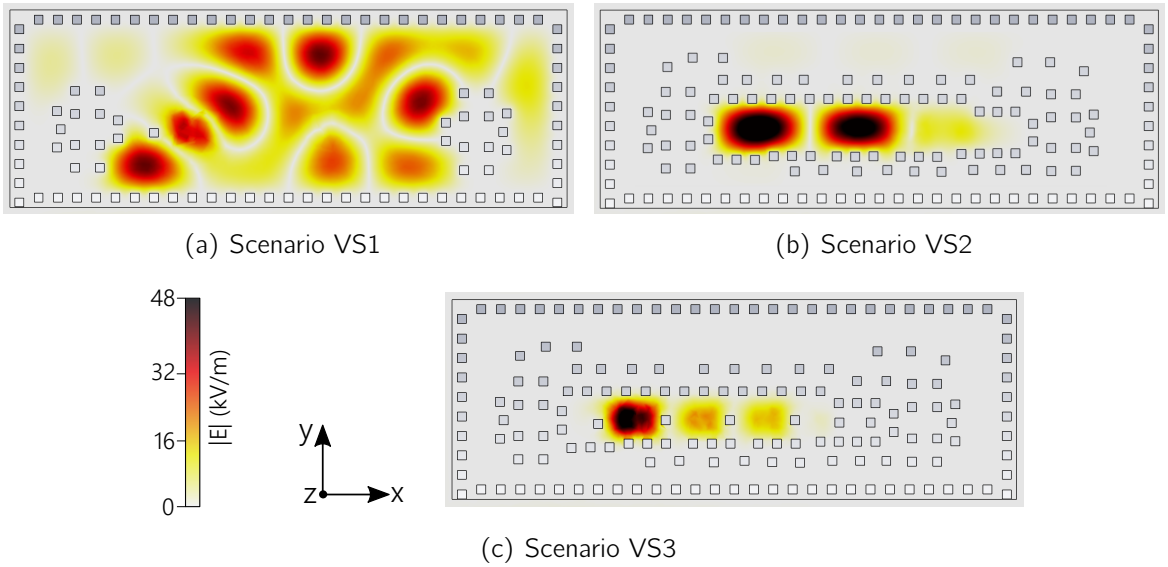
Figure 5.7: 3D-EM simulated S-parameters of the 4-stage PA-MMIC CST model depicted in Fig. 5.6: (a) simulated without backside process, and (b) VS1, (c) VS2 and (d) VS3 via placement.

purely passive four-stage MMIC—as the simulated S_{21} and S_{12} indicate the passband of the matching networks, shifted in frequency due to the missing active-device parasitics.

The VS1 simulation shows heavy resonances over the full frequency band from 200–500 GHz, similar to the measurement results. These resonances are suppressed up to 320 GHz, implementing the VS2 via placement (Fig. 5.7 (c)). By using the additional vias between the active multi-finger devices, wave propagation in the GaAs substrate and, hence, inter-device coupling is suppressed. The simulated S-parameters show, therefore, the ideal thick-wafer behavior of the passive simulation model up to frequencies above 400 GHz. Using the model depicted in Fig. 5.6, the field distribution within the substrate can be evaluated for different via-placement scenarios. As an example, the z-plane cross section at the center of the GaAs substrate is depicted in Fig. 5.8, showing the E-field magnitude at 340 GHz for the three different via-placement scenarios and visualizing the wave propagation underneath the PA cell, for the scenarios without vias between the active gain stages.

5.1.3 Conclusion

The measured and fully-passive simulated S-parameter characteristics of the above discussed via-placement scenarios clearly show, that vias have to be implemented in the



(a) Scenario VS1 (b) Scenario VS2

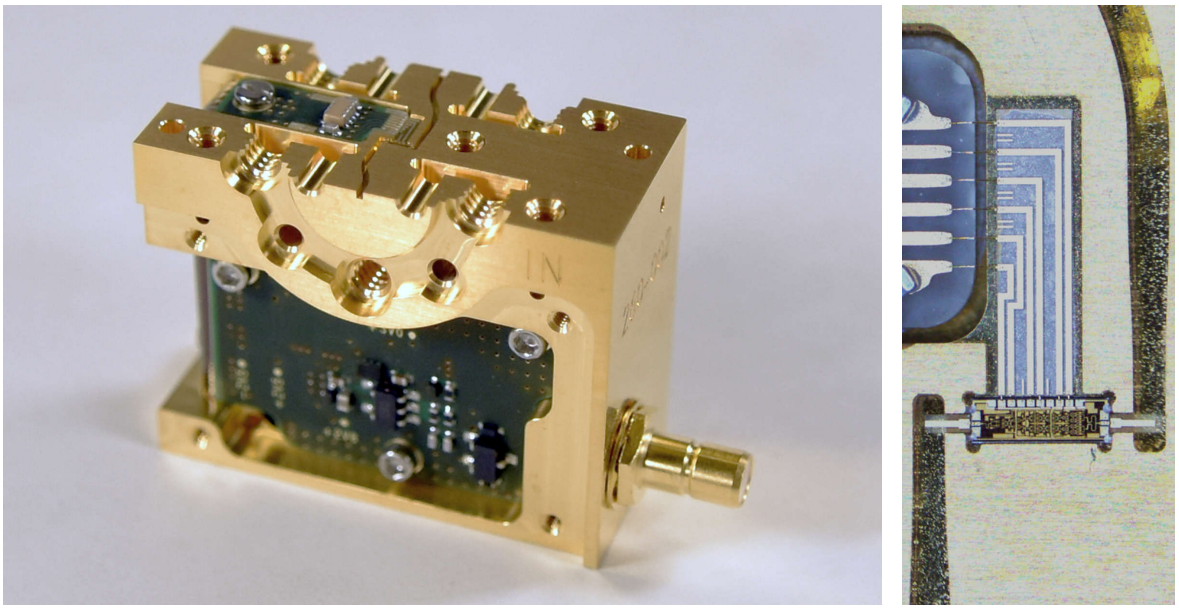
(c) Scenario VS3

Figure 5.8: Z-plane cross section at the center of the GaAs substrate showing the E-field magnitude at 340 GHz for the three different via-placement scenarios: (a) VS1, (b) VS2 and (c) VS3 via placement.

developed compact PA cells, in order to suppress unwanted substrate modes. The comparison of MMICs implemented in CS and cascode topology indicate, that the necessity of TSVs is dependent on the devices and topology used. At least for cascode devices, the implementation of vias needs to be considered in order to avoid substrate resonances and inter-device coupling. The resonances observed in the cascode circuits are caused by the finger structure of the common-gate devices, which require a larger MET1 ground-plane opening, in comparison to common-source transistors.

General design rules to prevent substrate resonances are hard to define, due to their device-layout and topology dependency. However, in order to avoid inter-device coupling in TFMSL circuits in the underlying mHEMT technology, a via cage enclosing the active circuit area in close proximity was found to be sufficient up to the cutoff frequency of the loaded waveguide formed by this via cage. At frequencies above this cutoff frequency, additional vias between the active devices might be required. The minimum via spacing (30 µm for the 50-µm-thick substrate) is sufficient for the 300-GHz cascode circuits investigated in this work. At frequencies above 500 GHz, the substrate is typically thinned down to sub-30-µm dimensions, which permits a smaller via-to-via spacing.

Therefore, the via placement needs to be taken into account during the design process, in order to avoid the requirement of layout changes in the later design stages—which would be necessary to free up chip space for via implementation, for example. To evaluate the via-placement in simulation, the usage of a simplified finger layout for the active devices is proposed. This permits the modeling and simulation of the full MMIC in a 3D-EM simulation software, including different via-placement scenarios. Using this approach, the via placement can be considered in the design process discussed in Section 4.1.



(a) (b)

Figure 5.9: Photographs of the packaged 300-GHz SSPA. (a) Opened lower-part of the split-block module and (b) close-up view of the packaged 300-GHz PA MMIC with bond connection to the waveguide transitions implemented on a quartz substrate.

5.2 300-GHz Power Amplifier Waveguide Module

The lower part of an opened 300-GHz waveguide module is shown in Fig. 5.9, including a close-up view of the packaged PA MMIC. The waveguide package includes a DC power supply for bias control and current sensing, which is connected to the PA MMIC via bond wires and DC feeding lines processed on a quartz substrate. The required external positive supply voltage is in the range of 3.3 V to 5 V, and the typical external DC current is around 350 mA. Hence, the resulting DC power consumption of the PA module is around 1.3 W for an external supply voltage of 3.6 V.

A chip photograph of the PA MMIC *HPA3*, which was integrated in the waveguide package, is shown in Fig. 5.10. The MMIC was developed based on the compact PA cells and thin-film combiners discussed in Chapter 4. The single-side DC-supply voltages are fed from the upper side to the parallel UA cells, using the vertical DC-bus network described in Section 4.2.2. The back-end used in this PA-MMIC design is the *BEOL-B* variant and the Wilkinson combiner used is the *Wilkinson 5* described in Section 4.3, which is implemented in *MET3 TFMSL* including the final passivation.

The schematic of the five-stage amplifier circuit *HPA3* is depicted in Fig. 5.11. In contrast to the two-way combined PA MMICs *HPA1* and *HPA2* described in Section 4.4—which have four 8-finger CS devices with 16-µm finger width integrated in the output stage—8-finger transistors with 12-µm finger width are implemented in the output stage of the packaged *HPA3* MMIC. This was done to improve the yield and relax the driving ratio between the last two CS stages. Furthermore, the power splitting is realized in the interstage matching network between the second and third cascode cell and an additional cascode stage is used to increase the small-signal gain. Within the active circuit area,

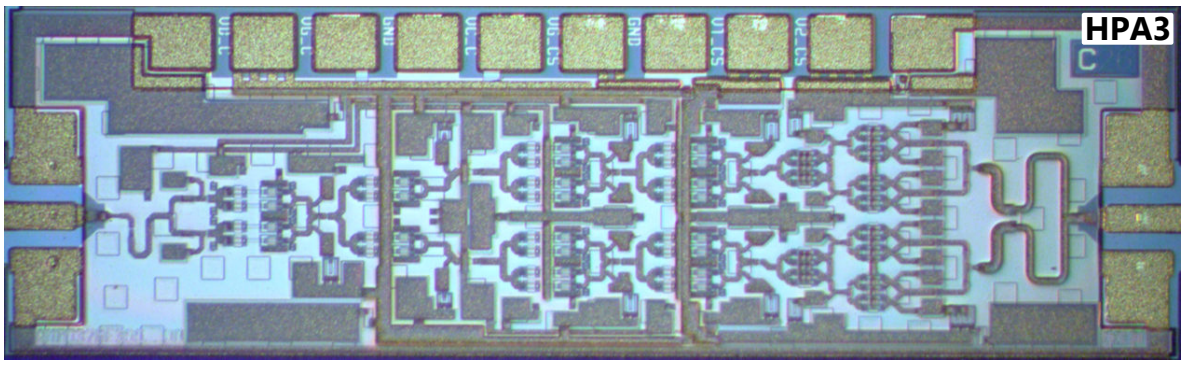


Figure 5.10: Chip photograph of the 300-GHz PA MMIC *HPA3*, which is implemented in the waveguide package depicted in Fig. 5.9(b). This PA circuit is based on the multi-finger devices, topology, and thin-film combiners developed in Chapter 3 and Chapter 4.

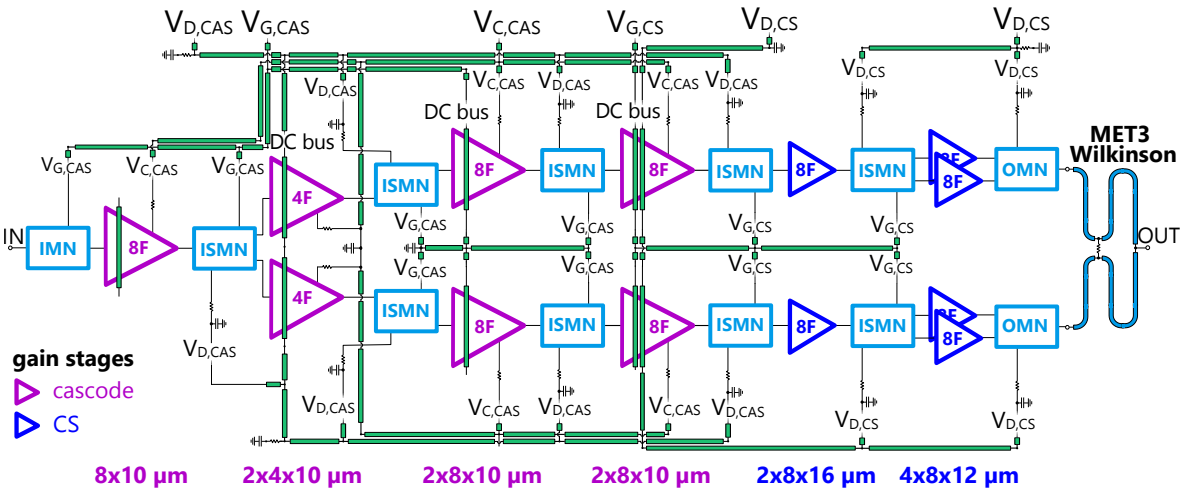
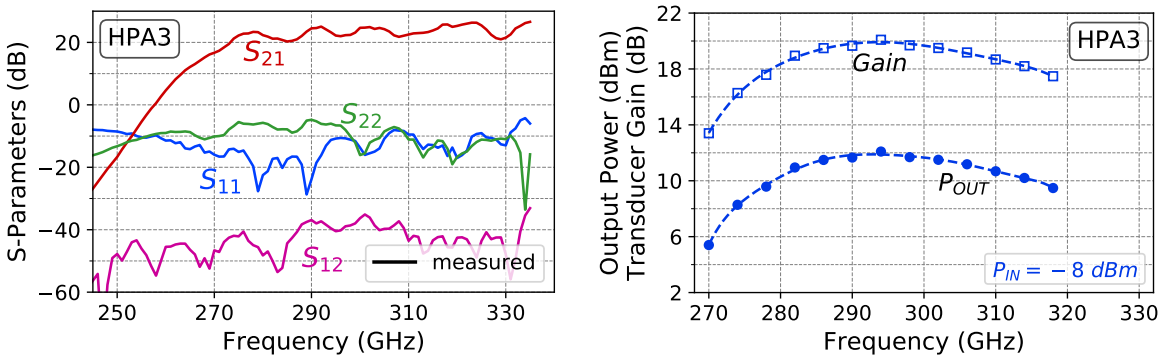


Figure 5.11: Simplified schematic of the PA core of the 300-GHz power amplifier circuit *HPA3* depicted in Fig. 5.10.

through-substrate vias have been implemented between as well as around the 8-finger cascode devices—based on the via-placement investigations described in the previous section, Section 5.1.

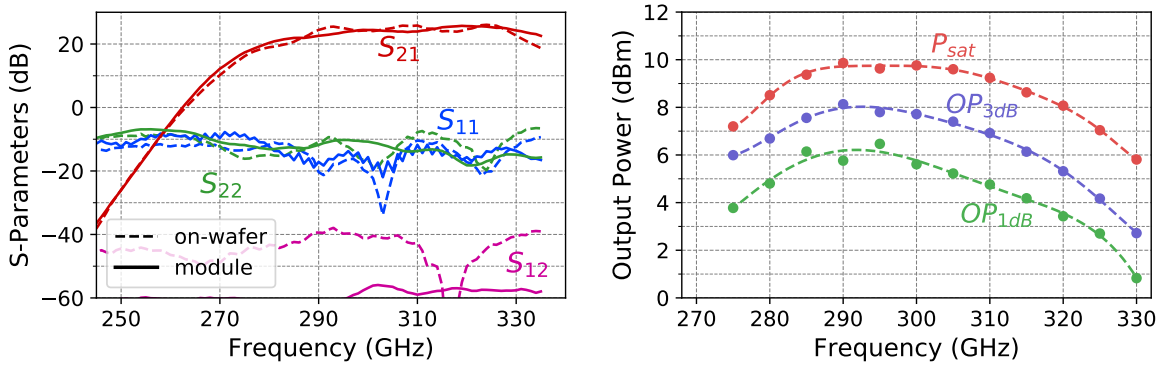
5.2.1 Measurement Results

To determine the actual performance of the PA-core implemented in the *HPA3* MMIC—excluding the impact of the RF bond pads—a breakout circuit has been fabricated for on-wafer characterization. The on-wafer measured S-parameters of the PA-core MMIC are depicted in Fig. 5.12(a), measured at H-band frequencies up to 335 GHz. The measured small-signal gain is exceeding 20 dB over the frequency range of 275 to 335 GHz, showing a 4-dB gain ripple caused by the on-wafer measurement environment. The CW measured maximum output power of the PA-core MMIC—which is depicted in Fig. 5.12(b)—is around 12 dBm for 290–300-GHz frequencies and larger than 10 dBm over the frequency span from 280 to 315 GHz, measured at −8 dBm constant input power. The saturated output power is approximately 1.5 dB below the power level of the *HPA2* MMIC described



(a) (b)

Figure 5.12: On-wafer measurement results of the PA-core circuit implemented in *HPA3* without the impact of the RF bod pads: (a) measured S-parameters and (b) CW measured transducer gain and output power −8-dBm input power.



(a) (b)

Figure 5.13: (a) Measured S-parameters of the 300-GHz PA module in comparison to the on-wafer measurement of the corresponding *HPA3* MMIC. (b) CW measured output power versus frequency of the amplifier module in saturation(P_{sat}), 3-dB gain compression (OP_{3dB}) and 1-dB gain compression (OP_{1dB}).

in Section 4.4, which is mainly because of the 25-% reduced total gate width in the output stage.

The measured S-parameters of the packaged PA module are depicted in Fig. 5.13(a)—plotted against the on-wafer measured small-signal characteristics of the specific cell. The small-signal gain on waveguide level is in the range of 20–25 dB with a 3-dB bandwidth of at least 285–335 GHz. The observed ripple on the gain response is significantly reduced for the packaged MMIC—which is mainly due to the improved isolation (S_{12}) in the waveguide package. The measured saturated output power of the 300-GHz PA module is around 10 dBm over the frequency range of 290–305 GHz, as depicted in Fig. 5.13(b). Output-power levels above 8 dBm are measured over a 40-GHz frequency band from 280 GHz to 320 GHz, with a linear output power ($OP_{1\mathrm{dB}}$) of 6 dBm around 300 GHz.

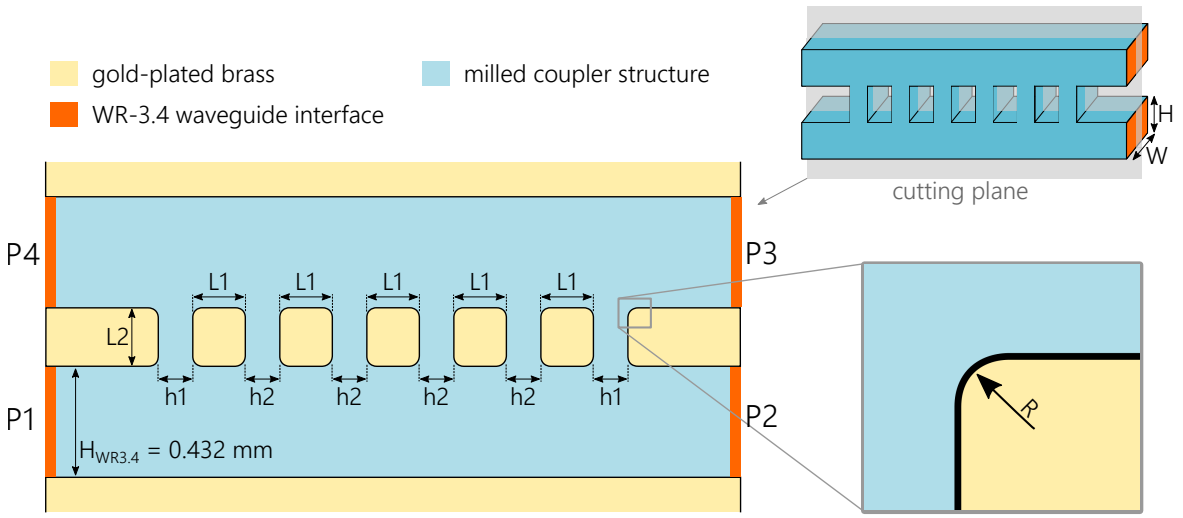


Figure 5.14: Cross section of the developed 300-GHz waveguide coupler with six branches and WR-3.4 interface.

Table 5.1: 3-dB coupler dimensions with six branches for 300-GHz operation

	Height of branches		Length and spacing of branches		Radius of corners
	h1 (mm)	**h2** (mm)	**L1** (mm)	**L2** (mm)	**R** (mm)
Theoretical coupler dimensions according to Reed [90]	0.063	0.137	$\lambda/4 = 0.36$	$\lambda/4 = 0.36$	0
Coupler dimensions of this work	0.13	0.13	0.2	0.22	0.04

5.3 Waveguide Power Combiner at 300-GHz

To increase the output power of the PA MMICS described in Chapter 4, further on-chip parallelization is possible by using the developed TFMSL combiners, for example. Yet, for the parallelization of the 350-µm-wide MMICs, additional TFMSL interconnections with a length of at least 120 µm are required to connect the PA-core outputs to the combiner. This significantly reduces the combining efficiency. Additionally, since a further parallelized PA MMIC would require a chip width of at least 800 µm, the effort for the suppression of unwanted cavity modes would grow significantly. The parallelization of several MMICs on waveguide level, on the other hand, offers the possibility of efficient power combining, avoiding the issues discussed in Chapter 1 related to the packaging of oversized amplifier MMICs.

The multiple-branch waveguide directional coupler has been known for decades for its good characteristics in terms of bandwidth, return loss and insertion loss. Hence, a branch-guide 300-GHz coupler has been developed for MMIC and module parallelization—the corresponding cross section of the coupler with six branches is shown in Fig. 5.14. Two parallel WR-3.4 main lines are connected via multiple branch lines which are made of waveguides with the same fixed WR-3.4 width of $W = 0.864$ mm, while the height of the branches (h1, h2), the length of the branches (L2) as well as the spacing between the branches (L1) are the key design parameters, determining the characteristics of the coupler.

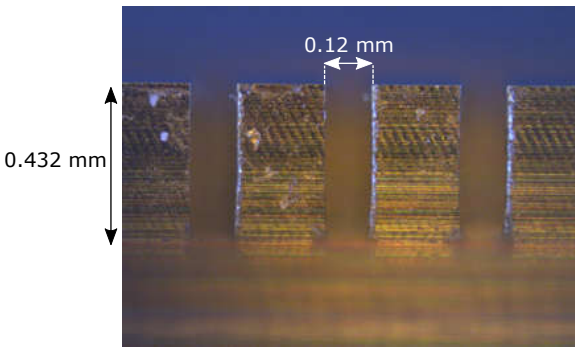


Figure 5.15: Photograph of a manufactured test structure of the connecting branches with the height of 0.12 mm.

The theoretical and analytical description of branch-guide directional couplers with up to 24 branches and coupling ratios in the range of 0 to 15 dB is well known and well covered in the literature [67, 90]. Considering the coupling ratio of 3 dB and P1 to be the input port, the power is equally split between the output ports P2 and P3 with a phase difference of 90 degree. P4 represents in this scenario the isolated port. The achievable bandwidth of this classical multiple-branch coupler is strongly dependent on the number of branches as described by Reed in [90]. As the achievable bandwidth increases with the number of branches, the height of these coupling slots, on the other hand, decreases with a larger number of slots. This poses a major challenge to the fabrication of the coupling structure—especially at the upper end of the mm-wave spectrum—and is the reason that mostly branch-guide couplers have been reported with seven or less branches [77, 100, 123].

A coupler with six branches was chosen in this work (Fig. 5.14), manufactured at Fraunhofer IAF's workshop for precision mechanics. Using this split-block technology, the coupler structure shown in Fig.5.14 is milled into a brass split-block module, which is gold plated at the final manufacturing step. Due to the E-plane split-block configuration, the coupler is made up of two parts and is cut in half along the depicted cutting plane in Fig.5.14. Hence, the depicted coupler structure needs to be milled 0.432-mm deep into the brass blank, which corresponds to the half of the WR-3.4 width of 0.864 mm.

The theoretical dimensions of the 6-branch 3-dB coupler according to [90] are listed in Tab. 5.1. This traditional combiner implementation includes a quarter-wave-length spacing as well as length of the main-lines-connecting branches. In addition, the height h1 of the two outer branches is reduced in comparison to the height h2 of the center connecting branch lines. According to [90], the resulting ideal height h1 of the outer branches is around 0.063 mm. This magnitude corresponds to an aspect ratio of $0.432 : 0.063 = 0.146$ for the depth and width of the slots, which need to be milled for the two outer branches. Since the milling of these slot dimensions is not feasible within the used split-block technology, the coupler dimensions listed in Tab. 5.1 have been chosen.

The coupler dimension were selected based on the simulation results of a scalable 3D model of the 6-branch coupler, which was implemented and optimized using CST. As lower boundary for the branch-height values h1 and h2, a limit of 0.12 mm was chosen. To ensure the feasibility of the branch-guide coupler fabrication, the test structure with 0.12-mm high connecting branches, depicted in Fig. 5.15, was fabricated for optical

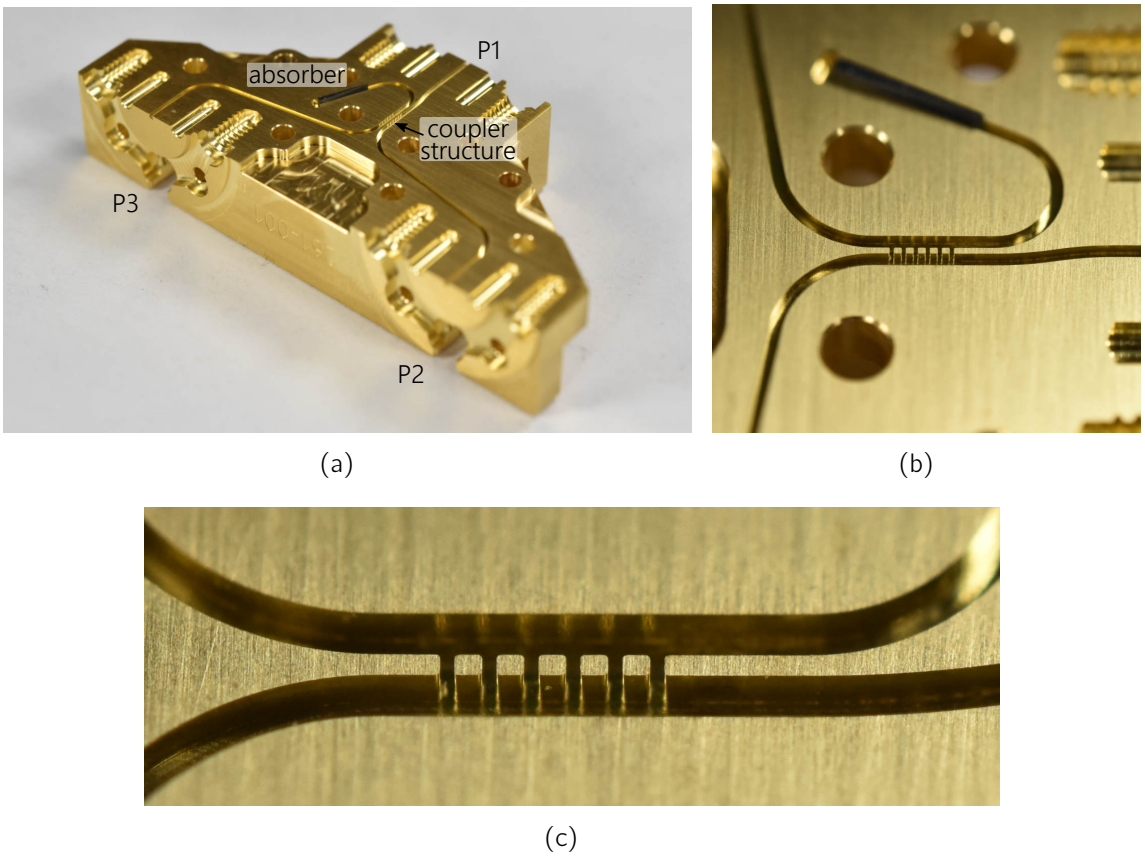
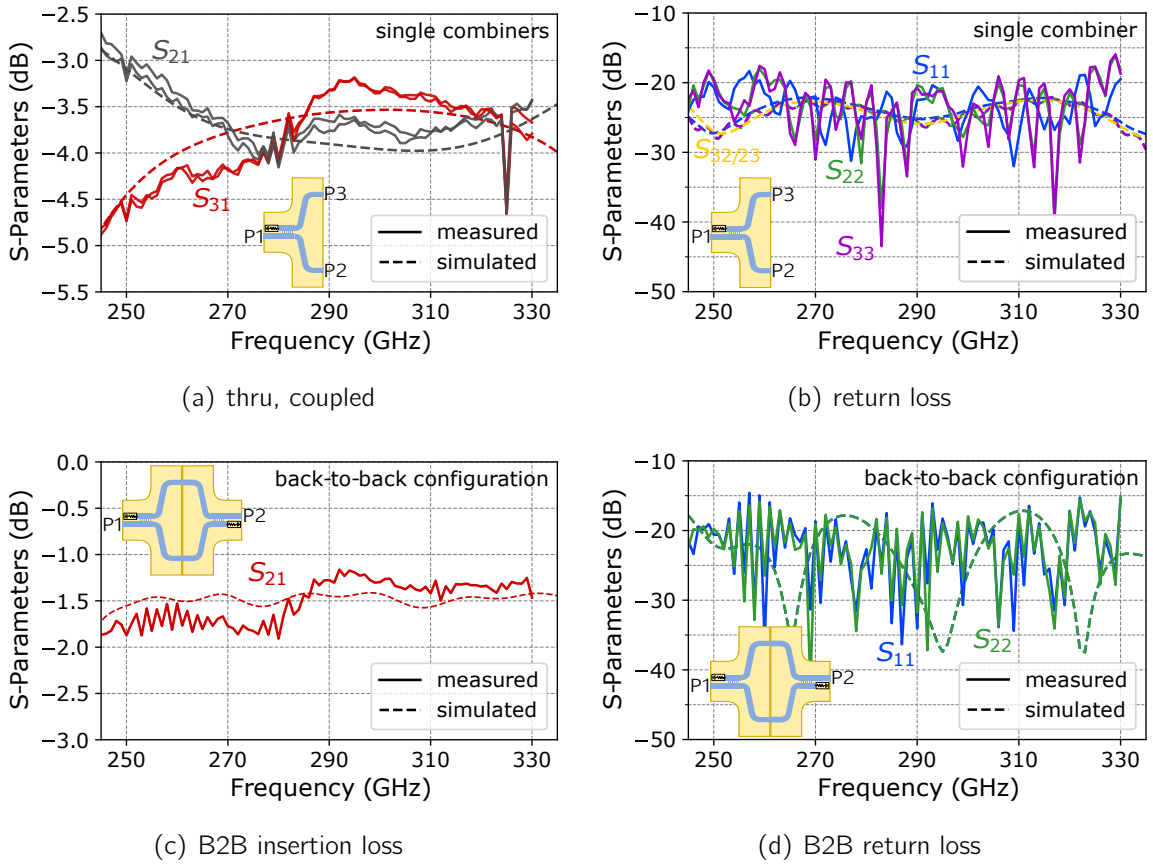


Figure 5.16: Photographs of the fabricated lower half of the 300-GHz two-way combiner/splitter including the 6-branch coupler depicted in Fig. 5.14.

inspection. Based on the positive results, the coupler design with the Tab. 5.1 values was finalized. To ensure a known and reproducible shape of the main-line-to-branch connection, the radius of the milled corners of the coupler structure was set to the fixed value of 0.04 mm.

The photographs of a fabricated 6-branch 300-GHz waveguide coupler are depicted in Fig. 5.16. The coupler is implemented as 90° two-way combiner with terminated port P4, which can be used to combine two PA modules in a balanced configuration. To terminate the fourth coupler port P4, a tapered absorber wedge is inserted into the corresponding waveguide extension.

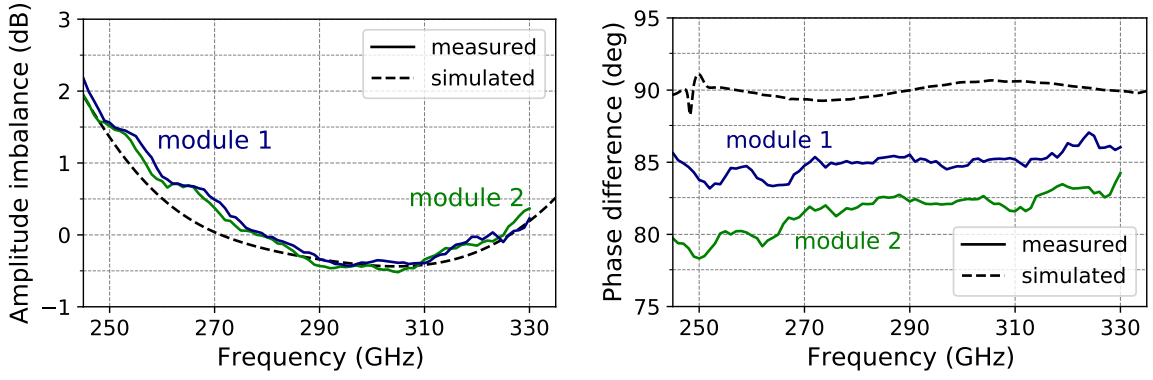
Measurement Results The measured S-parameters of the 90° two-way combiner/splitter depicted in Fig. 5.16 are shown in Fig. 5.17. Two combiner modules have been fabricated and characterized in stand-alone as well as back-to-back configuration. Fig. 5.17(a) includes the measured S_{21} and S_{31} parameters of both modules, which show an identical behavior. The measured return loss in Fig. 5.17(b) is shown for only one module for better clarity. In general, the measurements reproduce the simulation data to a very good extent. The return loss at all three ports is better than 20 dB and the back-to-back measurements indicate an insertion loss below 0.7 dB for the single modules over the 280–335-GHz frequency range. Below 280 GHz, the loss is increasing to 0.9 dB.



(a) thru, coupled (b) return loss

(c) B2B insertion loss (d) B2B return loss

Figure 5.17: Measured S-parameters of the 3-dB 300-GHz waveguide coupler in comparison to simulation. (a) Shows the very identical measurement data of two different coupler modules.



(a) (b)

Figure 5.18: Measured (a) amplitude imbalance and (b) phase difference of the two 3-dB 300-GHz waveguide-coupler modules in comparison to simulation.

The measured loss of 0.7 dB can be assumed to be mainly caused by the waveguide extensions of the two-way combiner. The WR3.4 extension at port P1 is 10-mm in length and the extensions at P2 and P3 have a length of 25 mm. Assuming 0.02-dB/mm waveguide loss at the upper end of the WR3.4 band—which is below typical commercially-specified values [120]—a loss of at least 0.7 dB needs to be expected. Hence, by directly

integrating the multi-branch coupler structure without waveguide extension into a multi-MMIC module, the output power level can possibly be almost doubled.

The power combining efficiency of an n-way power combiner, however, depends on the degree of imbalance among its input signals, as stated in [39]. This, furthermore, also applies for the amplitude as well as phase imbalance of couplers, which are implemented in balanced PA topologies. Amplitude imbalance as well as phase difference of the two fabricated 90° two-way combiners are shown in Fig. 5.18. The amplitude imbalance of both modules is in good agreement with the simulation and in the range of ±0.5 dB over the frequency range of 270–330 GHz. The power combining efficiency which is feasible with this amplitude imbalance, assuming the parallelization of two identical PAs, is better than 0.98 [39]. The measured phase difference between both combiner modules is below 5° over the frequency band of interest above 270 GHz. This 5° phase difference would be negligible in a balanced PA topology, as the combining efficiency is above 0.98 [39].

Yet, it has to be noted, that the accuracy of the phase measurement is limited to a couple of degrees—even on waveguide level. Hence, based on the very good agreement of the S-parameter magnitudes of both combiner modules, also the phase differences can be assumed to be nearly identical. Due to the very good agreement of both combiners, furthermore, the reproducibility of the implemented multi-branch coupler is verified—permitting the implementation in multi-chip PA modules, for example.

5.4 Two-Way Combined 300-GHz Power Amplifier

The photograph of the two-way combined PA setup—including two of the above discussed 300-GHz PA modules (*PA-1* and *PA-2*) and branch-guide couplers—is depicted in Fig. 5.19. The measured small-signal gain is above 20 dB over the 280–335-GHz frequency range, as can be seen in Fig. 5.20(a). Due to the balanced PA setup including

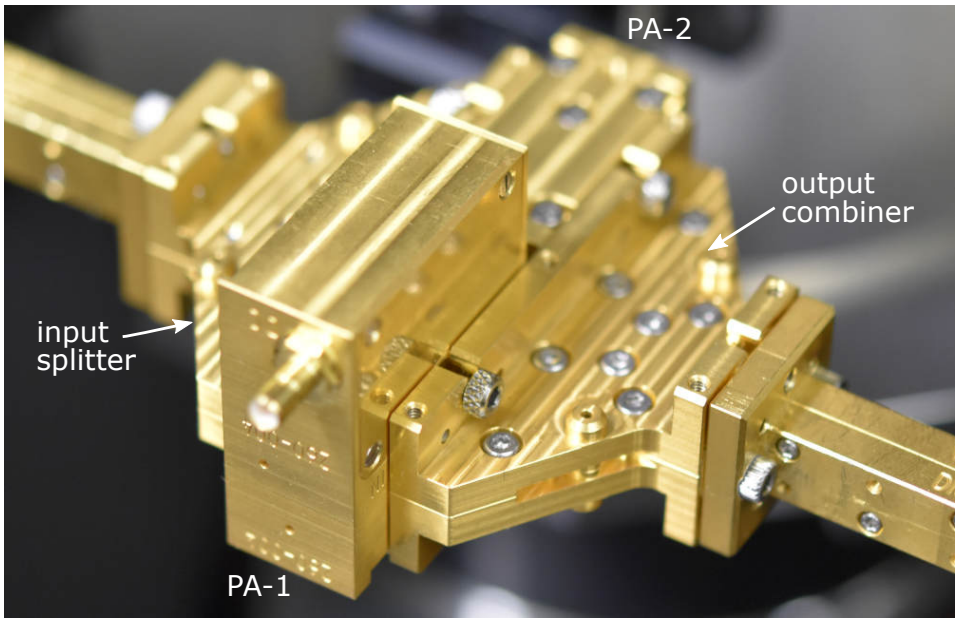


Figure 5.19: Photograph of the two-way combined 300-GHz PA modules *PA-1* and *PA-2* using two 90-degree branch-guide couplers.

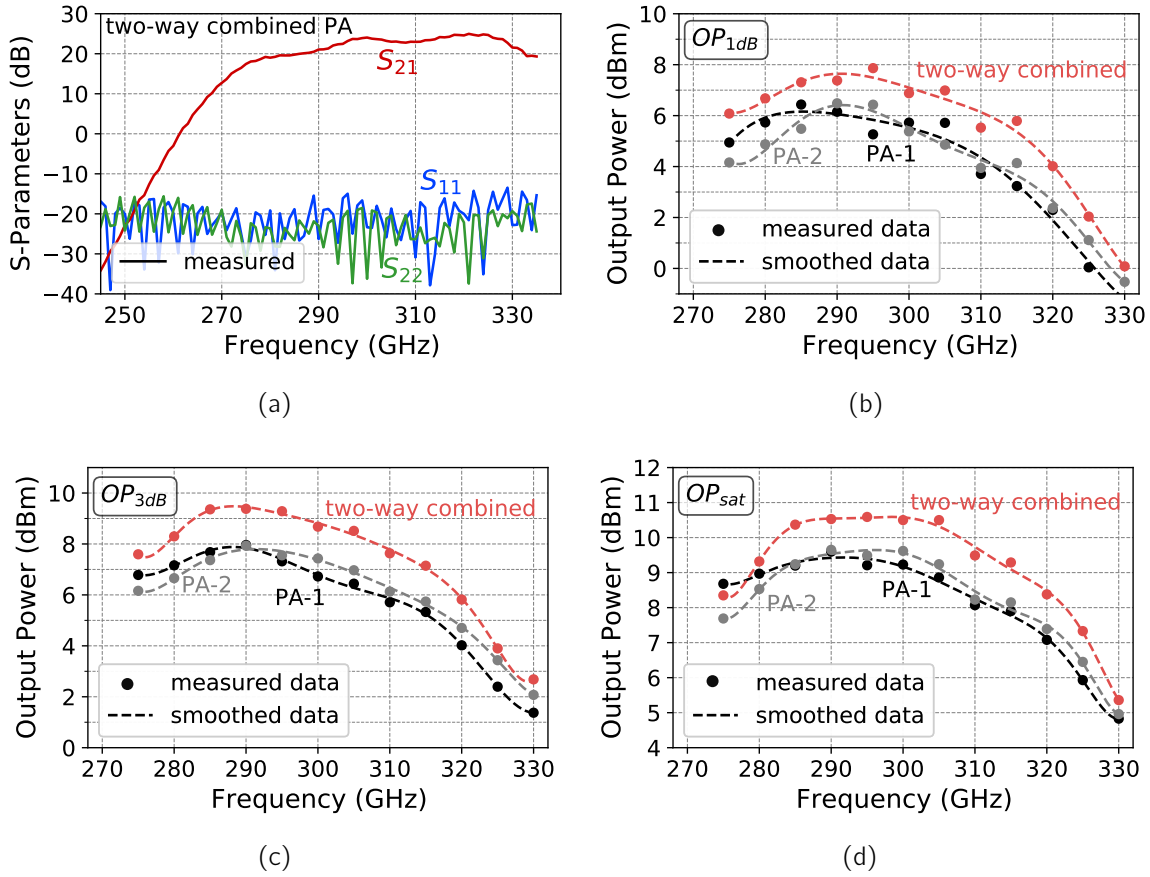


Figure 5.20: (a) Measured S-parameters and (b)–(d) large-signal characteristics of the two-way combined power-amplifier modules.

the 90-degree waveguide couplers, the input and output return loss is better than 15 dB over the full H-band—which is in particular beneficial when considering further system integration.

The large-signal performance of the two-way combined amplifier as well as the single *PA-1* and *PA-2* modules in 1-dB gain compression, 3-dB gain compression, and saturation is depicted in Fig.5.20(b)–5.20(d), respectively. Saturated output-power levels above 10 dBm are measured for the 285–305-GHz frequency span, achieving more than 9-dBm output power over a 35-GHz frequency range from 280–315 GHz.

Judging from the data, which was measured at a constant compression point—as for the OP_{3dB} depicted in Fig. 5.20(c), for example—the output-power improvement achieved with the two-way combined setup is around 1.5 dB. The main limiting factors to achieve a better combining efficiency are the length of the waveguide extensions in the combiner—which can be significantly reduced by direct integration into a multi-chip PA module—as well as the signal imbalance between the *PA-1* and *PA-2* modules. The impact on the combiner output power and efficiency degradation caused by input signal imbalance is described in detail in the literature [28, 34, 76, 93]. The overall combining efficiency η_c for two known input signals—where one input has a reduced power level by a factor r and a phase shift by an angle ϕ—can be calculated [39] from

$$\eta_c = \eta_{max}\left(0.5 + \frac{\sqrt{r}}{r+1}cos(\phi)\right), \tag{5.2}$$

with η_{max} being the maximum combining efficiency of the stand-alone combiner.

The phase and power imbalance of the two stand-alone PA modules which are used in the two-way combined configuration—measured in 3-dB compression—are depicted in Fig. 5.21(a). With the power imbalance being in the range of ± 1 dB ($r = 0.8$), this factor can be neglected for the combining-efficiency calculation in (5.2). The 40–50-degree phase imbalance, on the other hand, impacts the overall combining efficiency, as can be seen from the combining-efficiency degradation shown in Fig. 5.21(b) for the frequency range of 280–330 GHz. The depicted degradation is calculated using (5.2) with the phase imbalance of Fig. 5.21(a) for the case of an ideal loss-less combiner ($\eta_{max} = 1.0$) as well as considering the real combiner losses of 0.7 dB ($\eta_{max} = 0.85$).

The overall combining loss in the range of 1.3–1.5 dB—which is observed in Fig. 5.21(b) for frequency range around 300 GHz, including a constant 0.7-dB insertion loss for the single combiners discussed in the previous section—very well corresponds to the 1.5-dB output-power improvement of the two-way combined PA modules, depicted in Fig. 5.20. Hence the functionality of the developed branch-guide combiners is verified for PA parallelization—permitting the implementation in multi-chip assemblies with reduced waveguide extensions for increased combining efficiency. The results discussed in this section, furthermore, stress the requirement of appropriate chip selection and the need for great care during chip assembly—which is required to achieve reproducible phase characteristics for the waveguide packages and, hence, to maximize the combining efficiency.

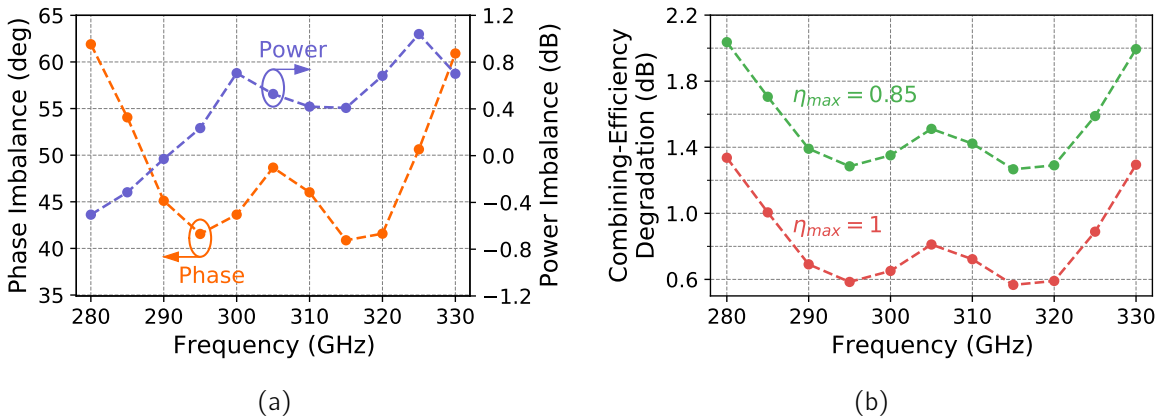


Figure 5.21: (a) Phase and power imbalance of the *PA-1* and *PA-2* modules in 3-dB gain compression. (b) Corresponding combining-efficiency degradation due to phase and power imbalance in dB. The degradation is calculated according to (5.2) with ideal combining efficiency $\eta_{max} = 1.0$ as well as the combiner's real approximated efficiency of $\eta_{max} = 0.85$.

5.5 Discussion and Conclusion on Chapter 5

To enable the integration of mHEMT-on-GaAs TFMSL circuits into waveguide packages—which requires wafer thinning and through-substrate-via processing for the transition from the MMIC to the waveguide—the requirement of through-substrate vias in the active circuit area of compact thin-film circuits was investigated in this thesis. As a result of the investigation of different through-substrate-via scenarios in experiment as well as in simulation it is demonstrated, that the via-implementation needs to be considered as a part of the design process—even though the vias are not required for the TFMSL matching networks to be functional. Due to the larger opening in the front-side ground plane for devices in CG configuration, substrate vias need to be implemented at least in cascode circuits, in order to avoid through-substrate coupling between the active devices. This finding is essential to ensure the functionality of thin-film circuits after backside processing.

The analysis of the investigated via-placement scenarios proves the dependency of the through-substrate coupling on the width of the GaAs-loaded waveguide underneath the active circuit core area. Hence, when only a limited number of through-substrate vias is implemented, the lower cut-off frequencies of the GaAs-loaded cavities—which are formed by the substrate vias—need to be considered as a general design rule for compact TFMSL circuits in the underlying technology. When operating at frequencies above the cut-off frequency of the waveguide, which is formed by the via cage around the active circuit area, for example, the implementation of vias in-between the active stages needs to be considered as a part of the design process. By using the proposed finger model to implement a passive 3D-EM model of the complete PA circuit, the risk of substrate resonances can be evaluated in simulation.

Based on this investigation and building on the compact PA circuits described in Chapter 4, 300-GHz amplifier modules with output-power levels above 10 dBm were developed and successfully demonstrated. To enable a further parallelization of the PA MMICs—without increasing the width of the cavity in the waveguide package above the critical 300-GHz limit of 0.5 mm—a 6-branch 300-GHz waveguide combiner was investigated for MMIC parallelization on waveguide level. The demonstrated isolation and return loss of the combiner is better than 18 dB while providing an insertion loss around 0.7 dB—which corresponds to a combining efficiency of 85 %. Considering the long waveguide extensions at the combiner's input ports, which are the main source of the observed insertion loss, the combining efficiency can be notably improved to values significantly above 90 % by integrating the developed coupler directly in a balanced multi-chip module.

The combiner was successfully used for the parallelization of 300-GHz PA modules with an overall combining efficiency around 70 %, demonstrating for the first time several combined SSPA modules at 300 GHz. Due to the balanced amplifier configuration, the input and output matching is better than 15 dB over the extended H-band frequency range from 220 to 335 GHz, demonstrating excellent return loss figures for system and measurement equipment integration. With linear output power levels in the range of 7–8 dBm, furthermore, state-of-the-art performance is achieved for solid-state power amplifier modules [40, 87]. The on-waveguide-level measured output-power performance above 10 dBm improves the state of the art for packaged 300-GHz mHEMT MMICs by 5 to 6 dB [106], increasing the available output-power level for 300-GHz system

applications. Hence, by using the state-of-the-art 300-GHz power amplifier MMICs and waveguide components developed in this thesis, the basis for the development of multi-chip PA modules with improved combining efficiency and even higher power levels in the range of 50 to 100 mW at the lower THz range is provided.

A detailed summary and comparison of reported 300-GHz PA waveguide modules in tabular form is given in Appendix A.2.

6 Conclusion and Discussion

Driven by the large absolute bandwidths that are available at the sub-mm-wave frequency range around 300 GHz, wireless high-data-rate communication systems and high-resolution imaging applications are being extensively investigated in recent years. Due to their superior characteristics in terms of noise figure and cutoff frequencies, InGaAs-channel HEMT devices have proven to be the key technology for the realization of the required active front-end MMICs at the lower THz frequency band, when ultra-high bandwidths and state-of-the-art noise performance are needed.

This work describes the extensive modeling, design, and characterization of novel 300-GHz HEMT-based power amplifier cells and demonstrates the implementation of amplifier MMICs and waveguide modules with state-of-the-art performance. These amplifiers are key components for the implementation of high-performance chip sets for wireless THz systems, providing high output power for the utilization of next-generation high-capacity communication and high-resolution imaging applications. A unique PA topology based on multi-finger cascode and CS devices was developed and evaluated, demonstrating for the first time more than 10-mW measured output power at the sub-mm-wave frequency range in a HEMT-based technology. Furthermore, measured output power in excess of 20 mW (13 dBm) is demonstrated over an outstanding bandwidth of 25 GHz. This represents the only 20-mW PA result featuring measured large-signal data at more than a single frequency point around 300 GHz. Moreover, a record peak output power of 24 mW (13.8 dBm) was measured around 300 GHz, advancing the state of the art for solid-state power amplifiers in the lower THz frequency range.

The successful demonstration of these high power levels is achieved based on the comprehensive analysis of single transistors and device configurations, their innovative integration and modeling in chip-size optimized PA cells, as well as the investigation of novel thin-film wiring techniques for highly-compact amplifier and combiner circuits. These design related procedures and the corresponding achievements on device level, circuit level, and module level are summarized and evaluated in detail in the following. All of the device-level and circuit-level related investigations were implemented to maximize the achievable output-power level with the smallest possible die size. Thus, the output power normalized to the required chip width is introduced as a key FOM for the evaluation of the compactness of PA circuits. This is done since this FOM indicates the efficiency of the implemented PA topology in terms of how much area is required on the wafer to achieve a certain output-power performance.

To increase the power density on the device level, an experimental investigation and **optimization of the lateral recess length** of the mHEMT devices towards increased breakdown voltages was carried out in the course of this thesis. Based on this study, a larger recess length was chosen as the new standard for the IAF-mHEMT devices, notably increasing the intrinsic gain by a factor of 1.2 as well as improving the off-state breakdown voltage by a factor of 1.6 to 4 V. The increased breakdown voltage, in turn, permits the

operation at higher bias voltages with larger power density and, hence, contributes to the excellent PA results achieved on circuit level. To further benefit from the increased voltage handling capabilities and to evaluate large-signal models as a part of the PA-design process, the implementation of innovative **on-chip load-pull circuits** has been demonstrated for the first time at a frequency above 200 GHz. This investigation offers unique insights and means to verify the load-target decisions in the lower THz band, which was used to define trade-off load targets for the circuits developed in this work.

With the in-depth **analysis of device configurations**, the prospects and practical limitations of in-series-connected HEMT devices are evaluated. Based on this investigation, it is shown that the best output-power performance per chip width at the lower THz band is achieved with highly parallelized CS devices. This is due to the larger required chip width of cascode devices and the limited benefit of stacked-HEMT topologies around 300 GHz, as shown in this work. Because of the f_T-related current limitations of common-gate devices, the cascode configuration cannot provide enough output power to compensate for the significantly larger required chip area. As a result of this investigation, the first-ever 300-GHz PA circuit based on cascode gain stages and CS devices in the output stages was implemented, realizing a "power-bar-like" topology. Using this new amplifier topology, state-of-the-art linear output power levels above 10 mW are demonstrated on MMIC level.

In addition to the analysis of active device configurations, the accurate modeling of the corresponding CS and cascode PA cells with up to 8 transistor fingers was investigated. To achieve a high level of integration density, a novel **multi-finger modeling approach** was developed, which is solely based on highly-parallelized HEMTs with two transistor fingers. This is done since a key issue in HEMT technologies with a limited number of metal-layers is the drastic impact of the feeding structures of multi-finger CPW transistors. Due to the large electrical size of the standard multi-finger feeding structures, the achievable bandwidth in the THz frequency range is strongly limited, as shown in this work. Using the proposed modeling approach, the limitations of previously-used and electrically-large feeding structures are overcome and broadband performance as well as small circuit dimensions are realized with multi-finger devices in a thin-film environment. At the same time, the superior accuracy of the 2-finger device models is used to precisely predict the behavior of complex multi-finger PA cells. This was demonstrated with the first-pass design success of PA-core cells with highly-compact size and excellent bandwidth.

As a basis for the implementation of ultra-compact 300-GHz PA cells and low-loss power combiners, **thin-film wiring** techniques have been investigated in the two available BEOL variants of the underlying technology—including the BEOL with top-metal layer in air-bridge technology as well as a recently developed variant featuring additional BCB layers. A key challenge for the realization of low-loss thin-film combiners is the utilization of high-impedance transmission lines. These are needed for the required impedance transformation in most 50-Ω power-combining concepts. Hence, to enable low-loss and high-impedance transmission lines, novel thin-film lines with structured ground metal were analyzed for the first time in a III-V technology in the lower THz frequency band. The investigated elevated-CPW transmission lines enable upper impedance-range limits well

above 70 Ω, which was not possible with the previously-used thin-film interconnections in this technology. At the same time, the attenuation is significantly reduced.

When increasing the frequency of operation well above 100 GHz, the electrical size of the isolation resistor of on-chip combiners such as the **Wilkinson combiner** is increasing. This electrically-large isolation resistor, however, is the main factor which is limiting the combiner characteristics in terms of insertion loss as well as return loss—even when the resistor-layout is implemented close to the minimum design rule limit. Thus, for the realization of new high-performance Wilkinson combiners, layout considerations have been studied and optimized combiner structures have been validated. As a result of this investigation, the characteristics of the on-chip combiners are significantly improved up to frequencies exceeding 500 GHz in simulation. Around 300 GHz, 0.4 to 0.5-dB insertion loss is achieved, while providing return-loss characteristics better than 20 dB. This demonstrates a substantial improvement in comparison to the 0.8-dB insertion loss of previously reported 300-GHz CPW combiners in HEMT technologies, which is enabled by the implementation of the investigated high-impedance transmission lines.

Based on the device and circuit level related investigations, **highly-compact 300-GHz PA MMICs** with a massive parallelized topology are successfully implemented. Using this advanced topology, a PA-core circuit including a total of 32 transistor fingers and a combined gate width of 512 µm is realized on an ultra-small chip width of only 0.35 mm. As a result of this, output power in excess of 20 mW is demonstrated, which corresponds to an output-power improvement by a factor of 4 to 8 for this mHEMT technology. Since this work's results are achieved with even smaller MMIC dimensions in comparison to previously-reported 300-GHz PA circuits, the output power per chip width is also notably improved by a factor larger than 4. The demonstrated output power per required chip width on MMIC level of almost 60 mW/mm represents the only reported 300-GHz PA result with more than 50 mW/mm. This considerable improvement is enabled by the very large total gate width which is integrated on an ultra-compact die area using the multi-finger design approach developed in this work. Furthermore, due to their small dimensions, the monolithic integration of the PA-core circuits as high-power IP blocks in multi-functional single-chip solutions is possible. Hence, the realization of innovative and broadband front ends with increased dynamic range is enabled on a single die.

To ensure the proper function of the chip-size-optimized circuits after backside processing, the **placement of through-substrate vias** was found to be a crucial part of the design process. Due to their large relative dimensions—when compared to the size of the active devices and matching networks around 300 GHz—the space for via implementation is very limited in circuits with high device density. Yet, a via cage around the active circuit area was found to be only sufficient up to the cut-off frequency of the GaAs loaded waveguide which is formed by this via cage. When operating the thin-film circuits above the cutoff frequency of this GaAs-loaded waveguide, vias need to be considered between the active stages, in order to avoid coupling between the transistors through the substrate. Therefore, even though through-substrate vias are not required for TFMSL matching networks to be functional, it is essential to consider their positioning during the design process of TFMSL circuits with high device density, as it was demonstrated in this work.

With their integration into **waveguide modules**, the successful packaging of the developed MMICs is shown. Additionally, a six-branch 300-GHz waveguide coupler was

investigated and tested, achieving an excellent combining efficiency of 85 % and enabling further parallelization of MMICs as well as waveguide modules. Using these components, the combination of two SSPA modules was realized for the first time in a balanced topology at 300 GHz. In this balanced PA topology, return-loss figures better than 18 dB were attained, which are key for system and measurement equipment integration. The developed PA modules demonstrate excellent gain above 20 dB in an outstanding measured 3-dB bandwidth of more than 50 GHz. Using the PA and combiner modules which have been realized in this work, more than 10 mW (10 dBm) of saturated output power is achieved at the lower THz frequency range around 300 GHz. Furthermore, with linear output-power levels in excess of 5 mW (7 dBm), state-of-the-art performance is reported on waveguide level.

Outlook and Further Results While the main focus of this thesis is on the lower THz frequency range around 300 GHz, the results and insights gained within the frame of this work have significantly contributed to the successful realization of compact TFMSL front-end circuits and high-gain amplifier solutions from D-band up to above 600 GHz. Around 400 GHz, for example, the first-pass design success of broadband PA MMICs with more than 100-GHz bandwidth has been achieved by implementing the proposed modeling approach for multi-finger cascode cells at 400 GHz [32]. Hence, the here investigated layout, topology, and device considerations substantially contribute to the on-going development of a fully-passivated InGaAs-channel HEMT technology for complex and high-dynamic range THz front ends with high device density and cutting-edge performance.

Furthermore, the developed power amplifiers are used as key enabling components in wireless THz systems and measurement applications. Based on the demonstrated output power in excess of 10 mW on waveguide-module level, the output-power performance for the underlying technology is increased by approximately 6 dB or a factor of 4. Thus, fundamentally improved output-power performance is provided for applications in wireless communication, radar and imaging systems as well as for measurement equipment and devices in the 300-GHz frequency band. With their excellent linear behavior, the PA modules realized in this work are being used in state-of-the-art 300-GHz P2P systems and permit the implementation of high-data-rate THz links in real-world scenarios with transmission distances of several hundred meters. Implemented in the backbone of future beyond-5G communication networks, these THz P2P links are considered as a key enabling technology to handle the predicted Tbit/s throughput, which will be required in the not too distant future. The waveguide PA modules will also be implemented in 300-GHz radar and imaging systems. This will permit increased sensing ranges and new applications for existing radar systems. By implementing the waveguide modules into measurement systems for large-signal device characterization, single-stage circuits with larger gate width can be evaluated in large-signal operation, overcoming the issue of limited input-power levels for on-wafer characterization. To further increase the output power on waveguide level, multi-chip PA modules are being developed based on the investigations, components and results of this thesis—targeting for the first time output-power levels in the range of 50 to 100 mW at the lower THz frequency band around 300 GHz.

A 300-GHz State-of-the-Art Power Amplifiers and On-Chip Combiners

A.1 300-GHz Power Amplifier MMICs

Table A.1: Summary of reported PA results around 300 GHz and comparison to this work's PA- MMICs.

Ref.	Frequency♣ (GHz)	Topology	W_{chip}♠ (mm)	TGW (µm)	V_{DC}★ (V)	P_{DC} (mW)	$P_{out,sat}$ (dBm)	PAE (%)	P_{out}/TGW‡ (mW/mm)	P_{out}/W_{chip}♠ (mW/mm)
Technology: 250-nm InP HBT										
[38]	290–307.5	3-stage, cascode, 2-way combined	0.25	32	1.95	848	7.8–10	1.1	312	40
[122]	300–305	4-stage, common-base, 4-way combined	0.4	40	1.8	720	9.5–9.8	1.1	238	24
[59]	301	4-stage, cascode, 2-way combined	0.5	96	2.2	1490	13.5	1.5	233	45
Technology: 130-nm InP HBT										
[3]	326–340	2-stage, double-stack, 4-way combined	0.7	80	1.8	1120	8.6–12.6	1.1	227	25
Technology: sub-35-nm InP HEMT										
[87]	338	4-stage, CS, 2-way combined	0.3	160	2.2	295	11†	3.5	79	42
Technology: 80-nm InP HEMT										
[41]	278–302	12-stage, CS, 8-way combined	0.6	640	1.2	2160	10.8–12.8†	0.61	24	32
Technology: 35-nm InGaAs mHEMT										
[109]	275–320	3-stage, cascode, 2-way combined	0.4	72	0.9	104	5–7†	–	69	13
[5]	270–310	1-stage, triple-stack	0.23	40	3.4	54	4–6	2.5	100	17
[4]	270–317	1-stage, triple-stack, 2-way combined	0.5	80	3.0	225	3–6	2.5	50	8
[97]	275–312	5-stage, CS, 4-way combined	0.48	128	1.2	2.02	5–8	2.9	49	13
This work										
[52] *CPA1*	280–310	4-stage, cascode, 4-way combined	0.4	160	0.9	678	6.7–8.3	0.85	42	14
– *CPA2*	280–310	3-stage, cascode	0.16	80	0.9	177	3.2–4.1	1.4	29	15
[56] –	280–320	4-stage, CS+cascode	0.17	128	1.3	254	6.8–8.6	2.0	57	42
[55] *UPA1*	280–328	5-stage, CS+cascode, 2-way combined	0.17	256	1.3	558	6.3–9.8	2.0	31	48
[55] *HPA1*	280–328	5-stage, CS+cascode, 4-way combined	0.35	512	1.3	1176	9.6–13.0	1.8	39	57
[55] *HPA2*	280–328	5-stage, CS+cascode, 4-way combined	0.35	512	1.3	1070	9.6–13.7	2.1	46	67

♣: the frequency range corresponds to the reported large-signal bandwidth.
♠: required chip width of the PA core including matching networks and the first stage of shunt capacitors in the bias insertion network, without RF/dc-pads.
★: applied drain-source voltage (V_{DS}) and collector-emitter voltage (V_{CE}) of single HEMT and HBT devices.
‡: total gate width, device periphery in the output stage.
†: only packaged results are reported. The depicted results include the reported values minus the specified transition loss.

A.2 300-GHz Power Amplifier Modules

Table A.2: Summary of reported PA-module results around 300 GHz and comparison to this work's waveguide modules.

Ref.	Technology	Frequency♣ (GHz)	Gain (dB)	P_{DC} (mW)	OP_{1dB} (dBm)	OP_{3dB} (dBm)	$P_{out,sat}$ (dBm)
[87]	sub-35-nm InP HEMT	338	15	295♠	5.3	7.6	10
[41]	80-nm InP HEMT	278–302	18–20	2160♠	6.4–7.4	9.8	10–12
[109]	35-nm InGaAs mHEMT	275–320	15–22	400★	1.2	3.3	3–5
This work	35-nm InGaAs mHEMT	275–320	20–25	1300★	4–8	6–9.5	8.5–10.6

♣: the frequency range corresponds to the reported large-signal bandwidth.
♠: DC power consumption of the packaged MMIC only. No power/voltage conditioning is implemented in the waveguide module.
★: DC power consumption of the waveguide module including a control unit for power/voltage conditioning and current sensing. The external supply voltage is 3.6 V.

A.3 300-GHz On-Chip Combiners

Tab. A.3 summarizes the state of the art of 300-GHz on-chip power combiners which are implemented in the state-of-the-art relevant III-V HBT and HEMT technologies listed in Tab. A.1. In general—as for the PA circuits described in Chapter 1—the combiners in InP HBT technology are implemented in TFMSL wiring, whereas CPW environment is typically used in InGaAs-channel HEMT technologies.

The lowest insertion loss for the Tab.-A.3 combiners is reported with 0.45–0.7 dB in [38, 59]. The combiners are implemented as $\lambda/4$-combiner topologies—such as the Wilkinson power combiner for example—implemented in a 4-metal-layer stack with 5-µm-thick BCB substrate for the TFMSL interconnections. Similar TFMSL Wilkinson combiners have been used up to 260 GHz in [37] to efficiently combine up to 16 Cascode PA cells.

Due to the improved return loss of balanced amplifier topologies, a large variety of 90° hybrid couplers have been implemented in HEMT based PA circuits, including Lange couplers, Tandem-X couplers, and broad-side couplers [4, 106, 87]. The reported insertion loss, however, is with 0.8–1.6 dB significantly higher compared to the listed TFMSL 2-way combiners, limiting the power combining efficiency. The inferior insertion loss of these substrate guided couplers is mainly due to the fact, that the couplers are implemented in the 300-nm-thick lowest metal layer which is introducing significant loss around 300-GHz. The signal line of the InP HBT TFMSL combiners, on the other hand, is implemented in the 3-µm-thick top-metal layer. However, also 4-way in-phase power combiners like the Dolph-Chebyshev combiner and Wilkinson combiner, for example, have been used in CPW PA circuits [6]. The demonstrated insertion loss of these substrate-guided combiner implementations is in the range of 0.8–2 dB. Measured over a wide bandwidth, the insertion loss is typically above 1 dB.

Since the position of the combiners' input ports typically strongly differ between different combiner and coupler topologies, a port extension of a significant length is often required to connect multiple PA cells to the inputs of the combiner network. The position of the input ports as well as the impact of the port extension are not considered in

Table A.3: Comparison of on-chip power-combiner results around 300 GHz.

Frequency (GHz)	**Technology**	**Combiner topology**	**Back end of line**	**Insertion loss** (dB)	**Isolation** (dB)	**Pad loss de-embedded** (Yes/No)	**Ref.**
255–330	250-nm InP HBT	2-way Wilkinson, TFMSL	4-metal-layer, BCB	0.45–0.5	11–15	Yes	[38]
230–320	250-nm InP HBT	4-way balun, TFMSL	4-metal-layer, BCB	1.0	N-R	N-R	[122]
220–320	250-nm InP HBT	2-way combiner, TFMSL	4-metal-layer, BCB	0.7	0	Yes	[59]
220–320	sub-35-nm InP HEMT	2-way tandem-X coupler, CPW	2-metal-layer, air-bridge	1.0–1.2†	N-R	Yes	[87]
249–296	35-nm InGaAs mHEMT	2-way tandem-X coupler, CPW	3-metal-layer, air-bridge	0.8–1.6	> 22	N-R	[4]
246–297	35-nm InGaAs mHEMT	2-way broadside coupler, CPW	3-metal-layer, air-bridge	0.8–1.4	> 15	N-R	[4]
220	35-nm InGaAs mHEMT	2-way broadside coupler, CPW	3-metal-layer, air-bridge	0.7	N-R	N-R	[79]
244–280	35-nm InGaAs mHEMT	4-way Dolph-Chebyshev, CPW	3-metal-layer, air-bridge	1.1–1.2	> 9	N-R	[6]
240–280	35-nm InGaAs mHEMT	4-way combiner, CPW	3-metal-layer, air-bridge	0.8–1.1	> 7	N-R	[6]
210–270	35-nm InGaAs mHEMT	4-way combiner, CPW + AirMSL	3-metal-layer, air-bridge	1.5–2	> 7	N-R	[25]
270–330	35-nm InGaAs mHEMT	2-way combiner, TFMSL Wilkinson	3-metal-layer, BCB	0.4–0.6	> 20	Yes	this work

N-R: not reported.
† : insertion-loss range estimated, only 1.2-dB inserion loss at 320 mentioned in [87].

the discussion here. The additional port extension loss, however, will effect the overall efficiency of the combiners when implemented in the PA circuit.

B Elevated-CPW and Slow-Wave Thin-Film Transmission Lines

The theory and considerations on transmission line characteristics described here are mainly based on [85] and in part on [27, 68, 82]. To evaluate the transmission lines described in Chapter 2, the complex line impedance Z_{line} and propagation constant γ are calculated from the simulated S-parameters according to

$$Z_{\text{line}} = Z_0 \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{B.1}$$

and

$$e^{-\gamma x_{\text{line}}} = \left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \sqrt{\frac{(1+S_{11}^2 - S_{21}^2)^2 - (2S_{11})^2}{(2S_{21})^2}} \right)^{-1}. \tag{B.2}$$

Based on (B.2) and (B.1), the four distributed transmission line parameters R_{eq}, L_{eq}, G_{eq}, and C_{eq} can be calculated, using

$$Z_{\text{line}} = \sqrt{\frac{R_{eq} + j\omega L_{eq}}{G_{eq} + j\omega C_{eq}}} \tag{B.3}$$

and

$$\gamma = \alpha + j\beta = \sqrt{(R_{eq} + j\omega L_{eq})(G_{eq} + j\omega C_{eq})}, \tag{B.4}$$

with α being the attenuation constant and β being the propagation constant of the transmission line. The resistance R_{eq}, inductance L_{eq}, conductance G_{eq}, and capacitance C_{eq} per unit length are then calculated with (B.5)–(B.8)

$$R_{eq} = Re\left(\gamma \cdot Z_{line}\right) \tag{B.5}$$

$$L_{eq} = Im\left(\gamma \cdot Z_{line}\right)/\omega \tag{B.6}$$

$$G_{eq} = Re\left(\gamma / Z_{line}\right) \tag{B.7}$$

$$C_{eq} = Re\left(\gamma / Z_{line}\right)/\omega. \tag{B.8}$$

To reduce the physical dimensions of matching and filter networks, the phase velocity of the slow-wave transmission line is reduced—increasing the electrical length of the

given transmission line. The phase velocity v_ϕ in dependency on the phase constant β and the equivalent inductance L_{eq} and the equivalent capacitance c_{eq} can be expressed by

$$v_\phi = \frac{\omega}{\beta} = \frac{1}{\sqrt{C_{eq} \cdot L_{eq}}} \tag{B.9}$$

in the case of a low-loss transmission line with the assumption of $G_{eq} \ll \omega C_{eq}$ and $R_{eq} \ll \omega L_{eq}$. Hence, in order to reduce the phase velocity of the transmission line, the conductor inductance and/or the capacitance needs to be reduced, as can bee seen from (B.9). This is typically done by structuring the ground-plane metal, as described in Chapter 2 for the underlying mHEMT technology.

By increasing the equivalent inductance L_{eq} and equivalent capacitance C_{eq}, the phase constant β is increased. When considering the implementation in power-combining networks, however, where the combing efficiency is of specific interest, the attenuation α of the transmission line is, additionally, a crucial factor. Therefore, the quality factor Q is often used to evaluate the efficiency of a given transmission line with

$$Q = \frac{\beta}{2\alpha}. \tag{B.10}$$

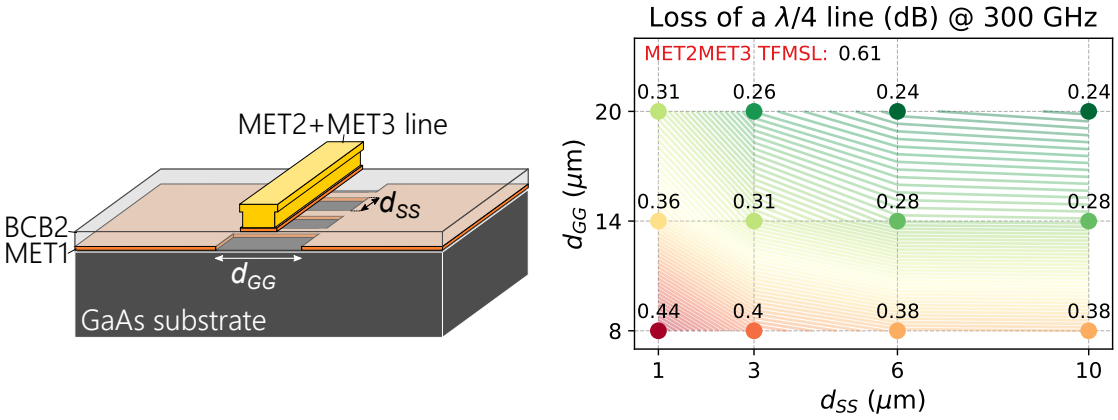
Q has no unit and shows the same behavior as the loss for a specific electrical length of a transmission line. Hence, when requiring a certain electrical length for impedance transformation and lowest insertion loss—as it is the case in power combiners, for example—the loss per wave length of or quality factor needs to be considered, to maximize the combining efficiency.

In silicon based CMOS and SiGe technologies, the implementation of the slow-wave metal strips are additionally motivated by the high losses of the Si substrate. By shielding the lossy Si substrate, the attenuation can be significantly reduced—improving both the attenuation as well as phase constant. This is typically not the case when using a low-loss GaAs substrate, where additional eddy-current losses are dominating the attenuation constant in the slow-wave transmission lines considered in this work, as shown in the following sections, which show additional figures of the ECPW thin-film transmission lines discussed in Chapter 2.

B.1 Additional Information on the MET2MET3 ECPW

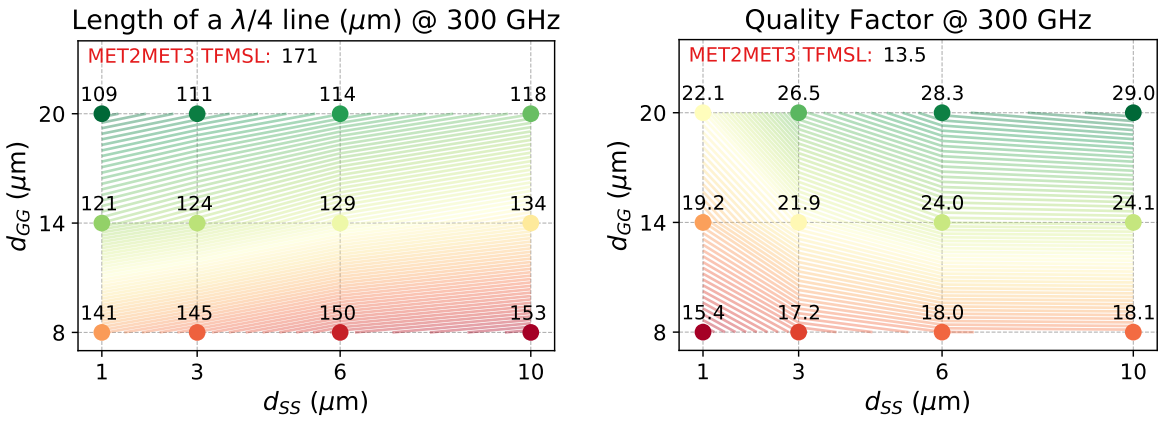
Fig. B.1 and Fig. B.2 show the heat-map simulation results of the *MET2MET3 ECPW* which are also discussed in Section 4.3. Depicted are the loss and the length of a quarter-wavelength transmission line as well as the corresponding quality factor. The two design parameters d_{SS} and d_{GG} are in the range of 8 to 20 µm in the case of the ground-to-ground spacing d_{GG} and 1 to 10 µm in the case of the strip-to-strip spacing d_{SS}.

Furthermore, Fig. B.3 shows the simulated attenuation constant α and phase constant β. The corresponding equivalent inductance L_{eq} and equivalent capacitance C_{eq} are depicted in Fig. B.4.



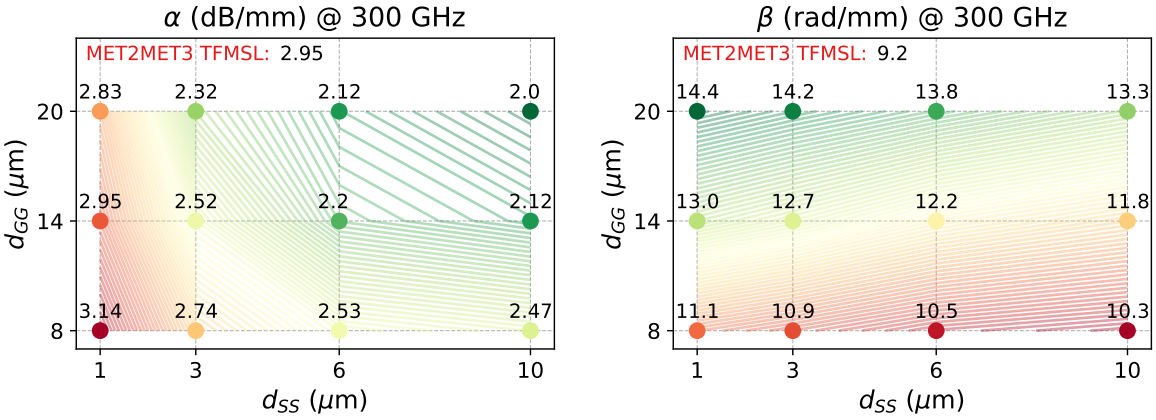
(a) (b)

Figure B.1: (a) *MET2MET3 ECPW* transmission line with the design parameters d_{gg} and d_{ss} (d_{gg}: ground-to-ground spacing, d_{ss}: MET1-stripe spacing). (b) Simulated loss of the *MET2MET3 ECPW* line for a length of $\lambda/4$.



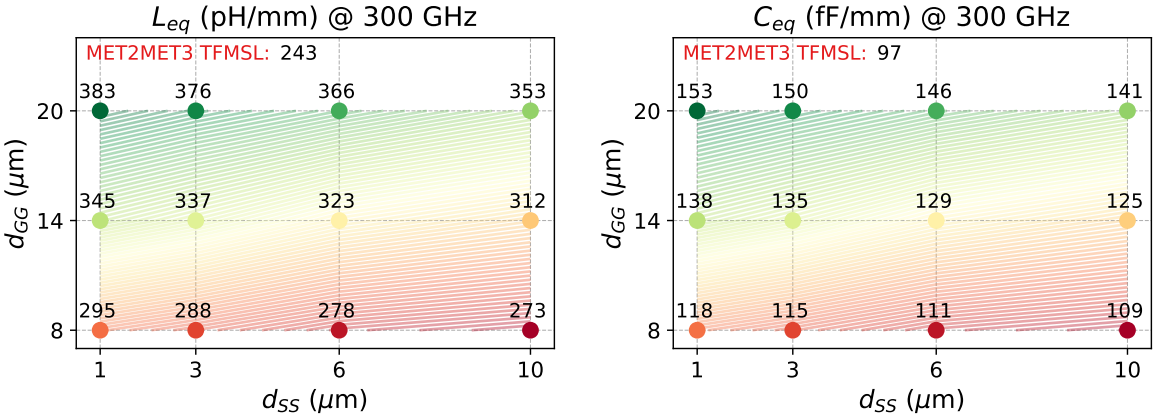
(a) (b)

Figure B.2: Simulated (a) quarter wavelength and (b) quality factor Q of the *MET2MET3 ECPW* line.



(a) (b)

Figure B.3: Simulated (a) attenuation constant α and (b) phase constant β of the *MET2MET3 ECPW* line.



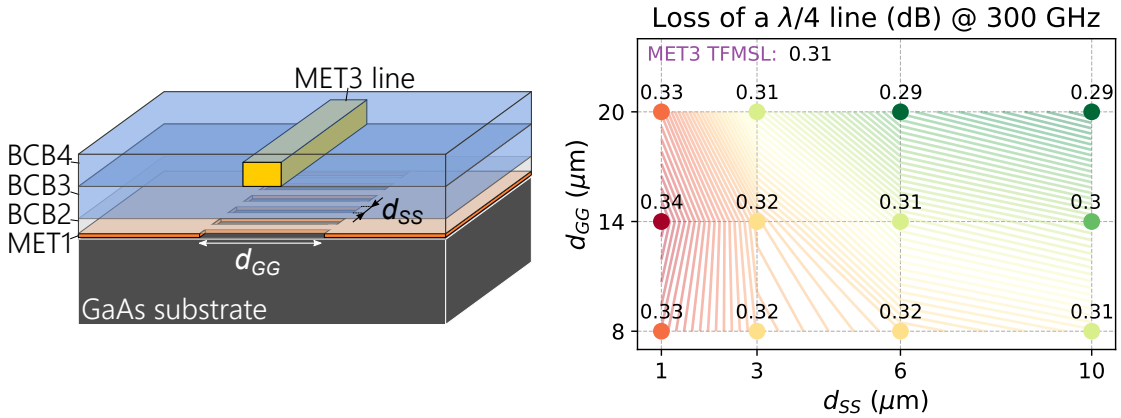
(a) (b)

Figure B.4: Simulated (a) equivalent inductance L_{eq} and (b) equivalent capacitance C_{eq} of the *MET2MET3 ECPW* line.

B.2 Additional Information on the MET3 ECPW

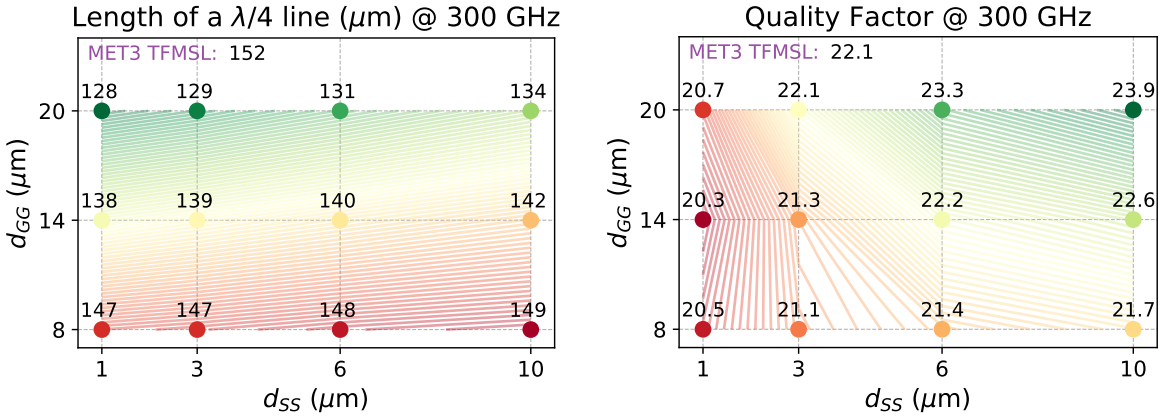
Fig. B.5 and Fig. B.6 show the heat-map simulation results of the *MET3 ECPW* which are also discussed in Section 4.3. Depicted are the loss and the length of a quarter-wavelength transmission line as well as the corresponding quality factor. The two design parameters d_{SS} and d_{GG} are in the range of 8 to 20 µm in the case of the ground-to-ground spacing d_{GG} and 1 to 10 µm in the case of the strip-to-strip spacing d_{SS}.

Furthermore, Fig. B.7 shows the simulated attenuation constant α and phase constant β. The corresponding equivalent inductance L_{eq} and equivalent capacitance C_{eq} are depicted in Fig. B.8.



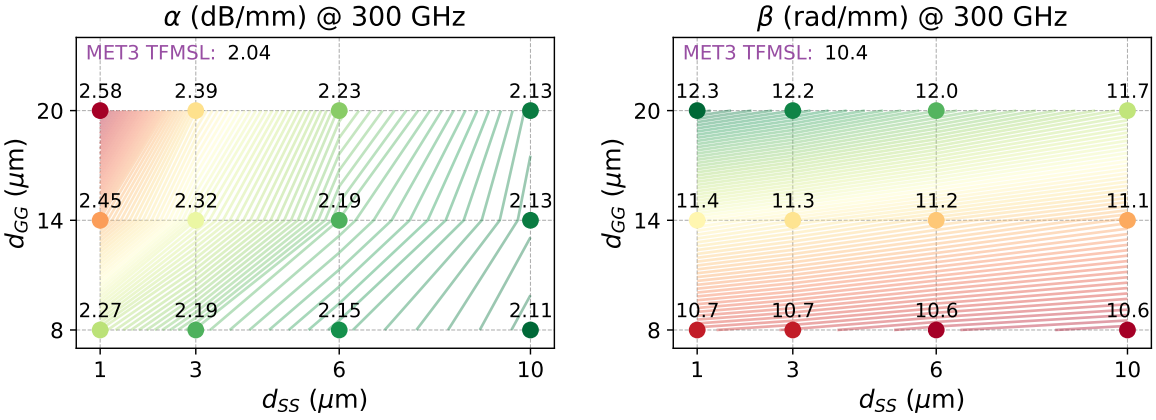
(a) (b)

Figure B.5: (a) *MET3 ECPW* transmission line with the design parameters d_{gg} and d_{ss} (d_{gg}: ground-to-ground spacing, d_{ss}: MET1-stripe spacing). (b) Simulated loss of the *MET3 ECPW* line for a length of $\lambda/4$.



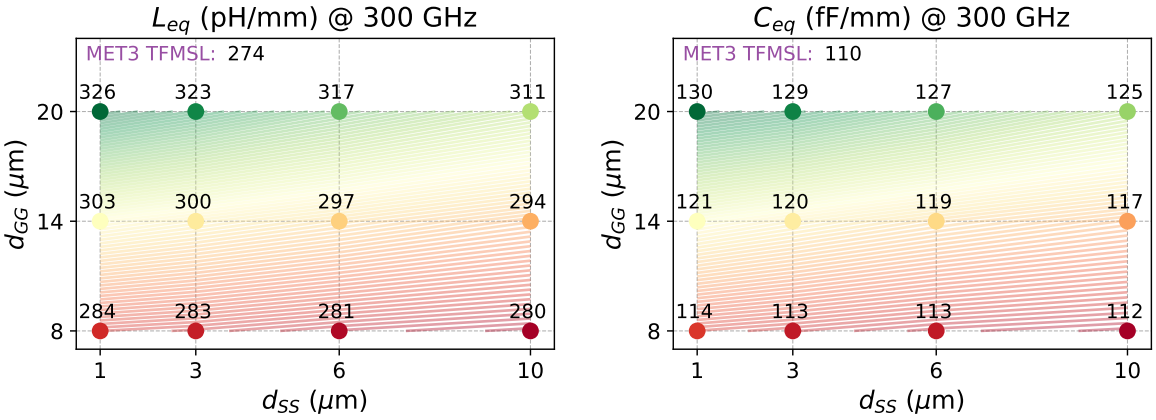
(a) (b)

Figure B.6: Simulated (a) quarter wavelength and (b) quality factor Q of the *MET3 ECPW* line.



(a) (b)

Figure B.7: Simulated (a) attenuation constant α and (b) phase constant β of the *MET3 ECPW* line.



(a) (b)

Figure B.8: Simulated (a) equivalent inductance L_{eq} and (b) equivalent capacitance C_{eq} of the *MET3 ECPW* line.

C Modeling of Passive TFMSL Components

For the implementation of scalable TFMSL schematic elements, TFMSL components are modeled in ADS using the "MLIN" model from the "TLines-Microstrip" library. For each TFMSL environment—e.g. *MET2 TFMSL*, *MET2MET3 TFMSL*, *MET3 TFMSL* described in Section 2.3—the substrate parameters of an "MSUB" substrate model are fitted to the 3D EM simulation data of the corresponding CST model, and are verified for different transmission line dimensions in the frequency band of interest. T-junctions and other transmission-line components are then modeled using the microstrip-line elements from the "TLines-Microstrip" library.

TFMSL parallel capacitors and series capacitors are modeled using the equivalent circuit diagrams depicted in Fig. C.1.These schematics represent the actual layout of the thin-film capacitors, which are shown in Fig. C.2—consisting of the rectangular capacitor and the required connecting lines at the input and at the output. For the depicted case of connections to the *MET3-TFMSL* environment, the corresponding substrate model is considered in the schematics in Fig. C.1. In the case of the series capacitor depicted in Fig. C.1(a) and Fig. C.2(a), respectively, the lower MET2 electrode is connected via an additional *MET2MET3 TFMSL* with the length L_{con} to the output MET3 output line.

To account for the actual electrical size of the capacitor, the rectangular MIM capacitor is modeled using the depicted transmission lines as well as a lumped capacitor in the middle. The transmission lines have the width W_{capa} and half of the length L_{capa} of the corresponding MIM-cap area. The size of the capacitor is calculated according to

$$C_{\mathrm{cap}} = (L_{\mathrm{capa}} - 2d_{\mathrm{oversize}}) \cdot (W_{\mathrm{capa}} - 2d_{\mathrm{oversize}}) \cdot C_{\mathrm{area}}, \tag{C.1}$$

with C_{area} being the 0.8-fF/µm^2 capacitance per area of the SiN layer. The two transmission lines are implemented in *MET2MET3 TFMSL* environment, since the layer sequence of the MIM capacitor corresponds to the one of the MET3 reinforced thin-film line, including the closed SiN layer. Hence, the distributed effects of the MIM caps are accurately described with this thin-film line.

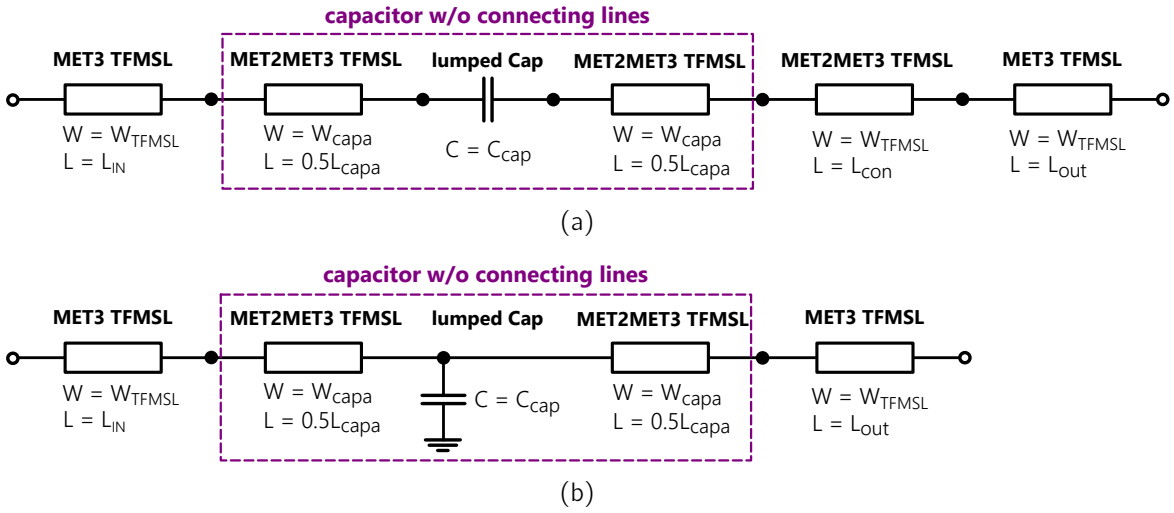


Figure C.1: Equivalent circuit diagram of (a) TFMSL series and (b) TFMSL parallel capacitors.

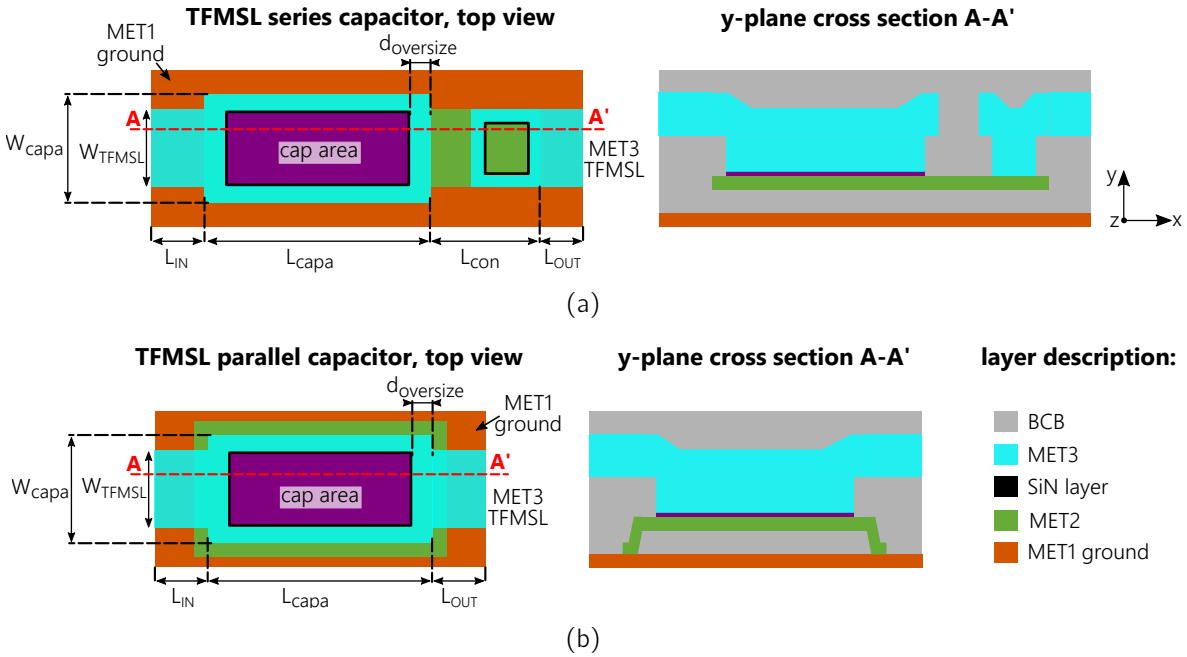


Figure C.2: Simplified layout and cross section of (a) TFMSL series and (b) TFMSL parallel capacitors.

D Waveguide to MMIC Transition

The simplified schematic view of the waveguide-to-MMIC transition, which is implemented in the waveguide package described in Section 5.2, is shown in Fig. D.1. Note that the depicted physical dimensions of the waveguide, substrates and metal layers are not to scale.

A longitudinal probe (typically described as E-field probe or E-plane probe) is used transverse to the propagation direction of the wave in the waveguide, to realize the transition from the waveguide to the microstrip line (MSL) on a 50-µm-thick quartz substrate. This E-field probe is inserted from the broad sidewall into the waveguide. The transition from the MSL to the RF pad and the TFMSL environment on the MMIC is then realized via wedge bonding with a 17-µm-diameter gold wire. To avoid this bond connection, the transition including the E-field probe can also be integrated directly on the GaAs substrate [49, 110, 108].

The TSVs around the RF pad play an essential role and are a key element of this transition, as they are required to realize the ground connection from the MSL to the front-side ground plane of the MMIC. Additionally, since the TFMSL circuits are implemented on a low-loss GaAs substrate, a via cage around the MMIC is typically required to avoid any energy from propagating into the substrate at the die edge. Hence, wafer thinning and backside processing of the GaAs wafers is required to implement this waveguide-to-MMIC transition.

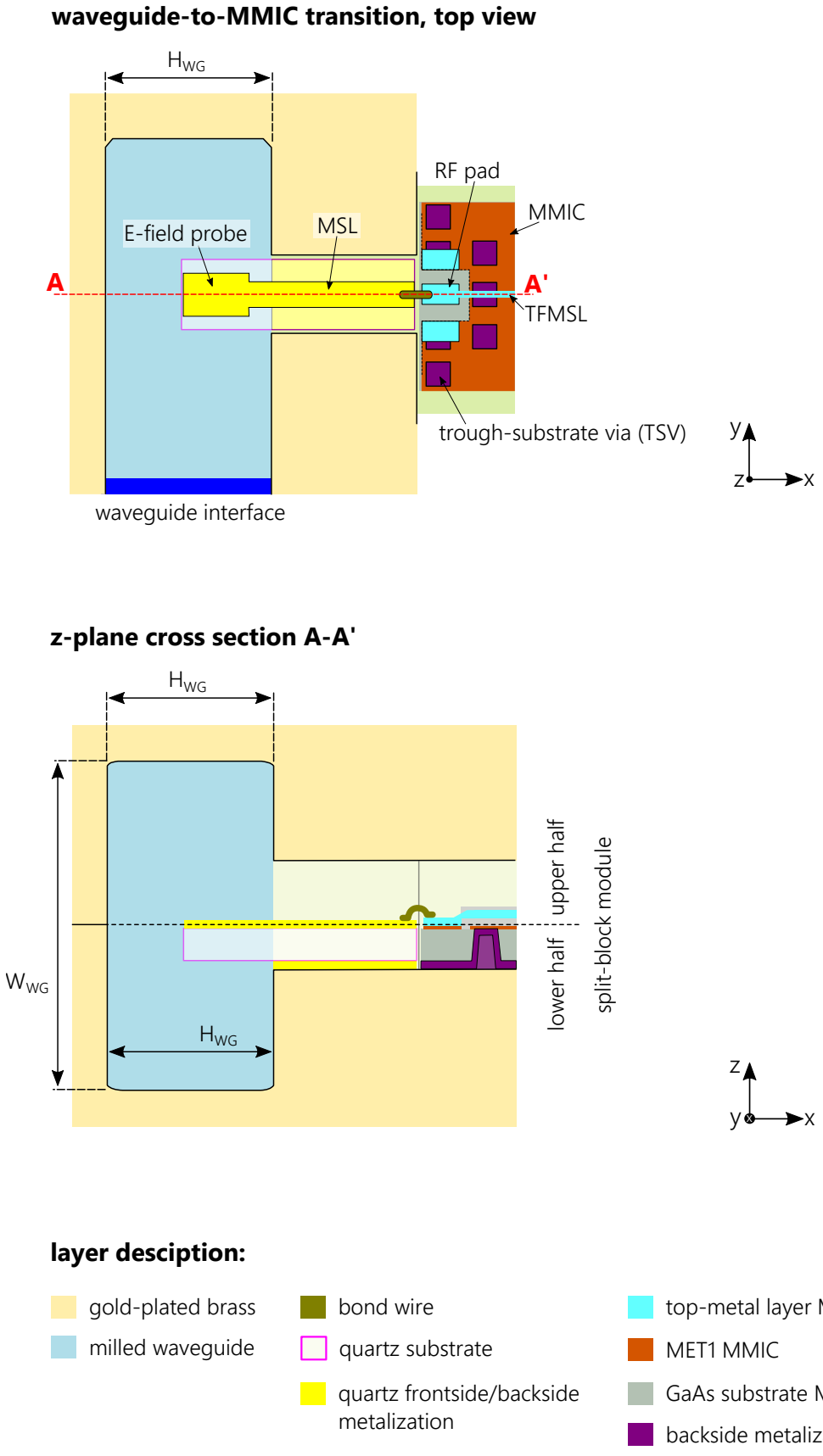


Figure D.1: Simplified schematic top view and cross section of the used waveguide to MMIC transition, including the quartz transition and a TFMSL circuit on a GaAs substrate. The depicted physical dimensions of the waveguide, substrates and metal layers are not to scale.

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Driven by the large absolute bandwidths that are available at the sub-mm-wave frequency range around 300 GHz, wireless high-data-rate communication systems and high-resolution imaging applications are being extensively investigated in recent years. Due to their superior characteristics in terms of noise figure and cutoff frequencies, InGaAs-channel HEMT devices have proven to be a key technology to implement the required active front-end MMICs for these wireless THz systems, enabling ultra-high bandwidths and state-of-the-art noise performance.

This work describes the modeling, design, and characterization of 300-GHz HEMT-based power amplifier cells and demonstrates the implementation of highly compact amplifier MMICs and broadband waveguide modules. These amplifiers are key components for the implementation of high-performance chipsets for wireless THz systems, providing high output power for the utilization of next-generation communication and imaging applications. A unique amplifier topology based on multi-finger cascode and common-source devices is developed and evaluated, demonstrating more than 20-mW measured output power at the sub-mm-wave frequency range around 300 GHz.

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