Efficiency Comparison of Three-Phase Four-Wire Inverter Topologies for Unbalanced and Nonlinear Loads

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Abstract

The transition of the energy system to renewable energy sources led towards a higher penetration of distributed energy production. Therefore, inverters have to provide a growing amount of grid services, like reactive power compensation, load balancing and harmonic elimination. In this paper, a three-leg and a four-leg four-wire inverter topology for grid building voltage source inverters for unbalanced and nonlinear loads are compared. Simulation results of the inverter efficiency at different operating points and the impact of the two topologies onto the DC-Link capacitors are presented.

1 Introduction

In island networks and micro grids, a high amount of energy sources, like wind-turbines, PV generators, batteries or fuel cells, are typically combined with smaller conventional generators. The rising amount of power electronic connected sources and loads makes it necessary that these devices support load balancing, reactive power and harmonic current compensation to prevent damage to conventional generators or transformers. Widely used three-phase current source inverters are designed to feed a symmetric three-phase current into the grid. Voltage source inverters (VSI) can support load balancing with grid-forming control methods or other power devices like unified-power-flow-controllers (UPFC) or transformers [1, 2].

Changing the topology of the grid inverter is another approach to face the problems of load unbalance by the current inverter itself, without using additional devices. In this paper, two possible topologies for micro grid and island grid inverters are compared by calculation and by simulation.

2 Comparison between three-leg and four-leg topologies

Typical four-wire VSI, shown in **Fig. 1**, consist of three half-bridges (legs) which are connected to a DC-link on one side and to a grid-tied sine filter on the other side. For the purpose of supplying grid-supporting control strategies, the common three-wire inverter is extended by an additional connection of the neutral wire to the centre point of the DC-link capacitors. This allows a neutral current flow to handle unbalanced and nonlinear loads.

In the four-leg topology, shown in **Fig. 2**, the neutral wire is not connected to the DC centre point, but instead to another half-bridge. In direct comparison to the three-leg topology, the four-leg topology requires two more semiconductor devices and the corresponding drivers, which results in an additional effort to the system.

Using the four-wire three-leg topology in **Fig. 1**, only sinusoidal pulse width modulation (SPWM) is possible because of the direct connection of the neutral wire to the centre point of the DC-link capacitors. Therefore modulation techniques like space vector modulation (SVPWM) or third-harmonic injection modulation (THIPWM) are not possible and unbalanced grid voltages and neutral currents lead to voltage alterations in the DC-link capacitors C_1 and C_2. The capacitors must be dimensioned to handle the neutral currents and to keep enough voltage to reach the peak voltage of the three phases.

Using the four-wire four-leg topology in **Fig. 2** prevents the voltage alteration between the upper and lower DC-link capacitors. Hence, the capacitance of the DC-link can be reduced compared to the three-leg topology [3].

The four-leg topology enables the inverter to modulate a common mode current onto the neutral wire and consequently enables the usage of modulation techniques like SVPWM or THIPWM. The minimum DC-link voltages [4] for both topologies are calculated by (1) and (2), with consideration of a safety margin k for control and voltage drop on the semiconductors as well as the magnetic components.

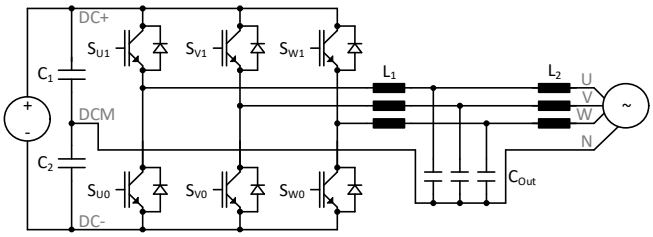

Fig. 1: Two-level three-leg VSI.

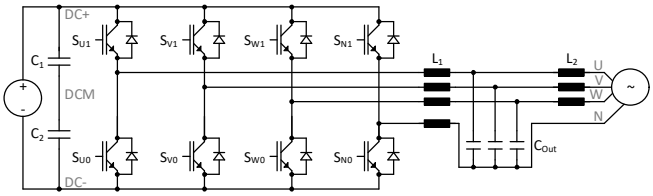

Fig. 2: Two-level four-leg VSI.

$$V_{DC,3-leg} = k \cdot V_{UN} \cdot \sqrt{2} \cdot 2 \tag{1}$$

$$V_{DC,4-leg} = k \cdot V_{UN} \cdot \sqrt{2} \cdot \sqrt{3} \tag{2}$$

The reduced DC-link voltage for the four-leg topology can lead to lower stress for the semiconductor devices as well as the DC-link capacitors and can increase the reliability of the system.

2.1 Capacitance Calculations

In the following subsections, the minimal DC-link capacitance for both topologies will be calculated. The calculation considers the worst-case unbalanced load scenario of full current in one phase, while the other two phases carry no current. This simplified approach is also valid for a two-phase load, since the neutral wire's current will always form according to the difference of the currents, presenting the same load for the DC-link capacitors.

We assume that the system's controller regulates the voltage deviations in the DC link capacitors to be centred around their nominal voltage to balance the voltage loads between them.

2.1.1 Capacitance calculation for the two-level three-leg topology for unbalanced loads

A simplified schematic for the case of an unbalanced load on only one inverter leg is depicted in **Fig. 3**. By applying Kirchhoff's laws onto the left-hand mesh and onto the node between the capacitors, we receive (3) and (4).

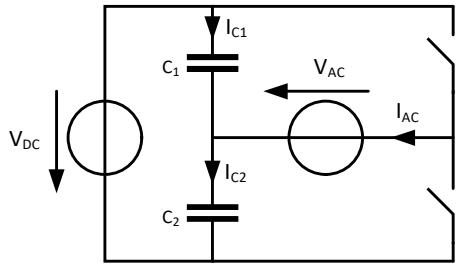

Fig. 3: Simplified schematic of the two-level three-leg VSI under unbalanced load on one phase leg.

$$V_{DC} = v_{c1} + v_{c2} \tag{3}$$

$$i_{AC} = i_{C2} - i_{C1} \tag{4}$$

We apply the formula for capacitor currents onto the right-hand side of (4) and insert (3) to receive (5), while assuming that the capacitors C_1 and C_2 are identical ($C_1 = C_2 = C$). Afterwards, we integrate that result with respect to time, which yields (6) as a general description for the time-dependent voltage function of v_{C1}. The integration constant c_1 can be found by applying the boundary condition at time zero, where v_{C1} has to start with maximum voltage deviation (7). Inserting (7) into (6), we receive (8) as the application-specific capacitor voltage function.

$$\begin{aligned} i_{AC} &= C\frac{d}{dt}(v_{C2} - v_{C1}) \\ &= C\frac{d}{dt}(V_{DC} - 2v_{C1}) \end{aligned} \tag{5}$$

$$\begin{aligned} v_{C1}(t) &= \frac{1}{C}\int i_{AC}dt \\ &= \frac{\hat{\imath}_{AC}}{2\omega C}\cos(\omega t) + \frac{V_{DC}}{2} - \frac{c_1}{2} \end{aligned} \tag{6}$$

$$\begin{aligned} v_{C1}(t=0) &= \frac{V_{DC} + \Delta v_C}{2} \\ \frac{\hat{\imath}_{AC}}{2\omega C} + \frac{V_{DC}}{2} - \frac{c_1}{2} &= \frac{V_{DC} + \Delta v_C}{2} \\ c_1 &= \frac{\hat{\imath}}{\omega C} - \Delta u_C \end{aligned} \tag{7}$$

$$v_{C1}(t) = \frac{\hat{\imath}_{AC}}{2\omega C}(\cos(\omega t) - 1) + \frac{V_{DC} + \Delta v_C}{2} \quad (8)$$

Looking for a description of the required DC-link capacitance, we can evaluate (8) at the end of the positive AC current half-wave, where $v_{C1}(t)$ reaches its minimum voltage, and solve that equation for C (9). This description allows the calculation of the required DC capacitance for the two-level three-leg VSI with respect to the AC current, the grid frequency and the allowable voltage deviation on the capacitor, which again depends on its type and manufacturer. This formula is valid for both C_1 and C_2, as the negative half-wave's load onto the DC link capacitors is symmetrical to the positive one.

$$v_{C1}\left(t = \frac{T}{2}\right) = \frac{V_{DC} - \Delta v_C}{2} \qquad C = \frac{\hat{\imath}_{AC}}{\omega \Delta v_C} \quad (9)$$

2.1.2 Capacitance calculation for the two-level four-leg topology for unbalanced loads

The four-leg topology (**Fig. 2**) does not possess a DC centre point connection; therefore, the DC link capacitance can be viewed as a single capacitor. If the voltage source possesses a sufficiently low impedance and the fourth leg for the neutral wire modulates a current that is the exact opposite of the phase current, then, by definition, the DC capacitor does not exhibit a voltage change at all.

This results in a theoretical possibility to omit the DC-link capacitance from this topology saving space and cost ($C_1 = C_2 = 0$). In practical applications however, the voltage source will not be ideal while the currents in the phase leg and the neutral leg will not be perfectly identical. Since real applications also exhibit parasitic inductances between the DC source and the VSI, there will also still be a requirement to supply a low-inductive path close to the semiconductors in order to address their switching transients.

The DC capacitor can therefore *not* be omitted entirely, yet its main load will not be defined by the AC phase current, but (largely) by the supply of the fast di/dt transients for the semiconductors.

It will thus be considerably smaller than in the two-level three-leg VSI – so much so that in comparison, it will have virtually no effect onto the total converter size.

3 Simulation and Results

To compare the behaviour and the properties of the three-leg and the four-leg topologies, both were modelled in PLECS. For the calculation of the semiconductors' switching and conduction losses, the thermal model of the SiC half-bridge module Infineon FF11MR12W1M1_B11 was used for every semiconductor device.

A three-phase inverter system with a total apparent power of $S_N = 42.5\ kVA$ was used to compare both topologies. The system line-to-neutral voltage is $V_{AC} = 230\ V$ with a nominal RMS phase current of $I_{AC} = 63\ A$. Further boundary conditions are defined in **Tbl. 1**.

The following sections illustrate the differences of the chosen topologies regarding their losses and the dimensioning of the DC-link capacitors.

Tbl. 1: Boundary conditions for the topology comparison through simulation

Phase current, RMS	63 A
Grid voltage, line-to-neutral	230 V
Output power per Phase	14.5 kVA
Grid frequency	50 Hz
Switching frequency	72 kHz
Heatsink Temperature	90° C

3.1 Pre-Simulation Investigations

To investigate the behaviour of the losses and of the voltage deviations for unbalanced and nonlinear loads, we will analyse the sequence components of each case according to [5]. In these analyses, the current amplitude and phase angle of a single phase are varied while the other two phases remain in nominal operation.

Fig. 4 represents the variation of the current's phase angle φ (nonlinear loads) and **Fig. 5** shows the variation of the phase current I_{AC} (unbalanced loads). Both figures' sequence components and neutral wire currents are normalised to the nominal phase current under symmetric load condition.

Fig. 4 shows that for nonlinear loads, the neutral wire's current reaches its minimum at a phase angle of zero and its maximum at angles of $\varphi = \pm\pi/3$, respectively. This means that we cannot allow nonlinear loads with phase angles $|\varphi| > \pi/3$ without exceeding the nominal phase current in the neutral wire, which would risk overheating and/or

damage to the system, if this condition were not anticipated during system design.

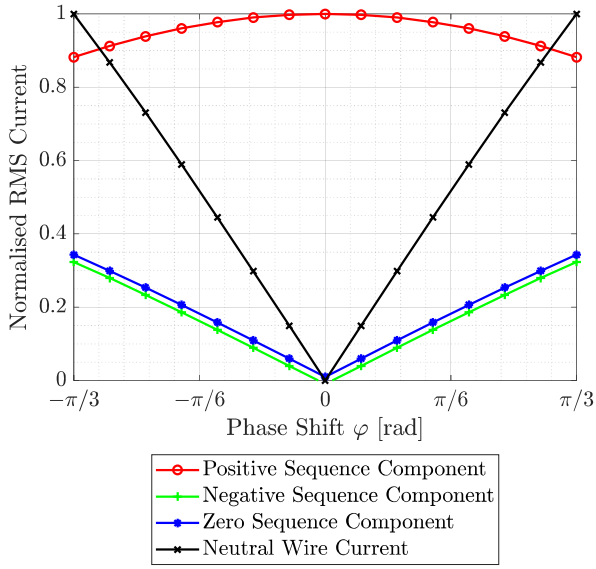

Fig. 4: Sequence components and neutral wire current for the three-leg and four-leg topologies, varying the phase angle φ of a single phase (nonlinear load condition).

In **Fig. 5**, we see that a reduction of a single phase current leads to an increase of the neutral wire's current. When the phase current is reduced to zero, the neutral wire current reaches its maximum value, leading to the worst-case condition for the DC-link capacitors as calculated in Section 2.1.

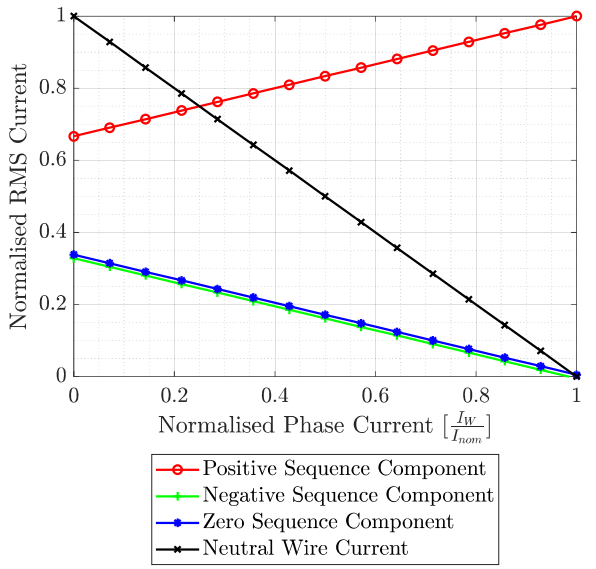

Fig. 5: Sequence components and neutral wire current for the three-leg and four-leg topologies, varying the current I_{AC} of a single phase (unbalanced load condition).

3.2 Simulation parameters and operating points

To simulate these topologies, the necessary voltages and capacitances need to be calculated for both variants.

3.2.1 Capacitance and DC voltage calculations for the three-leg topology

For the three-leg topology, an acceptable voltage variation in each of the split DC-link capacitors needs to be defined, i.e. for both C_1 and C_2 in **Fig. 1**. For the given application (see **Tbl. 1**), the aluminium electrolytic capacitor TDK B43547-A5567M000 with a capacitance of $C = 560\ \mu F$ was chosen. The datasheet provides information about a maximum RMS-current of $I_C = 5.37\ A$ at a ripple frequency of $f_{Ripple} = 100\ Hz$. For this topology and for unbalanced loads however, we need a current specification for a deviation frequency of $f_{Ripple} = 50\ Hz$, as the capacitor's voltage will vary with grid frequency. Following the datasheet, a corrective factor of $k_f = 0.8$ can be used to calculate the acceptable current load at this frequency.

We can find the allowable voltage variation Δv_C for this specific capacitor by evaluating its device equation, keeping in mind that the voltage variation Δv_C will reach its maximum after half a grid cycle (10).

$$\begin{aligned}\Delta v_C &= \frac{1}{C}\int_0^{\frac{T}{2}} i_C(t)\,dt \\ &= \frac{k_f \cdot \hat{I}}{C}\left[-\frac{1}{\omega}\cos(\omega t)\right]_0^{\frac{T}{2}} \\ &= \frac{2\cdot\sqrt{2}\cdot 0.8\cdot 5{,}37\ A}{2\pi\cdot 50\ Hz\cdot 560\mu F} \\ &\approx 69\ V\end{aligned} \tag{10}$$

Using that value, we can further find the minimum required capacitance for each half of the DC-link by inserting this result into (9):

$$\begin{aligned}C_{3leg} &= \frac{I_{AC}\cdot\sqrt{2}}{2\pi f\cdot\Delta v_C} \\ &= \frac{63\ A\cdot\sqrt{2}}{2\pi\cdot 50\ Hz\cdot 69\ \mathrm{V}} \\ &\approx 4.1\ mF.\end{aligned} \tag{11}$$

Since the selected capacitor only comes with fixed values per piece, a minimum amount of 8 devices per half of the DC-link is required, totalling to 16 devices overall. Taking the square footprint area

as the minimum PCB space required, these 16 capacitors occupy a volume of about 1.1 Litres and will add a weight of approx. 1.3 kg to the system.

To guarantee that each half of the DC-link carries enough voltage to be able to feed power into the AC grid at all times, we have to increase the nominal DC voltage. While the DC voltage can be considered as constant, the individual capacitors' voltages also need to be kept above half the minimum value defined by (1) while they are being discharged by an unbalanced AC current. Hence, their nominal voltage has to be increased by at least $\Delta v_C/2$ (per capacitor) to account for this effect. This means that the total DC voltage has to be increased by at least Δv_C, which in turn has to be added to (1).

With a safety margin factor of $k = 1.1$, we receive a minimum total DC voltage for the three-leg topology according to (12).

$$\begin{aligned} V_{DC,3leg} &= k \cdot V_{AC} \cdot \sqrt{2} \cdot 2 + \Delta v_C \\ &= 1.1 \cdot 230\,V \cdot \sqrt{2} \cdot 2 + 69\,\mathrm{V} \\ &\approx 785\,V \end{aligned} \tag{12}$$

3.2.2 Capacitance and DC voltage calculations for the four-leg topology

For the four-leg topology, we can use the THIPWM modulation scheme, as it is possible to modulate a common mode voltage onto the neutral leg of the inverter. We can therefore use a reduced DC voltage for this topology while still enabling full power transfer.

As described in Section 2.1.2, in theory there is no significant voltage alteration to be expected on the DC capacitors. It is therefore not necessary to increase the DC voltage by the capacitor's voltage imbalance and we can calculate the minimum DC voltage for the four-leg topology directly using (2):

$$\begin{aligned} V_{DC,4leg} &= k \cdot V_{AC} \cdot \sqrt{2} \cdot \sqrt{3} \\ &= 1.1 \cdot 230\,V \cdot \sqrt{2} \cdot \sqrt{3} \\ &= 620\,V. \end{aligned} \tag{13}$$

As no significant voltage alteration will be present here, we can reduce the DC capacitance to a minimum. For the PLECS simulation, the capacitance for one half of the DC-link is arbitrarily defined as $C_{4leg} = 50\,\mu F$, which should still be plenty more than would be needed to address the low-inductive current demand of the semiconductor's switching transients.

3.3 Simulation model

The DC-link parameters that follow these calculations and that are used in the PLECS simulation are summarised in **Tbl. 2**. The designed simulation models are based on a simplified modulation schemes and ideal semiconductor models. They are shown in **Fig. 6** and **Fig. 7**.

Tbl. 2: Summary and comparison of the Three-Leg and Four-Leg topology simulation parameters

Three-Leg	DC-Link Voltage	785 V
	Capacitance C_1, C_2	4.1 mF
Four-Leg	DC-Link Voltage	620 V
	Capacitance C_1, C_2	50 µF

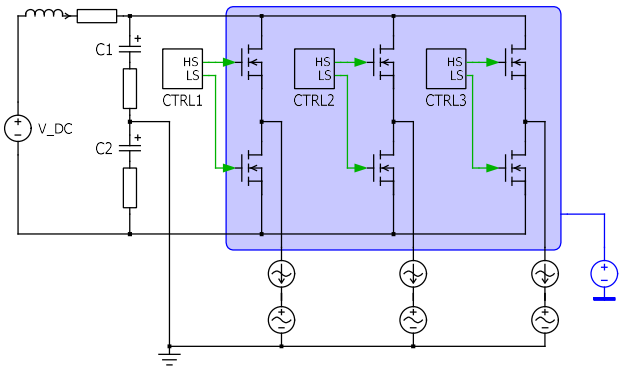

Fig. 6: Three-leg two-level simulation model

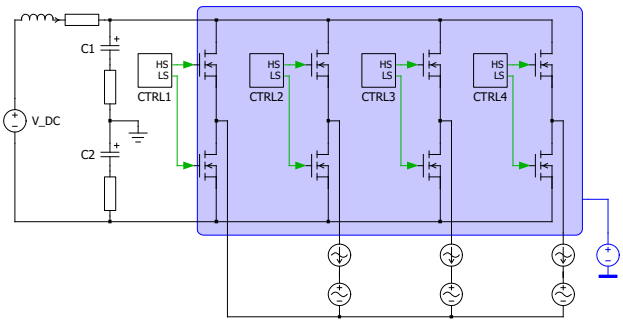

Fig. 7: Four-leg two-level simulation model

3.4 Simulation Results

The first analysis of the simulated topologies compares the respective capacitor voltages in case of nominal power in a single phase and no current flow in the other two phases

Afterwards, the semiconductor switching and conduction losses as well as the voltage deviations of the DC-link capacitors for the investigated topologies are investigated. They are further compared

by altering the phase angle and the amplitude of a single phase.

3.4.1 Capacitor Stress Comparison under Nominal Load

In **Fig. 8**, we can clearly identify a drastic reduction in the capacitors' voltage deviations when comparing the four-leg and the three-leg topology. The remaining deviation of $\Delta v_{C,4leg} \approx \pm 2.5\,V$ around the nominal capacitor voltage consists of both a grid-frequency component as well as the transient currents imposed by the semiconductors. Though the investigation in Section 2.1.2 predicted a negligible AC-component in the capacitors' voltages, these components do play a role in this simulation because a small LR filter had to be implemented between the DC source and the capacitors, resulting in a non-ideal decoupling of the DC capacitors from the AC currents.

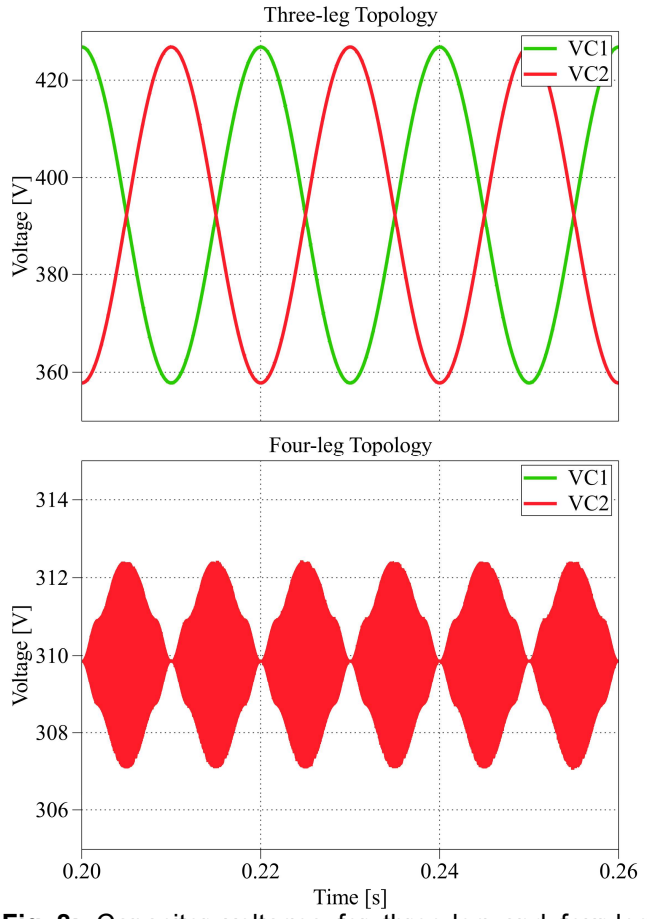

Fig. 8: Capacitor voltages for three-leg and four-leg topology under worst-case unbalanced load conditions.

For the three-leg topology, we can also validate the maximum voltage swing of about 69 V per capacitor, as calculated in (10).

3.4.2 Nonlinear Loads

Fig. 9 presents the losses and voltage deviation in the DC-link capacitors for nonlinear load conditions by varying the phase angle φ of one phase. A phase angle of zero represents nominal operation (full active power), while phase angles of up to $\varphi = \pm\pi/3$ correspond to the highest allowed inductive and capacitive reactive power states on this phase (see Section 3.1).

We can see that the four-leg topology experiences lower switching losses and similar conduction losses for phase angles of approx. $\varphi \leq \pm\pi/5$ when compared with the standard three-leg VSI. Up to this nonlinearity, we can expect a better efficiency for the four-leg inverter, while the three-leg inverter will be more efficient for larger phase angles (higher nonlinear loads).

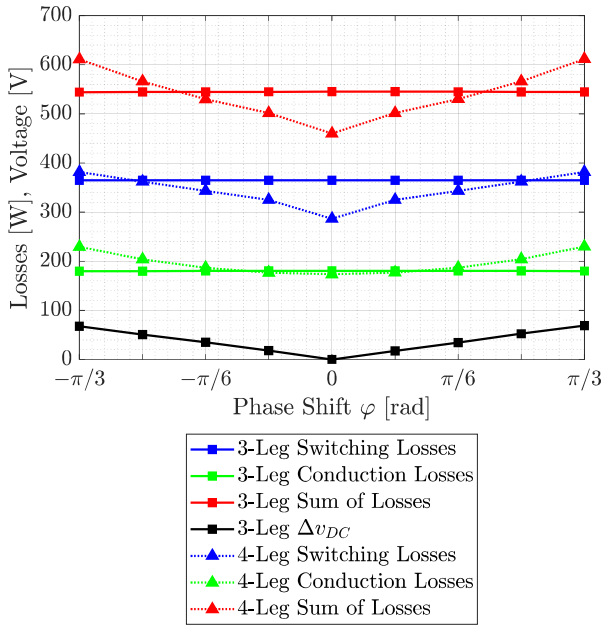

Fig. 9: Voltage deviation, switching- and conduction losses for the three-leg and four-leg topology under nonlinear load conditions.

3.4.3 Unbalanced Loads

The influences of unbalanced loads of varying intensity can be seen in **Fig. 10**. For this investigation, the simulated VSIs are subjected to unbalanced load conditions by varying the output current in one phase from $I_{AC} = 0\,A$ to $I_{AC} = 63\,A$.

We can again identify operating conditions in which the four-leg topology exhibits lower total losses than the three-leg inverter, at or above unbalanced phase currents of $I_{AC} \approx 30\,A$. For more nonlinear loads (lower phase currents), both the switching and conduction losses of the four-leg

topology become dominant and again, the three-leg VSI will provide higher efficiencies.

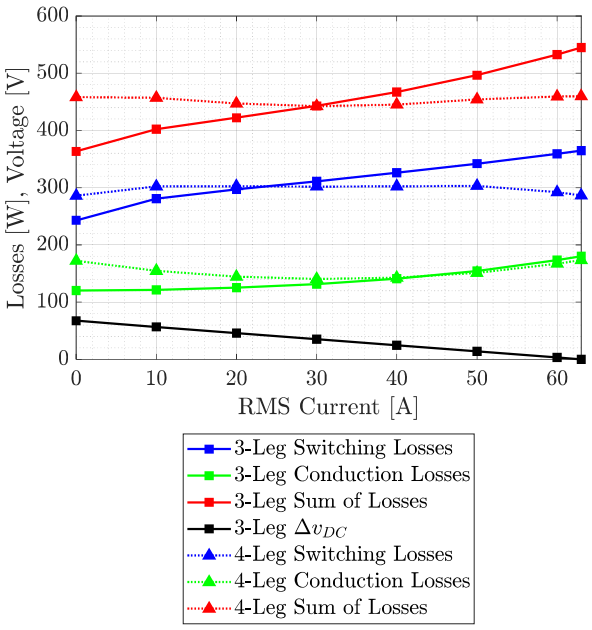

Fig. 10: Voltage deviation, switching- and conduction losses for three-leg and four-leg topology under unbalanced load conditions.

3.4.4 Simulation Summary

At first, it may seem beneficial to use three-leg inverters for environments that experience non-linear and/or unbalanced loads, yet such extreme conditions in which there *can* be lower losses than with the four-leg topology are quite rare. This seeming “advantage” of the three-level topology is also paid for with a comparatively large DC-link capacitance, increasing its cost, volume and weight. Additionally, this three-leg capacitance will have to operate at a higher DC-voltage, as the fixed connection between the DC centre point and the neutral wire only allows sinusoidal modulation.

The four-leg VSI on the other hand enables the possibility to use THIPWM as a modulation scheme, which leads to a reduction of the DC-link voltage by $165\,V$, compared to the three-leg topology. This lower voltage reduces the occurring switching losses of the semiconductors in the points of operation that are most likely to appear.

Looking at the best-case loss improvements for nonlinear and unbalanced loads however, we can identify a semiconductor-based loss reduction of about $80\,W$ or about $15\,\%$ for the four-leg inverter.

There is still the need of an additional AC inductance for the four-level converter that will generate additional losses. Due to the lower DC voltage in the four-leg topology, its inductors can be dimensioned smaller than for the three-leg inverter for the same ripple current. The losses for these devices will have to be investigated further to enable a fair overall efficiency comparison between these candidate topologies.

4 Conclusion

This paper presents a comparison between two topologies of voltage source inverters for micro and island grids that are capable of handling unbalanced and nonlinear load conditions. A calculation method for the DC-link capacitance for the three-leg topology and simulation results of the semiconductor losses for different load conditions are presented. A comparison of switching and conduction losses shows a higher efficiency of the four-leg topology for mild unbalanced and non-linear load conditions, while the three-leg topology is more efficient in cases where these properties are larger. It is identified that this behaviour coincides with very large capacity values for the three-leg VSI’s DC-link capacitors, while the four-leg topology almost exclusively needs to be dimensioned for the transient currents imposed by the power semiconductors.

5 References:

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