HIGH-EFFICIENCY SILICON SOLAR CELLS FOR LOW-ILLUMINATION APPLICATIONS

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ABSTRACT

At Fraunhofer ISE the fabrication of high-efficiency solar cells was extended from a laboratory scale to a small pilot-line production. Primarily, the fabricated cells are used in small high-efficiency modules integrated in prototypes of solar-powered portable electronic devices such as cellular phones, handheld computers etc. Compared to other applications of high-efficiency cells such as solar cars and planes, the illumination densities found in these mainly indoor applications are significantly below 1 sun. Thus, special care was taken to keep the cell efficiency level high even at very low illumination levels. For this reason, particularly the cell border was analyzed and optimized carefully. The excellent cell characteristics achieved at low illumination densities increase the benefit of a solar power supply for such devices by an order of magnitude if compared to standard solar cells.

INTRODUCTION

Although there is a general trend for more efficient cell structures in the industrial solar cell production, cells with efficiencies above 20% are still too expensive to compete with standard commercial cells in terms of price per Wp. The general strategy at Fraunhofer ISE is to develop simplified processing sequences enabling the transfer of high-efficiency structures into industrial production. A recent successful example for such a development is the Laser Fired Contacts (LFC), a simple way to fabricate dielectrically passivated rear surfaces [1].

Additionally, there is already a market for high-efficiency cells (η > 20%) even if their price per Wp is still higher. Portable electronic devices like cellular phones or portable computers have a quite high power consumption but only a small area available for photovoltaic modules. Also, the illumination level available in the typical environment of such devices is significantly below 1 sun. These two factors are important arguments for the use of high-efficiency cells.

SOLAR CELL PROCESS

Since it is not necessary to reach the absolute top level of efficiency for these applications, we have chosen the RP-PERC (Random Pyramid – Passivated Emitter and Rear Cell) structure as a good compromise between efficiency and process complexity. The cell incorporates random pyramids, one-step emitter, a dielectrically passivated front and rear surface and no boron BSF [2]. The production requires two oxidations, one phosphorus diffusion and two or three photomasking steps with relaxed alignment. The two necessary photomasking steps (pm) are the definition of the front grid and of the rear contact points. The third optional pm is needed for the definition of the emitter area for a planar diffusion. While this definition of the emitter area is not absolutely necessary for cells operating at one sun, we will show in the following that a well-defined and passivated emitter border is extremely important for a good cell performance at low illumination densities. Thus, we have included the masked emitter diffusion into our production of high-efficiency cells for low illumination densities.

The front grids of our cells are prepared for interconnection with the shingle technique, reducing the shadowing losses in the finished module to an absolute minimum (see Fig. 1).

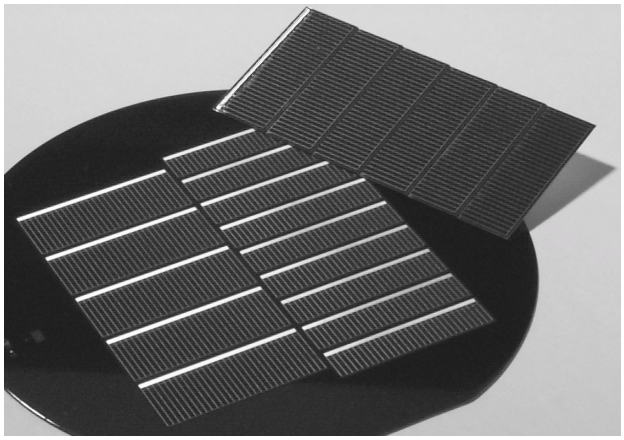

Fig. 1 High-efficiency cells before cutting and after inter-connection with the shingle technique.

PROCESS EQUIPMENT

In order to supply sufficient cells needed for prototype developments of PV-powered portable electronic devices, it was necessary to extend the lab-scale cell fabrication at Fraunhofer ISE. We identified those process steps which were particularly time-consuming and automated them. In addition to commercially available devices as e.g. a robot-handled photo-resist processing system (see Fig. 2), we

also have developed new systems like a semi-automated electro-plating unit especially designed for solar cells.

Another important goal of this activity is to achieve a much better cost evaluation for the fabrication of high-efficiency cells. The conclusions drawn from the analysis of our cost spread sheets allow us to reduce the cost of high-efficiency cells and give substantial input for the development of new cell structures and process sequences (as e.g. LFC) and their transfer into industrial production.

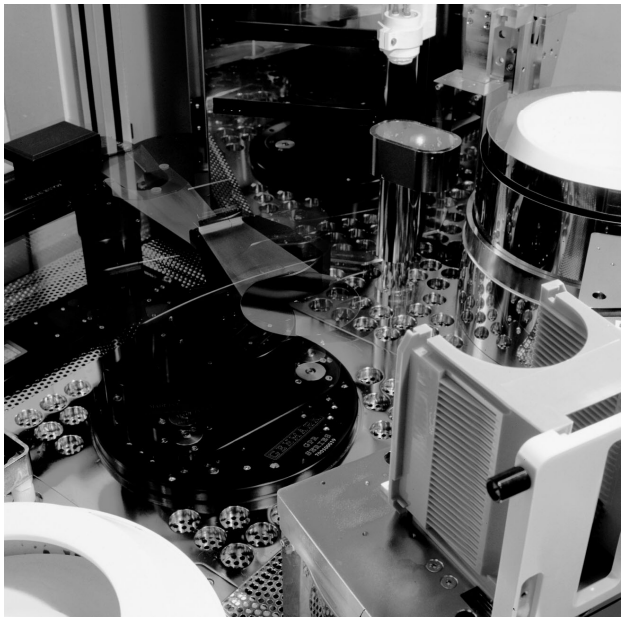

Fig. 2 Automated photo-resist processing system.

SOLAR CELL RESULTS

Fig. 3 and Tab. 1 show the distribution of the efficiency, open circuit voltage, short circuit current and fill factor of RP-PERC cells from our semi-automated high-efficiency line. Both, the high average values and the low deviations are very satisfying.

Tab. 1 Average efficiencies of RP-PERC cells fabricated at Fraunhofer ISE.

	Average	**Abs. deviation**	**Rel. deviation**
η	21.3%	0.5%	2.3%
$\mathbf{V_{oc}}$	673.5 mV	5 mV	0.7%
$\mathbf{J_{sc}}$	39.5 mA/cm^2	0.6 mA/cm^2	1.5%
FF	80.0%	1.4%	1.5%

Although it would be possible to reach efficiencies higher than 23% with available equipment, for example using the PERL process [3,4] which includes additionally a local boron back surface field, inverted pyramids and a two-step emitter, this increase of efficiency of about 10 % relative can not justify a process which is at least two or three times more complicated.

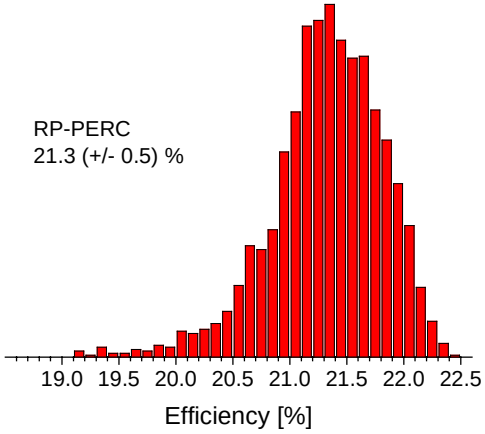

Fig. 3 Efficiency distribution of RP-PERC cells

The question might be justified if it is really necessary to increase efficiency from about 14% for a commercial cell to above 20% for an application in small portable electronic devices. In addition to the lower area consumption for the same power output at one-sun illumination there is a more important argument for the use of high-efficiency cells: their superior low-illumination characteristics (see next page) which is extremely important for the use in portable electronic devices which are mainly used under indoor conditions.

Fig. 4 Cellular phone S25 (Siemens AG) with a photovoltaic module including 8 shingled monocrystalline high-efficiency cells.

Fig. 4 shows a cellular phone (Siemens S25) with a ISE PV-module consisting of 8 shingled high-efficiency cells. All components, including cells, module interconnection, module integration and electronic circuitry were developed and fabricated at Fraunhofer ISE in a project with Siemens AG. The PV module has a high performance even at indoor conditions and increases the operational readiness significantly.

LOW ILLUMINATION CHARACTERISTICS

As already mentioned, it is extremely important that cells for such applications have an excellent output not only for the standard condition of one-sun illumination but also for significantly lower illumination levels. With conventional cells, the cell voltage falls off so rapidly for lower illumination intensity that significantly more cells are required to guarantee the voltage needed for a specific application under indoor conditions (i.e. charging of a battery). The higher number of cells on the same available area reduces the power output of the module dramatically.

Fig. 5 shows the efficiency as a function of illumination level for a high-efficiency cell and commercially available silicon solar cells. The strong drop of efficiency of the commercial cells is mainly due to a strong voltage reduction with decreasing illumination density.

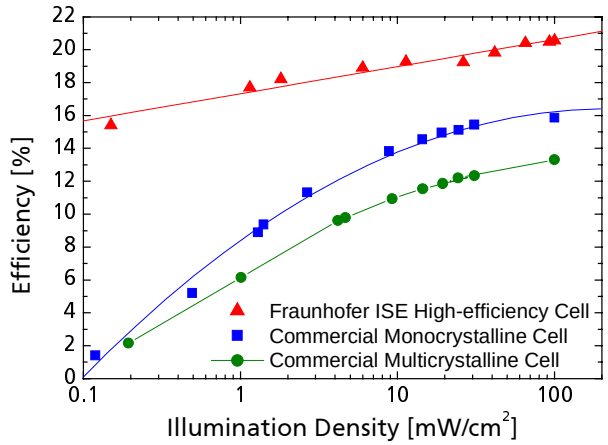

Fig. 5 Efficiency as a function of illumination level for a high-efficiency cell and commercial silicon solar cells.

Several authors have described the detrimental effect of cell borders on the overall cell performance (see e.g. Refs. 5-8). A strong increase of the space charge region dark saturation current, J_{02}, was reported for pn-junctions bordering unpassivated cell surfaces [7,8]. This increase of J_{02} is especially detrimental for the cell parameters at low illumination levels since the cell performance is then mainly influenced by the lower part of the diode characteristics which is dominated by J_{02} and R_p. Thus, an increase of J_{02} will significantly reduce the voltage at low illumination levels while V_{oc} at one sun can still be reasonable. Thus, in our study we have analyzed especially the low illumination performance as a function of cell border quality.

Fig. 6 shows the scheme of a high-efficiency cell for module integration. A special feature of high-efficiency cells is that the emitter diffusion is limited to an area smaller than the total cell area. Thus, there is a small border of undiffused p-type silicon around the cell. This cell structure guarantees on optimal passivation of the pn-junction which borders the thermally oxidized front surface, keeping the recombination current in the space charge region, J_{02}, on a very low level.

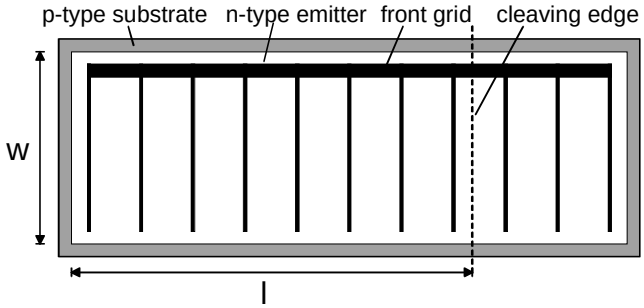

Fig. 6 Cell scheme.

In order to investigate the detrimental effect of unpassivated cell borders on the cell parameters, we have scribed our cells on the rear side with a diamond scriber and cleaved along this line (see Fig. 6). Now the pn-junction at this edge is bordering an unpassivated surface, increasing the space charge recombination current dramatically. This increase of recombination current can be observed directly by an increased temperature in a thermographic map (right cell border in Fig. 7) taken with a high resolution IR camera.

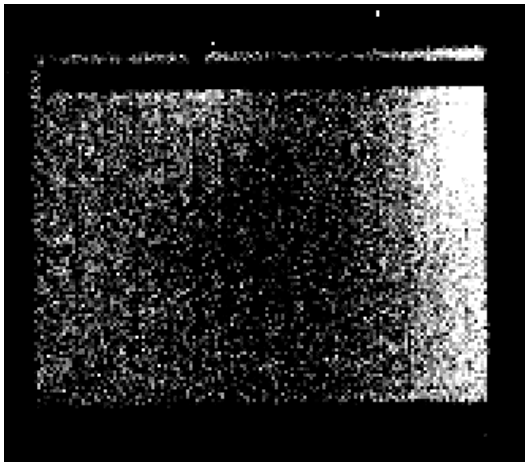

Fig. 7 Thermographic map (white = warm, black = cold) of a high-efficiency cell with one badly prepared border (right border). The bus bar can be seen as the black thick line at the top.

By subsequent cutting we have prepared cell fractions with decreasing length l and thus increasing border-to-area aspect ratios.

$$\text{Aspect Ratio} = \frac{\text{Bad Border}}{\text{Area}} = \frac{W}{W \times l} = \frac{1}{l} \qquad (1)$$

In the case of two cleaved borders the expression changes to 2/l.

After each cleavage the illuminated IV-characteristic of the remaining cell fraction was measured at four different illumination densities.

Fig. 8 shows the measured open circuit voltages for the different cell fraction and illumination densities.

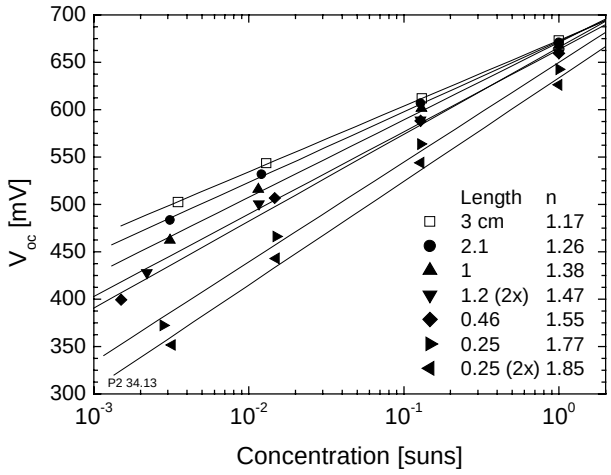

Fig. 8 Open circuit voltage as a function of concentration for cell fractions with different lengths. The first cell with a length of 3 cm is the original cell without any cleaved borders (open symbols). Cells indicated with a "2x" have two cleaved cell borders (aspect ratio = 2/l) The lines represent a one-diode fit with different ideality factors.

Using the simple one-diode cell description, V_{oc} can be expressed in the following way:

$$V_{oc} \approx n\frac{kT}{q}\ln\left(\frac{J_{sc}}{J_0}\right) = n\frac{kT}{q}\ln\left(\frac{C \times J_{sc,1sun}}{J_0}\right), \qquad (2)$$

where n is the ideality factor, kT/q is the thermal voltage, J_{sc} is the short circuit current density, J_0 is the dark saturation current density, C is the concentration in suns, and $J_{sc,1sun}$ is short circuit current for one-sun illumination.

Thus, when plotting V_{oc} versus ln(C), the slope of the resulting line is $n \times kT/q$. Fig. 9 shows the ideality factors determined from the data shown in Fig. 8.

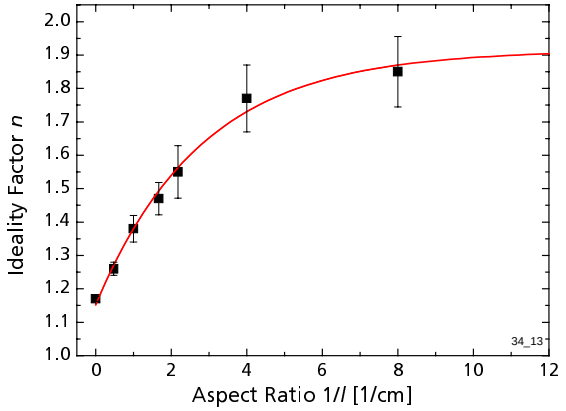

Fig. 9 Ideality factors as a function of aspect ratio *1/l* determined from the measurements shown in Fig. 8.

The ideality factor increases from a quite good value of 1.17 for the uncleaved original cell to high values close to 2 for a very small cell with a high aspect ratio *1/l*. This demonstrates the increasing influence of the space charge recombination current (with n = 2) on the cell characteristics. While the one-diode fit describes the situation for the original cell quite good (see line in Fig. 8) the fit gets more inaccurate for increasing aspect ratio 1/l.

Using the more accurate 2-diode description the dark saturation current can be calculated as a function of aspect ratio, under the assumption that the recombination current density in the bulk and emitter is not varied:

$$J(V) = J_0\left(e^{qV/nkT} - 1\right) + \frac{1}{l}J_{0,surf}\left(e^{qV/(n_{surf}kT)} - 1\right) \qquad (3)$$

where J_0 and n are the dark saturation current density and ideality factor of the original cell and $J_{02,surf}$ is the space charge recombination current density per length in A/cm. We have fitted all measured V_{oc} values simultaneously by varying n_{surf} and $J_{0,surf}$ with constant parameters for the first term (J_0 = 7.4 x 10^{-12} A/cm^2 and n = 1.17, both values derived from the one-diode fit of the uncleaved original cell). The best choice for n_{surf} and $J_{0,surf}$ is

$J_{02,surf}$ = 1.3 x 10^{-8} A/cm

n_{surf} = 2 ± 0.1 .

The value of n_{surf} = 2 shows that the additional loss channel generated at the cell border is really mainly due to the increased recombination in the space charge region.

Kühn et al. [8] have simulated numerically $J_{o,surf}$ for an ideality factor of 2 as a function of surface recombination velocity S. Our value of 1.3 x 10^{-8} A/cm is in excellent agreement with their calculation for a S value of 1x10^6 cm/s.

Our study shows that the measured perimeter losses of our cells can be described analytically very well and demonstrates the importance of properly designed cell borders especially for applications at low-illumination densities.

Acknowledgements

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