BTI variability of SRAM cells under periodically changing stress profiles

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***Abstract*—We present a BTI compact model that is able to account for the complex BTI stress patterns encountered in complex electronic circuits. Such stress patterns are composed of various blocks corresponding to different circuit operation states, protocol modes or input conditions, and the blocks repeat within a composite, hierarchical structure. The present work extends a previously introduced physics-based accurate NBTI modeling while preserving its numerical efficiency. We provide insight into some principal characteristics of BTI degradation under hierarchical stress patterns, such as a non-trivial dependence on multiple duty cycles. In particular, the NBTI degradation can sensitively depend on the temporal sequence of NBTI stress blocks, and building a model on just the average stress or on stress histograms can be misleading. An SRAM cell example demonstrates this method and compares the cell's BTI failure statistics for two different hierarchic-periods stress patterns.**

I. Introduction

Circuit designs in advanced technologies require the accurate prediction of bias temperature instability (BTI) margins. This trend triggers the development of accurate BTI compact models, addressing in particular BTI recovery and variability [1–4]. Industry standards traditionally use power-law models for time independent stress [5] and multiply duty factors for digital patterns. Advanced digital-stress modelings introduce capture-emission time (CET) maps and calculate the mean degradation mostly analytically [6]. Their generalization to analog stress [7, 8] takes into account the defect dynamics beyond CET maps. Deeply scaled technologies show a strong NBTI variability, the corresponding statistical distributions [9, 10] were applied to an SRAM failure analysis under time-independent BTI stress [11] with high resolution of the distribution tails. A methodically independent approach calculates the NBTI variability of an operational amplifier [12].

We aim at a BTI compact model for application in analog and digital circuit design. This compact model accounts for BTI recovery and BTI variability. It provides high-accuracy degradation predictions and has a fast numerical implementation [12], permitting its coupling to Spice-type electric circuit simulators. The model's benefit are predictions about the BTI drift and BTI variability of performance parameters for a particular circuit design after arbitrarily large (virtual) operation times. It thereby assists a circuit designer in the preparation of reliable circuits while reducing the costly overdesign.

This paper presents the generalization of NBTI compact models from simple digital or analog periodic stress to stress voltages with a complex periodic structure, such as encountered in complex electronic systems. Due to the particular nature of NBTI recovery, the full information about the stress pattern sequence (beyond stress histograms) is important to correctly predict the NBTI degradation. We demonstrate this method on the example of an SRAM cell and calculate its failure statistics under BTI stress with periodically changing profile.

II. BTI Compact model

The Markov two-state model [3] accounts for interface-state defects (double-well model) and (projected) oxide traps (non-radiative multi-phonon model): each defect occupies either an electrically neutral or a positively charged state (Fig. 1). The latter contributes to the NBTI threshold voltage shift via a modification of the oxide electric potential. We parametrize our effective NBTI model from the statistical defect sampling [13] for a 22nm technology [14], this provides the transition rates (discretized in voltage and temperature space) and the defect-specific step height for ~ 3000 representative defects (Fig. 2).

The two-state model defects undergo transitions between the neutral state "1" and the positively charged state "2" with an effective capture time τ_c and effective emission time τ_e. These defect-specific times sensitively depend on the gate voltage and temperature. The probability $w(t)$ of being in state "2" satisfies a first-order differential equation

$$\dot{w}(t) = a(t)w(t) + b(t), \qquad w(t_0) = w_0, \tag{1}$$

its coefficients

$$a(t) = -\left(\tau_e^{-1}(t) + \tau_c^{-1}(t)\right), \qquad b(t) = \tau_c^{-1}(t) \tag{2}$$

inherit (from the analog gate-source voltage V_{gs}) the property of taking continuous values. A fast solution algorithm [7] rewrites $w(t)$ as follows: the quantities

$$P_1(t_2, t_1) = \exp\left(\int_{t_1}^{t_2} \mathrm{d}s\ a(s)\right), \tag{3}$$

$$P_2(t_2, t_1) = \int_{t_1}^{t_2} \mathrm{d}s\ b(s) \exp\left(\int_{s}^{t_2} \mathrm{d}r\ a(r)\right) \tag{4}$$

are arranged in the 2×2 matrix

$$P(t_2, t_1) := \begin{pmatrix} P_1(t_2, t_1) & P_2(t_2, t_1) \\ 0 & 1 \end{pmatrix}, \tag{5}$$

which propagates the solution from the initial time t_0 to the solution time $t > t_0$,

$$\begin{pmatrix} w(t) \\ 1 \end{pmatrix} = P(t, t_0) \begin{pmatrix} w(t_0) \\ 1 \end{pmatrix}. \tag{6}$$

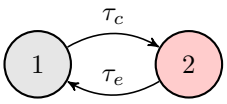

Fig. 1: Two-state model defects undergo transitions between a neutral state "1" and a positively charged state "2" with an effective capture time τ_c and effective emission time τ_e. These defect-specific times sensitively depend on the gate voltage and temperature. The probability $w(t)$ of being in state "2" satisfies a first-order differential equation with time-dependent coefficients.

Notice that the matrices $P(t_2, t_1)$ and $P(t_4, t_3)$ in general do not commute. This reflects the particular nature of the NBTI recovery, where the full information about the stress pattern sequence (beyond simple stress histograms) is important to correctly predict the degradation.

The BTI-induced mean (in the sense of averaging about stochastic processes) threshold voltage shift

$$\Delta V_{\rm th}(t) = \sum_{\rm defects\, j} \eta_j \times w_j(t) \tag{7}$$

results from the contribution of all defects j, which is summed with the defect-specific step height η_j as a weighting factor. This method calculates the degradation and the NBTI variability after an arbitrarily large stress time with little numerical effort.

III. Hierarchic-periodicities stress

In many cases, complex digital or analog circuits generate complex gate-source stress voltages at the transistor level. Such stress patterns are composed of various blocks corresponding to different circuit operation states, protocol modes or input conditions. These blocks repeat with complex hierarchical periodicities. The present model is able to accurately calculate the BTI degradation (including BTI variability) resulting from such stress patterns. We demonstrate our method on the simplest non-trivial pattern. More complicated stress patterns (analog voltages, more pattern blocks, more hierarchy levels, dynamic voltage/frequency scaling) can be easily treated with the present methodology.

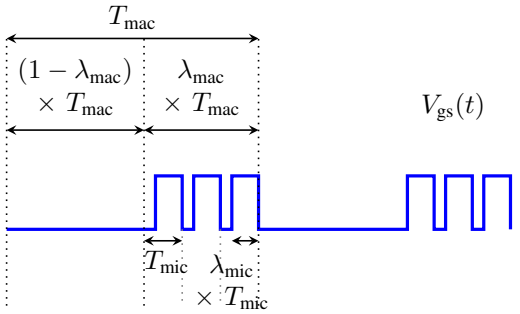

Fig. 3: Stress voltage pattern with two hierarchic periodicities: a digital AC pattern (period $T_{\rm mic}$, duty cycle $\lambda_{\rm mic}$) is periodically switched on/off with period $T_{\rm mac}$ and duty cycle $\lambda_{\rm mac}$. The phases of this stress signal are chosen such that the maximum degradation $\Delta V_{\rm th}$ occurs at the end of each $T_{\rm mic}$ stress period (and not at any other time within one period). In this study, we fix $T_{\rm mic} = 100$ns and $T_{\rm mac} = 10$h. *We use two duty cycle scenarios A, B (see main text), both have the same effective duty cycle* $\lambda_{\rm eff} := \lambda_{\rm mic} \times \lambda_{\rm mac}$ *but lead to very different aging.*

The $V_{\rm gs}(t)$ pattern of Fig. 3 results from a FET exposed to standard digital AC stress (period $T_{\rm mic}$ =100ns, duty cycle $\lambda_{\rm mic}$). Furthermore, the circuit is periodically switched on/off with period $T_{\rm mac}$ =10h and duty cycle $\lambda_{\rm mac}$. In this example, we associate the microscopic periodicity with a pattern inherent to the circuit operation, whereas the macroscopic switching mimics a user interaction. The circuit designer will be interested in the maximum $\Delta V_{\rm th}$ occurring within each stress period. Therefore, the present stress signal was chosen to start with a recovery interval followed by a stress interval, such that the largest $\Delta V_{\rm th}$ occurs at the end of each $T_{\rm mic}$ period.

One might expect that an effective duty cycle $\lambda_{\rm eff} := \lambda_{\rm mic} \times \lambda_{\rm mac}$ sufficiently characterizes this BTI stress pattern. However, we find that *two stress scenarios with equal* $\lambda_{\rm eff}$*, namely*

(A) $\lambda_{\rm mic} = 0.99$, $\lambda_{\rm mac} = 0.50$ and
(B) $\lambda_{\rm mic} = 0.50$, $\lambda_{\rm mac} = 0.99$,

lead to very different NBTI degradation: Fig. 4 shows the normalized mean $\Delta V_{\rm th}$ after 100 $T_{\rm mac}$ periods for a 22nm pFET. Notice that

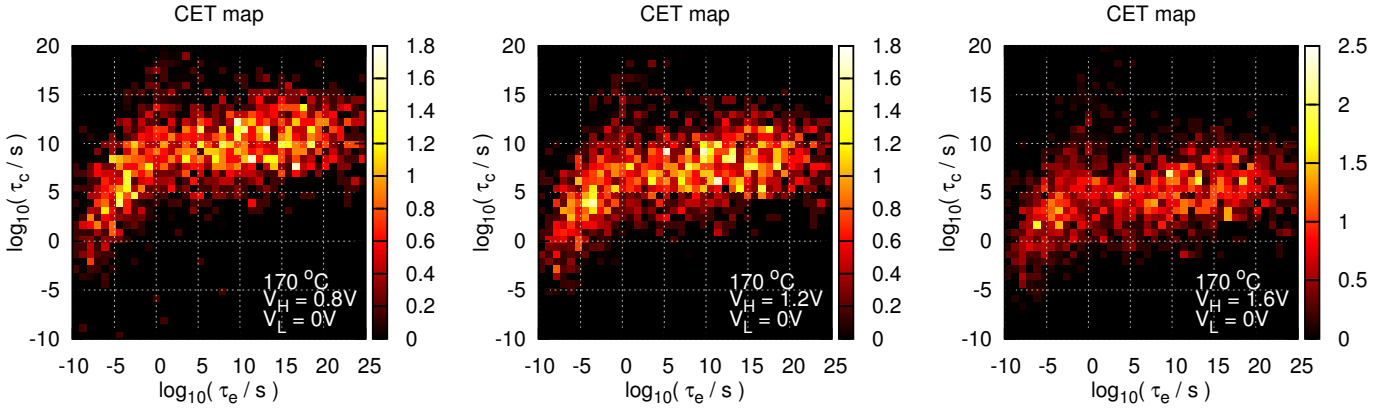

Fig. 2: Our approach uses multi-state defects with statistically distributed properties. We illustrate the present 22nm defect dataset [14] by three capture-emission-time maps relevant for digital-circuit studies. Our approach is not limited to digital applications, though.

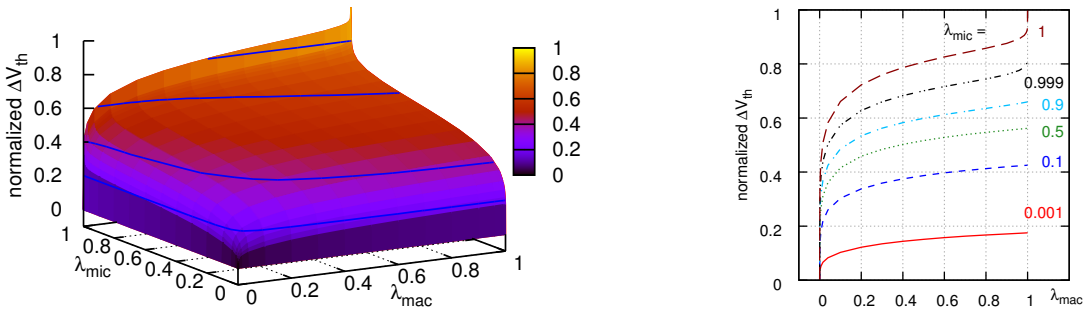

Fig. 4: ***Left:*** The stress pattern of Fig. 3 with multiple periodicities causes a non-trivial dependence of the NBTI degradation on the duty cycles λ_{mic}, λ_{mac}. It cannot be described with just one "effective" duty cycle $\lambda_{\text{eff}} = \lambda_{\text{mic}} \times \lambda_{\text{mac}}$. Instead, ΔV_{th} shows a sharp peak near $\lambda_{\text{mic}} = \lambda_{\text{mac}} = 1$. Apart from that, ΔV_{th} levels off, without a large slope, at $\lambda_{\text{mac}} = 1$. ***Right:*** Sections of the left plot: *only* $\lambda_{\text{mic}} = 1$ *features the well-known "s-shape" duty cycle dependence.* The degradation data results from 100 T_{mac} periods and is normalized to $\Delta V_{\text{th}}(\lambda_{\text{mic}} = \lambda_{\text{mac}} = 1) \approx 86\text{mV}$.

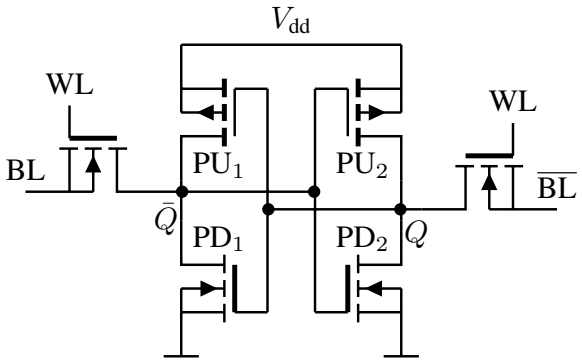

Fig. 5: 6T-SRAM schematic. We study the BTI degradation of the four pull-up and pull-down FETs.

(a) the limiting cases $\lambda_{\text{mic}} = 1$ or $\lambda_{\text{mac}} = 1$ lead to the well-known "s-shape" dependence [15],
(b) ΔV_{th} has a sharp peak at $\lambda_{\text{mic}} = \lambda_{\text{mac}} = 1$, and
(c) away from $\lambda_{\text{mic}} = 1$, the dependence on λ_{mac} is not s-shaped: instead, it levels off near $\lambda_{\text{mac}} = 1$.

Notice furthermore that if the description of this hierarchical-periodicities stress pattern in terms of λ_{eff} was sufficient, the NBTI ΔV_{th} contour lines (blue lines in Fig. 4, left) would be simple hyperbolas $\lambda_{\text{mic}} = \lambda_{\text{eff}}/\lambda_{\text{mac}}$, which in particular is not true for larger λ_{mic}.

Technically, the application of many BTI compact models to stress voltages with complex periodicities is numerically highly challenging. In the present scheme, the matrix $P(t_1, t_0)$ mediates the solution of the two-state-model differential equation (1), and it satisfies the "composition property" $P(t_2, t_0) = P(t_2, t_1)P(t_1, t_0)$. The resulting simplification $P(nT_{\text{mac}}, 0) = [P_{\text{dAC}}P_{\text{off}}]^n$ permits the efficient (and exact) solution of the differential equation for hierarchic-periodicities stress.

IV. Application to SRAM

We apply the present method to the analysis of a 6T-SRAM cell (Fig. 5) in a 22nm predictive technology model [16] plus the corresponding MoRV NBTI defect characterization [14]. The FETs are 25nm long and 80nm (PU), 50nm (PG), 60nm (PD) wide. Exposing the cell to the bit pattern $Q(t)$ of Fig. 3 generates a BTI drift of both the pull-up and pull-down FETs, and results in a reduction of the cell's read

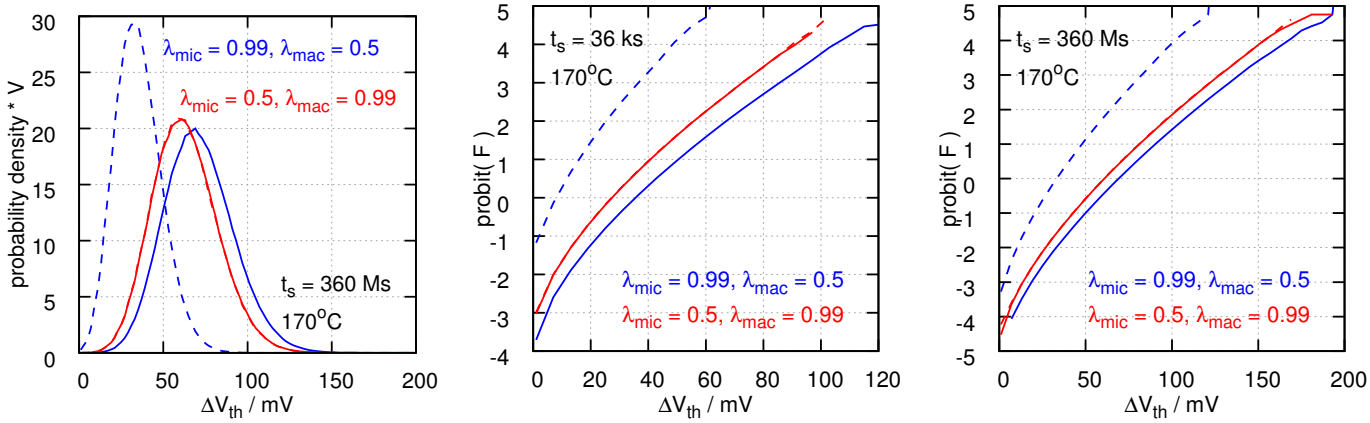

Fig. 6: NBTI degradation of the SRAM pull-ups under the bit pattern of Fig. 3. ***Left:*** ΔV_{th} probability density after 10^4 T_{mac} periods. ***Right (two plots):*** ΔV_{th} cumulative probability F after 1 and 10^4 T_{mac} periods. The PU_1 (dashed line) and PU_2 (solid line) degrade differently for $\lambda_{\text{mic}} = 0.99$, $\lambda_{\text{mac}} = 0.5$ (blue), whereas they age similarly for $\lambda_{\text{mic}} = 0.5$, $\lambda_{\text{mac}} = 0.99$ (red). In fact, the two red curves are practically indistinguishable in each of three the plots. The plots on the left and on the right contain the same information.

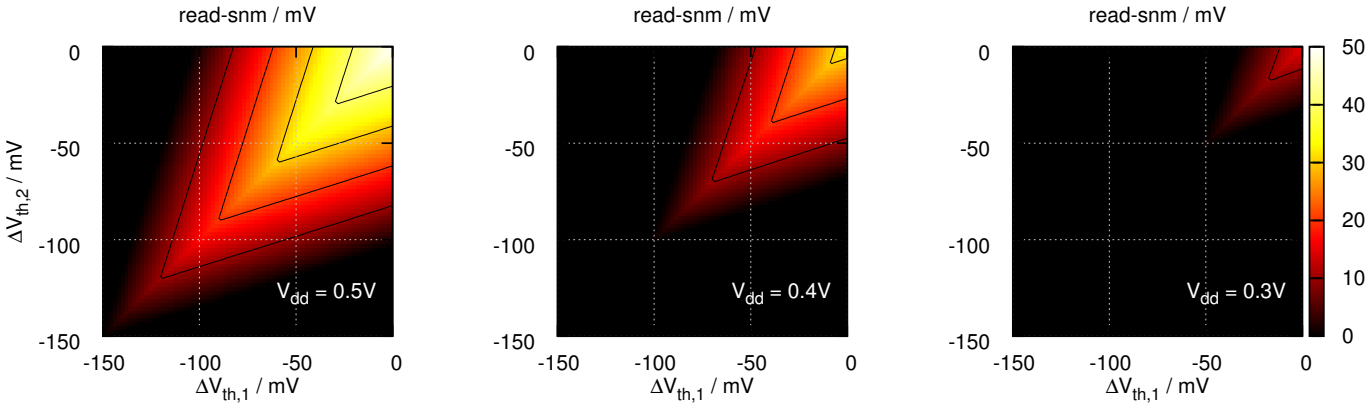

Fig. 7: The SRAM read-snm as a function of the pull-up FETs' shifts $\Delta V_{\mathrm{th},1}$ and $\Delta V_{\mathrm{th},2}$, at decreasing read-phase power supplies V_{dd} (left to right).

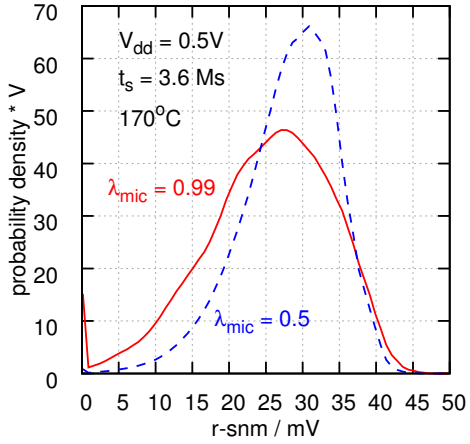

Fig. 8: SRAM read-snm probability distributions after 100 T_{mac} cycles. The Fig.-3 stress scenarios A (solid line) vs. B (dashed line) generate a vastly different SRAM aging, despite coinciding λ_{eff}.

static noise margin (rsnm, [17]). To be specific, the bit state $Q = V_{\mathrm{gs}}^{\mathrm{PD1}}$ corresponds to the gate-source voltage of PD1 and takes the values $V_{\mathrm{h}} = V_{\mathrm{dd}}$ or $V_{\mathrm{l}} = 0$. As a result, $Q = V_{\mathrm{gs}}^{\mathrm{PD1}} = -V_{\mathrm{gs}}^{\mathrm{PU2}}$ and $\bar{Q} = V_{\mathrm{dd}} - Q = V_{\mathrm{gs}}^{\mathrm{PD2}} = -V_{\mathrm{gs}}^{\mathrm{PU1}}$. We choose $V_{\mathrm{dd}} = 2V_{\mathrm{dd,nom}}$ to be twice the nominal V_{dd} and a temperature of 170°C, such that high BTI stress is generated.

Since currently no PBTI two-state-model defect sampling is available, we use the modified NBTI data (with step heights multiplied by $-1/2$) as an estimate in the present demonstration.

Using our modeling in combination with a Monte Carlo approach (10^6 FET samples), we calculate the pull-up FETs' distributions of the threshold voltage shift resulting from NBTI variability, see Fig. 6. Whereas for scenario B (Sec. III) both SRAM pull-ups see the same stress and age equally (red curves), scenario A leads to a strongly asymmetric degradation of these two FETs (blue curve). This qualitative difference has immediate consequences on the SRAM stability and originates from two facts: on the one hand, PU_1 is exposed to quite different NBTI stress in the two scenarios (this is an effect of really switching the circuit on/off on the macroscopic scale). On the other hand, PU_2 ages differently in both setups because of the $\lambda_{\mathrm{mic}} - \lambda_{\mathrm{mac}}$ asymmetry discussed in the previous section (notice the difference in the two solid lines in the Fig.-6 plots).

Via a Spice circuit simulation, we translate the ΔV_{th} distributions into distributions for the cell's read static noise margin. Fig. 7 shows the rsnm as a function of the pull-up ΔV_{th}s for several inverter power supplies V_{dd}. We thus obtain for the

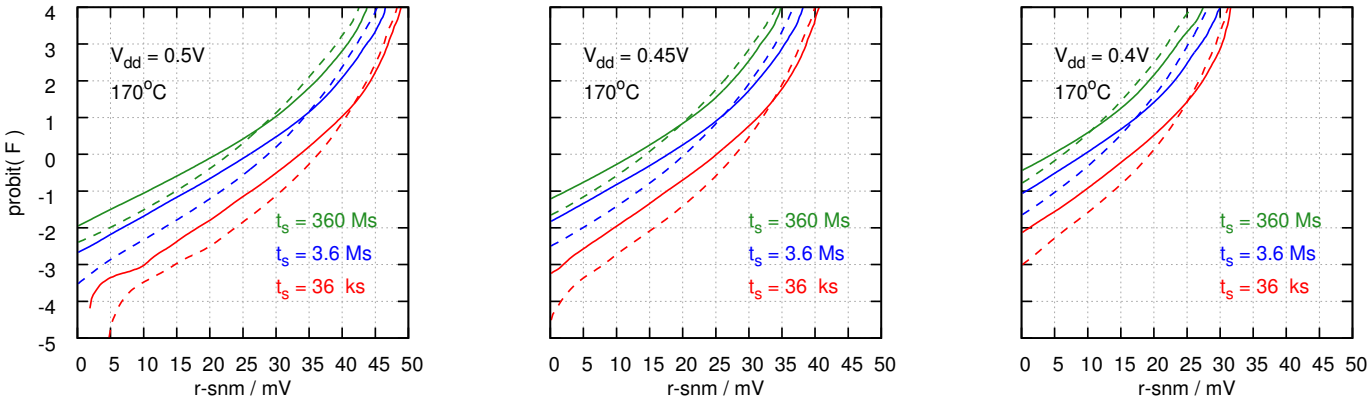

Fig. 9: Read-snm cumulative probability F for different read-V_{dd} (left to right) and for increasing number of stress periods in the Fig.-3 pattern (bottom-up). Stress patterns with similar effective duty cycle show a different behavior (solid line: $\lambda_{\mathrm{mic}} = 0.99$, $\lambda_{\mathrm{mac}} = 0.5$ vs. dashed line: $\lambda_{\mathrm{mic}} = 0.5$, $\lambda_{\mathrm{mac}} = 0.99$). In particular, there are substantial deviations in the small-snm tail and hence in the cell failures.

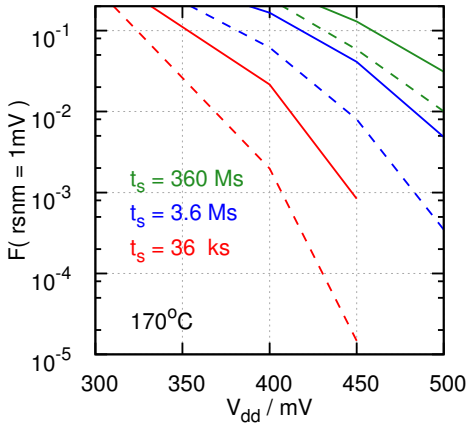

Fig. 10: Small-rsnm distribution tail for various t_s and V_{dd} (conventions: Fig. 9). The probability F(1mV) of failing devices at 1mV SRAM noise can differ by a factor of $10 \ldots 100$ between the Fig.-3 scenarios A (solid), B (dashed).

hierarchical-periods stress the rsnm distributions of Figs. 8 and 9, for several combinations of the power supply V_{dd} (during rsnm testing) and of the stress time t_s. As expected from Fig. 6, the two scenarios A (solid lines) vs. B (dashed lines) result in very different rsnm distributions. In particular, *there are substantial deviations in the small-rsnm tail and hence in the device failures.* For instance, after 36ks stress and at V_{dd} =0.45V plus 1mV circuit noise (Fig. 10), 0.1% of the SRAM cells fail in scenario A (asymmetric aging) as opposed to 0.001% failures in scenario B (symmetric aging).

V. Conclusions

The present BTI study demonstrates how to exactly treat complex realistic stress patterns within a physically validated compact model. Due to the particular nature of BTI recovery, conventional stress histogram approaches (e.g. based on λ_{eff} in the digital case) lack important periodicity information to correctly predict the BTI degradation of a pFET under hierarchical-periods stress. Instead, an accurate simulation requires to take into account further information about the hierarchical periodicities (period durations, duty cycles, block sequence). The predicted aging deviations in the given SRAM example emphasize the relevance of the presented modeling.

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