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Design of a Time Gain Compensation Amplifier for an Ultrasound Analog Receiver Front End Using 0.18 µm SOI Process

Master's Thesis

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Abstract

The work presents a time gain compensation amplifier as a part of ultrasound analog front-end circuit. The circuit compensates the attenuation which is experienced by the ultrasound echoes while traveling. The simulations have been done both for pre- and post-layout. The circuit is designed to interface 10 pF CMUT and to drive 5 pF capacitive load. The circuit provides 106 dB gain for the weakest echoes and linear-in-dB 30 dB gain range with analog control. The noise at the maximum and minimum gain is 4.505 pA/$\sqrt{Hz}$ and 99.96 pA/$\sqrt{Hz}$, respectively. The complete circuit consumes 5.35 mW and a total area of 0.03 mm^2 (210 μm $\times$ 141 μm). The project is realized using 0.18 μm Silicon on Insulator (SOI) process technology from X-FAB. The simulation is done using Spectre in the Cadence Virtuoso with BSIM4v4.70 as the transistor model.

Keywords: Ultraound, Analog Front-End, Time Gain Compensation, Linear-in-dB, Transimpedance Amplifier

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List of Abbreviations

ADC Analog-to-Digital Converter

AFE Analog Front-End

BSIM Berkeley Short-channel IGFET Model

CMOS Complementary Metal-Oxide-Semiconductor

CMUT Capacitive Micromachined Ultrasonic Transducer

EVG Exponential Voltage Generator

NMOS N-type Metal-Oxide-Semiconductor field-effect transistor

OTA Operational transconductance amplifier

TGC Time-Gain Compensation

PMOS P-type Metal-Oxide-Semiconductor field-effect transistor

TIA Transimpedance Amplifier

VGA Variable Gain Amplifier

1. Introduction

1.1. Ultrasound Systems

The ultrasound systems are still an on going development and used in many application like research [1], [2], clinical [3], and nondestructive testing [4]. Depending on the applications, the implementation of the systems varies. There are systems built from off-the-shelf commercial components[4], open-platforms (OP) [1], as well as monolithic integrated circuits [3].

From the physical size of the system, ultrasound systems can be categorized into three types, i.e., the traditional cart-based [1], handheld [5] [6], and microprobe [7] [3] [8] [9]. In general, all types of system consist of the same functional blocks although the implementation platforms and specifications could be different. The traditional static ultrasound systems send the analog signals from each transducer to the processing unit hardware. This means that the connection requires multiple cables as much as the number of transducer. The handheld ultrasound systems do all signal processing in the handheld probe and send the signal to an external PC for only imaging purpose. While the traditional static ultrasound systems are limited by its application, the handheld systems are limited by power consumption and size. Communication with the PC can be done wirelessly via Wi-Fi. The trend even goes further to have the probe in micro scale size. In this kind of systems, the power dissipation is very limited because we do not want to burn the tissue which is being scanned. The issues and challenges in AFE design for ultrasound are well discussed in [5] [10] and will not be repeated here unless necessary.

The result of the ultrasound system in general is either a 2D image which maps the acoustic impedance mismatch spatially [11] or time-of-flight data. In order to construct this image, the systems will transmit an ultrasound pulse into the target. If along the way of travel, the pulse experiences impedance mismatch at the interface between two materials, some of energy of the pulse will be reflected. This reflected pulse is called echo. If we can obtain information about the speed of sound in that

material, we can calculate the distance between the transducer and the location of impedance mismatch by measuring the time required from transmitting until an echo is received. Along the travel, the echo experiences attenuation because some of its energy is transfered to the matter it passes through. While the time measurement shows us the location of the impedance mismatch, the amplitude of the received echo informs us about the degree of the impedance mismatch. Higher impedance mismatch produces higher reflection and vice versa. One might wonder how the system could recognize a high impedance mismatch located far from the receiver from a low impedance mismatch located near. In one transducer system, this is solved by limiting the receive phase duration, so the system knows the probing range before hand. However, it assumes that the speed of ultrasound in that medium is known as well. In a more advanced system using 1D and 2D array of transducers, the system decides the focusing point even before firing. So it is more obvious in these kind of systems.

The ultrasound systems works in pulse-echo mode. It is described in Figure 1.1. It transmits an ultrasound pulse as the probing signal in transmitting phase. After that, it receives the echoes in receive phase. The systems actually want to measure the location of sound impedance mismatch and how much different is this mismatch. The location of sound impedance mismatch can be calculated from the time required by the ultrasound wave from the start of transmitting the pulse until the received echoes are detected. This is shown in equation (1.1). The sound impedance mismatch difference is measured by measuring the amplitude of the echoes. This amplitude inform us about the energy of reflected wave. This is shown in equation (1.2).

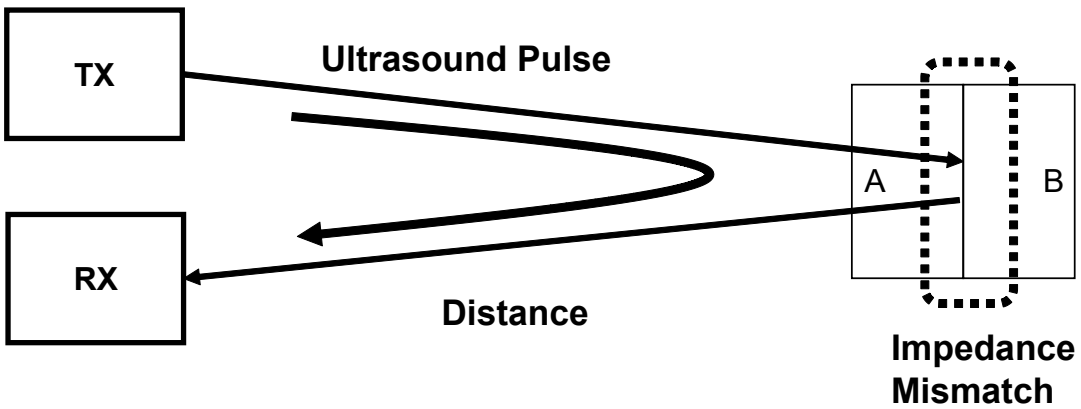


Figure 1.1.: Illustration of the pulse-echo mode of ultrasound systems.

$$d = \frac{1}{2}vt \tag{1.1}$$

$$R = \frac{z_2^2 - z_1^2}{z_2^2 + z_1^2} \tag{1.2}$$

Both distance and reflection ratio can be measured by a system that has only one transducer. However, to form an image, both information must be gathered from many points on the image field of interest. This is done usually by using an array of transducers. e.g., linear array or 2D array, and beamforming techniques to direct the probing wave.

For all of the types mentioned above, the functional building block are almost the same. In the transmit path, there are high voltage pulser circuits which actuate the transducers to produce ultrasound signals. In the receive path, the backscattered signals are sensed by the transducers and it will go through an Low Noise Amplifier (LNA), Time Gain Compensation (TGC), beamformer circuit, and Analog to Digital Converter (ADC). In the systems with thousands of transducer, subarray beamformer is required. LNA is used to convert the current information from the transducer into voltage. This part is implemented as a Transimpedance Amplifier (TIA). Echo signals that come from the deeper scanned region are attenuated. The attenuation is around 1dB/cm/MHz in human body [12]. TGC is needed to compensate this attenuation. In order to get rid of connection issue in applications with high number of transducers [13], beamforming technique is needed.

For the sake of completeness, clarity, and showing what have been done, it would be fair to mention that ultrasound system without TGC feature does exist [14]. It just means that the whole analog front end must deal with the full dynamics range of the information signal before it quantized by the ADC. It also means that in cases where TGC is not implemented in the very first stage of circuit chains, the preceding circuits need to deal with the full dynamic range.

The main focus of this master thesis is to realize the TIA with TGC feature using 0.18 μm Silicon on Insulator (SOI) process technology from X-FAB. The simulation is done using Spectre in the Cadence Virtuoso with BSIM4v4.70 as the transistor model. The specifications are listed in Table 1.1.

This report is structured as following:

- Chapter 2: The basic theoretical information regarding the circuits used in the final design. Some topologies to realize each block are also discussed in this

Parameter	Unit	Target
Gain Range	dB	≥ 30
Maximum Gain	dB	≥ 106
Control Voltage Range	mV	-
3dB Bandwidth	MHz	≥ 5
Input-referred Noise Current at 5 MHz	pA/$\sqrt{Hz}$	≤ 5
Transducer Capacitance	pF	10
Load Capacitance	pF	5
Power Consumption	mW	≤ 6
Area	μm^2	-

Table 1.1.: Target specification of the TIA with TGC feature using 0.18 μm Silicon on Insulator (SOI) process technology from X-FAB.

chapter.

- Chapter 3: In this chapter, the reasoning of design decision is outlined, from block diagram to the topology of each block. At the transistor level, the size of each transistor are also summarized. The simulation results are also discussed here.
- Chapter 4: The top level simulation is discussed in this chapter.
- Chapter 5: Conclusion. It will contain the conclusion for the main tasks on this work.

2. Circuit Description

This chapter discusses the fundamental understanding of each circuit block. The advantages and disadvantages of possible topologies are reviewed. The required formulas to benchmark the circuit are also stated here.

2.1. Noise Consideration

Linear two-port network can be characterized by using a matrix whose elements are a set of parameters. One of the parameter sets used here is ABCD parameters. There are several other parameter sets, e.g., impedance (z), admittance (y), hybrid (h), and scattering (s). The decision to use one rather than the other is solely based on the convenience, i.e., analyzing a particular circuit is easier if a certain parameter is used. However, all parameter sets are equivalent to each other. Each element in ABCD parameters are the ratios of voltage or current of port 1 with respect to those of port 2. A good summary can be found here [15].

Using the ABCD Parameters in the way like it is explained in [16] and the Lemma from [17], all the device's noise source can be easily translated to any point in the circuit. It is usually easier to translate it to either output or input point and use the transfer function to translate back or forward. Understanding the ABCD parameter is important to have a complete noise representative.

It is understood that the input-referred noise can be represented completely by a current source and voltage source. However, depending on the circuits and it does make sense to do so, it is enough to use only one source, either current source or voltage source to represent noise source in order to simplify the hand-calculation.

$$\begin{pmatrix} v_i \\ i_i \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_o \\ i_o \end{pmatrix} \tag{2.1}$$

Referring to a common-source configuration, the following transformation can be derived. The detail equation are shown in Table 2.1. Those equations can be used to

Parameter	Definition	Value
A	$\left.\frac{v_{in}}{v_{out}}\right\|_{i_{out}=0}$	$-\frac{s(c_{db}+c_{gd})r_o+1}{r_o(sc_{gd}-g_m)}$
B	$\left.\frac{v_{in}}{i_{out}}\right\|_{v_{out}=0}$	$-\frac{1}{g_m}$
C	$\left.\frac{i_{in}}{v_{out}}\right\|_{i_{out}=0}$	$-\frac{s(c_{gd}+c_{gs})}{g_m r_o}$
D	$\left.\frac{i_{in}}{v_{out}}\right\|_{v_{out}=0}$	$-\frac{s(c_{gd}+c_{gs})}{g_m}$

Table 2.1.: The table contains the equations for ABCD parameters used to translate the noise source to either output or input point.

each MOSFET in more complex circuits.

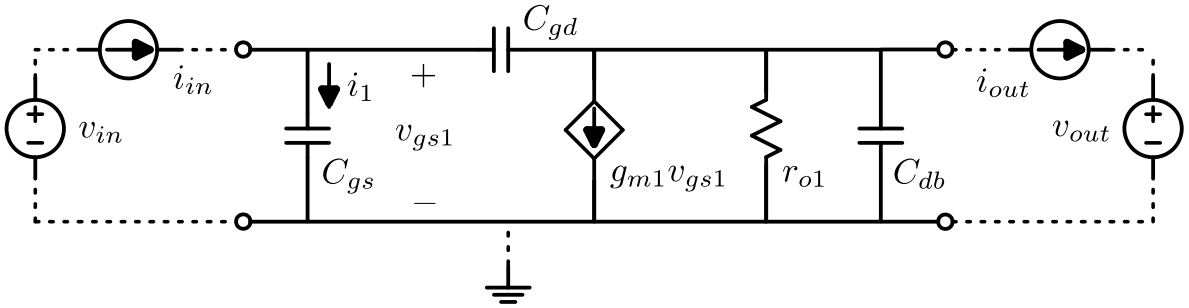


Figure 2.1.: Common source small-signal equivalent circuit used as the reference to derive the equations of ABCD parameters. Small-signal voltage and current sources must be close or open depending on the parameters' definitions.

2.2. g_m/I_D Method

This method is a powerful tool to help us in design process. By using this method, device performance parameters, e.g., transconductance g_m, small signal output resistance r_{out}, and transit frequency f_T, can be used directly to predict circuit performance parameters. It can be used directly because those device performance parameters show up in the analytic equations of the circuit performance parameter. In order to use this method, we need to characterize our devices to extract the device parameter

and plot them with respect to the transconductance efficiency g_m/I_D. At the end, in addition of defining bias current, we need to define the size of the transistors by linking g_m/I_D and I_D/W. We can also see the benefit of this method from the perspective of inversion level because g_m/I_D is linked directly with the inversion level, just like the overdrive voltage, V_{OV}, does. From [18], the range values for g_m/I_D which corresponds with the inversion level is described. Figure 2.2 shows the g_m/I_D of NMOS with respect to V_{GS} for the process technology used in this work.

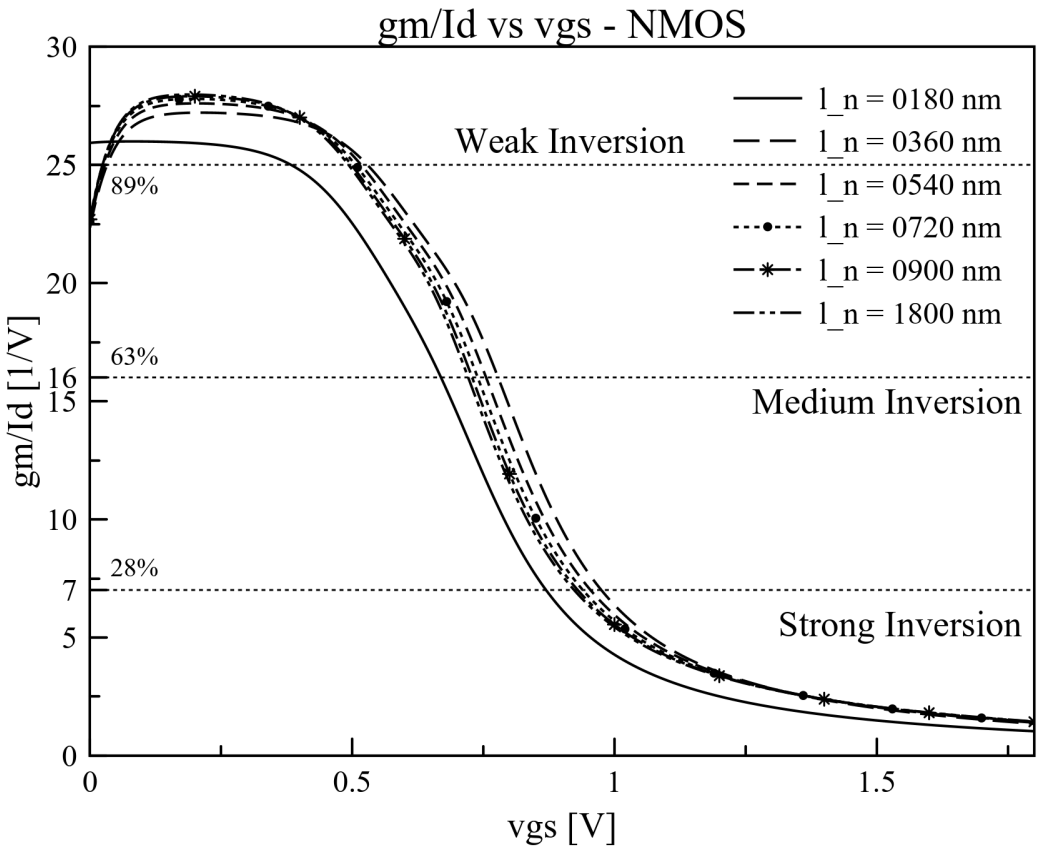
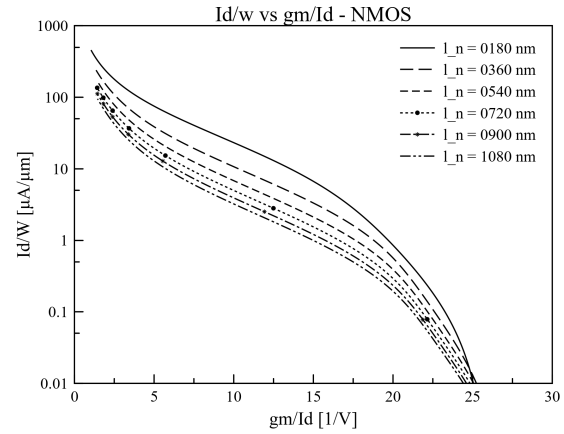
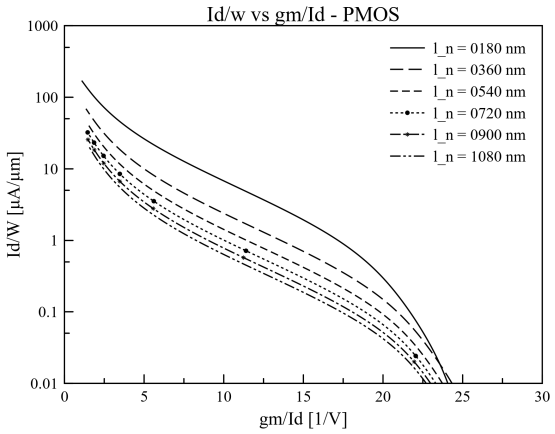


Figure 2.2.: The graph shows the g_m/I_D of NMOS with respect to V_{GS}. The g_m/I_D values corresponds with the inversion levels are also marked on the graph.

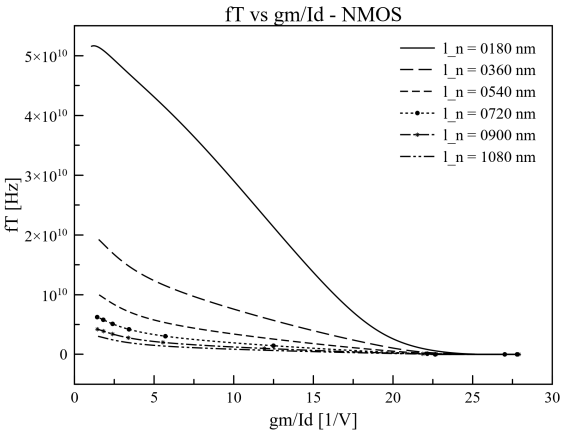
As already suggested in [19], it is a must to have the analytical formulae handy. Indeed, without this g_m/I_D method, we can still see the trend of the circuit performance. But we cannot grasp how the nonlinear nature of the device's behavior affecting our circuit performance. By using this method, we can map the device performance parameters to the circuit performance parameters by plugging them in to the analytical formulae. It must be kept in mind though, that the mapping results are just as accurate



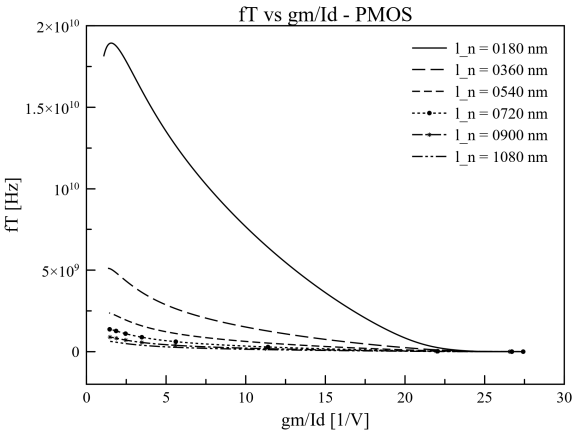
(a) I_D/W vs g_m/I_D - NMOS



(c) I_D/W vs g_m/I_D - PMOS



(b) f_T vs g_m/I_D - NMOS



(d) f_T vs g_m/I_D - PMOS

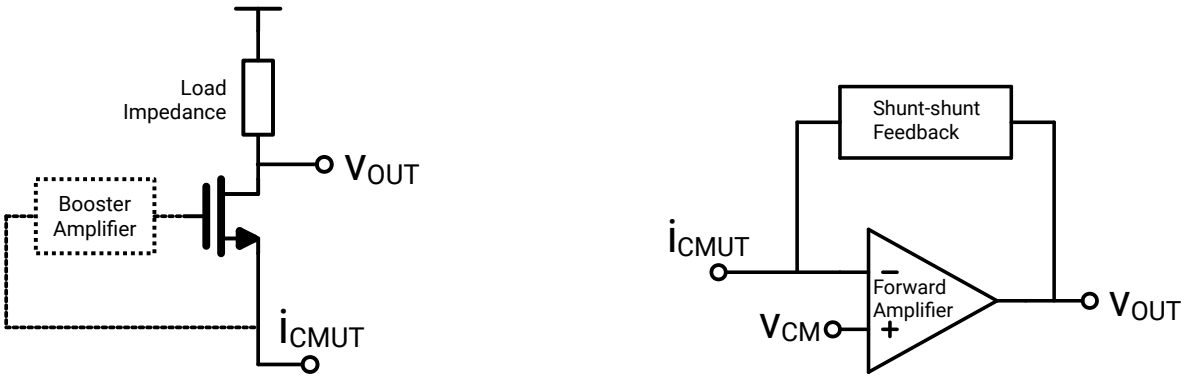
Figure 2.3.: The graph show I_D/W vs g_m/I_D and f_T vs g_m/I_D for both NMOS and PMOS. These plots are used during the design to determine the size of the transistors.

as the analytical formulae's accuracies.

In a certain occasion, some analytical equations need to be rehashed in order to use this method. The rehashing is done with the aim to have the term g_m/I_D or other parameters that are directly linked with this method, e.g., the current density, I_D/W, in the equation. After rehashing, the the values for g_m/I_D and other values can be plugged in to the equations and the theoretical upper or lower bound of a certain circuit parameter can be found. Figure 2.3 shows the plots, i.e., I_D/W vs g_m/I_D and f_T vs g_m/I_D for both NMOS and PMOS, that frequently used in this work.

2.3. Transimpedance Amplifier

Transimpedance amplifier is needed because CMUTs have high output impedance. So, we need an amplifier that has low input impedance in order to allow as much current as possible to flow to the circuit. Transimpedance amplifier can be categorized into two types of circuits [20], [21] . First, the topologies whose input terminal is the low impedance terminal of the input device, e.g., common gate topology and its variant [22] . This will provide approximately an input impedance of $1/g_m$ multiplied by the total input capacitance. This first type of topology usually consists of small number of transistors. So, they can be very small and consume low power. One of the disadvantages are the difficulty in optimizing the device to fulfill the specification. For example, the noise requirement is very important to this type amplifier because it acts as an LNA located at the very front end of the circuits. Due to its tuning limitation, it could be hard to obtain low noise performance even though we are willing to sacrifice other circuit performance parameter, e.g., power. This does not mean that their noise performance are bad though, it is just that they have limited tuning capabilities.



(a) TIA based on common-gate topology

(b) TIA based on shunt-shunt feedback topology

Figure 2.4.: The picture shows two possible general structures of transimpedance amplifier.

The second type is the topologies that utilize shunt-shunt feedback, i.e., voltage sampling-current mixing. As explain in [23], any linear functionality are possible if we have high enough forward gain and a correct passive circuit as a feedback. This concept is also mentioned here [24], [25]. So this kind topology can be considered transimpedance amplifier despite of its high input impedance originating from the forward amplifier. This kind of circuit have high input impedance which is then

lowered due to feedback. Simple five transistor OTA with resistor feedback is one example of this topology [14]. There is also an implementation that use common source configuration as a forward amplifier [26]. Despite of their advantages and disadvantages, both types of topologies have been implemented in ultrasound application [22], [26], [3], [13] . Figure 2.4 shows the general structure of these topologies.

2.3.1. Circuit Parameters

Before we go into the detail, it would be nice to introduce the circuit parameters here. Most of them are similar with ones from the voltage amplifier. So, the same understanding or concepts which are discussed in standard text book are still valid.

Transimpedance Gain This is defined as the ratio of the small signal output voltage with respect to the small signal input current calculated at low frequency. This is just the same as small signal gain of voltage amplifier. Because it is a small signal ratio, the circuit is linearized and the input is small enough such that the circuit still behave linearly.

$$Z_T = \frac{v_{out}}{i_{in}} \tag{2.2}$$

Frequency Response This is an extention from the concept of transimpedance gain. The frequency response is a collection of transimpedance gain from DC to high frequency. In addition to that, there is also phase to describe how the output can follow the changing input.

$$Z_T(f) = \frac{V_{out}}{I_{in}} \tag{2.3}$$

3dB Bandwidth 3dB Bandwidth is defined as the frequency at which the power at the output becomes half of that of the input. This frequency is marked when the transimpedance gain fall 3dB from the value in the low band. The 3dB bandwidth can be roughly estimated by the inverse of total time constant. So the output and input capacitance, i.e., the load capacitance and the capacitance of the CMUT, take part in defining the 3dB bandwidth. This is the reason that CMUT capacitance must be included in the amplifier's specification. By including this value, comparison among transimpedance circuits becomes fair and valid.

Input-referred Noise Current Input-referred noise current [1] is defined as the measurable noise voltage spectrum at the output divided by the transimpedance gain. Obviously, it is defined at a certain frequency. This value is very important because it defines the capability of of the circuit to read the weakest signal generated by the CMUT. One can see that this definition is not complete because to describe noise completely, there must be a current source and a voltage source connected at the input. But, since the input impedance of the circuit is low, the value of input-referred noise current dominates. The value of CMUT capacitance affects input-referred noise current as well. This is clearly seen when deriving the noise equation in which the denominator is the frequency response whose denominator is composed of poles. The CMUT capacitance defines the poles at the input node. The higher the capacitance, the higher the noise.

2.3.2. Common Gate

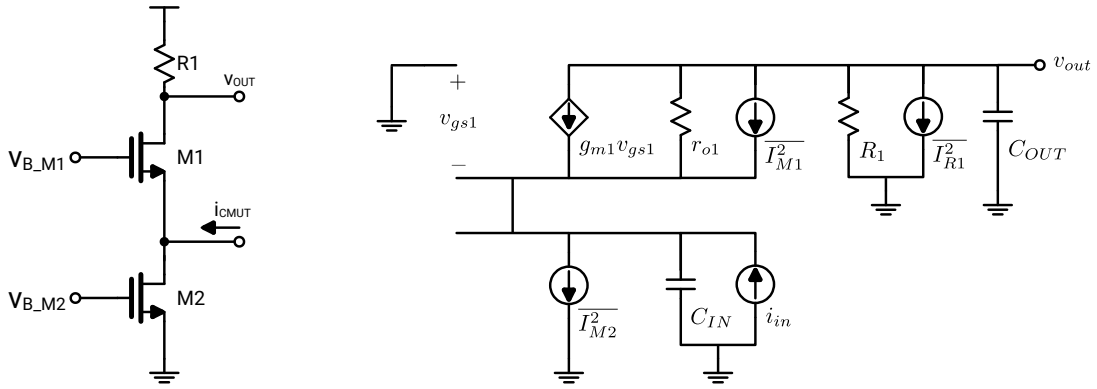
From the CMOS Transimpedance survey in [22], it is shown that the regulated cascode has the best noise performance than the other seven topologies. In that review, the specification is quite similar with the specification in this work. In order to easily understand the improvement of this topology, common gate topology is discussed first.

Figure 2.5 shows the common gate topology and its small signal equivalent circuit. The analytical formula for input-referred noise current, transimpedance gain, and input impedance are shown on equation (2.4), equation (2.5), and equation (2.6), respectively.

$$\begin{aligned}\overline{I_{n,in}^2} = 4k_BT\Bigg[&\frac{(2\pi f C_{IN} r_{o1})^2 + (g_{m1} r_{o1})^2 + 1}{(1 + g_{m1} r_{o1})^2}\frac{1}{R_1} \\ &+ g_{m2}\gamma_n \\ &+ \frac{(2\pi f C_{IN} r_{o1})^2}{(1 + g_{m1} r_{o1})^2} g_{m1}\gamma_n\Bigg]\end{aligned} \tag{2.4}$$

$$\frac{v_{out}}{i_{in}} \approx \frac{(1 + g_{m1} r_{o1})\, R_1}{(sC_{OUT}R_1 + 1)\left[sC_{IN}(r_{o1} + R_1) + g_{m1} r_{o1} + 1\right]} \tag{2.5}$$

[1] Input-referred noise current is used to refer to input-referred noise current spectral density with unit A/$\sqrt{Hz}$ in this report. The same convention when referring to input-referred noise voltage spectral density in which the unit V/$\sqrt{Hz}$ is used.



(a) Common gate amplifier

(b) Common gate small signal equivalent circuit

Figure 2.5.: The common gate topology and its small signal equivalent circuit.

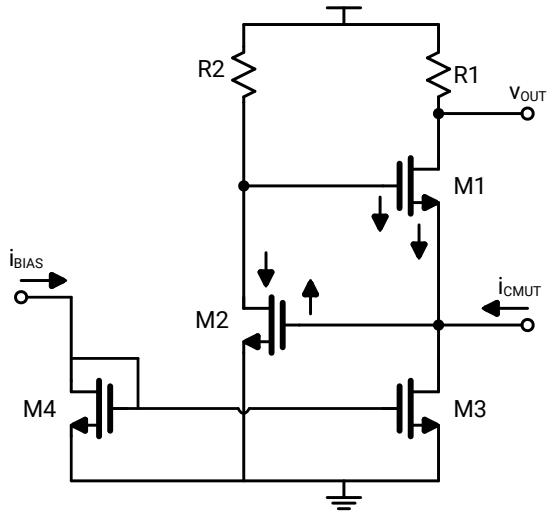
$$\frac{v_{in}}{i_{in}} \approx \frac{(sC_{OUT}R_1 + 1)\, r_{o1} + R_1}{(sC_{OUT}R_1 + 1)\left[sC_{IN}(r_{o1} + R_1) + g_{m1}r_{o1} + 1\right]} = Z_{in}(s) \tag{2.6}$$

From equation 2.4, we can see that if we want to optimize the noise, we can scale down the noise contribution from the resistor and transistor M1 by increasing g_m. However, higher g_m means higher current because we can only increase the size of the transistor to a certain extent before the device come into weak inversion region. By increasing the drain current of M1, which is equal to the drain current of M2, the g_m of M2 is increased as well. This is not wanted because it increases the noise contribution of M2 and this noise cannot be scaled. We are stuck with a very limited possibility to tune the noise of this circuit. This becomes the motivation of the next circuit, regulated cascode TIA.

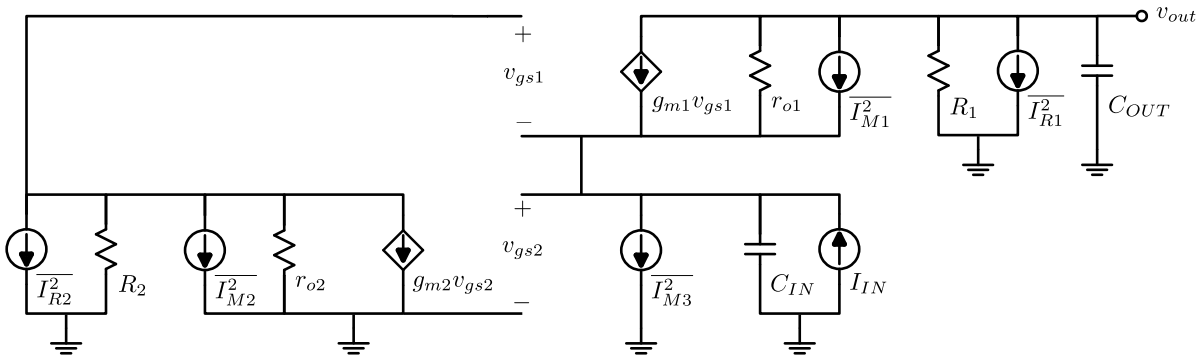
Depending on the application, the bandwidth can be limited by whether the input pole or the output pole. In this application, the pole at the output node is the dominant one. The output pole should be maximized by having a small load resistor and a small input capacitance of the cascaded circuit. However, having a small resistance at this node means reducing the gain. Putting optimization aside, the input pole tends not to be a problem since it can be shifted to a higher frequency by increasing the transconductance g_m of the transistor M1. But again, this option is very limited if we want to keep the device in strong inversion region.

2.3.3. Regulated Cascode

Due to the very limited possibility to tune the noise on common gate topology, the regulated cascode is introduced as an improvement from common gate topology discussed before. Figure 3.2 shows the schematic diagram of this topology and its small signal equivalent circuit.



(a) regulated cascode topology



(b) regulated cascode small signal equivalent circuit

Figure 2.6.: The picture shows the regulated cascode topology. It is an improvement from common gate topology.

$$\frac{v_{out}}{i_{in}} = \frac{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2))R_1}{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) + sC_{IN}(r_{o1} + R_1))(sC_{OUT}R_1 + 1)} \tag{2.7}$$

$$\omega_{p1} = \frac{g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) + g_{m1}r_{o1} + 1}{C_{IN}\,(r_{o1} + R_1)} \tag{2.8}$$

$$\omega_{p2} = \frac{1}{C_{OUT}R_1} \tag{2.9}$$

$$\begin{aligned}\overline{I_{n,in}^2} = 4k_BT\Bigg[&R_1\left|\frac{i_{in}}{v_{out}}\right|^2 + \gamma_n g_{m1}R_1^2\left|\frac{i_{in}}{v_{out}}\right|^2 + \gamma_n g_{m3} \\ &+(\frac{1}{R_2} + \gamma_n g_{m2})(R_2\|r_{o2})^2\left(g_{m1}R_1\right)^2\left|\frac{i_{in}}{v_{out}}\right|^2\Bigg]\end{aligned}$$

with

$$\left|\frac{i_{in}}{v_{out}}\right|^2 = \frac{[\omega^2(r_{o1}+R_1)C_{IN}R_1C_{OUT}]^2 + \omega^2((r_{o1}+R_1)^2C_{IN}^2 + C_{OUT}^2R_1^2A^2) + A^2}{A^2R_1^2} \tag{2.10}$$

and A is defined as

$$A = 1 + G_m r_{o1}$$

with G_m as

$$G_m = g_{m1} + g_{m1}g_{m2}(r_{o2}\|R_2)$$

$$\frac{v_{in}}{i_{in}} \approx \frac{(sC_{OUT}R_1+1)\,r_{o1} + R_1}{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}\|R_2) + sC_{IN}(r_{o1}+R_1))(sC_{OUT}R_1+1)} = Z_{in}(s) \tag{2.11}$$

The noise analysis of this circuit can be a continuation from the common gate. We just need to change the transfer function that scale the noise from common gate stage and its load resistor and add the common source stage transistor and its load resistor.

From the equation (2.10), it can be seen that we have more options to optimize the noise. The main idea is, of course, to minimize the noise contribution from the noise source that cannot be scaled down. In this circuit, same like in the common gate configuration, it is the biasing transistor. We need to minimize this noise to a fraction of our total noise budget. After that, to minimize the noise from other devices, we try to increase the g_m. This can be done by increasing the size and/or allowing more current. By using this strategy, g_m from the common source stage can be increased to scale down the input-refereed noise current.

If we plug in some relevant values into the noise equation, we can see that the noise contribution from the common source stage could be the dominant one. It could be ten times higher that other noise sources. This high noise is because the noise current of the device is scaled up by many factors, i.e., the input capacitance, the transconductance

g_m of M1, and load resistor of common source stage. All of this factors go in the same direction to maximize other circuit parameters like gain and bandwidth. An attempt to reduce this noise by increasing the effective transconductance G_m is not worth the effort because the total input-referred noise current comes under a square root. This leads to an insignificant reduction of total input-referred noise current for many applicable possible combinations of component values.

The similar case like in the common gate, nothing much can be done to increase the pole frequency at the output node. This really becomes the hard limit for the bandwidth, given a certain value of input capacitance of the next cascaded circuit and the gain which is expected to be of a high value. Such high gain is expected because the input-referred noise current of the whole circuit will be scaled down by this gain value.

On the other hand, the pole frequency at the input pole can be shifted quite easily. It is because the transconductance g_m of M1 is scaled up by the voltage gain of common source. The transconductance gain of this circuit is also increased by the effective transconductance G_m. Increasing R_2 leads to higher BW but it increases the input-referred noise current. From [22], regulated cascode TIA topology has the best performance in the specification range similar to the specification of the circuit in this work. The noise of this topology is the lowest among other seven topologies while targeting either minimum noise or minimum power.

2.4. Variable Gain Amplifier

From the discussion in the previous chapter, it is understood that compensating the attenuation means the gain needs to be adjusted. The first coming echo will experience the smallest gain and the last coming one within the receive phase will be amplified the most. In this discussion, the input impedance requirement and application fields are put aside for a while.

2.4.1. Gain Varying Methods

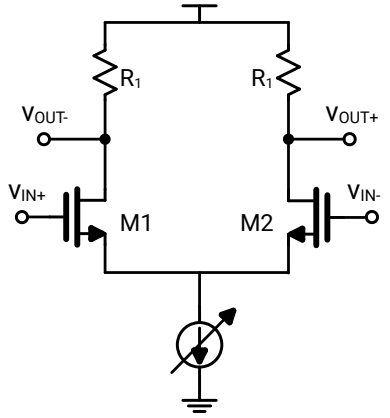
One way to change the gain is by changing the feedback impedance. It can be thought just like changing the resistor value of the feedback resistor as it is applied in circuits with discrete components. Digital switch can be used to cut off the electrical path and turn on another switch that connect the path with other impedance value.

Digital controller is needed for this type of topology. Some publications in ultrasound systems use this topology [27], [28]. However, the switching of digital switch may cause imaging artifacts [3]. This is the main disadvantage of this topology. Despite this limitation, the implementation of discretely varying gain for imaging system does exist [29].

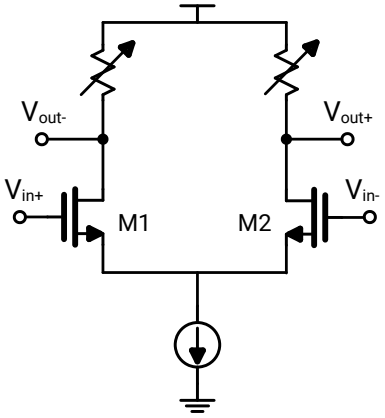
Other kind of gain control is by using an analog control signal to change the transconductance g_m of the biasing device [30], the resistance value of the MOSFETs that work as a resistor [31], [32], [33]. The drawback of varying impedance topology is it might need special biasing circuit to control the analog switch [31]. One topology that kind of work between these two main categories utilize an interpolation method [3]. It does change the path where the current flow to give a certain gain or at least a fraction of current goes to the path with certain impedance while the rest to other path with other impedance value. It is its own topology because it does not change the impedance value of the feedback component. The disadvantage of this topology is it requires an analog circuit to orchestrate the interpolation technique.

One important thing to consider is the bandwidth. For example in the inverting configuration of OPAMP circuit, assuming the system is single pole system, it easy to see that increasing the close-loop gain leads to a reduced bandwidth, unless we change the open-loop gain. This is the same like increasing the transimpedance g_m, the technique mentioned above. It is also obvious that in the methods with varying load or feedback impedance, the bandwidth changes when the those impedance changes. In other words, they have gain-dependent bandwidth since those impedance determines the gain as well. Depending on the application, this might be not wanted in variable gain amplifier circuit as mentioned here [30]. So, in general, it is expected that the bandwidth of the amplifier will be constant while the gain is varying.

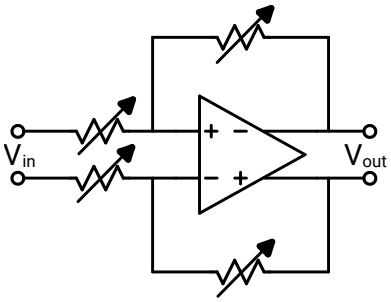
The varying transconductance g_m has this benefit of gain-bandwidth independent while other two topologies, i.e., varying feedback impedance, varying load impedance, suffer from gain-bandwidth dependency. Figure 2.7 show the general structure of these topologies. One example of circuit that use varying transconductance g_m is Gilbert cell. It has been used to realize variable gain amplifier [34], [32]. Depending on the power budget, the Gilbert cell might suffer from a very low gain or even attenuation.



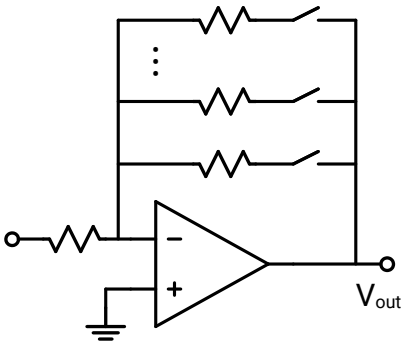
(a) Varying bias current



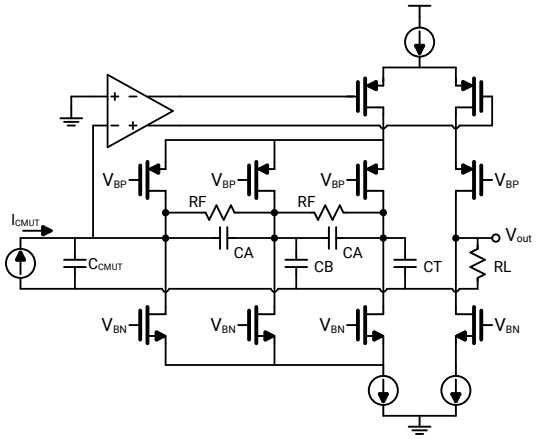
(b) Varying load impedance



(c) Varying feedback impedance



(d) Switching feedback impedance



(e) Interpolation

Figure 2.7.: These are the general structures to realize Variable Gain Amplifier (VGA). Some important things to consider are some topologies have gain-dependent bandwidth characteristic which might not be wanted in certain applications [30], discreetly switching feedback impedance might not be suitable for imaging application because it produce switching artefacts, and the fact that some topologies require complex biasing circuits or additional peripheral circuits.

2.4.2. Circuit Parameters

In addition to the circuit parameters which are related to voltage amplifier, e.g., gain and bandwidth, the circuit parameters which are specific for this circuit are introduced here. In general, the circuit is looked from the voltage amplifier perspective.

Maximum and Minimum Gain Maximum gain is the maximum gain obtained at certain value of gain control voltage. This gain is the gain that amplifies the weakest echo. The opposite definition is valid for minimum gain.

Gain Range Gain range is defined as the difference between the maximum and the minimum of gain.

Gain Error Gain error is defined as the difference between the gain of the circuit and the ideal linear-in-dB gain which is a linear line.

2.4.3. Bias Varying Differential Amplifier

This is the very basic topology when we want to change the gain by varying the bias. In order to change the gain, the bias current must be changed. It is expected that the biasing current changes linearly, at least approximately linear over a certain range. There is a possibility to change it exponentially as well. But the biasing device must operates in subthreshold region. Figure 2.7 (a) describe this topology.

The bandwidth is determined by the pole frequency at the output node. This dictates the maximum value for the load resistance, given a certain value of input capacitance of the cascaded stage. This means the maximum gain is also limited. The gain can be increased by increasing the transconductance g_m but only to a certain amount before the transistor enter linear region. Equation (2.13) and equation (2.12) show the dominant pole frequency and the small signal gain for this topology, respectively.

$$\omega_{p1} = \frac{1}{C_{OUT}R_1} \tag{2.12}$$

$$A_v = g_m R_1 \tag{2.13}$$

2.4.4. Folded Gilbert cell

This topology is an improvement of the simple differential amplifier discussed before. While the previous topology can vary the gain only in a positive or negative direction,

Gilbert cell topology can vary the gain in both direction. This implies that Gilbert cell topology provides linear range wider than the previous topology does. If we compare it with the original Gilbert cell, folded Gilbert cell require less voltage headroom. It is because we fold the current source. One of the consequence of this folding is it requires more power. The circuit can be described as two differential amplifier with slightly different bias current. Both bias current vary in an opposite direction and is controlled by control voltage. Then, the output of two differential amplifier are cross-coupled. Two output currents are driven through the load resistors and the voltage difference is taken out. Figure 2.8 shows the schematic diagram of folded Gilbert cell topology.

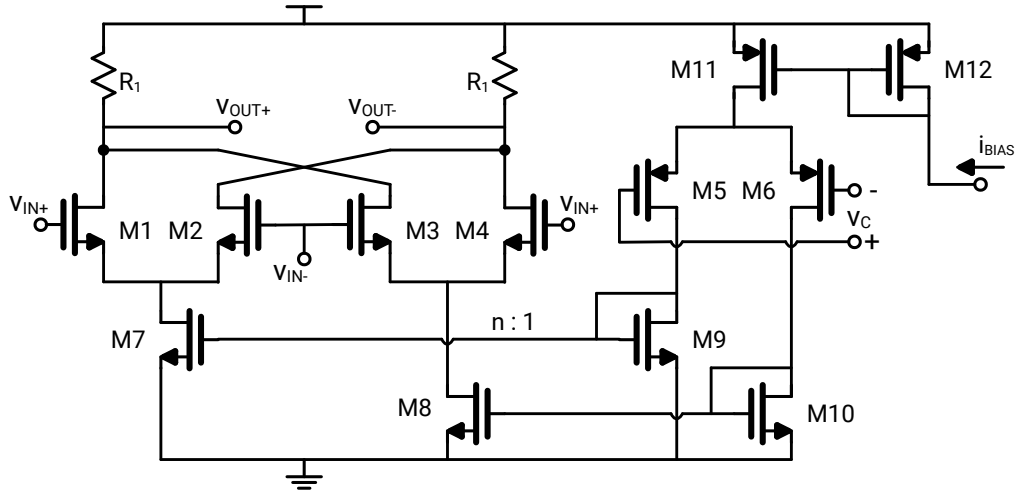


Figure 2.8.: The picture shows the schematic drawing of folded Gilbert cell topology.

Same like the previous topology, the bandwidth is determined by the pole frequency at the output node. With the same analysis, it is obvious that the maximum value for the load resistance is limited. In other words, the gain is limited. Equation (2.14) and equation (2.15) show the dominant pole frequency and the small signal gain for the folded Gilbert cell topology, respectively.

$$\omega_{p1} = \frac{1}{C_{OUT} R_1} \tag{2.14}$$

$$A_v = \sqrt{\frac{n\mu_0 C_{ox} (W/L)_{1,4}}{2I_{11}}} g_{m5} (v_{c+} - v_{c-}) R_1 \tag{2.15}$$

2.5. Exponential Voltage Generator

As already mentioned, the attenuation of ultrasound is logarithmic by nature. So the changing of gain to compensate this attenuation must be logarithmic as well, or at least approximately. Some amplifiers are intentionally designed to have this feature [35]. If the amplifier is a linear amplifier, the analog control signal used to change the gain must be exponential. Thus, a circuit that takes a linear input and produces an exponential output is required [34]. An exponential characteristic of the device biased in subthreshold is utilized in both circuits. Subthreshold region has its own disadvantage though, e.g., more sensitive to temperature, threshold voltage variation, and noise [36]. Other device that can be used to provide exponential characteristic is BJT transistor. Figure 2.9 shows the general structure of the exponential voltage generator circuits which use exponential devices.

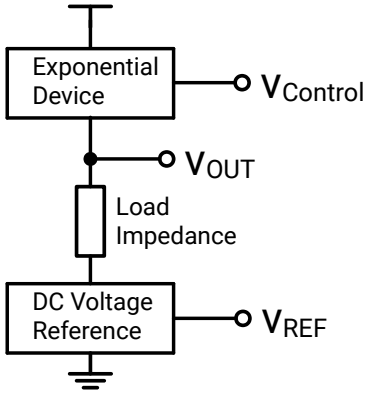


Figure 2.9.: The general structure of exponential voltage generator (EVG).

Another way to realizes an exponential behavior is by designing a linear circuit that realize a mathematical function that approximates exponential function [37], [35]. Since this is just an approximation, applications that need accurate exponential behavior should pay more attention realizing the circuit with this option.

2.6. Post Amplifier

Depending on the topology used to realize the variable gain amplifier and the whole system, a post amplifier might be required, especially for the circuits that use Gilbert cell due to its low gain characteristic. On the other side, there might be a need to convert differential signal to single-ended.

The simple OTA is one of the candidate but it provides only small gain. It requires only small area, though. Symmetric OTA is one of the possible topology to realize this post amplifier. It requires only one biasing and provide higher gain than the simple five transistor OTA can provide. Another possible option is folded-cascode topology. However, it consumes more power due to its needs of three biasing and it requires to be in a close-loop configuration due to its very high open-loop gain.

To summarize, in this chapter, all the theoretical understanding has been discussed. g_m/I_D method will be used in designing the circuits. The candidate topologies which are expected to deliver the performance we need have been discussed. The analytical equations used to describe the circuit performance have also been introduced. In the next chapter, the design phase will be summarized, start from the block diagram and down to the component level where the component sizes and values are determined.

3. Circuit Design and Simulation

This chapter discusses the design of each block required to realize a Time Gain Compensation (TGC) Amplifier. All reasonings and issues which have influence on circuit performance are also included. The output is the component sizes and values required to meet specification both as individual block and as a whole system. The simulation results and circuit performance parameters are also summarized.

3.1. Block Diagram

Ideally, it would be better if the design can be implemented in a single stage, including all the features like low input and output impedance, varying gain, etc. The benefits are we do not have to deal with the input and output port requirements for cascading and other effects that might come up from cascading, e.g., the next stage bandwidth must be higher than that of the previous stage. In addition to that, the noise requirement can be meet in a more confident way, without worrying whether the next circuit would have too much input-referred noise. The complete circuit might not be simpler though since such topology might need peripheral circuitry that allow the core amplifier to have varying gain or other features [3]. On the other hand, the design can be implemented by assigning a certain function to a specific circuit. For example, this can be done by separating the low input impedance requirement from varying gain feature. This leads to cascading structure which is used in this work.

In this work, the low input impedance feature is separated from the gain varying feature. Both are taken care of by separate circuits. In order to provide the similar DC level on the differential input on the VGA, a dummy TIA is connected at the VGA negative input. It is also found out later that a post amplifier is needed to provide more gain. That cascading chain changes its gain in a linear way. So, in order to have a linear-in-dB feature, we need to provide a control voltage that changes exponentially. This is done by the exponential voltage generator. The top level block diagram is shown in Figure 3.1.

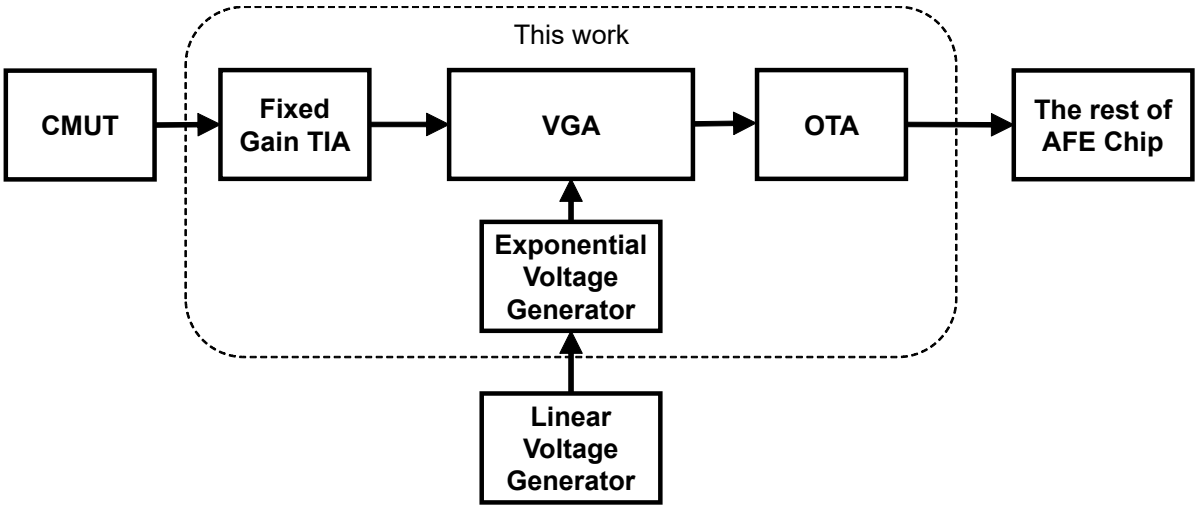
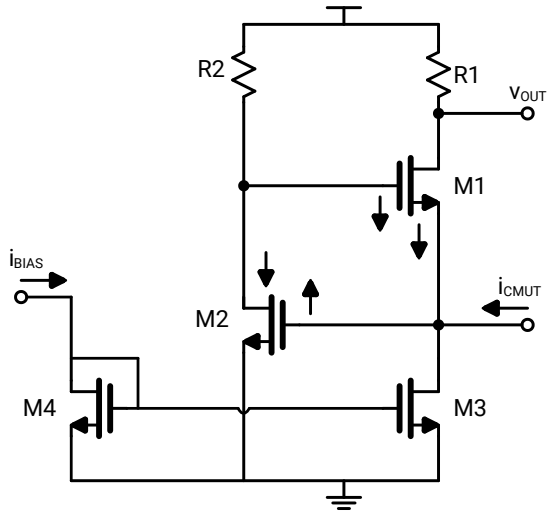


Figure 3.1.: The block diagram of of the top level circuit.

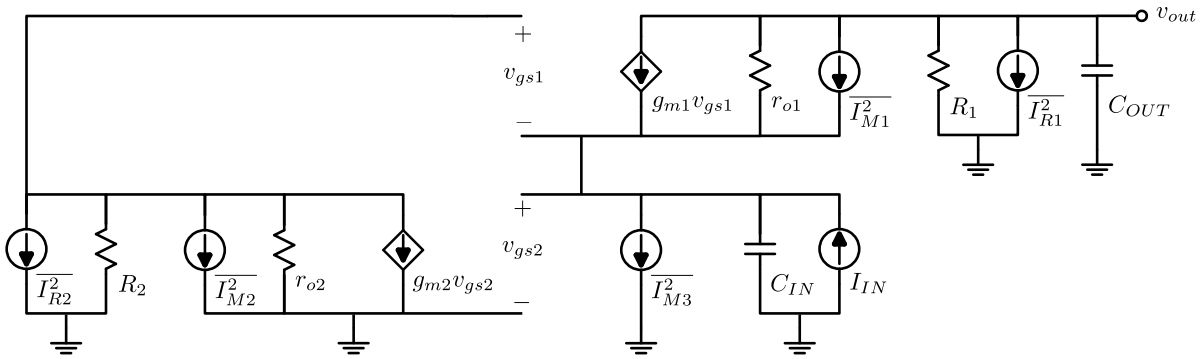
3.2. Regulated Cascode

This topology is selected by considering the result from the CMOS transimpedance amplifier survey discussed here [22]. It is shown in that review that regulated cascode topology provides the best input-referred noise current performance for the applications with specification close with the specification of this work. One can start optimizing this circuit from different way. But, since this is the first stage, it is suggested that it would be better to optimize the noise first [16]. If we optimize other parameter first, we let the noise parameter be at the loose end and that might lead to the result which is not within the target specification. The regulated cascode topology and its small signal equivalent circuit are shown again in Figure 3.2 for convenience.

The g_m/I_D methodology is a recommended standard practice in design. Obviously, we can always benefit from this method regardless the complexity of analytical equation of the circuit parameter. However, especially in this circuit, it really shows its benefits when the analytic equation that describe a circuit parameter is complex. It is because this method catches the nonlinear characteristics of the device. Table 3.1 summarizes some numbers as references to keep in mind. In this technology, if (g_m/I_D) equals to 5 and minimum width are chosen, I_D is around 3.3 μA. So the bias current of 10 μA is chosen to bias M1. The biasing device M3 contributes input-referred noise current of around 0.74 pA/ $\sqrt{Hz}$. If we allocate 3 pA/ $\sqrt{Hz}$ noise budget for this circuit, this means the biasing device already contributes to around 25% of the total noise budget.



(a) regulated cascode topology



(b) regulated cascode small signal equivalent circuit

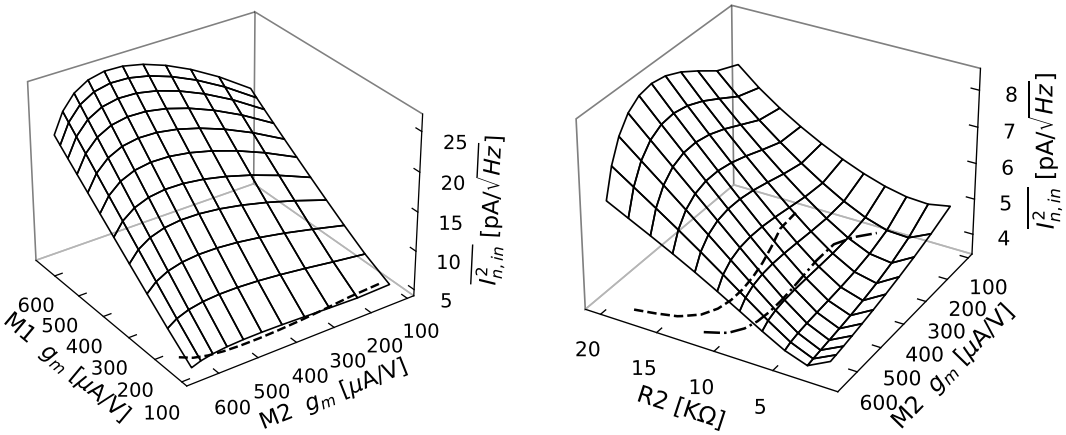
Figure 3.2.: The regulated cascode topology and its small signal equivalent circuit are shown again here for convenience.

Parameter	(g_m/I_D)	(I_D/W)	I_D	g_m	$I_{n,in,th}$
Unit	[1/V]	[μA/μm]	[μA]	[μA/V]	[pA/$\sqrt{Hz}$]
Value	5	≈ 15	3.3	16.5	0.43
	5	≈ 15	10	50	0.74

Table 3.1.: Summary of some reference values related with (g_m/I_D). The first row data is for NMOS with minimum width.

From the equation (2.10), it can be seen that increasing R_2 will scale down the noise, at least it can easily be observed at two of the terms. The value of R_2 must be chosen such that M1 and M2 are still in saturation. The value of $(g_m/I_D)_1$ and $(g_m/I_D)_2$ are also kept at the medium inversion level, g_m/I_D is kept less than 16. By iteration, it can be shown that R_2 must be around 15 KΩ. Figure 3.3 shows how the input-referred

noise current would vary over g_{m1}, g_{m2}, and R_2. The bias current of M2 is chosen to be double that of M1 and R2 values is chosen to be 15 KΩ. The transfer function and noise spectrum are shown in Figure 3.4. It can be seen from the plot that the noise is below 5 pA/$\sqrt{Hz}$ at 5 MHz and the bandwidth is slightly above 5 MHz.



(a) (b)

Figure 3.3.: The graph shows the input-referred noise current of regulated cascode topology with respect to g_{m2} and (a) g_{m1} with R_1 = 10 KΩ and R_2 = 15 KΩ and (b) R_2 with g_{m1}= 150 μA/V. It is used as a tool to choose the proper value for transconductance g_m for M_1 and M_2. The lines are the projection of the input-referred noise current of 6 pA/$\sqrt{Hz}$ (dashdot) and 5 pA/$\sqrt{Hz}$ (dash) onto the g_{m1}-g_{m2} or g_{m2}-R_2 pane. It is important to keep in mind though, this is not really accurate and the mapping result is only used as a starting point.

The upper bound of R_1 can be calculated from the bandwidth equation. It is shown in equation (3.1). The value of R_1 should be less than 15.9 KΩ. Resistance value of 10 KΩ is chosen. It is also important to keep in mind that this circuit is the very first stage so it is the slowest circuit whose bandwidth determines the bandwidth of the whole cascade chain. The transient response of the circuit is shown in Figure 3.5 (b). The summary of component sizes and values are shown in Table 3.2. The circuit performance is summarized in Table 3.3.

$$\begin{aligned} \omega_{p2} &= \frac{1}{C_{OUT}R_1} \geq 5 \text{ MHz} \\ R_1 &\leq \frac{1}{2\pi C_{OUT} BW} = \frac{1}{2\pi(2 \text{ pF})(5 \text{ MHz})} \\ R_1 &\leq 15.9 \text{ K}\Omega \end{aligned} \tag{3.1}$$

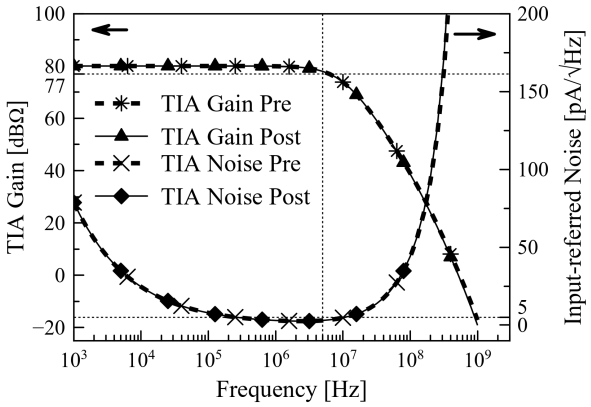


Figure 3.4.: Pre-layout and post-layout transimpedance gain and noise spectrum of regulated cascode.

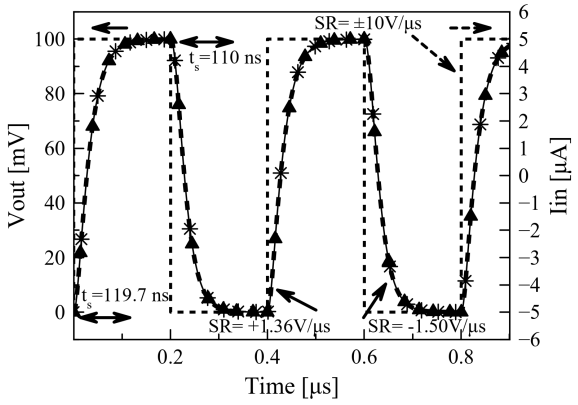


Figure 3.5.: Pre-layout and post-layout transient response with square wave input of regulated cascode.

Component	W/L	Value
M_1	8 μm/0.9 μm	-
M_2	16 μm/0.9 μm	-
M_3	0.42 μm/0.9 μm	-
M_4	0.42 μm/0.9 μm	-
R_1	-	10 KΩ
R_2	-	15 KΩ

Table 3.2.: Summary of transistor sizes and other components' value of the regulated cascode.

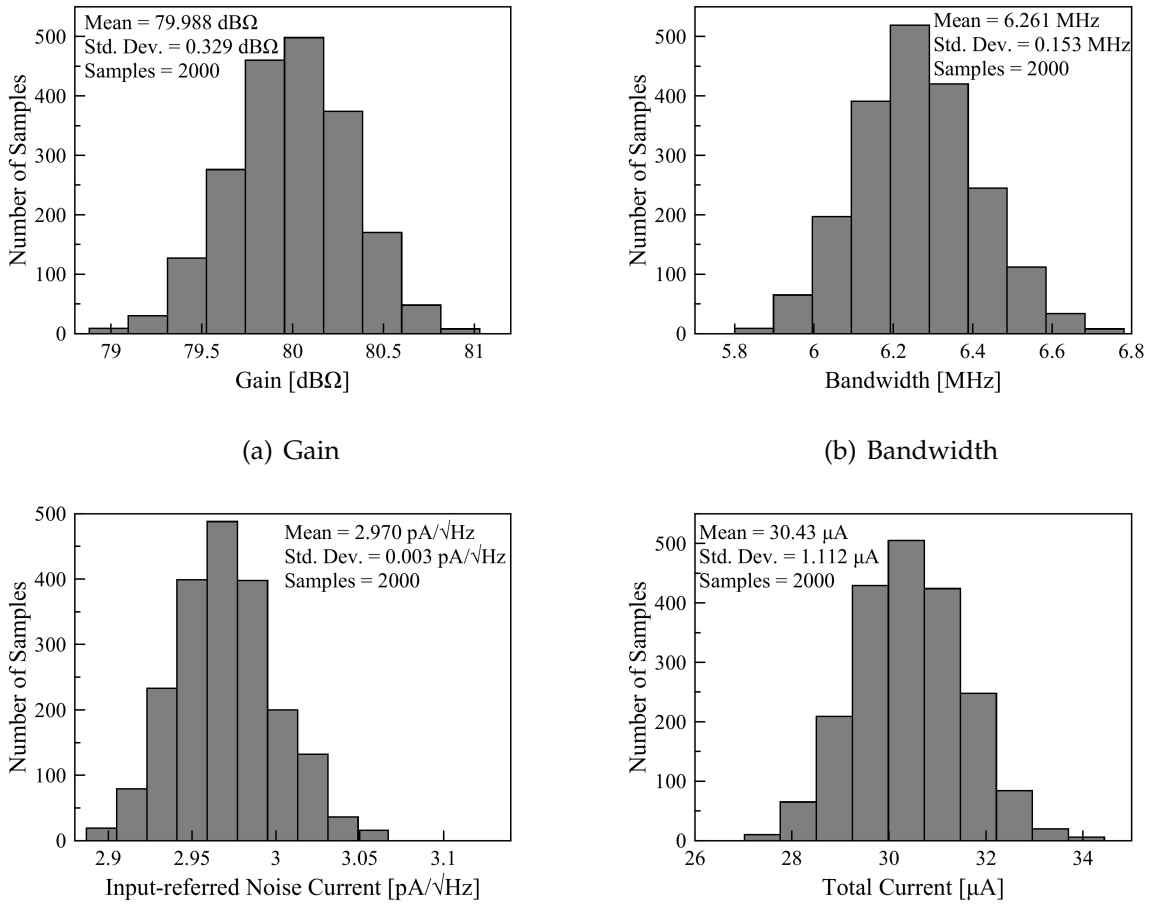
Parameter	Unit	Target	pre-layout	post-layout
Gain	dBΩ	≥ 80	79.99	80
BW	MHz	≥ 5	6.262	6.262
Input-referred Noise Current at 5 MHz	pA/$\sqrt{Hz}$	≤ 5	2.969	2.972
Positive Slew Rate/Negative Slew Rate	V/μs	-	1.36/1.50	1.36/1.50
Settling Time	ns	-	119.7/109.8	119.7/110
Transducer Capacitance	pF	10	10	10
Load Capacitance	pF	2	2	2
Power Consumption	μW	-	54.74	54.70
Area	μm^2	-	-	32×37

Table 3.3.: Summary of pre- and post-layout circuit performance parameters of regulated cascode.

In order to include the effect of process variation, corner simulation and monte carlo simulation have been performed. The results of corner simulation and monte carlo simulation are shown in Table 3.4 and Figure 3.6, respectively. As can be seen from the Table 3.4, the transimpedance gain at low frequency at corner wp is below specification. At corner wp, the output resistance of both NMOS and PMOS are lower than the typical values. So the parallel result of this resistance with R_1 like it is shown in the circuit leads to a slightly lower low frequency gain result. Since the gain and the noise performance of this circuit is critical, the post-layout corner simulation was performed as well. The results are summarized in Table 3.5.

Corner	Current	Noise@5MHz	Bandwidth	Gain@10KHz
Unit	uA	pA/$\sqrt{Hz}$	MHz	dBΩ
tm	30.41	2.969	6.262	79.99
wo	32.73	2.920	6.417	79.99
wp	37.44	2.876	7.082	78.70*
ws	24.95	3.119	5.541	81.19
wz	28.11	3.028	6.090	79.99

Table 3.4.: Summary of pre-layout corner simulation of the regulated cascode at 27 °C. * lower than the target value.



(a) Gain

(b) Bandwidth

(c) Input-referred noise current

(d) total current consumption

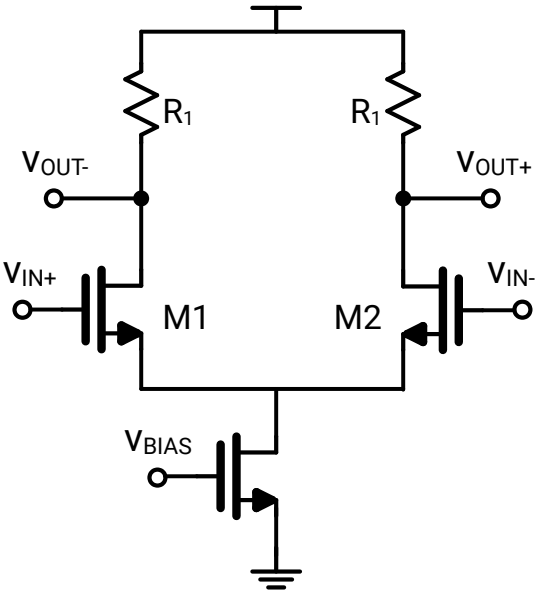
Figure 3.6.: Pre-layout monte carlo simulation of the regulated cascode at 27 °C.

Corner	Current	Noise@5MHz	Bandwidth	Gain@10KHz
Unit	uA	pA/$\sqrt{Hz}$	MHz	dBΩ
tm	30.39	2.972	6.262	80.00
wo	32.71	2.923	6.417	80.00
wp	37.41	2.879	7.081	78.71*
ws	24.93	3.123	5.542	81.19
wz	28.10	3.031	6.090	80.00

Table 3.5.: Summary of post-layout corner simulation of the regulated cascode at 27 °C.
* lower than the target value.

3.3. Folded Gilbert Cell

As already mentioned before, the main function of this block is to realize gain variation. The chosen topology is the varying transconductance one, to be exact, folded Gilbert cell. In order to understand the reasoning behind this decision, it is important to show why a simpler candidate cannot provide the gain range specified in this work. The simpler circuit is bias varying differential amplifier. This circuit is shown in Figure 3.7.



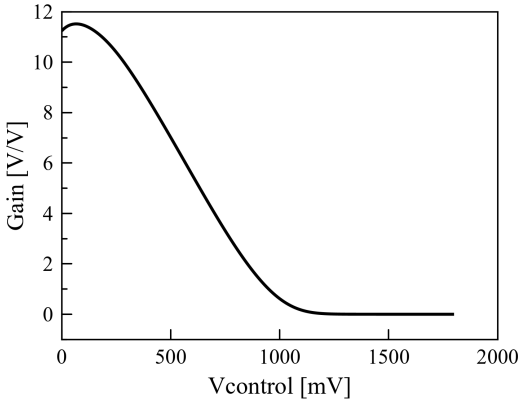
(a)

Figure 3.7.: The schematic drawing of simple current bias varying differential amplifier.

The minimum gain range expected from the circuit is 32 V/V. This gain range could cover arbitrary gain values but it is expected to be of as high as possible. In order to see whether the expected gain is possible to realize, the small-signal gain equation need to be modified as shown in equation (3.2). If the gain of ×1 - ×32 V/V and the voltage drop across the load resistance of 400 mV are expected, the circuit must be able to provide the maximum gain of ×32 V/V. This requirement corresponds with a g_m/I_D value of 80, which is impossible in this process technology. Another possible gain values are on the opposite way. It ranges from ×0.032 - ×1 V/V. But the lower bound is located deep into the nonlinear region. This is shown in Figure 3.8. This shows that the circuit cannot provide enough gain range. It is also important to keep

in mind that the linear section on Figure 3.8 is only approximately linear.

$$\begin{aligned} A_v &= g_m R_1 \\ &= \frac{g_m}{I_{R_1}} V_{R_1,drop} \end{aligned} \tag{3.2}$$



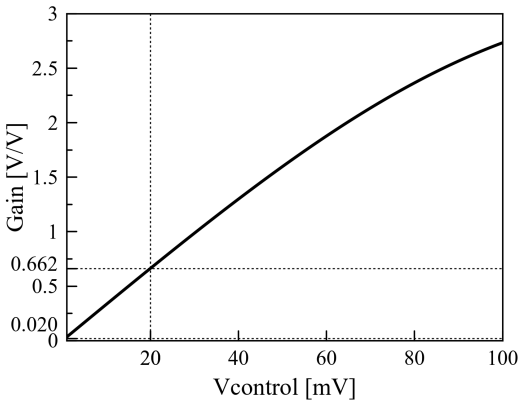
(a)

Figure 3.8.: The simulation result of the simple current bias varying differential amplifier. It shows how gain varies with control voltage.

The gain equation of this circuit is shown in equation (3.3). The same calculation can be done like before but with one difficulties in approximating $\mu_0 C_{ox}$. If we assume the dropping voltage on the load resistor is 250 mV, control voltage difference is 40 mV, and $(g_m/I_D)_5$ is approximately around 12, it can be shown that the gain cannot be of high value because we multiply small number with another small number. The gain plot is shown in Figure 3.9. The lower bound of the gain is the main specific characteristic of this circuit compared with the simple differential amplifier discussed before.

$$\begin{aligned} A_v &= \sqrt{\frac{n(\mu_0 C_{ox})_{1,4}(W/L)_{1,4}}{2I_{D11}}} g_{m5} R_1 (v_{C+} - v_{C-}) \\ &= V_{R_1,drop} \sqrt{\frac{n(\mu_0 C_{ox})_{1,4}\,(W/L)_{1,4}}{2I_{D11}}} \left(\frac{g_m}{I_D}\right)_5 (v_{c+} - v_{c-}) \end{aligned} \tag{3.3}$$

From equation (3.3), it can be seen that increasing the $(g_m/I_D)_5$ and the voltage drop on the load resistor will increase the gain. The higher value of n also provides higher



(a)

Figure 3.9.: The simulation result of the folded Gilbert cell. It shows how gain varies with control voltage.

gain but it will increase power consumption. The value of n of 0.4 is chosen in this circuit while considering that- the maximum possible current that flows through M1-M4 still keep those transistor in saturation, not get pinched into triode by the voltage drop of the load resistors. The size of M1-M4 are chosen in such away their g_m/I_D is around 13. The drop voltage on the load resistor is selected by considering the input common mode range of the next stage. The size of M5-M6 are also chosen so their g_m/I_D is around 13. The rest of the transistors, which are part of current mirrors, are bias in a strong inversion with g_m/I_D around 5.

The upper bound for the load resistance value can be calculated from the bandwidth equation. This is shown in equation (3.4). The higher bandwidth value is chosen in order to compensate the gain drop at the -3dB frequency of the previous stage. The summary of component sizes and values are shown in Table 3.6.

$$\begin{aligned} \omega_{p1} =& \frac{1}{C_{OUT}R_1} \geq 10\ \text{MHz} \\ R_1 \leq& \frac{1}{2\pi C_{OUT} BW} = \frac{1}{2\pi(2\ \text{pF})(10\ \text{MHz})} \\ R_1 \leq& 7.9\ \text{K}\Omega \end{aligned} \tag{3.4}$$

The input-referred noise of this circuit is expected to be less than 15 nV/$\sqrt{Hz}$. When referred back to the input of the transimpedance amplifier, this value is equivalent to 1.5 pA/$\sqrt{Hz}$. The transfer function and noise spectrum are shown in Figure 3.10 and Figure 3.11, respectively. The transient response with square wave input is shown in

Component	W/L	Value
M_1, M_2, M_3, M_4	64 μm/0.9 μm	-
M_5, M_6	576 μm/0.9 μm	-
M_7, M_8	16 μm/0.9 μm	-
M_9, M_{10}	40 μm/0.9 μm	-
M_{11}	360 μm/0.9 μm	-
M_{12}	20 μm/0.9 μm	-
R_1	-	2 KΩ

Table 3.6.: Summary of transistor sizes and other components' value of the folded Gilbert cell.

Figure 3.12. The performance is summarized in Table 3.7.

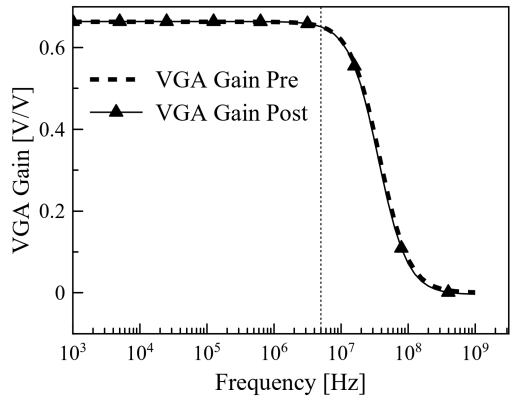


Figure 3.10.: Pre-layout and post-layout transfer function of folded Gilbert cell.

Parameter	Unit	Target	pre-layout	post-layout
Gain Range	dB	≥ 30	32	32
Maximum gain	dB	-	0.662	0.662
Gain Error	dB	-	± 2*	± 2*
Gain Control Type	-	-	analog	analog
Control Voltage Range	mV	-	40	40
BW	MHz	≥ 8	37.58	35.91
Input-referred Noise Current at 5 MHz	nV/$\sqrt{Hz}$	≤ 15	12.97	13.1
Load Capacitance	pF	2	2	2
Power	mW	-	1.71	1.71
Area	μm^2	-	-	99×131

Table 3.7.: Summary of pre- and post-layout circuit performance parameters of folded Gilbert cell.

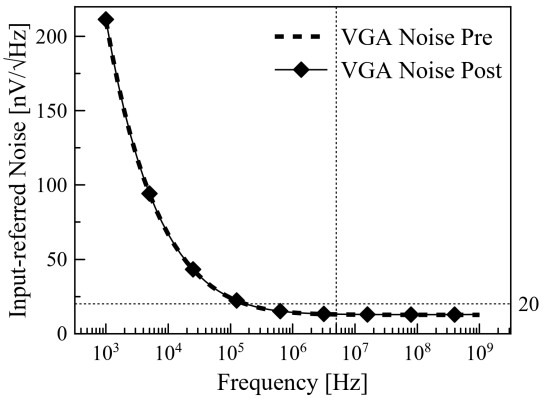


Figure 3.11.: Pre-layout and post-layout input-referred noise voltage of folded Gilbert cell.

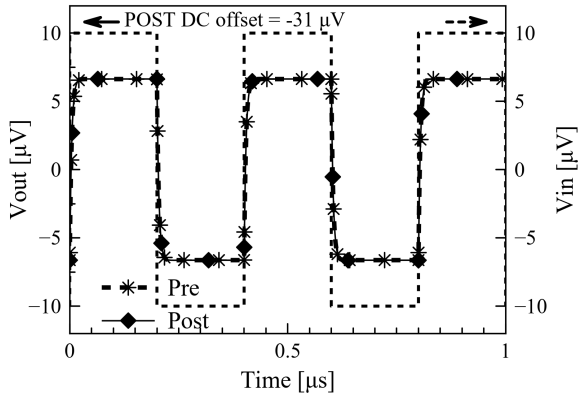


Figure 3.12.: Pre-layout and post-layout transient response with square wave input of folded Gilbert cell

3.4. Exponential Voltage Generator

The BJT-based exponential voltage generator circuit is chosen in this work. The exponential current from the BJT is driven through into a load resistor whose the other terminal is connected to a voltage reference. This allows us to adjust the DC level of the output voltage. Figure 3.13 shows this topology. Since all MOSFETs in this circuit work as current mirror, they are all sized in such a way they are all in saturation over a range of linear input voltage.

It is also important to mention that this topology can be realized using either NPN or PNP BJT. In this work, PNP BJT is used as the exponential device because this is the only BJT that is compatible with the MOSFET device used. It is all related to the

technology restriction.

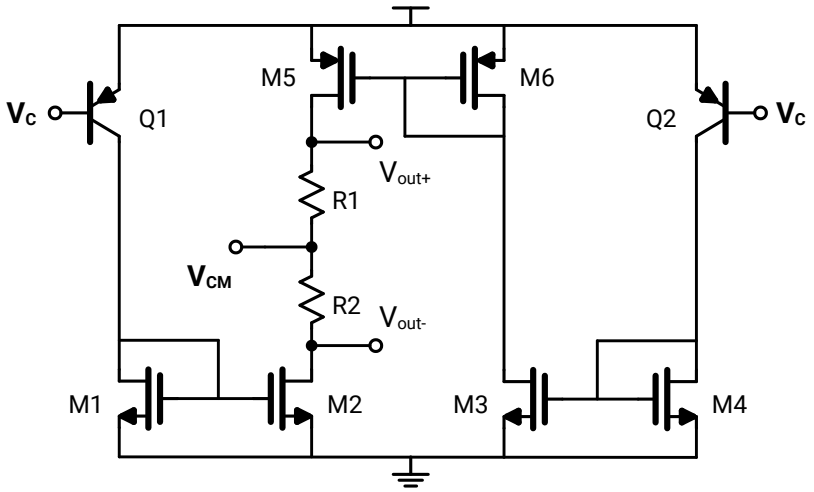


Figure 3.13.: The schematic drawing of exponential voltage generator circuit.

The upper bound for the load resistance value can be calculated from the bandwidth equation. This is shown in equation (3.5). The exact value is chosen based on the DC level of control voltage requirement expected from the VGA circuit. The summary of component sizes and values are shown in Table 3.8. The input-output response of the circuit is depicted in Figure 3.14. The simulation result is summarized in Table 3.9.

$$\begin{aligned} \omega_{p1} =& \frac{1}{C_{OUT}R_1} \geq 10\ \text{MHz} \\ R_1 \leq& \frac{1}{2\pi C_{OUT}BW} = \frac{1}{2\pi(2\ \text{pF})(10\ \text{MHz})} \\ R_1 \leq& 7.9\ \text{K}\Omega \end{aligned} \tag{3.5}$$

Component	W/L	Value
M_1, M_2, M_3, M_4	3 μm/0.9 μm	-
M_5, M_6	6 μm/0.9 μm	-
M_7, M_8	16 μm/0.9 μm	-
Q_1, Q_2	-	$2 \times 2\ \mu\text{m}^2$
R_1, R_2	-	500 Ω

Table 3.8.: Summary of transistor sizes and other components' value of the exponential voltage generator. For the BJT transistors, the value shows the emitter area.

Parameter	Unit	Target	pre-layout	post-layout
Positive Output Voltage	mV	-	433 - 401	433 - 401
Negative Output Voltage	mV	-	367 - 399	367 - 399
Input Voltage	mV	-	960 - 1066	960 - 1066
Power	mW	-	0.611	0.596
Area	μm^2	-	-	37×57

Table 3.9.: Summary of pre- and post-layout circuit performance parameters of exponential voltage generator circuit.

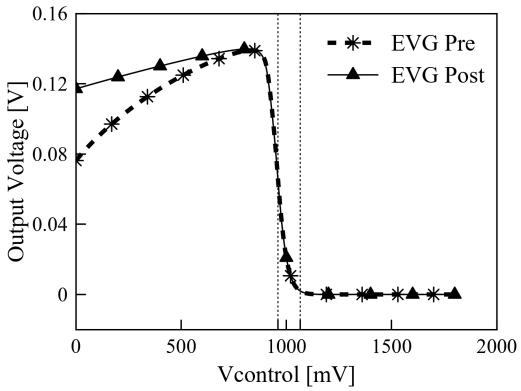


Figure 3.14.: Pre-layout and post-layout input-output DC response of the exponential voltage generator circuit.

3.5. Symmetric OTA

It can be seen from the VGA discussion above that its output is quite small. This leads to the need of having an amplifier to compensate the attenuation of the VGA. This amplifier is also used to convert differential signal at the input into a single ended. This is also a needed feature in this work. A simple differential pair amplifier is a possible candidate but the gain is not sufficient. The gain of this amplifier is expected to be above 31 dB.

Symmetrical OTA is one of the most used OTAs [38]. The topology is shown in Figure 3.15. Its input transistors drive balance load whose current then is copied into the third current mirror load. The current at the output stage can be set to be a couple more time higher than the bias current of the input transistors. With combination of the high impedance at the output node, this can provide us with a high enough gain.

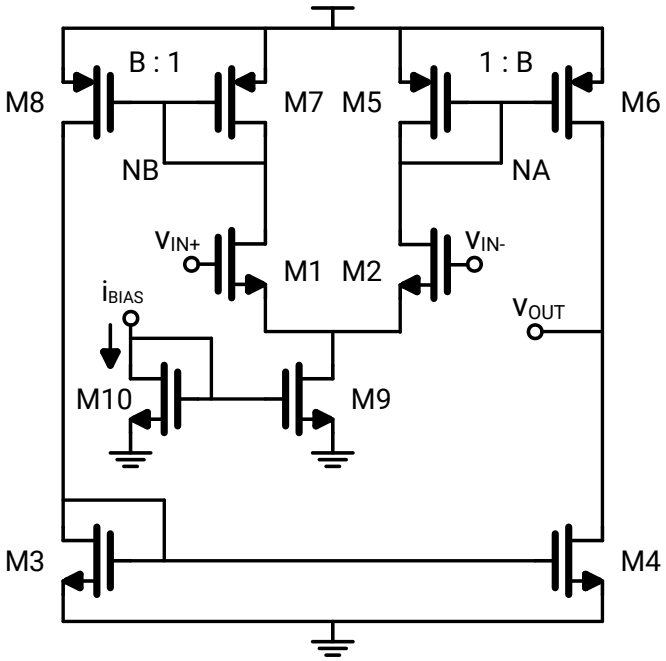


Figure 3.15.: The schematic drawing of symmetrical OTA.

The bandwidth is determined by the load capacitor and the output resistance of the circuit. It is expected to have output resistance less then 11.3 KΩ to achieve around 7 MHz bandwidth. Equation (3.6) shows this calculation. Since the total resistance at the output node is the parallel resistance of $r_{o4}||r_{o6}$, r_{o4} and r_{o6} must be less than 22.6 KΩ. In order to achieve this value, the transistors at the output stage must have shorter channel length, wider channel width, or higher bias current. The simulation shows that the output resistance of M4, r_{o4}, and that of M6, r_{o6}, are close to 18 KΩ.

$$\begin{aligned} \omega_{p1} &= \frac{1}{C_{OUT} r_o} \geq 7\ \text{MHz} \\ r_o &\leq \frac{1}{2\pi C_{OUT} BW} = \frac{1}{2\pi(2\ \text{pF})(7\ \text{MHz})} \\ r_o &\leq 11.3\ \text{K}\Omega \end{aligned} \tag{3.6}$$

In order to have good phase margin, the second pole must be taken case of. The second pole frequency is defined by the f_T of M5 and the current gain B, as described in equation (3.8). g_m/I_D method shows its benefits again in designing this circuit. From the f_T vs. g_m/I_D plot, one can see the possible transit frequency f_T for a given channel length value and its inversion level. Shorter channel length provides higher f_T. We need to choose suitable f_T and B such that the f_{2p} is around three times the bandwidth. This is not a hold a fast rule though, for many reasons. Picking higher

B leads to lower output resistance but the circuits will consume higher current. The worse thing is, even if we allow for more current consumption, it shifts the second pole frequency f_{2p} to the lower value [39]. It is because we increase the transistor width at the output stage and this leads to higher parasitic capacitance at node NA which is an already high capacitance node to start with. The required gain-bandwidth calculation is shown in equation (3.7).

$$GBW = 10^{(31/20)} \times 7\text{MHz} \approx 250\text{MHz} \tag{3.7}$$

$$f_{2p} \approx \frac{f_{T5}}{B+3} \tag{3.8}$$

After fixing the the size of the transistors at the output stage, it is found that the current needs to be of a high value to obtain lower output resistance. This means that B should be around $B = 8$. In order to fulfill this, the transit frequency f_T must be more than 8.25 GHz. This is a problem because the device with higher channel length cannot provide that value even for the channel length of only two times the minimum width. It is due to the fact that M5 is PMOS transistor whose transit frequency f_T is around five times lower than that of NMOS given the same channel length and inversion level. This forces the design to have significant lower phase margin. The g_{m1} needs to be limited as well in such a way that the gain is only enough without having too high gain-bandwidth while the second pole frequency is constant. Otherwise, the phase margin will degrade as well. The transfer function and noise spectrum are shown in Figure 3.16 and Figure 3.17, respectively. The simulation result is summarized in Table 3.10. The transistor sizes is summarized in table 3.11.

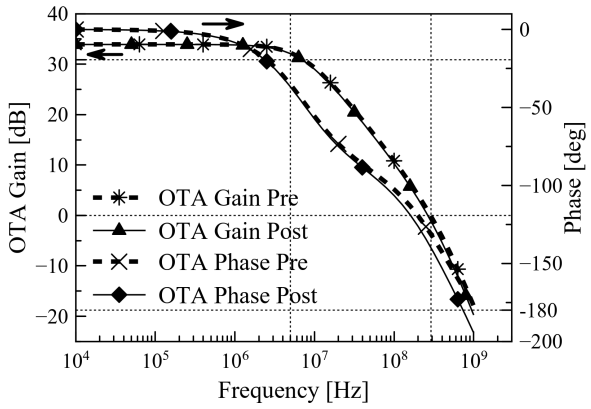


Figure 3.16.: Pre-layout and post-layout frequency response of symmetrical OTA.

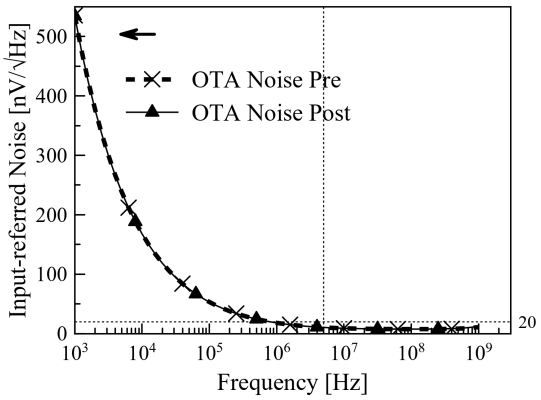


Figure 3.17.: Pre-layout and post-layout input-referred noise current spectrum of symmetrical OTA.

Parameter	Unit	Target	Pre-layout	Post-layout
Gain	dB	≥ 31	33.94	33.91
Phase Margin	deg	-	49.44	43.86
Gain-Bandwidth	MHz	≥ 250	362.1	344.2
Unity Gain Bandwidth Frequency	MHz	-	290.4	267.9
Bandwidth	MHz	≥ 7	7.262	6.925
Power	mW	-	2.623	2.626
Area	μm^2	-	-	43×60

Table 3.10.: Summary of pre- and post-layout circuit performance parameters of symmetrical OTA.

Component	W/L
M_1, M_2	20 μm/3.6 μm
M_3, M_4	26 μm/0.27 μm
M_5, M_7	24 μm/0.36 μm
M_6, M_8	88 μm/0.235 μm
M_9	24 μm/0.9 μm
M_{10}	12 μm/0.9 μm

Table 3.11.: Transistor sizes and other components' value of the symmetrical OTA.

In order to see the process variation, corner simulation was performed and the result is summarized in Table 3.12. From Table 3.10 and Table 3.12, it is can be seen that the bandwidth from post-layout simulation is below the required value, even in typical value and get worst in corner ws. It seems that the output resistance of M4 and

M6 must be reduced to give more margin. Choosing lower output resistance means higher power consumption. It can be done if there is some room on the power budget while in this work, the symmetrical OTA consumes already around 50% of the total power consumption.

Corner	Current	Phase Margin	Bandwidth	Gain@10KHz
Unit	mA	degree	MHz	dB
tm	1.459	43.86	6.925*	33.91
wo	1.459	43.52	7.112	33.74
wp	1.553	43.83	7.614	33.83
ws	1.373	43.82	6.360*	33.88
wz	1.458	44.20	6.766*	34.03

Table 3.12.: Summary of post-layout corner simulation of the symmetrical OTA at 27 °C. * lower than the target value.

3.6. Layout Considerations

In general, it is always recommended to provide the uniform environment around the device in order to reduce mismatch. Other motivation to follow such practices is to avoid substrate noise. These expectations can be achieved by performing the following layout practices:

- All transistors were aligned in the same direction, in this work, vertically.
- Common centroid layout technique was performed to design the layout where matching is very important, e.g., differential pair. This technique cancels gradient in both axes.
- Interdigitized layout technique was used as well. This technique cancels gradient in one axis only.
- Dummy transistors were used for the device located at the edge to provide uniform environment.
- Guard rings were used to reduce the substrate noise [17].

To summarize, all the design decision have been made and all the component sized and values are calculated. The layout have been made. The pre- and post-layout simulations are also summarized. The next chapter will show the simulation of the top level circuit.

4. Top Level: Time Gain Compensation (TGC) Transimpedance Amplifier

Each block to realize the linear-in-dB transimpedance amplifier has been design, down to the component level where the component sizes and values are determined. In this section, the simulation results of top level circuit are summarized. The layout of the top level circuit is shown in Figure 4.1.

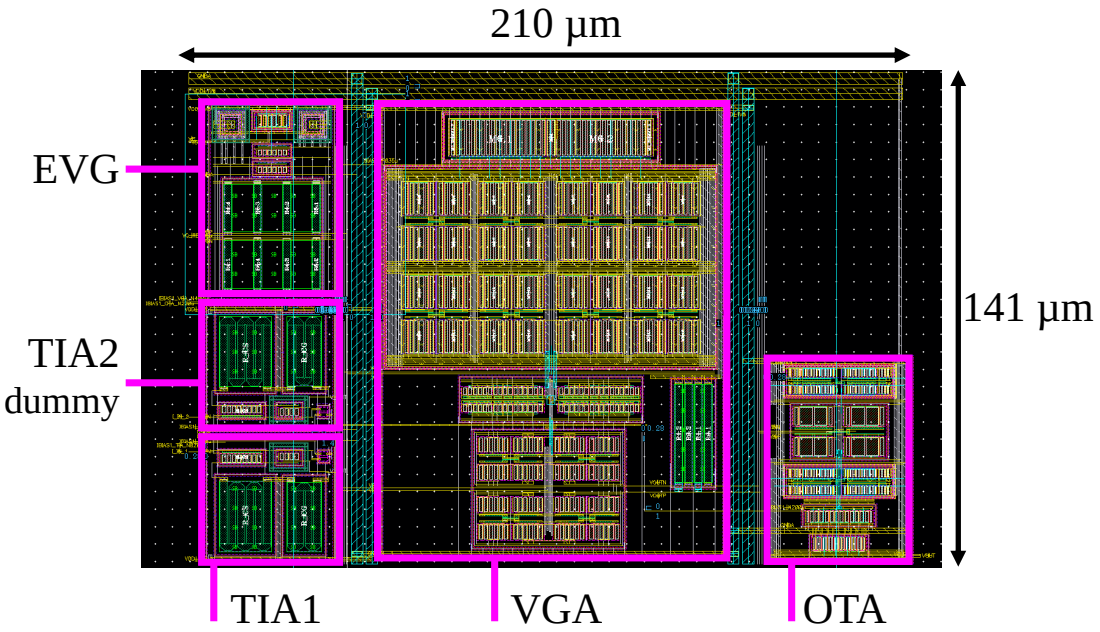


Figure 4.1.: The picture shows the top level layout of the time gain compensation (TGC) amplifier designed using 0.18 μm Silicon on Insulator (SOI) process technology from X-FAB. Each block is marked and labeled accordingly. The total area of the circuit is 210×141 μm^2.

Figure 4.2 shows the gain variation and input-referred noise current with respect to control voltage of the top level circuit. As can be seen from the transfer function

plot, the result from pre-layout simulation shows nothing unusual. The post-layout simulation result shows an issue though. It is most probably caused by the parasitic components, which are not there in the pre-layout simulation. These parasitic components create unwanted poles and/or zeros. However, this happens outside the working region of the circuit.

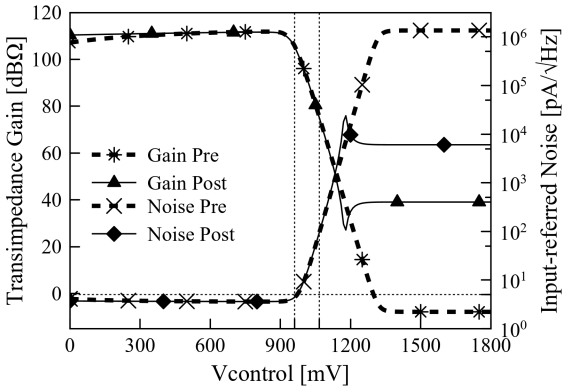


Figure 4.2.: Pre-layout and post-layout transimpedance gain and input-referred noise current of the top level circuit evaluated with 5 MHz input signal.

The corner simulation at 27 °C is summarized in Table 4.1. It can be seen that all corners fulfill the specification except the bandwidth is below the required value at corner ws. This is caused by the symmetrical OTA whose issue propagates to the top level circuit. The symmetrical OTA suffers from this bandwidth problem as can be seen in Table 3.12. This has been discussed in the previous chapter.

In order to evaluate the gain error, the gain values which are within the working region are compared with an ideal linear line. It shows the highest gain error is ≈ +1.58 dB. Figure 4.3 shows the gain error with respect to control voltage. In this work, the gain of 106 dBΩ is located close to the nonlinear region. This leads to higher gain error. The gain error can be improved by having an OTA with higher gain. So the upper boundary of the gain range is located in a more linear region. Figure 4.4 shows the gain range with respect to control voltage for all corners, i.e., tm, wo, wp, ws, wz, at three different temperature points, i.e., −40 °C, 27 °C, 150 °C. As can be seen from the plot, the system still needs temperature compensation circuit to give a proper control voltage value, as expected [34]. This is outside of the scope of this work. Within the same temperature point, the gain plot shows a consistent result.

Figure 4.5 and Figure 4.6 shows the frequency response and input-referred noise current of the top level circuit for different control voltages, respectively. It can be

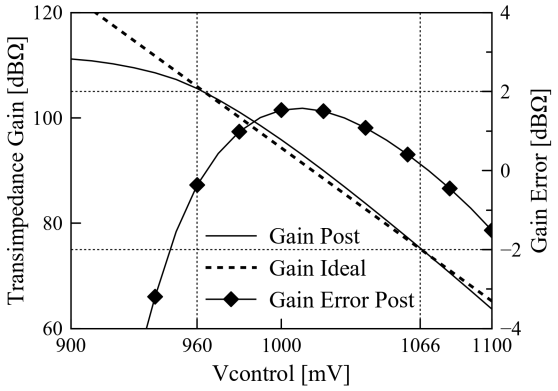


Figure 4.3.: Post-layout gain error of the top level circuit.

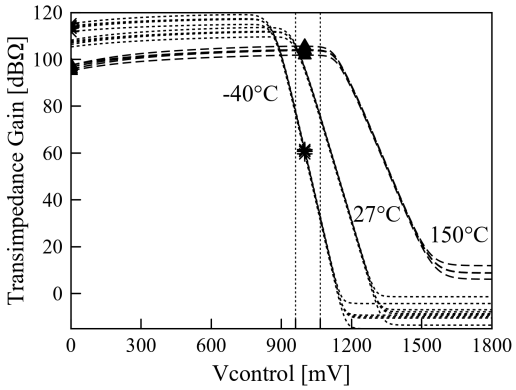


Figure 4.4.: Pre-layout transimpedance gain as a function of control voltage for all corners, i.e., tm, wo, wp, ws, wz, at three different temperature −40 °C, 27 °C, 150 °C.

seen from this plot that the bandwidth is relatively constant, as predicted from the characteristic of this topology as discussed before. This also can be verified from Figure 4.7 which plot the calculated bandwidth with respect to the control voltage. Figure 4.7 also shows the total current consumption as the gain varies. Figure 4.9 shows the monte carlo simulation results of the top level circuit at 27 °C.

The transient simulation test bench is setup with two inputs, i.e, the exponentially decaying signal which supposed to be the information carrying signal and the linear ramping signal. The result is shown in Figure 4.8.

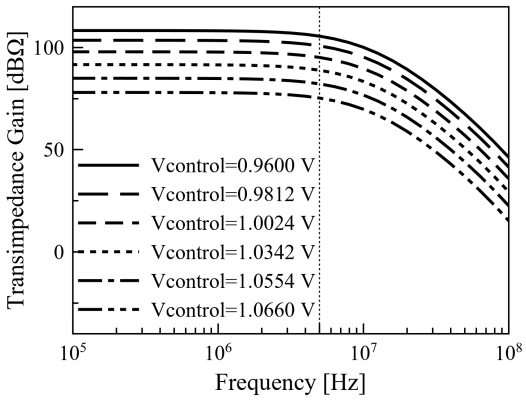


Figure 4.5.: Post-layout frequency response of the TGC transimpedance amplifier for different control voltages.

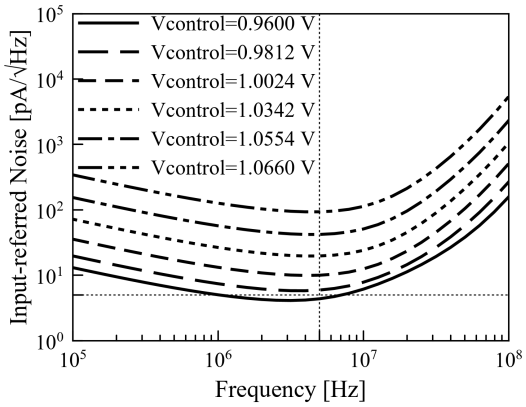


Figure 4.6.: Post-layout input-referred noise current of the TGC transimpedance amplifier for different control voltages.

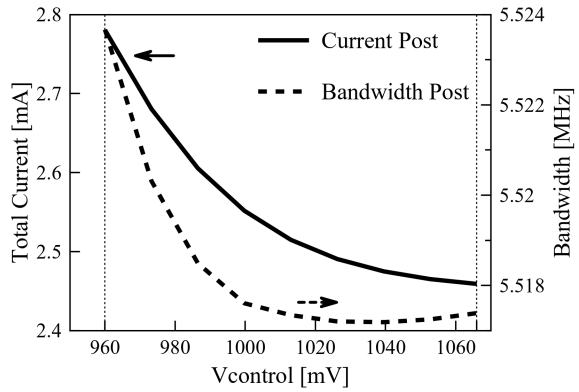
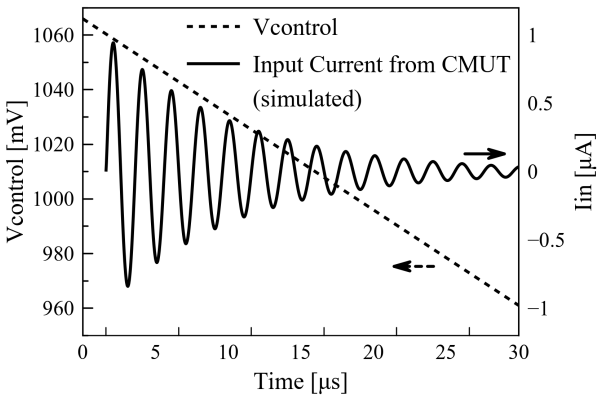
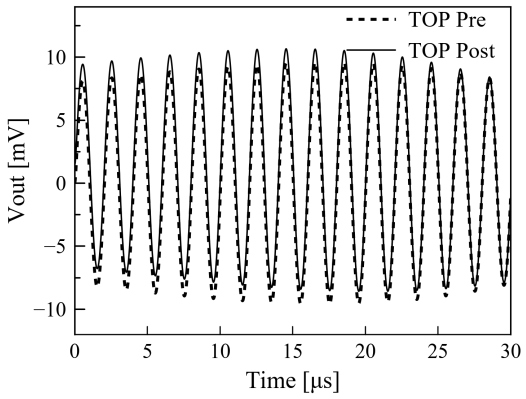


Figure 4.7.: Post-layout total current consumption and bandwidth over a complete gain range of the top level circuit.



(a)

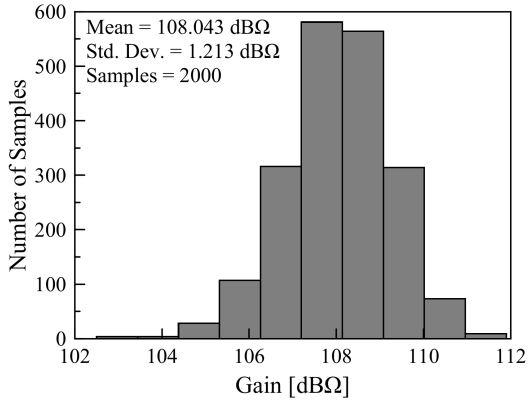


(b)

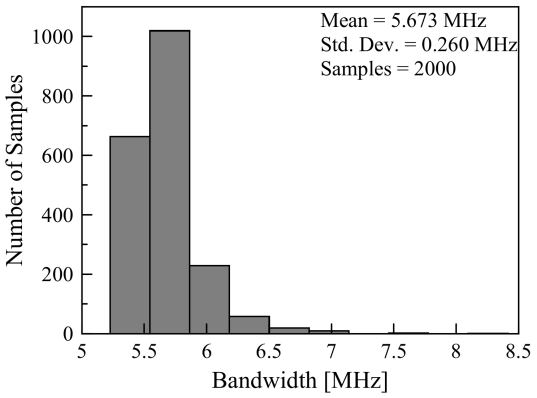
Figure 4.8.: Pre- and post-layout transient simulation results of the top level circuit with 500 KHz sine wave input: (a) Input current from CMUT (simulated) and gain control voltage (b) Output voltage.

Corner	Current	Noise_@MaxGain	Noise_@MinGain	Bandwidth	Gain@10KHz	Gain Range
Unit	mA	pA/ $\sqrt{Hz}$	pA/ $\sqrt{Hz}$	MHz	dBΩ	dBΩ
tm	2.780	4.366	93.36	5.263	108.3	30.30
wo	2.780	4.307	92.26	5.441	108.2	30.28
wp	2.971	4.505	99.96	5.803	106.8	30.14
ws	2.618	4.420	91.30	4.788*	109.2	30.27
wz	2.780	4.440	94.72	5.087	108.4	30.31

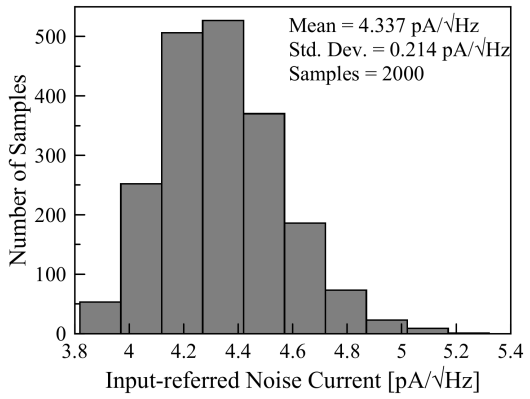
Table 4.1.: Summary of post-layout corner simulation of the top level circuit at 27 °C. Noise simulation was done at 5 MHz. * lower than the target value.



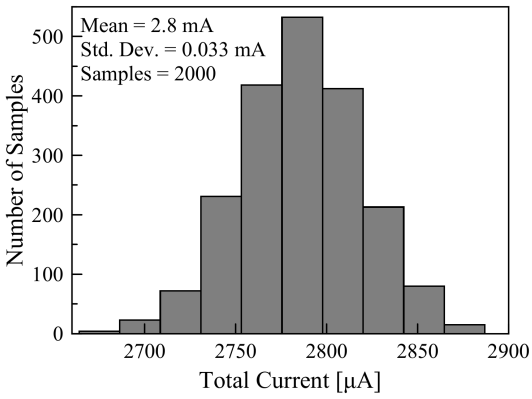
(a) Gain



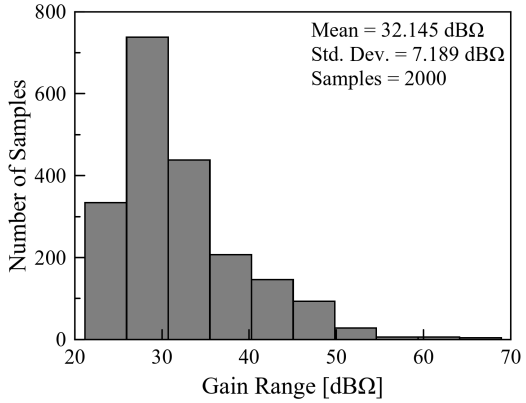
(b) Bandwidth



(c) Input-referred noise current



(d) Total current consumption



(e) Gain range

Figure 4.9.: Pre-layout monte carlo simulation of the top level circuit at 27 °C.

4.1. Possible Improvement

- Improve the driving capacity of the post amplifier. Using symmetrical OTA to drive 5 pF load capacitance is not possible with the power budget given in this work.
- Improve the bandwidth of the symmetrical OTA by allowing more current flowing through M4 and M6. This will reduce the output resistance at the output node. This suggestion is intended to give more margin for corners tm, ws, and wz during post-layout simulation of symmetrical OTA.
- Use PMOS input on the symmetrical OTA. During the design of symmetrical OTA, it was a little bit difficult to increase the second pole frequency due to low transit frequency f_T of M5. This can be improved by using PMOS as input transistor. This is also related with the previous suggestion, i.e., to improve simulation results of corners tm, ws, and wz during post-layout simulation of symmetrical OTA.
- Use PMOS input also for TIA and folded Gilbert Cell. The reason NMOS input transistors were used at symmetrical OTA is related with its input common-mode range. This can be traced back to the design of the folded Gilbert Cell or even the TIA.
- Use other topology than BJT based or even exponential device based to realize exponential voltage generator because exponential device based circuit have strong dependency on temperature. This depends also on the block diagram used to realize the whole system though.
- Complete the system to be a closed-loop system. This way, the system becomes fully automatic.

5. Conclusion

The design and layout of the Time Gain Compensation (TGC) Amplifier using 0.18 μm Silicon on Insulator (SOI) process technology from X-FAB have been done. The circuit fulfills all the specifications at simulated at process corners at room temperature except at corner ws. The main step taken to realize the circuit is assigning each feature into a circuit. A regulated cascode transimpedance amplifier provides the low input impedance needed to amplify the input current signals to voltage output from the high impedance ultrasound transducer in the receive mode. The gain variation needed to compensate the attenuated echoes is taken care of by the folded Gilbert cell. In order to realize linear-in-dB feature, an exponential voltage generator is used to generate exponential control from a linear input ramping voltage. At the end of the chain, a post amplifier is used to compensate the attenuation from folded Gilbert cell. The comparison with other similar works is shown in Table 5.1. In general, other works are chosen based on the close similarities on specification and application.

Parameter	Unit	Target	This work	[3]	[40]	[41]
Gain Range	dBΩ	≥ 30	30	33	18	36
Maximum Gain	dBΩ	≥ 106	108	107	97	41.6
Gain Error	dBΩ	-	± 2	± 1	-	-
Gain Control Type	-	-	Analog	Analog	Discrete	Discrete
Control Voltage Range	mV	-	100	800	-	0.5
Gain Varying Type	-	-	a	c	b	b
3dB Bandwidth	MHz	≥ 5	5	7	7.5	10-25
Input-referred Noise Current at 5 MHz	pA/$\sqrt{Hz}$	≤ 5	4.5-99	1.7	4.8	-
Transducer Capacitance	pF	10	10	15	5.5	-
Load Capacitance	pF	5	2	-	-	-
Power Consumption	mW	≤ 6	5.2	5.2	0.18	3.6
Area	μm^2	-	210×141	400×400	76×50	320000
Process Technology	-	0.18 μm SOI	0.18 μm SOI	0.18 μm HV BCDMOS	65 nm	0.18 μm

Table 5.1.: Performance comparison with other similar works. a = varying current bias, b = Varying feedback impedance, c = Interpolation.

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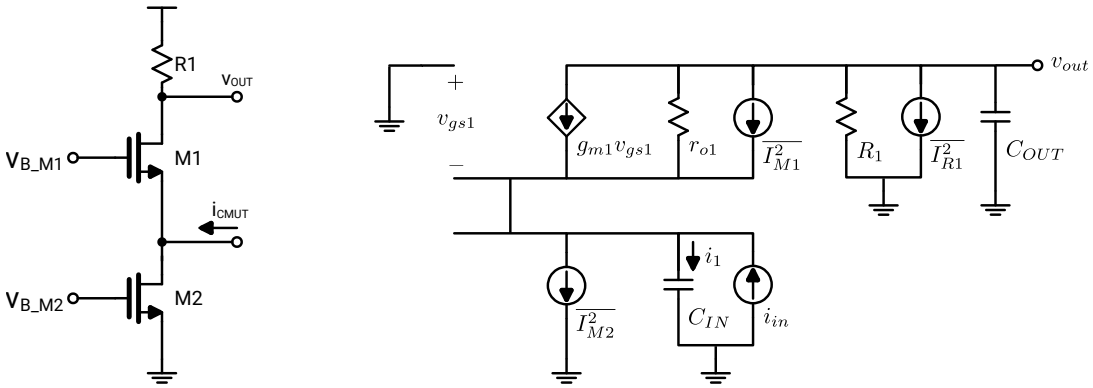
A. Transfer Function and Noise Equations

A.1. Common Gate



(a) Common gate amplifier

(b) Common gate small signal equivalent circuit

Figure A.1.: The common gate topology and its small signal equivalent circuit.

Transfer Function

From observation:

$$v_{s1} = \frac{1}{sC_{IN}} i_1 \tag{A.1}$$

$$v_{out} = \left(R_1 \| \frac{1}{sC_{OUT}}\right)(i_{in} - i_1) \rightarrow i_1 = i_{in} - \frac{v_{out}}{R_1/(sC_{OUT}R_1 + 1)} \tag{A.2}$$

$$(v_{s1} - v_{out}) = (i_{in} - i_1 + g_{m1}v_{gs1})r_{o1} \tag{A.3}$$

$$v_{gs1} = \left(0 - \frac{1}{sC_{IN}} i_1\right) \tag{A.4}$$

Solve for v_{out}/i_{in} by eliminating v_{s1}, v_{gs1}, i_1.
Two checkpoints are written here:

$$\frac{1}{sC_{OUT}}i_1 - v_{out} = \left[i_{in} - \left(i_{in} - \frac{v_{out}}{R_1/(sC_{OUT}R_1+1)}\right) + g_{m1}\left(-\frac{1}{sC_{IN}}i_1\right)\right] r_{o1} \tag{A.5}$$

$$v_{out}\left(1 + \frac{(sC_{OUT}R_1+1)r_{o1}}{R_1}\right) = \left(\frac{1}{sC_{IN}} + g_{m1}\frac{1}{sC_{IN}}r_{o1}\right)\left(i_{in} - \frac{v_{out}}{R_1/(sC_{OUT}R_{1D}+1)}\right) \tag{A.6}$$

At the end, we get:

$$\frac{v_{out}}{i_{in}} = \frac{(1+g_{m1}r_{o1})R_1}{sC_{IN}R_1 + [(sC_{OUT}R_1+1)(sC_{IN}r_{o1}+g_{m1}r_{o1}+1)]} \tag{A.7}$$

By assuming

$$R_1 r_{o1} \approx R_1(r_{o1}+R_1)$$

for

$$r_{o1} >> R_1$$

The denumerator of equation (A.7) originally can be written fully as follow:

$$s^2C_{OUT}R_1C_{IN}r_{o1} + s(C_{IN}R_1 + C_{IN}r_{o1} + C_{OUT}R_1g_{m1}r_{o1} + C_{OUT}R_1) + (g_{m1}r_{o1}+1)$$

By using the assumption mentioned above, the denominator of equation (A.7) becomes:

$$s^2C_{OUT}R_1C_{IN}(r_{o1}+R_1) + s(C_{IN}R_1 + C_{IN}r_{o1} + C_{OUT}R_1g_{m1}r_{o1} + C_{OUT}R_1) + (g_{m1}r_{o1}+1)$$

only then can it be factored as:

$$(sC_{OUT}R_1+1)\left[sC_{IN}(r_{o1}+R_1) + g_{m1}r_{o1} + 1\right]$$

The transfer function becomes:

$$\frac{v_{out}}{i_{in}} = \frac{(1+g_{m1}r_{o1})R_1}{(sC_{OUT}R_1+1)\left[sC_{IN}(r_{o1}+R_1) + g_{m1}r_{o1} + 1\right]} \tag{A.8}$$

Input-referred Noise Current

It is assumed that the input pole is the dominant pole. By using the dominant pole only, the magnitude of the transfer function can be written as:

$$\left|\frac{v_{out}}{i_{in}}\right|^2 = \frac{(1+g_{m1}r_{o1})^2R_1^2}{(\omega C_{IN}(r_{o1}+R_1))^2+(g_{m1}r_{o1}+1)^2} \tag{A.9}$$

$$\approx \frac{(1+g_{m1}r_{o1})^2R_1^2}{(\omega C_{IN}(r_{o1}+R_1))^2+(g_{m1}r_{o1})^2+1} \tag{A.10}$$

Now noise contribution from each component can be calculated.
Resistor R_1

$$\overline{I_{n,in,R_1}^2} = \frac{\frac{4k_BT}{R_1}R_1^2}{\frac{(1+g_{m1}r_{o1})^2R_1^2}{(\omega C_{IN}(r_{o1}+R_1))^2+(g_{m1}r_{o1}+1)^2}} \tag{A.11}$$

$$= 4k_BT\frac{(2\pi f C_{IN}(r_{o1}+R_1))^2+(g_{m1}r_{o1}+1)^2}{(1+g_{m1}r_{o1})^2}\frac{1}{R_1} \tag{A.12}$$

$$\overline{I_{n,in,R_1}^2} \approx 4k_BT\frac{(2\pi f C_{IN}r_{o1})^2+(g_{m1}r_{o1})^2+1}{(1+g_{m1}r_{o1})^2}\frac{1}{R_1} \tag{A.13}$$

Transistor M1
For this device, refer the noise current to the series voltage source at the gate using the parameter B from ABCD parameter, find the equivalent output voltage, and then referred back to the input using the transfer function.

$$\overline{I_{n,in,M1}^2} = \overline{I_{n,M1}^2}(\frac{1}{g_{m1}})^2(g_{m1}R_1)^2\frac{(\omega C_{IN}(r_{o1}+R_1))^2+(g_{m1}r_{o1})^2+1}{(1+g_{m1}r_{o1})^2R_1^2} \tag{A.14}$$

$$= \overline{I_{n,M1}^2}\frac{(\omega C_{IN}(r_{o1}+R_1))^2+(g_{m1}r_{o1})^2+1}{(1+g_{m1}r_{o1})^2} \tag{A.15}$$

$$\overline{I_{n,in,M1}^2} \approx 4k_BT\gamma_n g_{m1}\frac{(2\pi f C_{IN}r_{o1})^2}{(1+g_{m1}r_{o1})^2} \tag{A.16}$$

Transistor M2

$$\overline{I_{n,in,M2}^2} = \overline{I_{n,M2}^2} = 4k_B T\gamma_n g_{m2} \tag{A.17}$$

The total input-referred noise current becomes

$$\overline{I_{n,in}^2} = \overline{I_{n,in,R_1}^2} + \overline{I_{n,in,M1}^2} + \overline{I_{n,in,M2}^2} \tag{A.18}$$

$$\begin{aligned}\overline{I_{n,in}^2} = 4k_B T \Bigg[& \frac{(2\pi f C_{IN} r_{o1})^2 + (g_{m1} r_{o1})^2 + 1}{(1 + g_{m1} r_{o1})^2} \frac{1}{R_1} \\ & + g_{m2}\gamma_n \\ & + \frac{(2\pi f C_{IN} r_{o1})^2}{(1 + g_{m1} r_{o1})^2} g_{m1}\gamma_n \Bigg]\end{aligned} \tag{A.19}$$

A.2. Regulated Cascode

Transfer Function

From observation:

$$v_{g1} = -g_{m2} v_{gs2} (r_{o2} || R_2) \tag{A.20}$$

$$v_{s1} = \frac{1}{sC_{IN}} i_1 = v_{gs2} \tag{A.21}$$

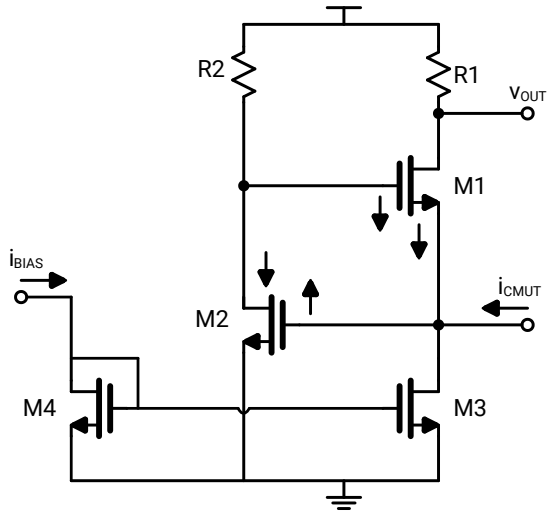
$$v_{out} = (R_1 || \frac{1}{sC_{OUT}})(i_{in} - i_1) \rightarrow i_1 = i_{in} - \frac{v_{out}}{R_1/(sC_{OUT}R_1 + 1)} \tag{A.22}$$

$$-(v_{out} - v_{s1}) = (g_{m1} v_{gs1} + i_{in} - i_1) r_{o1} \tag{A.23}$$

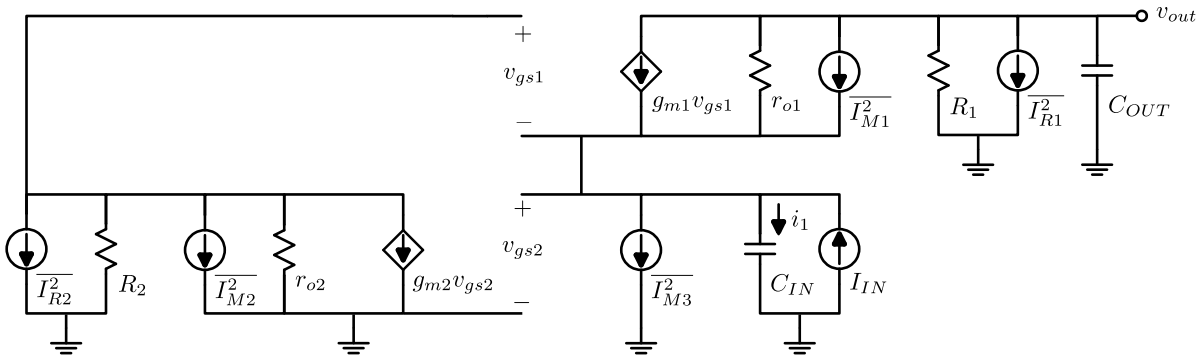
Solve for v_{out}/i_{in} by eliminating $v_{s1}, v_{gs1}, v_{gs2}, i_1$.
Some checkpoints

$$\frac{1}{sC_{IN}} i_1 + \frac{1}{sC_{IN}} g_{m1} r_{o1} i_1 + r_{o1} i_1 + g_{m1} r_{o1} g_{m2} (r_{o2} || R_2) \frac{1}{sC_{IN}} i_1 = v_{out} + i_{in} r_{o1} \tag{A.24}$$

$$\begin{aligned}(\frac{1}{sC_{IN}} + \frac{1}{sC_{IN}} g_{m1} r_{o1} + \frac{1}{sC_{IN}} g_{m1} r_{o1} g_{m2} (r_{o2} || R_2)) i_{in} = \\ (\frac{1}{sC_{IN}} + \frac{1}{sC_{IN}} g_{m1} r_{o1} + \frac{1}{sC_{IN}} g_{m1} r_{o1} g_{m2} (r_{o2} || R_2)) \frac{v_{out}}{R_1/sC_{OUT}R_1 + 1} + v_{out}\end{aligned} \tag{A.25}$$



(a) regulated cascode topology



(b) regulated cascode small signal equivalent circuit

Figure A.2.: The picture shows the regulated cascode topology. It is an improvement from common gate topology.

$$(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2))R_1 i_{in} = (1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) + sC_{IN}r_{o1})(sC_{OUT}R_1 + 1)v_{out} + sC_{IN}R_1 v_{out} \tag{A.26}$$

At the end, we get:

$$\frac{v_{out}}{i_{in}} = \frac{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2))R_1}{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) + sC_{IN}r_{o1})(sC_{OUT}R_1 + 1) + sC_{IN}R_1} \tag{A.27}$$

By assuming

$$R_1 r_{o1} \approx R_1(r_{o1} + R_1)$$

for

$$r_{o1} >> R_1$$

$$(A + sC_{IN}r_{01})(sC_{OUT}R_1) + (A + sC_{IN}r_{01}) + sC_{IN}R_1$$

with

$$A = 1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2)$$

By using that assumption, the denumerator of equation (A.27) can be written as follow:

$$(A + sC_{IN}(r_{01} + R_1))(sC_{OUT}R_1) + (A + sC_{IN}(r_{01} + R_1))$$

and then

$$(A + sC_{IN}(r_{01} + R_1))(sC_{OUT}R_1) + 1)$$

The transfer function then can be written as:

$$\frac{v_{out}}{i_{in}} = \frac{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2))R_1}{(1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) + sC_{IN}(r_{o1} + R_1))(sC_{OUT}R_1 + 1)} \tag{A.28}$$

Instead of assuming the input pole is the dominant pole like in the common gate discussion, the complete transfer function is used to form the input-referred noise current. One can find the denominator of the magnitude of the transfer function as follow:

$$\begin{aligned} &[\omega^2(r_{o1} + R_1)C_{IN}R_1C_{OUT}]^2 + \omega^2((r_{o1} + R_1)^2C_{IN}^2 + C_{OUT}^2R_1^2A^2) + A^2 \\ &\text{with} \\ &A = 1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) \end{aligned} \tag{A.29}$$

One then can find the magnitude of the transfer function as follow:

$$\left|\frac{v_{out}}{i_{in}}\right|^2 = \frac{A^2R_1^2}{[\omega^2(r_{o1} + R_1)C_{IN}R_1C_{OUT}]^2 + \omega^2((r_{o1} + R_1)^2C_{IN}^2 + C_{OUT}^2R_1^2A^2) + A^2} \quad \text{with} \tag{A.30}$$

$$A = 1 + g_{m1}r_{o1} + g_{m1}r_{o1}g_{m2}(r_{o2}||R_2) \tag{A.31}$$

Input-referred Noise Current

The noise contributions from each device are summarized below.
Resistor R_1

$$\overline{I^2_{n,in,R_1}} = 4k_BTR_1 \left|\frac{i_{in}}{v_{out}}\right|^2 \tag{A.32}$$

Transistor M1

$$\overline{I^2_{n,in,M1}} = \overline{I^2_{n,M1}} \left(-\frac{1}{g_{m1}}\right)^2 (-g_{m1}R_1)^2 \left|\frac{i_{in}}{v_{out}}\right|^2 \tag{A.33}$$

$$= 4k_BT\gamma_n g_{m1} R_1^2 \left|\frac{i_{in}}{v_{out}}\right|^2 \tag{A.34}$$

Transistor M3

$$\overline{I^2_{n,in,M3}} = \overline{I^2_{n,M3}} = 4k_BT\gamma_n g_{m3} \tag{A.35}$$

Transistor M2 and Resistor R_2

$$\overline{I^2_{n,in,M2}} + \overline{I^2_{n,in,R_2}} = (\overline{I^2_{n,M2}} + \overline{I^2_{n,R_2}})(R_2||r_{o2})^2 (-g_{m1}R_1)^2 \left|\frac{i_{in}}{v_{out}}\right|^2 \tag{A.36}$$

$$= (\frac{4k_BT}{R_2} + 4k_BT\gamma_n g_{m2})(R_2||r_{o2})^2 (-g_{m1}R_1)^2 \left|\frac{i_{in}}{v_{out}}\right|^2 \tag{A.37}$$

Then the total noise is as follow:

$$\overline{I^2_{n,in}} = \overline{I^2_{n,in,R_1}} + \overline{I^2_{n,in,M1}} + \overline{I^2_{n,in,M3}} + \overline{I^2_{n,in,M2}} + \overline{I^2_{n,in,R_2}} \tag{A.38}$$

$$\overline{I_{n,in}^2} = 4k_BT\left[R_1\left|\frac{i_{in}}{v_{out}}\right|^2 + \gamma_n g_{m1}R_1^2\left|\frac{i_{in}}{v_{out}}\right|^2 + \gamma_n g_{m3} + (\frac{1}{R_2} + \gamma_n g_{m2})(R_2||r_{o2})^2\left(g_{m1}R_1\right)^2\left|\frac{i_{in}}{v_{out}}\right|^2\right]$$

with

$$\left|\frac{i_{in}}{v_{out}}\right|^2 = \frac{[\omega^2(r_{o1}+R_1)C_{IN}R_1C_{OUT}]^2 + \omega^2((r_{o1}+R_1)^2C_{IN}^2 + C_{OUT}^2R_1^2A^2) + A^2}{A^2R_1^2} \quad \text{(A.39)}$$

and A is defined as

$$A = 1 + G_m r_{o1}$$

with G_m as

$$G_m = g_{m1} + g_{m1}g_{m2}(r_{o2}||R_2)$$

B. Scripts

(X,Y)=(gm1,gm2)

```
# -*- coding: utf-8 -*-
"""
Created on Mon Nov 30 23:32:45 2020

@author: Budi Mulyanto

https://github.com/winpython/winpython/releases/download/3.0.20201028/
    Winpython64-3.9.0.2cod.exe
"""
#    ================================================================================

# This script generate input-refered noise current, gain,
# input pole frequency of the regulated cascode.
# (X,Y) = (gm1, gm2)
# The script will plot only input-refered noise current to make it short.
# But the function for gain and input pole frequency are already defined.

import pandas
import numpy
import matplotlib
import matplotlib.pyplot as plt
from mpl_toolkits.mplot3d import axes3d # <--- This is important for 3d
    plotting
from matplotlib.ticker import FormatStrFormatter
from matplotlib import cm
#    ================================================================================

# from matplotlib import ticker
# niceMathTextForm = ticker.ScalarFormatter(useMathText=True)
#    ================================================================================


#%matplotlib qt       # when you want graphs in a separate window and
#%matplotlib inline   # when you want an inline plot
#    ================================================================================

# Read the extracted data from Cadence
NMOS_gm_gmid = pandas.read_csv('NMOS_gm_gmid.csv', sep=',' , encoding='UTF
    -8')
NMOS_gm_gmid = NMOS_gm_gmid.apply(pandas.to_numeric, errors='coerce')
NMOS_ro_gmid = pandas.read_csv('NMOS_ro_gmid.csv', sep=',' , encoding='UTF
    -8')
NMOS_ro_gmid = NMOS_ro_gmid.apply(pandas.to_numeric, errors='coerce')

n=800
m=1800
s=100

gm1_ = NMOS_gm_gmid.iloc[n:n+m:s,7]
ro1_ = NMOS_ro_gmid.iloc[n:n+m:s,9]
```

```
gm2_ = NMOS_gm_gmid.iloc[n:n+m:s,7]
ro2_ = NMOS_ro_gmid.iloc[n:n+m:s,9]

#
    ================================================================================#=

# Your constants and variable definitions

gm1,gm2 = numpy.meshgrid(gm1_,gm2_)
ro1 = ro1_
ro2 = ro2_
ro1 = ro1.to_numpy() # cast dataframe column into array
ro2 = ro2.to_numpy()
ro2 = numpy.transpose([ro2_]) # transpose 1D array

gmnB = 050e-6 #actually not used
gm3 = 038e-6
R1 = 10000 #define your DC gain
R2 = 15000 #the R above M2
C_CMUT = 10e-12
C_OUT = 2e-12
freq = 5e6
gamman = 2/3

#
    ================================================================================

# Functions Definitions
def noise(gm1, gm2, ro1, ro2,
          gmnB, R1, R2, C_CMUT, C_OUT,
          freq, gamman):
    """
    Noise calculation
    """
    Gm = gm1*gm2*(ro2*R2/(ro2+R2)) + gm1
    A    = (Gm*ro1) + 1
    DN1  = ((2*numpy.pi*freq)**2*(R1+ro1)*C_CMUT*R1*C_OUT)**2
    DN2  = (2*numpy.pi*freq)**2*(((R1+ro1)*C_CMUT)**2 + (R1*C_OUT*A)**2)
    DN3  = A**2
    N1   = A**2 * R1**2
    imTF2  = (DN1+DN2+DN3)/(N1) #inverse magnitude transfer function
   square

    NR1 = R1*imTF2
    NM1 = (gamman*gm1*R1**2)*imTF2
    NM3 = (gamman*gm3)
    NM2 = (gamman*gm2)*(gm1*R1*(R2*ro2/(R2+ro2)))**2*imTF2
    NR2 = (1/R2)*(gm1*R1*(R2*ro2/(R2+ro2)))**2*imTF2
    N_total = NR1+NM1+NM3+NM2+NR2
    noise  = numpy.sqrt((N_total)*1.66e-20)
    print("noise = \n",noise)
    return(noise)

def noise_cg(gm1, gm2, ro1, ro2,
          gmnB, R1, R2, C_CMUT,
          freq, gamman):
    """
    Noise calculation
    """
    A  = ((2*numpy.pi*freq*C_CMUT*ro1)**2 + (gm1*ro1)**2 + 1) / (R1*(1 +
   gm1*ro1)**2)
    B  = (2*numpy.pi*freq*C_CMUT*ro1)**2 / (1 + gm1*ro1)**2 * (gm1*gamman)
    C  = gmnB*gamman
    noise  = numpy.sqrt((A+B+C)*1.66e-20)
    #print("noise = \n",noise)
    return(noise)

def gain(gm1, gm2, ro1, ro2,
          gmnB, R1, R2, C_CMUT, Cout,
          freq, gamman):
```

```
    """
    Gain calculation
    """
    Gm = gm1*gm2*(ro2*R2/(ro2+R2)) + gm1
    A  = (Gm*ro1 + 1)*R1
    B  = (2*numpy.pi*freq*Cout*R1) + 1
    C  = 2*numpy.pi*freq*(ro1+R1)*C_CMUT + Gm*ro1 + 1
    gain = A/(B*C)
    return(gain)

def pole_input(gm1, gm2, ro1, ro2,
          gmnB, R1, R2, C_CMUT, Cout,
          freq, gamman):
    """
    input pole frequency calculation
    input pole is the non dominant pole
    """
    Gm = gm1*gm2*(ro2*R2/(ro2+R2)) + gm1
    A  = Gm*ro1 + 1
    B  = 2*numpy.pi*(ro1+R1)*C_CMUT
    freq = A/B
    return(freq)

#def plot_noise1()
#   ================================================================================

# Noise calculation
# Varying gm1, gm2
z  = noise(gm1, gm2, ro1, ro2,
              gmnB, R1, R2, C_CMUT, C_OUT,
              freq, gamman) * 1e12

freq_title = freq/1e6

fig = plt.figure()
ax = plt.axes(projection='3d')
norm = plt.Normalize(z.min(), z.max())
colors = cm.coolwarm(norm(z))

gm1_x = gm1*1e6
gm2_y = gm2*1e6
surf = ax.plot_surface(gm1_x,gm2_y,z, rstride=1,cstride=1,alpha=0,
   linewidth=1,edgecolors='black')
surf.set_facecolor((0,0,0,0))
ax.grid(False)
ax.xaxis.pane.set_edgecolor('black')
ax.yaxis.pane.set_edgecolor('black')
ax.xaxis._axinfo['tick']['inward_factor'] = 0
ax.xaxis._axinfo['tick']['outward_factor'] = 0.4
ax.yaxis._axinfo['tick']['inward_factor'] = 0
ax.yaxis._axinfo['tick']['outward_factor'] = 0.4
ax.zaxis._axinfo['tick']['inward_factor'] = 0
ax.zaxis._axinfo['tick']['outward_factor'] = 0.4
ax.xaxis.pane.fill = False
ax.yaxis.pane.fill = False
ax.zaxis.pane.fill = False
ax.view_init(elev=30, azim=145)
ax.set_xlabel('M1 $\ g_{m} $ [$\\mu$A/V]')
ax.set_ylabel('M2 $\ g_{m} $ [$\\mu$A/V]')
ax.set_zlabel('$\ \overline{I^2_{n,in}} $ [pA/$\sqrt{Hz}$]')
mapc1 = ax.contour(gm1_x,gm2_y,z, zdir='z', levels=[6], offset=z.min(),
   colors='black', linestyles=('--',))
#mapc1 = ax.contour(gm1_x,gm2_y,z, zdir='z', levels=[5], offset=z.min(),
   colors='black', linestyles=('dashdot',))
ax.clabel(mapc1, inline=True, fontsize=10)
plt.savefig('Input-referred_Noise_Current.pdf', bbox_inches='tight')
```

Listing B.1: gmid.py

(X,Y)=(gm1,R2)

```
# -*- coding: utf-8 -*-
"""
Created on Mon Nov 30 23:32:45 2020

@author: Budi Mulyanto

https://github.com/winpython/winpython/releases/download/3.0.20201028/
    Winpython64-3.9.0.2cod.exe
"""
#
    ================================================================================

# This script generate input-refered noise current of the regulated
    cascode.
# (X,Y) = (gm1, R2)
import pandas
import numpy
import matplotlib
import matplotlib.pyplot as plt
from mpl_toolkits.mplot3d import axes3d # <--- This is important for 3d
    plotting
from matplotlib.ticker import FormatStrFormatter
from matplotlib import cm
#
    ================================================================================

# from matplotlib import ticker
# niceMathTextForm = ticker.ScalarFormatter(useMathText=True)
#
    ================================================================================

#%matplotlib qt       # when you want graphs in a separate window and
#%matplotlib inline   # when you want an inline plot
#
    ================================================================================

# Read the extracted data from Cadence
NMOS_gm_gmid = pandas.read_csv('NMOS_gm_gmid.csv', sep=',' , encoding='UTF
    -8')
NMOS_gm_gmid = NMOS_gm_gmid.apply(pandas.to_numeric, errors='coerce')
NMOS_ro_gmid = pandas.read_csv('NMOS_ro_gmid.csv', sep=',' , encoding='UTF
    -8')
NMOS_ro_gmid = NMOS_ro_gmid.apply(pandas.to_numeric, errors='coerce')

n=800
m=1800
s=100

gm1_ = NMOS_gm_gmid.iloc[n:n+m:s,7]
ro1_ = NMOS_ro_gmid.iloc[n:n+m:s,9]
gm2_ = NMOS_gm_gmid.iloc[n:n+m:s,7]
ro2_ = NMOS_ro_gmid.iloc[n:n+m:s,9]

R2_ = numpy.linspace(1000,20000,11)

#
    ================================================================================

# Your constants and variable definitions
R2,gm2 = numpy.meshgrid(R2_,gm2_)
ro1 = ro1_
ro2 = ro2_
ro1 = ro1.to_numpy() # cast dataframe column into array
ro2 = ro2.to_numpy()
ro2 = numpy.transpose([ro2_]) # transpose 1D array

gmnB = 050e-6
gm3 = 050e-6
gm1 = 150e-6
```

```
R1 = 10000 #define your DC gain
#R2 = 11000 #the R above M_CS
C_CMUT = 10e-12
C_OUT = 2e-12
freq = 5e6
gamman = 2/3
#
   ================================================================================

# Functions Definitions
def noise(gm1, gm2, ro1, ro2,
          gmnB, R1, R2, C_CMUT, C_OUT,
          freq, gamman):
    """
    Noise calculation
    """
    Gm = gm1*gm2*(ro2*R2/(ro2+R2)) + gm1
    A    = (Gm*ro1) + 1
    DN1  = ((2*numpy.pi*freq)**2*(R1+ro1)*C_CMUT*R1*C_OUT)**2
    DN2  = (2*numpy.pi*freq)**2*(((R1+ro1)*C_CMUT)**2 + (R1*C_OUT*A)**2)
    DN3  = A**2
    N1   = A**2 * R1**2
    imTF2  = (DN1+DN2+DN3)/(N1) #inverse magnitude transfer function
   square

    NR1 = R1*imTF2
    NM1 = (gamman*gm1*R1**2)*imTF2
    NM3 = (gamman*gm3)
    NM2 = (gamman*gm2)*(gm1*R1*(R2*ro2/(R2+ro2)))**2*imTF2
    NR2 = (1/R2)*(gm1*R1*(R2*ro2/(R2+ro2)))**2*imTF2
    N_total = NR1+NM1+NM3+NM2+NR2
    #noise  = numpy.sqrt(1/imTF2)
    noise  = numpy.sqrt((N_total)*1.66e-20)
    #noise  = numpy.sqrt((NR1+NM1+NM3+NM2+NR2)*1.66e-20)
    print("noise = \n",noise)
    return(noise)

#
   ================================================================================

# Noise calculation
# Varying R2, gm2
z  = noise(gm1, gm2, ro1, ro2,
          gmnB, R1, R2, C_CMUT, C_OUT,
          freq, gamman)* 1e12

freq_title = freq/1e6

fig = plt.figure()
ax = plt.axes(projection='3d')
norm = plt.Normalize(z.min(), z.max())
colors = cm.coolwarm(norm(z))

x_axis = R2 /1000
y_axis = gm2*1e6
surf = ax.plot_surface(x_axis,y_axis,z, rstride=1,cstride=1,alpha=0,
   linewidth=1,edgecolors='black')
surf.set_facecolor((0,0,0,0))
ax.grid(False)
ax.xaxis.pane.set_edgecolor('black')
ax.yaxis.pane.set_edgecolor('black')
ax.xaxis._axinfo['tick']['inward_factor'] = 0
ax.xaxis._axinfo['tick']['outward_factor'] = 0.4
ax.yaxis._axinfo['tick']['inward_factor'] = 0
ax.yaxis._axinfo['tick']['outward_factor'] = 0.4
ax.zaxis._axinfo['tick']['inward_factor'] = 0
ax.zaxis._axinfo['tick']['outward_factor'] = 0.4
ax.xaxis.pane.fill = False
ax.yaxis.pane.fill = False
```

```
ax.zaxis.pane.fill = False
ax.view_init(elev=30, azim=120)
ax.set_xlabel('R2 [K$\\Omega$]')
ax.set_ylabel('M2 $\ g_{m} $ [$\\mu$A/V]')
ax.zaxis.set_rotate_label(False)
ax.set_zlabel('$\ \overline{I^2_{n,in}} $ [pA/$\sqrt{Hz}$]', rotation=90)
mapc1 = ax.contour(x_axis,y_axis,z, zdir='z', levels=[6], offset=z.min(),
    colors='black', linestyles=('--',))
mapc1 = ax.contour(x_axis,y_axis,z, zdir='z', levels=[5], offset=z.min(),
    colors='black', linestyles=('dashdot',))
plt.savefig('Input-referred_Noise_Current_R2.pdf', bbox_inches='tight')
```

Listing B.2: gmid_R2.py