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TECHNOLOGICAL VIABILITY AND PROOF-OF-CONCEPT OF APPLYING LOW-TEMPERATURE PECVD SIN_X FOR INKJET-MASKED SELECTIVE EMITTERS

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ABSTRACT: One of the major barriers for the adoption of selective emitter technology is the trade-off between optimal shielding of minority carriers and increased recombination due to the laser-induced damage. One method to form defect-free self-aligned selective emitters is to use innovative inkjet materials within adapted PERC-processes, like the PECVD of silicon nitride Herein, we utilize a novel UV-Polymer ink as mask in selective etching processes for patterning silicon and, in addition, in a thermally triggered lift-off process for patterning silicon nitride, prior to a self-aligned plating step. To address the thermal stability of the UV-Polymer inks during PECVD, the deposition process needs to be developed at low temperatures. In this work, we first investigate the maximum thermal budget that can be applied on inks during the PECVD passivation process. Based upon this temperature limit, a low temperature PECVD deposition process is developed and both optical and electrical properties of the developed layers are investigated in detail. Deposition at 250°C provided adequate optical properties (n=1.99, k=0.004) and comparable passivation quality to the PERC reference layer. At the same time, 250°C is the process temperature compatible for the innovative UV-Polymer inks investigated in this work.

Keywords: passivation, anti-reflection, PECVD, selective emitter, inkjet printing

1. INTRODUCTION

The passivated emitter and rear cell (PERC) solar cell features the highest market share in industrial production [1]. The losses in the emitter region account for a significant fraction of total recombination losses in such solar cells. For high-efficiency PERC solar cells, selective doping allows diffusion of an emitter with low surface concentration and, thus, low saturation current density between the fingers ($j_{0,pass}$), whereas facilitating a low contact resistivity and low recombination in contact areas. This motivates the optimization of highly and lowly doped regions of the emitter as a necessary step towards the roadmap to reach even higher efficiencies [2]. Furthermore, it also develops an interest towards qualifying alternative technologies and process routes to form selective emitter on PERC solar cells. One source of a high saturation current density in metallized area ($j_{0,met}$) is the use of a selective laser doping process that could leave substantial laser-induced damage on c-Si surface [3]. Therefore, development of a selective emitter route, which avoids any surface damage, is of high interest not only as a relevant approach to form selective emitters for PERC, but also applicable for novel high-efficiency concepts such as TOPCon.

One innovative method to form selective emitters is to use a new typ of ink inkjet on top of highly doped (n^+-type) emitters in order to mask this region during the emitter etch-back process, to perform a thermally triggered lift-off process of low-temperature SiN_x layers, used as antireflection coating (ARC), and plating in order to establish a self-aligned selective emitter technology for PERC. Therefore, the ink has to not only to withstand the emitter etch-back process that aims to form lowly doped regions, but also the thermal conditions of a plasma enhanced chemical vapour deposition (PECVD) process.Due to the elimination of complex alignment procedures and the utilization of copper plating instead of silver, such a PERC process has a high potential in performance and low-cost. . To fetch the potential, several process developments are essential in order to investigate the technological viability of this approach. First, inkjetable and UV curable polymer inks are to be screened and selected on the basis of their stability against the successive cell processing steps.

Figure 1 shows the designated process route for self-aligned PERC processing, for which a low temperature ARC SiN_x is developed in this work. p-type Cz wafers are textured and subjected to a $POCl_3$-based tube diffusion process aiming to form a heavily doped n^+ emitter to reach a low contact resistivity between metal and silicon. After single-sided emitter removal (CEI) on the rear, etching of PSG layer, and cleaning, the rear side of the substrate is passivated by spatial ALD AlO_x, followed by a low-temperature annealing step [4] to out-diffuse the excess hydrogen species in the layer. This is followed by the deposition of a rear-side capping layer (PECVD SiN_x). Afterwards,

inkjet printing of an UV-curable polymer is implemented as a cost-efficient and industrially viable technology to print mask lines covering the front contact areas. The self-aligned selective emitter then is formed by the emitter etch-back process, which allows the formation of lowly doped emitter regions besides the ink. Here, it is crucial for the ink to withstand not only the etch-back process, but most importantly also the PECVD SiN_x deposition process, before lift-off from the substrate prior to the plating process. The integration of individual process steps such as inkjet printing, selective emitter etch-back, PECVD, Lift-off and subsequent plating into a PERC technology is topic of investigation in a parallel paper from R. Efinger et al. at this conference [5]. The main focus here is to develop PECVD SiN_x layers at low deposition temperatures, where the critical temperature limit is set based upon the thermal stability of the inks. In general, low-temperature SiN_x layers are interesting for thermally sensitive technologies and offer a higher degree of flexibility during designing process sequences towards lower production costs. The developed SiN_x layer not only requires good optical properties to be used as ARC, but also needs to offer an excellent emitter passivation.

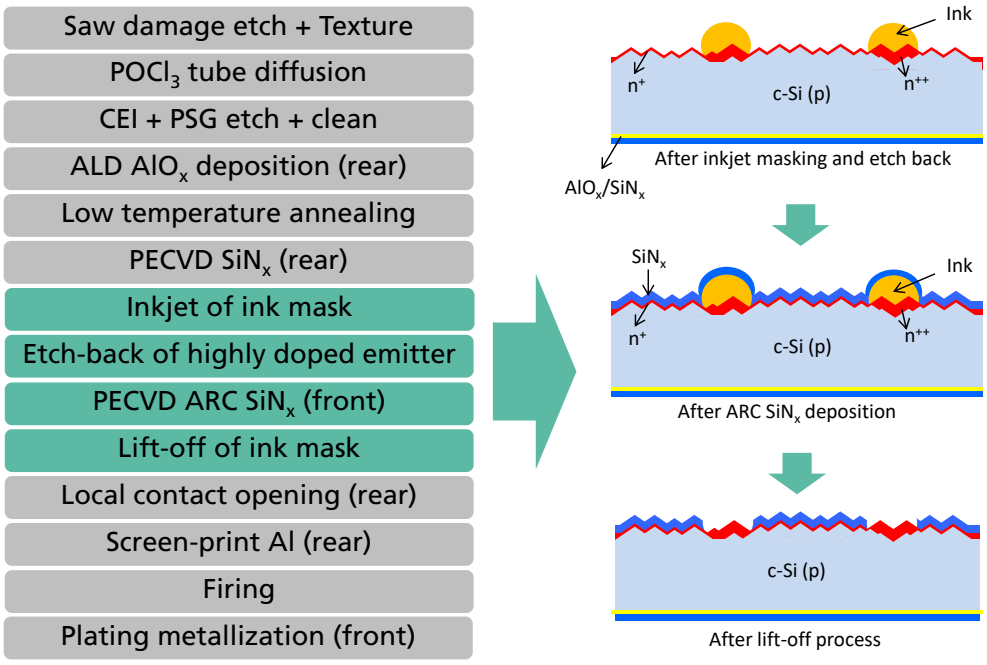

Figure 1: Process route designed for *p*-type PERC solar cells with selective emitter and self-aligned patterning. Additional steps (highlighted in green) require process development and integration into the conventional PERC technology as utilized in the PV-TEC of Fraunhofer ISE.

2. EXPERIMENTAL

After thermal treatment, the change in morphology and aspect ratio of ink masks is estimated using laser confocal microscope, which is able to perform 3D surface profiling. Before deposition of PECVD layers, a thin (d = 1-2 nm) oxide layer is grown on the *c*-Si surface to enhance the surface/emitter passivation. One method used is by applying a low-temperature (T=600°C, N_2) annealing or so called 'outgassing' process in a tube furnace [4], which is typically used to desorb excess H atoms from ALD AlO_x. Meanwhile, to address the thermal stability limit of the UV-polymer-hotmelt ink used in this work, a plasma oxidation process at a low deposition temperature of 200°C is developed in the same PECVD tool, which is used for ARC SiN_x deposition.

The plasma oxidation process uses nitrous oxide (N_2O) as the oxidation source, as is shown to form thin SiO_x layers with high passivation quality when stacked with PECVD dielectric layers [6]. PECVD deposition of ARC SiN_x layers is carried out by using an industrial inline prototype tool from Roth&Rau, whereby a linear source microwave generator is utilized for plasma activation [7]. Symmetrical samples are prepared to measure minority charge carrier lifetimes using transient mode of quasi-steady-state photo-conductance (QSSPC) technique. Implied open-circuit voltage (iV_{OC}) samples are derived from precursor wafers from Solar World that feature an alkaline texture and phosphorous emitter (n^+) on the front- and an intrinsic silicon surface coated with a layer of silicon rich oxynitride (SiO_xN_y) for passivation on the rear-side. Afterwards, the front-side is

passivated using a stack of thin SiO_x and PECVD SiN_x layers as developed in this work. Both for symmetric lifetime samples and iV_{OC} samples, fast-firing is performed using an industrial belt furnace at the peak temperature of 820°C. iV_{OC} values are extracted from QSSPC at 1-sun illumination. Figure 2 shows schematically the sample architecture used for iV_{OC} samples.

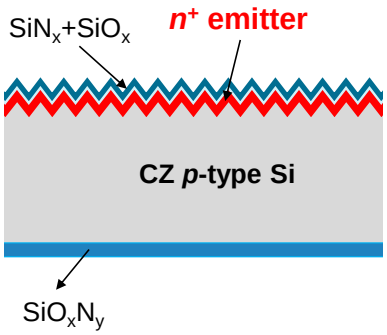

Figure 2: Schematic showing sample architecture used to fabricate implied V_{OC} (iV_{OC}) samples

3. RESULTS

3.1 Thermal stability of ink-masks

Figure 3 plots the maximum height of ink masks just after printing (T_{dep}=25°C) and after passing them through the PECVD-tool without performing any deposition process (no gas flux and no plasma ignition). The process duration was kept to match the thermal budget of typical SiN_x deposition processes. The height of the printed ink is measured by using confocal microscopy. The height of the evaluated polymer inks seem to change dramatically after 250°C, which sets the upper limit for the maximum T_{dep} allowed in the PECVD process.

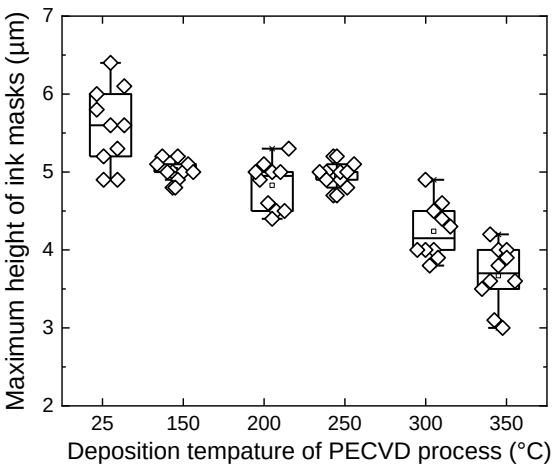

Figure 3: Plot showing a) change in height of ink lines when subjected to various deposition temperature and process times typically used for PECVD SiN_x deposition in a PECVD tool.

3.2 Optical and structural characteristics

Figure 4 plots the dynamic deposition rate of PECVD SiN_x with an increasing T_{dep}. All other process parameters are kept constant. An exponential decay of deposition rate can be observed with increasing deposition temperature.

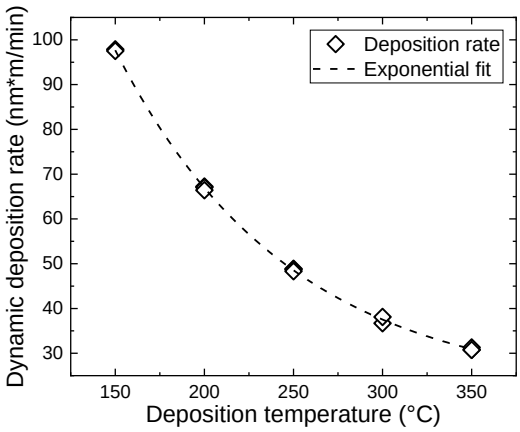

Figure 4: Change in dynamic deposition rate of PECVD SiN_x with an increasing deposition temperature (T_{dep}), whereas keeping all other process parameters constant

Figure 5 plots the thickness-normalized fourier transform infrared spectroscopy (FTIR-) measured absorption spectra of SiN_x layer deposited at different deposition temperatures at deposition rates shown in Figure 4. FTIR spectra show that the layers are not structurally very different at low deposition temperatures with distinct peaks 825 cm^{-1} (Si-N stretching), 1180 cm^{-1} (N-H wagging), 2170 cm^{-1} (Si-H stretching), and 3343 cm^{-1} (N-H stretching) [8,9].

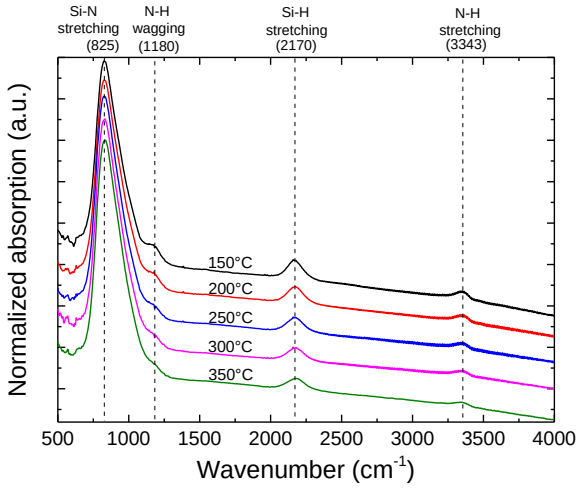

Figure 5: Thickness-normalized FTIR measured spectra of PECVD layers deposited by using different (T_{dep}) with other process parameters being identical, b) estimated total H incorporation in the layer for different T_{dep} values.

In Figure 6, we determine the total H content in the SiN_x layers for different deposition temperatures.

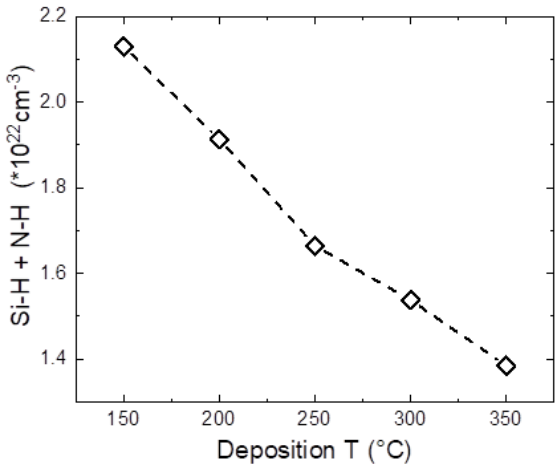

Figure 6: Estimated total H incorporation in the layer for different T_{dep} values based upon FTIR-measured Si-H and N-H bond densities.

The amount of H incorporation in the layers is determined by the combination of the Si-H and N-H bond densities around 2170 cm^{-1} and 3340 cm^{-1}, respectively, by using the method proposed by Lanford and Rand [10]. It can be observed that the degree of [H] incorporation in SiN_x layer is higher at lower PECVD deposition temperatures. This could be attributed to the increase in desorption of hydrogen species from the *c*-Si surface at higher deposition process, which consequently can also lower the deposition rate [11]. Surprisingly, none of the layers show blister formation that is typically considered to be related to a high H concentration in the dielectric layers [12][13]. This could be attributed to a slightly higher porosity of PECVD SiN_x layers deposited at low T_{dep}, which could facilitate effective out-diffusion of H species during the firing process, and hence avoiding accumulation of H species in the SiN_x layer.

3.3 Design of experiments (DOE)

A design of experiments (DOE) is used to perform statistical variation of PECVD process parameters, aiming to find an optimum set of processes at low deposition temperatures, as shown in Table 1.

Table 1: Table showing process parameters varied for design of experiments (DOE). In total, four process parameters are varied with 3 levels. A reduced factorial plan of 3^{4-1} (27) experiments is followed, and each experiment is repeated once.

Process parameters	Unit	Level		
		Low	Mid	High
Temperature	°C	150	250	350
Pressure	mBar	0,15	0,2	0,25
Gas-Ratio	-	2	2,5	3
Total gas flow	sccm	525	725	925

The independent variables are set to be T_{dep} in °C (150, 250, 300), pressure, total gas flux, gas ratio of NH_3 to SiH_4, whereas plasma peak power is kept identical. The output or dependent variables are set to be refractive index (*n*), absorption coefficient (*k*), bond densities (Si-N, Si-H, N-H), and QSSPC-measured minority charge carrier lifetimes. The substrate used is *p*-type, shiny etched FZ wafer of 90 Ω cm base resistivity. The PECVD layers are deposited after cleaning the wafers with hot HNO_3, followed with HF-dip. The H-terminated surfaces are then subjected to the low-temperature oxidation process in tube furnace to grow thin SiO_x layer, before deposition of PECVD layers. An in-depth statistical analysis of the results is performed using statistical tool '*Statistica*', however, a detailed discussion is out of scope of this paper and will be published elsewhere.

Figure 7 plots the refractive index *n* of PECVD SiN_x layers measured for all process parameter combinations vs. the ratio of Si-H/N-H bond densities, grouped according to the deposition temperature.

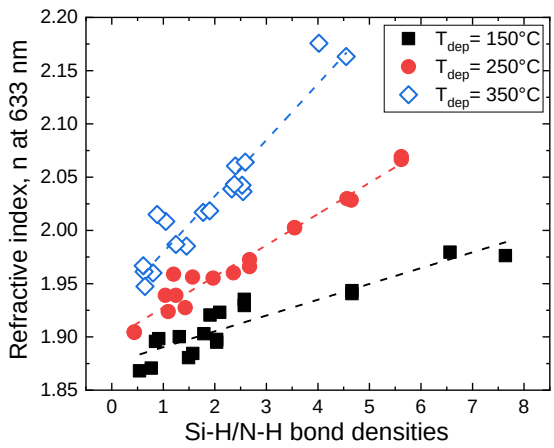

Figure 7: Plot showing the dependence of refractive index (*n*) of PECVD SiN_x layers (as measured by spectroscopic ellipsometry and extracted at 633 nm) on the ratio of FTIR-estimated Si-H and N-H bond densities.

For all investigated deposition temperatures, a higher value of *n* correlates with increasing silicon content in the SiN_x layer. The optical and structural characterization of the layers suggests that

anti-reflective layers with excellent optical properties can also be realized at lower T_{dep} of 150°C and 200°C. No clear trend could be established for the influence of individual process parameters on QSSPC-measured lifetime values. The reason is that the lifetime values are simultaneously influenced by various process parameters, and by their interaction effects. Nevertheless, we plot the lifetime values measured after the firing process against the T_{dep} for all process parameter combinations in Figure 8 a).

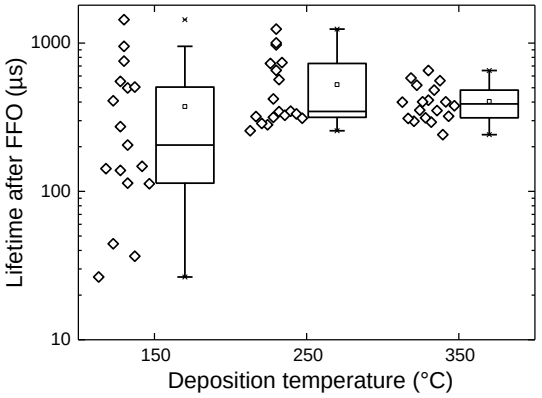

Figure 8: Plot showing the QSSPC-measured effective lifetime of samples symmetrically passivated by a stack of thin 'outgassing' SiO_x and PECVD SiN_x layer, after the fast-firing process.

A high deviation of lifetime values is observed at the lowest T_{dep} of 150°C, which suggests that the change in other process parameters have a very large influence on electrical quality of the layer. Looking closely, it was noticed that at T_{dep} = 150°C, lifetime of majority charge carriers are positively influenced by reduction of the total gas flux, which consequently also lowers the deposition rate. Nevertheless, even at this temperature, high effective lifetime values, similar to higher deposition temperature, are achieved. At T_{dep} = 250°C, lifetime values only show a slightly higher deviation in effective life time than at T_{dep} = 350°C. In fact, many process parameter combinations both at T_{dep} = 150°C and T_{dep} = 250°C still show equivalent or even higher lifetimes, compared to the layers deposited at higher temperature. After considering the best compromise of reproducibility, deposition rate, and the limit of thermal budget that can be applied on the investigated UV-hotmelt inks; T_{dep} = 250°C is considered to be used for solar cell batches featuring self-aligned selective emitters. First solar cell results incorporating the developed low temperature SiN_x layers are presented by Efinger et al. in the same conference [5].

3.4 Passivation quality of SiN_x layers on iV_{OC} samples

In the next step, we applied low temperature PECVD SiN_x at T_{dep} = 250°C to the iV_{OC} samples featuring textured surface and n^+-emitter on front-side and already-passivated rear-side, as previously explained in section 1.2. After HNO_3 cleaning and HF-dip, front-side passivation is realized by growing a thin SiO_x followed with the low temperature PECVD SiN_x layer. In the next sections, we briefly discuss the iV_{OC} results of these samples.

Figure 9 shows the iV_{OC} results of samples, that either received the low-temperature thermal oxidation inside a tube furnace or plasma oxidation in the same PECVD tool that is later used to deposit PECVD SiN_x at 250°C. A reference PECVD process at 400°C is also carried out for comparison.

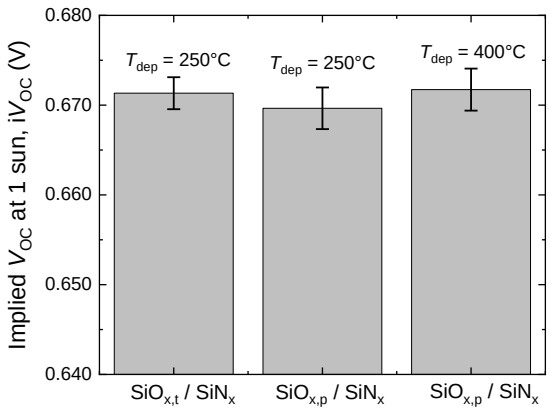

Figure 9: iV_{OC} results of the samples featuring a selection of PECVD SiN_x layers deposited either at 250°C or 400°C. Oxide growth is performed before PECVD SiN_x either by a low temperature oxidation process ($SiO_{x,t}$) or by a plasma oxidation at 250°C ($SiO_{x,p}$). The reference process (T_{dep} = 400°C) is performed in a different PECVD tool from the same manufacturer.

It is observed that the developed PECVD SiN_x process at 250°C reaches similar iV_{OC} results compared to the reference PECVD process that is used for PERC process. In general, samples of all the three processes showed a lower iV_{OC} value than typically known from the reference process, which is expected to arise from the limitations of the bulk material.

4. CONCLUSION

In this work, a PECVD SiN_x layer is developed at lower deposition temperature for its application in selective emitter process routes featuring inkjet-printed mask layers. The typical PECVD deposition temperature (T_{dep} > 350°C) leads to a significant change in morphology and aspect ratio of the evaluated inks, which were successfully printed on phosphorous emitters by applying inkjet processes. In fact, the upper limit for deposition temperature T_{dep} is set as 250°C based upon the

thermal stability tests. Statistical design of experiments (DOE) of PECVD process parameters are performed in order to find the optimum set of parameters that allow deposition of SiN_x layers with adequate optical and electrical properties. FTIR-measured spectra exhibit that layers deposited at lower temperature show typical Si-N, Si-H and N-H peaks for SiN_x layers, which suggests that the structural composition of the layers do not entirely differ with layers deposited at higher temperature. SiN_x layers deposited at lower T_{dep} even show significantly higher Si-H and N-H bond densities in comparison to the standard layers. Although these layers are very H-rich, they do not suffer with any blistering phenomena both after deposition and fast-firing processes. This is unlike what is typically expected for H-rich dielectric layers. For selected process parameter combinations, these H-rich and blister-free SiN_x layers show excellent surface passivation on flat surface ($S_{eff,max}$ = 7.5 cm/s at T_{dep} = 150°C and $S_{eff,max}$ = 10 cm/s at T_{dep} = 250°C). Meanwhile, on textured and diffused surfaces, the deposition rate is found to play a major role in defining the surface passivation. Optimized PECVD SiN_x layers at T_{dep} = 250°C reach comparable average iV_{OC} (iV_{OC} = 670 mV) to the standard SiN_x layer deposited at 400°C. The results pave our way towards fabrication of high-efficiency PERC cells with inkjet-masked self-aligned emitters.

5. ACKNOWLEGEMENT

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