# Reliable wafer-level-bonding method for MEMS packaging using LTCC interposers

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**Abstract**

The anodic bonding of low temperature co-fired ceramics (LTCC) for the wafer-level-packaging of MEMS represents a cost efficient and highly reliable packaging method. To enable for a reliable bonding between the LTCC and the Si wafer the ceramic should have a surface roughness below 50-100 nm. With the aim of avoiding the polishing step for realizing a low ceramic surface roughness a newly developed manufacturing process was deployed, which is based on the optimization of the necessary lamination and sintering steps. The positional accuracy of the electrical feedthroughs within the LTCC ceramic should also become considerably optimized compared to the standard manufacturing process. First promising results will be presented, illustrating the anodic bonding experiments of the wafer level processed Si and ceramic LTCC wafer. Additional a MEMS concept will be introduced to demonstrate the high reliability of ceramic-Si bonding and packaging at operation temperature of up to 300 °C.

Key words: LTCC, MEMS, Wafer-Level-Packaging, Anodic Bonding

## Introduction

Wafer-level-packaging is one of the most promising assembly techniques for the future. Compared to standard technologies this technology offers reduced packaging costs and dimensions, optimized functional and reduced parasitic parameters for the joining of MEMS [1].

Anodic Bonding is usually a process to bond borosilicate glass wafers to silicon wafers in the temperature range of 300-500 °C to get hermetic sealed packages. The bond process is characterized by high bond yields, large process windows and excellent alignment capability, even though this process doesn't require any intermediary layers to form a bond. An applied electric field assists in the thermal diffusion of sodium ions across the bond interface to achieve solid-state mixing of glass and silicon [2].

Low temperature co-fired ceramic (LTCC) technology is commonly used for the packaging of MEMS at Chip-Scale or in BGA-technology [3], [4]. LTCC is a multilayer based technology and is characterized by its high reliability, its robustness against environmental influences and its excellent thermomechanical adaption to Si.

For this work a new LTCC tape developed at Fraunhofer IKTS [5] for Wafer-Level-Packaging processes was applied. It has special anodic bonding properties and comes with a thermal expansion (CTE) as low as 3.4 ppm/K to match the CTE of silicon very closely. The bondable tape is composed of alumina, cordierite and $Na^+$ containing low TEC glass.

## Manufacturing Process of bondable LTCC

Like in the standard LTCC manufacturing process (Fig. 1), the bondable ceramic substrates are processed in form of flexible tapes. They are structured by punching as well as laser processes to form vias, cavities, and channels. Subsequently, the vias having a minimal diameter of 50 µm are filled with conductive paste to create the vertical electrical connections. The conductor layout is printed on the unfired tapes either using screens or stencils printing. To ensure for an excellent adaption of the CTE low expansive gold paste is used for vias and conductors. These processed layers are stacked and laminated together, before they are sintered to compact, monolithic modules at 850°C in a batch furnace. While sintering the bondable LTCC a shrinkage in the range of 16-17 % occurs during the firing process. Afterwards the anodic bonding process with the Si-Wafer occurs. During the post-firing steps the panels containing multiple devices are singularized by dicing or laser cutting of the fired components. Finally, the microelectronic components will be assembled and external contacts can be joined.

Because of its multilayer processing ability LTCC is more flexible and more suited for high volume production at lowest cost than alternative borosilicate glass wafers which are usually used for anodic bonding of MEMS [6].

**Table: Specification of anodically bondable LTCC wafer**

| | |
|---|---|
| Thermal expansion | 3.4 ± 0.2 ppm/K |
| Dielectric constant $\varepsilon_r$ | 5,35 |
| Isolation Resistance | $2.6 \times 10^{13}$ Ωcm |
| Surface Resistance | $2.4 \times 10^{12}$ Ω |
| Dielectric Strength | 27.03 kV/mm |

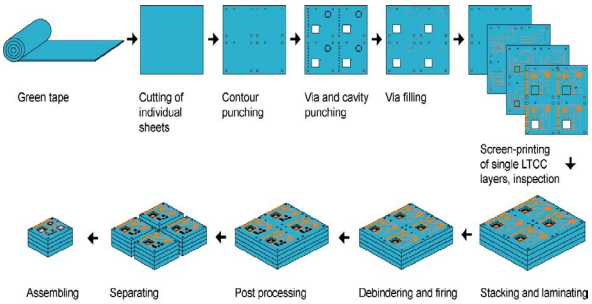


**Figure 1: LTCC Manufacturing Process [7]**

## Experimental Methods

*Modifications of the firing process to optimize roughness and waviness*

The Anodic Bonding process requires a relatively low roughness (Ra < 100 nm) of the LTCC surface and a wafer flatness of <10µm/20 mm for obtaining optimum bonding results [8].

By applying pressure assisted sintering technology (PAS) the necessary lapping and polishing efforts, having the aim to increase the surface quality of the LTCC, can be minimized. Therefore, the LTCC substrates are fired at 850°C and pressed with pressures up to 2 MPa. A steady uniaxial pressure inhibits the in-plane shrinkage of the tapes and at the same time reduces the surface roughness. Sticking between the pressure plate and the LTCC is avoided by non-sintering alumina tapes or setter plates like glassy carbon plates [8]. Fig. 2 shows the first promising results in terms of roughness and wafer flatness after the sintering of the anodic bondable LTCC laminates.

The average wafer flatness Wa < 2 µm/ 20 mm of all tapes sintered by the PAS process could be highly decreased in comparison to free sintered tapes (Wa ~ 12.2 µm/ 20 mm). Furthermore the roughness of the PAS processed tapes is significantly reduced to Ra ~ 0.14 µm (glassy carbon setter) compared to tapes of the free sintering process with a average roughness of Ra ~ 0.78 µm. Further experiments with optimized parameters should improve the wafer roughness close to the range of the anodic bonding specifications (Ra≤ 0.05 µm).

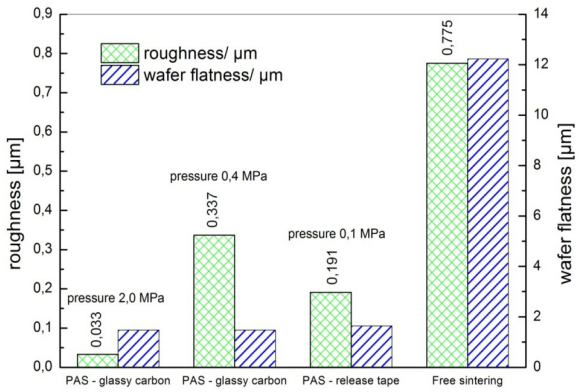


**Figure 2: Results on roughness and wafer flatness of processed LTCC laminates**

*Accuracy of via positions in the LTCC wafer*

The typical accuracy of via positions of 4 inch diameter LTCC wafers is ca. ± 50 µm in a free sintering process. The Pressure assisted sintering process (PAS) allows control of the shrinkage in X-Y-direction of 0 ± 0,05 %, in z-direction the LTCC wafer shows a shrinkage of 41 % [9]. Thereby the via position accuracy can decreased to≤ 25 µm for an 4 inch LTCC wafer 8 (see Fig 3).

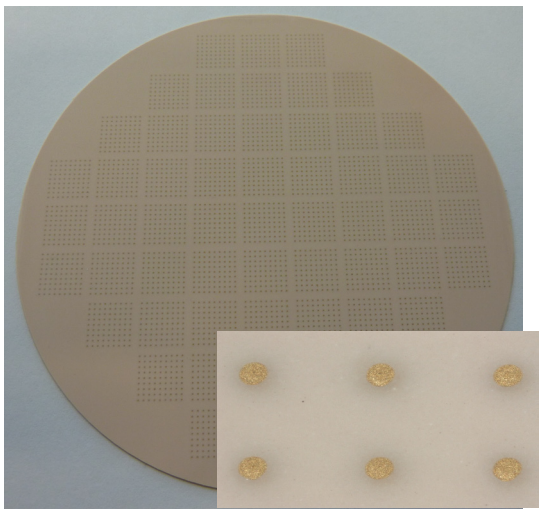

**Figure 3: 4 inch LTCC-integrated gold vias (PAS processed) for contacting with MEMS TSV**

*Results of the anodic bonding process*

For the investigation of the anodic bondability PAS (with release tape) processed LTCC wafers are selected for first lapping and polishing tests, with the aim of lowering the surface roughness down to 100 µm. Tab. 2 shows the results of the wafer bow and the wafer roughness of the first samples measured by an atomic force microscope (AFM). A microroughness (Ra) of 65,8 nm and wafer bow of 19,8 µm was achieved. Further optimization of the polishing process should decrease the roughness down to 10 nm.

**Table 1: First lapping and polishing results - Surface quality and wafer bow**

| Sample | RMS [nm] | Ra [nm] | Rmax [nm] | |
|---|---|---|---|---|
| Polished LTCC | 117,335 | 65,812 | 386,183 | |
| | Bow_min 0° [µm] | Bow_max 0° [µm] | Bow_min 90° [µm] | Bow_max 90° [µm] |
| Polished LTCC | -2,3 | 17,4 | -19,8 | 0 |

First successful anodic bonding tests with a 4 inch LTCC- and Si-wafer used a bonding temperature of 450 °C and a bonding voltage of 500 V, which is comparable to conventional borosilicate glass wafers. Fig. 4 represents a typical characteristic curve of the applied current and voltage during the bonding procedure. Fig. 5 shows an inseparably 4 inch LTCC-Si bond. Sodium depositions on the surface of the LTCC are visible which occurs by sodium diffusion through the LTCC wafer. After dicing into 5 x 5 mm samples a bonding yield of 100 % could be achieved (see Fig. 6). The bonding strength of the bonded samples will furthermore be evaluated by fracture toughness measurements (Micro Chevron Test).

With an optimized surface quality of the LTCC wafer a bonding temperature of ≤ 400 °C and voltage of ≤ 400 V should be used.

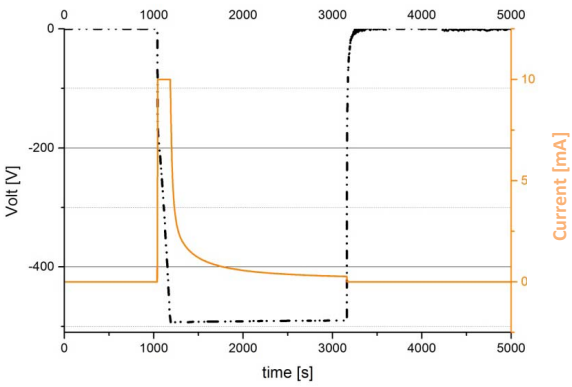


**Figure 4: Characteristic curve of current and voltage while anodic bonding of LTCC and Si**

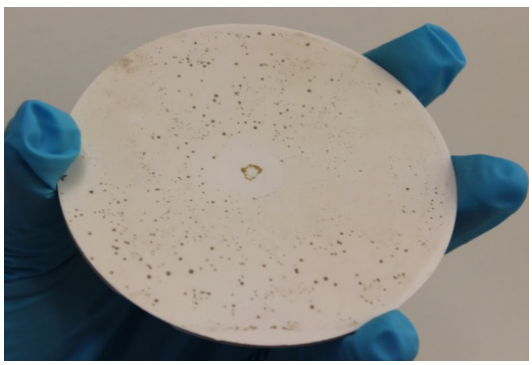

**Figure 5: Successful Si to LTCC bond**

a) b)

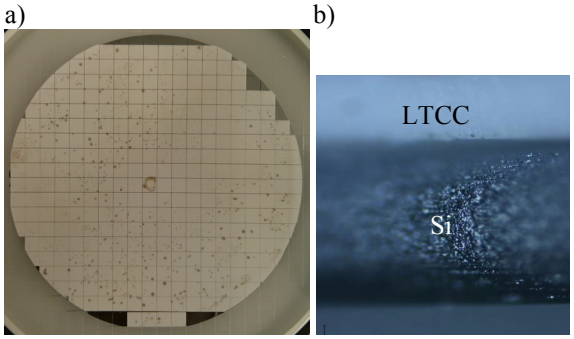


**Figure 6: a) Successful dicing experiment of a bonded wafer, b) Bonded chip-side view (10x)**

**Wafer Level Packing of MEMS**

The developed packaging concept should be adapted to MEMS which operates at 300 °C service temperature. For this aim the MEMS will be anodically bonded to an LTCC interposer that redistributes the electrical interconnects to the system terminals at the backside of the interposer.

To enable highest functionality at minimal size, through silicon vias are used to connect the top and bottom electrodes with the backside of the sensor.

The MEMS should be a multi-functional sensor. It comprises on an array of electrostatic cells capable of receiving and transmitting ultrasonic sound as well as temperature and pressure sensors (see Fig. 7). Hence the package needs to be stable up to this high temperature and has to connect the electrical signals reliably to the backside of the package. Based on this concept just the ultrasonic cells of the MEMS will directly face the harsh environment, whereas most of the other parts can be protected by the package. Still, the entire system will be exposed to the high temperature.

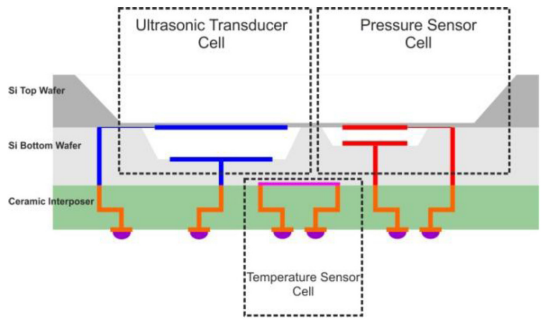


**Figure 7: Schematic Sensor Design as a cross-sectional view.**

LTCC and Si will be joined by wafer-level packaging, as it is well known for MEMS packages. This zero level packaging approach enables highest throughput due to the fact that every device is packaged simultaneously. However, the numerous electrical vias in both parts make this process quite challenging requiring precise placement and high

accuracy of the vias. The subsequent dicing step generates the individual devices.

Criteria's that have to be fulfilled by the bonding step are: mechanical robustness, electrical interconnection, hermetic sealing (at least for the MEMS) and suitability for 300°C operation temperature.

**Conclusion**

A highly reliable wafer-level-bonding method at wafer-level is under development using an anodically bondable ceramic-based LTCC material. Several investigations were done to improve the surface quality and the waviness of the LTCC bodies during the sintering process.

By combining heterogeneous materials of ceramic multilayer bodies and Si wafer a promising packaging concept is realized by anodic bonding. The final result of the development will be a highly reliable multi-functional MEMS sensor.

**References**


[1] Masayoshi Esahi, "Wafer Level Packaging of MEMS, Transducers 2009, Denver Co, USA, June 21-25, 2009

[2] Roy Knechtel, "Low Temperature Wafer Bonding for MEMS Processes and 3D Integration", LTB-3D, Tokyo, May 22-23, 2012

[3] Jens Müller, "Wafer Level Chip Scale Packages – Anforderungen an Design, Substrat- und Fertigungstechnologie", IMAPS Seminar Multi-Chip-Module, Göppingen, February 02, 1999.

[4] A. Bessemoulin, "A Hermetic Surface-Mount Ball Grid Array (BGA) LTCC Package for Multi-function T/R MMICs up to Ku-band", COMCAS, Tel Aviv, November 07-09, 2011

[5] Michael Stelter, "Mesoscale Sensor/ Systems Integration based on Multilayer Ceramics", Joint International IMEKO Symposium, Jena, September 02, 2011

[6] Thomas Gessner, "Wafer bonding in micro mechanics and microelectronics - an overview". The World of Electronic Packaging and System Integration. pp. 307-31, 2005

[7] Klaus-Jürgen Wolter: Aufbau- und Verbindungstechnik 1. Vorlesungsskript, Technische Universität Dresden, 2007

[8] Bjoern Brandt, "LTCC substrates for high performance strain gauges" CICMT, Erfurt April 16-19, 2012

[9] Michael Hintz, „Generic Investigation on 0- Shrinkage processed LTCC", IMAPS Nordic, Stockholm, 2002