POLYSILICON TUNNEL JUNCTIONS AS ALTERNATES TO DIFFUSED JUNCTIONS

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ABSTRACT: We report use of heavily doped polysilicon combined with a tunnel dielectric to provide an alternate to diffused junctions for silicon solar cells. Thin tunnel dielectrics (6-12Å) are fabricated using methods adapted from IC processing. These serve as diffusion barriers and passivation layers. When combined with heavily doped polysilicon, they can form an ideal step junction with interface passivation, enabling low dark currents not possible with diffused emitters. We show that it is possible to obtain hyper-abrupt junctions with the tunnel layer providing interface passivation, and that these junctions obtain a V_{OC} of 676 mV on 780 μm thick substrates.
Keywords: Polysilicon, tunnel junction, emitter

1 INTRODUCTION

The deep diffusions required for a two-step junction [1] to provide the emitter and contact passivation required for high efficiency cells is a complex and expensive process. An attractive alternate approach is to form junctions with deposited layers, such as amorphous silicon [2] or poly-silicon [3,4,5,6]. In this work, we further look at the use of polysilicon to form emitter and contact layers.

Polysilicon emitters (PE's) were investigated in the early 80's. Several groups had reported relatively high V_{OC} values with deposited polysilicon layers [4,5]. Green had noted that the PE is an extension of the MIS cell, and suggested use of a thin interfacial oxide can greatly enhance performance [7].

PE's are of interest because (1) they form a near-ideal hyper-abrupt junction, (2) they do so with a deposited layer, requiring no diffusion (with a shorter process time and smaller thermal budget) and (3) their compatibility with high temperature processing provides flexibility in cell processing and integration, especially for advanced structures. For a thin, heavily doped hyper-abrupt emitter with a passivated interface, it is possible to obtain emitter dark currents significantly lower that achievable with diffused emitters [8]. It should be noted that the band structure of a polysilicon emitter is quite similar to the HIT cell (3), as shown in figure 1, and both could be expected to obtain similar performance.

The polysilicon emitter has benefits over amorphous silicon in reduced absorption and, by virtue of its tolerance to high temperatures, greater process integration capability. However, it requires a thin tunneling dielectric to block dopant diffusion and passivate the interface. IC scaling has driven considerable technical progress in this area. Modern ICs using polysilicon gates require low poly sheet resistance, a sharp doping step at the dielectric, and dielectric thicknesses consistent with solar cell tunnel dielectric requirements. The IC processes are planar and scalable, so there is an opportunity to apply these to PV once suitable performance is demonstrated.

The objective of this work is to use IC processing to understand the process requirements for a polysilicon emitter. This enables use of well-characterized and controlled processes to determine which processes are best and to establish the process window. In general, processes are limited to a temperature window of

<1050ºC and time window in the 20-60 second range, to allow scaling while maintaining control.
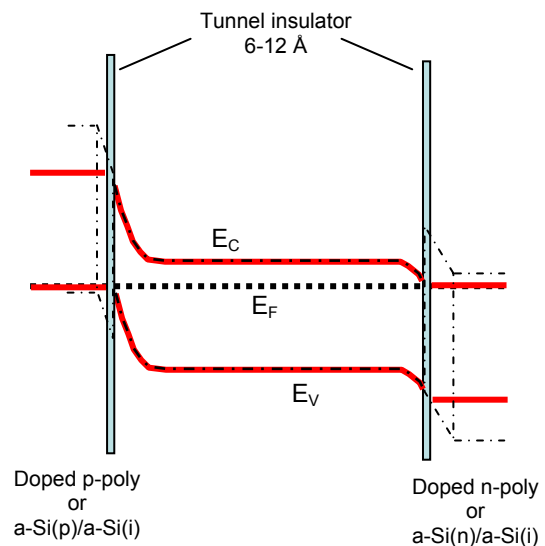

Figure 1: Comparison of band structures for doped polysilicon--c-Si(n) cell with a tunnel insulator passivated interface (red and blue) and a-Si(p)--c-Si(n) heterojunction (black) cells.

2 PROCESSES

The development test vehicle is a single-sided device, with a diffused back surface field and a front tunnel layer, as shown in figure 2, with the process flow given in figure 3. The standard back side enables understanding of the physics of the polysilicon emitter on the front. Two variations are being examined. The first uses a thin p-type poly with an overlaid ITO as an anti-reflection (AR) coating and contacting layer. The second uses a thicker poly with a Si_3N_4 AR coating. Lithography is used to define contacts.

Because the IC equipment runs 300 mm wafers, we have been restricted to 780 μm thick CZ substrates without texture, and are constrained to available 300 mm substrates. The n-type substrates, with resistivity of 3-6 Ω-cm, consistently show lifetimes > 1 msec, but the p-type substrates of similar resistivity are variable.

Therefore, most processing has been on n-type. This is in any case preferred to achieve higher bulk lifetime, but requires special consideration to block boron diffusion through the tunnel layer.
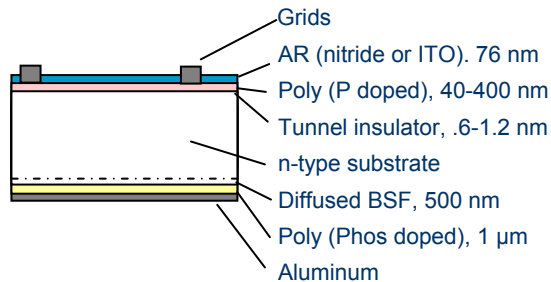

Figure 2: Device structure and process flow. A) with diffused BSF (formed by diffusion during Rapid Thermal Anneal (RTA) of phosphorous doped poly) on n-type Si.

Figure 3: Process flow.

Figure 4 shows the boron SIMS profile for a junction test sample. Layers used in actual devices are thinner. Note that a sharp junction profile is obtained, in large part due to the blocking tunnel dielectric. The peak at the interface is in part due to the SIMS crossing the buried dielectric, as evidenced by the peak in the silicon profile (blue line), but may in part arise from boron segregation at the interface.

A critical component of this device is the tunnel dielectric. This is formed using standard methods and low-cost source gasses. Figure 5 shows physical thickness for films made with three different processes as a function of growth time. In general, it is believed that a physical thickness of ≤ 12Å is sufficient.

3 EXPERIMENTAL RESULTS

To characterize the passivation performance of the PE structure, n-type CZ wafers were coated front and back with a thin tunnel layer. Three base oxide layers were used: chem-ox, which is a chemical oxide formed after the standard MOS clean, and 8 and 10Å thick rapid thermal oxides (RTO). Amorphous silicon was then

deposited and crystallized with a 30 second RTA at 1000ºC. Lifetime was then measured using the Quasi Steady-State Photoconductance method (QSSPC). Figure 6 shows the results of this experiment.
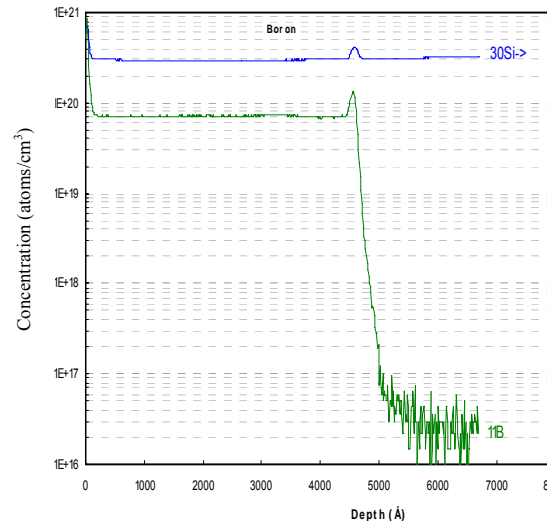

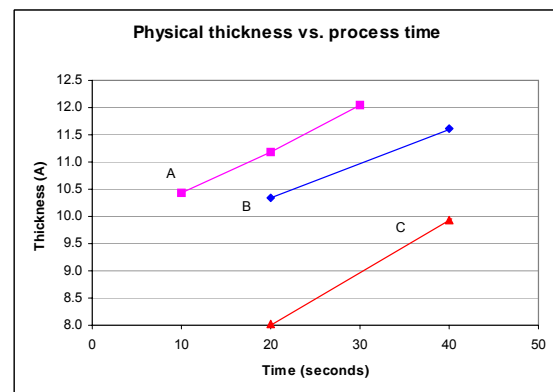**Figure 4:** SIMS boron and reference silicon profile for a boron-doped polysilicon test structure.

Figure 5: Physical thickness as measured with XPS as a function of growth time for three different tunnel dielectric processes, A, B and C.

The passivation is a function of the poly thickness. This can be expected, as a thinner poly minimizes the effect of polysilicon layer on the diffusion current formed with the structure. The advantage of the thinner base oxide is less clear, although this may arise because the thicker oxide forms a hole trap at the interface (the cause of an S-shaped IV for tunnel barriers that are too thick, as will be discussed below).

Full PE cell structures have been made. These are similar to the structure shown in figure 2, with base oxides of chem-ox and 8Å under 300, 350 and 400 nm of in-situ doped p-type poly. Note that the base oxides underwent additional processing to provide suitable properties for this application, and this processing affects the final physical thickness. The data presented in Fig 7 are averages for seven 2x2 cm^2 cells in a 12.5x12.5 cm^2 area. The Suns-Voc measurement of Voc for these structures is shown in figure 7, indicating high Voc values consistent with the expected low J_0 structure. Higher values are found for the RTO dielectrics than the chem-ox, consistent with the

results of figure 6, which suggests that the RTO provides improved interface passivation. Note that use of thinner poly provides a significant improvement in V_{OC}.
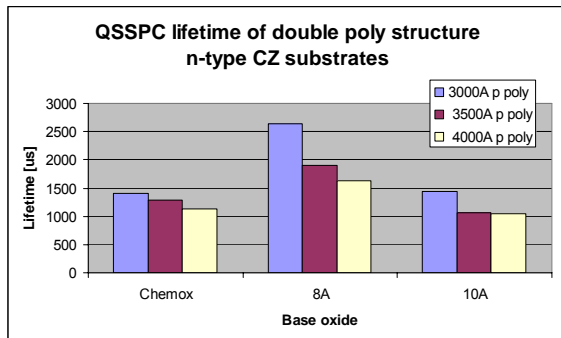

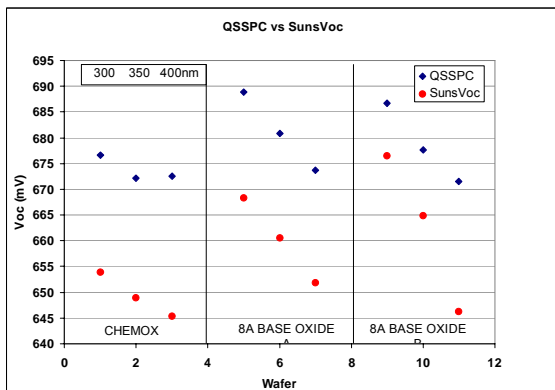**Figure 6**: QSSPC lifetimes for symmetric front/back PE structures on n-type CZ.

Figure 7: QSSPC (black) and Suns-Voc (red) measurements of Voc for PE structures, for three increasing poly thicknesses (300, 350 and 400 nm)and three tunnel dielectric layers.
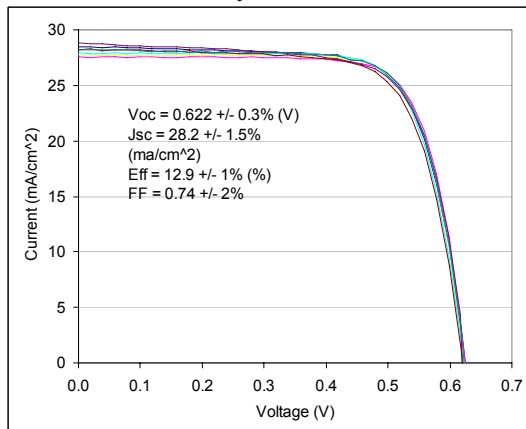

Figure 8: IV curves for seven 2x2 cm isolated PE cells in a 12.5x12.5 cm^2 area with 400 nm p-type poly on n-Si.

The measured 1-sun IV curves for seven cells using chem-ox as a base oxide are shown in figure 8. The tight distribution results from use of highly uniform processes.

The degradation in V_{OC} from the Suns-Voc values in figure 7 is due to edge effects. The cells in figure 6 were not isolated; the ones in figure 7 were isolated using a dicing saw.

There is considerable room for improvement in these results. The V_{OC} can be increased substantially with improved edge isolation, or by increasing the cell area

and use of thinner wafers. The J_{SC} can be increased with texturing and use of thinner poly, and the high resistivity substrate, with a thickness of 780 μm adds series resistance that reduces the fill factor intrinsically by approximately by 4-5%.

The thick poly affects blue response. Figure 9 shows internal quantum efficiency (IQE) for structures with 100, 300, 350 and 400 nm poly. Note that the absorption in the blue becomes quite severe. This points to the need for thinner poly layers to achieve high efficiency, or, alternately, improvement in the optical properties of the poly.
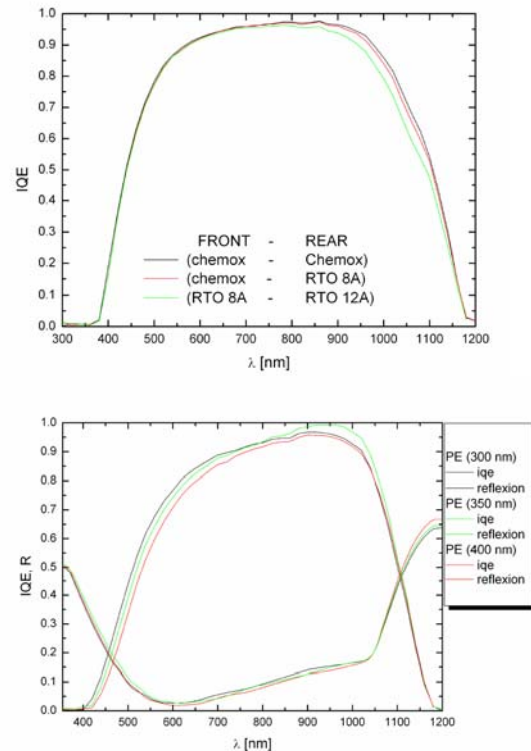

Figure 9: Internal quantum efficiencies for PE cells. Top: 100 nm n-type emitter, three types of base oxides. Bottom: 300, 350 and 400 nm p-type emitters.

We have also addressed requirements for tunnel layer thickness. A thick layer creates a potential well at the emitter boundary that traps holes (for p on n structures). This leads to a degradation in the fill factor, as shown in figure 10. Note that the Suns-Voc measurement is not sensitive to this issue, and shows a high pseudo fill factor of 0.83. This shows that high tunnel layer thickness causes a strong series resistance problem.

It is possible to model the tunnel interface using a device simulator such as Sentaurus [10]. The output of such a model is shown in figure 11, which shows there is minimal fill factor degradation for a p-type emitter on an n-type substrate when the dielectric thickness is ≤12Å.

3 CONCLUSION

On the basis of these results, the path to a high efficiency PE cell structure is clear. The requirements include:

- A p-PE/c-Si(n) structure to minimize J_0 and maximize lifetime,
- A tunnel layer with thickness <12Å, formed with a rapid thermal process, and
- A thin poly, probably using a TCO layer to obtain lateral conductivity, as shown in figure 2a, or a thicker poly with optimized optical properties and a low sheet resistance.
- A textured front for higher J_{sc} and a lower c-Si wafer thickness for higher V_{oc} and FF.

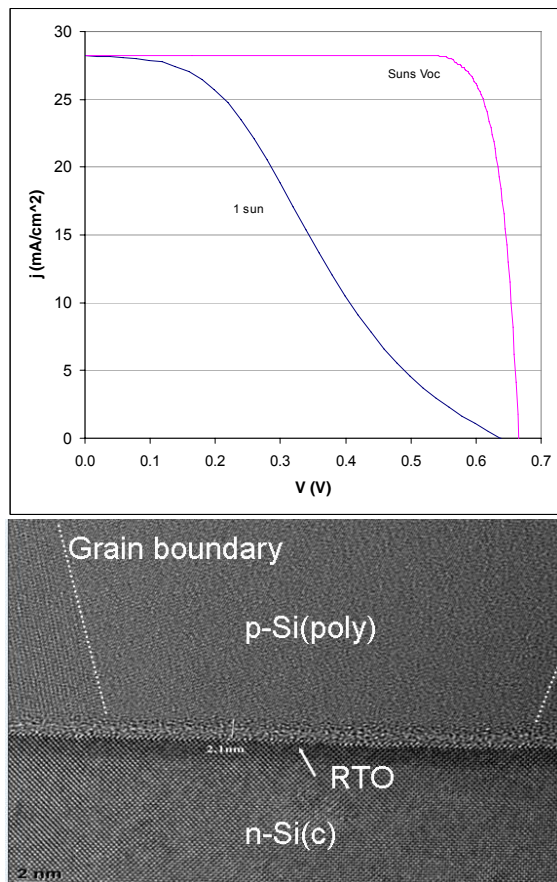Following these guidelines, it should be possible to exceed 20% efficiency with a planar PE cell structure.

Figure 10: Suns-Voc and measured IV for a cell with a thick tunnel oxide as shown in the TEM of the interface, with poly on top and crystal silicon underneath

4 ACKNOWLEDGEMENTS

6 REFERENCES

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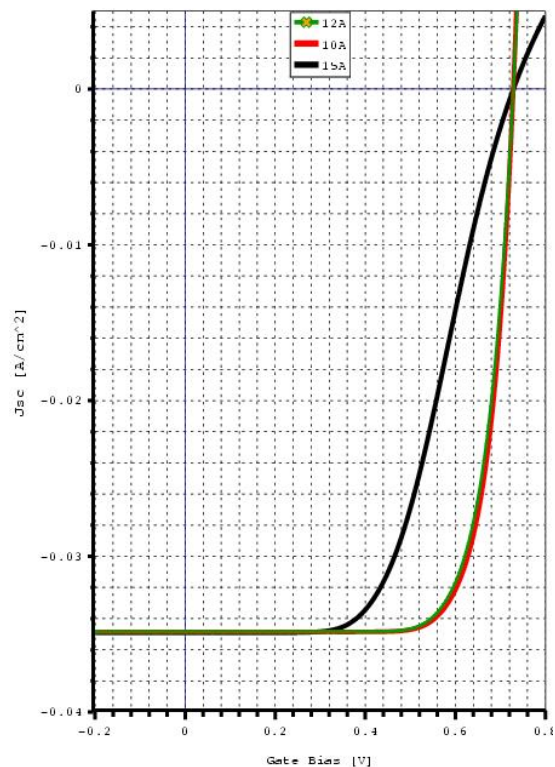[9] Sentaurus® TCAD Simulator, Synopsys Corporation.

Figure 11: Sentaurus® model of PE structure for tunnel dielectric thicknesses of 10, 12 and 15Å, showing fill factor degradation with thicker layers.