Epitaxial GaInP/GaAs/Si Triple-Junction Solar Cell with 25.9% AM1.5g Efficiency Enabled by Transparent Metamorphic $Al_xGa_{1-x}As_yP_{1-y}$ Step-Graded Buffer Structures

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III–V/Si multi-junction solar cells are potential successors to the silicon single-junction cell due to their efficiency potential of up to 40% in the radiative limit.[1] Herein, latest results of epitaxially integrated GaInP/GaAs/Si triple-junction cells are presented. To reduce parasitic absorption losses, which have limited the current density in the Si bottom cell in the previous devices, transparent $Al_xGa_{1-x}As_yP_{1-y}$ step-graded metamorphic buffers are investigated. Compared with previous $GaAs_yP_{1-y}$ step-graded buffers, the transmittance is enhanced significantly, while no significant impact on the threading dislocation density is observed. Implemented into a new triple-junction solar cell, an increase in short-circuit current density from 10.0 to 12.2 mA cm^{-2} is achieved, leading to a new record conversion efficiency of 25.9% under AM1.5g conditions.

1. Introduction

Overcoming the efficiency limit of silicon (Si) single-junction solar cells is one possibility to enable an even more cost-effective conversion of sunlight to electrical power. Si solar cells are basically limited to a conversion efficiency below 29.6%,[2] whereas multijunction solar cells can reach significantly higher values. The current record efficiency of 39.2%[3] under AM1.5g spectral conditions, achieved with a six-junction III–V design, clearly demonstrates the potential of these concepts. However, fabrication costs are currently orders of magnitude higher due to complex deposition methods and expensive substrates such as GaAs

or InP. III–V on active Si multijunction cells have gained attention in the last decade because the substrate costs are significantly lower compared with pure III–V multijunction cells. The main challenge of the III–V/Si approach is the lattice constant mismatch of 4% between Si and III–V semiconductors with appropriate bandgaps such as GaAs and $GaIn_{0.5}P_{0.5}$. Direct wafer bonding of the Si bottom cell to the III–V tandem cell stack has been used successfully to overcome the mismatch and reach a conversion efficiency of 34.1%[4] for a GaInP/AlGaAs/Si design in a 2-terminal configuration. With a 4-terminal configuration, a value of 35.9%[5] was achieved via mechanical stacking of the individual subcells. The implementation of both approaches is challenging from the perspective of technology, prohibiting the scalability to large-volume production. Direct epitaxial growth in contrast enables a simplified fabrication route as the III–V subcells are deposited onto the Si bottom cell by epitaxial methods such as metalorganic vapor-phase epitaxy (MOVPE)[6,7] or molecular beam epitaxy (MBE).[8] In 2020, an epitaxial GaAsP/Si dual-junction solar cell with a verified AM1.5g conversion efficiency of 23.4% has been presented by Lepkowski et al.[9] Fan et al. presented a similar GaAsP/Si design with an in-house measured (uncertified) efficiency of 25.0%.[10] Both results show the intense research leading to a strong efficiency increase over the last years. In this work, we focus on the development on GaInP/GaAs/Si triple-junction cells as they have an even higher efficiency potential than their dual-junction counterparts.[1] In previous publications, the authors have demonstrated a 19.3%[11] and 22.3%[6] GaInP/GaAs/Si cell, the latter being mainly limited by parasitic absorption within the $GaAs_yP_{1-y}$ step-graded buffer structure. In this work, we present a new generation of this device (gen IV) which does not show significant parasitic absorption in the buffer layers and thus leads to a new certified AM1.5g conversion efficiency of 25.9%.

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2. Experimental Section

An overview of the structural properties of the device discussed in article is shown in **Table 1**. For the Si bottom cell, a (001)-oriented

Table 1. Structural properties of two generations of GaInP/GaAs/Si triple-junction solar cells. Gen II has been presented in a previous publication.[6]

	Gen II	Gen IV
Si bottom cell		
Base resistivity	$2\,\Omega\,cm$	$20\,\Omega\,cm$
Miscut	$2°$ toward (111)	$6°$ toward (111)
Surface finish	CMP	Stock Polish
Step graded buffer	$GaAs_yP_{1-y}$	$Al_xGa_{1-x}As_yP_{1-y}$
Protection layer	–	5 nm GaAs
GaAs middle cell	760 nm	790 nm
GaInP top cell	390 nm	400 nm
ARC Ta₂O₅/MgF	79 nm/110 nm	65 nm/110 nm

100 mm p-type wafer with a miscut of $6°$ toward (111) and a base resistivity of $20\,\Omega\,cm$ was used. On the front side, a simplified low-cost "stock polish" process was applied instead of a costly chemical-mechanical polishing (CMP) process to generate the epi-ready Si wafer surface. In **Figure 1**, two atomic force microscopy scans (Park XE 150) of the "stock polish" as well as a reference CMP surface are shown. On the stock polish, surface traces of the mechanical polishing steps are still visible and lead to a root mean square (RMS) roughness of 0.34 nm, whereas the CMP surface does not show any significant features and the roughness is below 0.16 nm RMS. Details about this simplified polishing process will be presented in an upcoming publication.

An $\approx 20\,\Omega\,sq^{-1}$ n-Si emitter was established via a phosphorous diffusion process on the front side after an initial Radio Corporation of America cleaning procedure. The backside of the Si wafer was passivated and protected by a 5 nm Al_2O_3/ 70 nm SiN_x layer stack before the epitaxial growth. A 30 nm GaP nucleation layer followed by a 200 nm GaNP (lattice-matched to Si) layer was grown via MOVPE in a CRIUS close coupled showerhead reactor from AIXTRON in a "7×4" configuration. Details regarding the GaP nucleation can be found in previous publications.[6,12] The intention of the GaNP layer is to keep the GaP/Si interface clear of misfit dislocations as they likely increase the interface recombination velocity and thus lower the voltage of the Si bottom cell.

The grading of the lattice constant from GaP to GaAs was achieved via homogeneous composition steps in a graded

$Al_xGa_{1-x}As_yP_{1-y}$ buffer consisting of 14 layers with a thickness of 160 nm, respectively (in a separate epitaxy-run—decoupled from the GaP/Si nucleation). The uppermost $Al_{0.29}GaAs$ layer of the graded buffer was capped by 5 nm of GaAs to prevent oxidation. After the growth of the graded buffer, the wafer was transferred to an AIX-2800 G4-TM reactor from AIXTRON in which the GaInP/GaAs dual-junction structure including tunnel junctions was grown. The thicknesses of the GaInP top and GaAs middle cell were altered from the gen II to the gen IV device to adjust the current distribution among the three subcells. The individual cell thicknesses are shown in Table 1. Simulations have suggested that the diffusion lengths in the emitters of the GaAs and GaInP subcells were not sufficient in our previous cells. Thus, the thicknesses of the emitters in the gen IV device have been reduced by 33% for the GaInP cell and by 25% for the GaAs cell.

All cells discussed herein have been coated with an antireflective coating (ARC) consisting of Ta_2O_5/MgF_2 to reduce optical losses due to reflections at the front surface. The thicknesses of the ARC layers have been changed from gen II to the recent gen IV cell according to the values shown in Table 1. The metal contact on the backside was realized by the evaporation of 2 μm of aluminum followed by a laser fired contact process[13] to locally penetrate the dielectric passivation stack and obtain ohmic contacts. The grid on the front side, optimized for AM1.5g conditions with a total shading of 0.8%, was deposited via evaporation and standard photolithographic techniques. Individual cells on the wafer were separated by a wet-chemical mesa-isolation which also separates the pn-junction of the Si bottom cells.

Calibrated characterization of the best 4 cm² cell on each wafer was conducted in the III–V CalLab at Fraunhofer ISE. During IV characterization under AM1.5g conditions, an aperture mask was applied to the cell to avoid current contribution in the Si bottom cells from outside the dedicated cell area.

Threading dislocation densities have been measured via electron channeling contrast imaging[14,15] in an SU-70 scanning electron microscope from Hitachi in a backscatter geometry. Using the crossing of two {220} bands as the channeling condition, several random spots of the sample with a total area of >2000 μm² were scanned to obtain the averaged dislocation density.

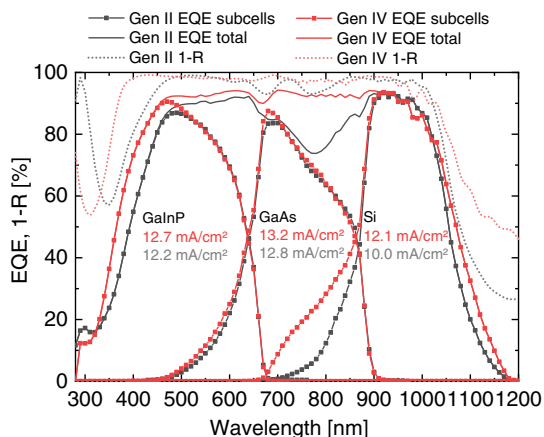Transmittance (T) and reflectance (R) were characterized in a Lambda 950 Spectrophotometer from PerkinElmer in the wavelength range from 280 to 1200 nm.
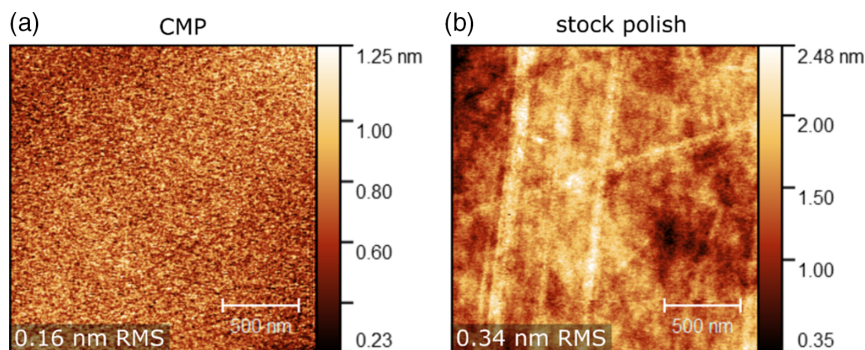
Figure 1. AFM scans ($2 \times 2\,\mu m^2$) of a) a CMP-treated Si surface and b) a Si surface prepared by a low-cost "stock polish" process developed by Topsil. The latter one is used for the solar cell presented within this work.
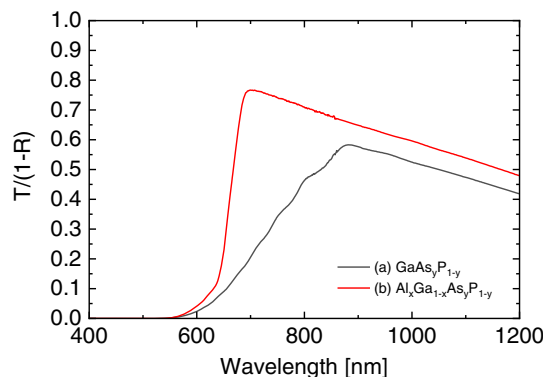
3. Transparent $Al_xGa_{1-x}As_yP_{1-y}$ Step-Graded Buffer Structures

The total external quantum efficiency of our previous gen II triple-junction cell, shown in **Figure 2** as a black solid line, states a strong parasitic absorption in the spectral range between 670 and 870 nm. The GaAs middle cell is designed semitransparent to achieve a nominally current-matched device. Thus, light with energy higher than the GaAs bandgap (1.42 eV–873 nm) is partly transmitted through the GaAs subcell. This light is supposed to be absorbed in the Si bottom cell to enhance its current density. But unfortunately, a significant part of this light is absorbed within the $GaAs_yP_{1-y}$ metamorphic buffer structure which is located between the Si bottom and the GaAs middle cell to transform the lattice constant. This parasitic absorption reduces the light intensity reaching the silicon bottom cell and limits the current as well as the overall efficiency of the full device.

To overcome this limitation, we designed and investigated a step-graded metamorphic buffer with increased transparency within this spectral range. Using $Al_xGa_{1-x}As_yP_{1-y}$ instead of $GaAs_yP_{1-y}$ for the uppermost layers, the bandgap of each layer could be tuned to nominally be above 1.8 eV. As shown in **Figure 3**, two different buffer structures were investigated. The nominal compositions (Figure 3a,b) as well as the nominal bandgaps (Figure 3c) of all layers are given for the reference structure (a) and the Al-containing structure (b). To measure the transmittance characteristics, the structures were deposited on (001) GaP wafers, 2° miscut toward (a) (011) and (b) (111)A. As the bandgap of the GaP substrate (2.3 eV) is higher than the one of all buffer layers, no influence of the substrate is expected—except for free carrier absorption. In **Figure 4**, the transmittance T normalized by $1-R$ is plotted for both buffers (a) and (b). The $T/(1-R)$ metric enables to determine the part of the light that is transmitted through the graded buffer, taking only the light into account which really penetrates into the material (disregarding the reflected light as there will hardly be any internal reflection in the case of the full triple-junction device).

Figure 2. EQE measurement of the gen II[6] and gen IV triple-junction solar cells. The parasitic absorption of the gen II device in the range between 670 and 880 nm is overcome. Stated subcell current densities have been calculated using the AM1.5g spectrum.

Figure 4. Transmittance normalized by $1-R$ of the two different (Al)GaAsP step-graded buffers. The negative slope toward higher wavelength is caused by free carrier absorption in the GaP substrates.
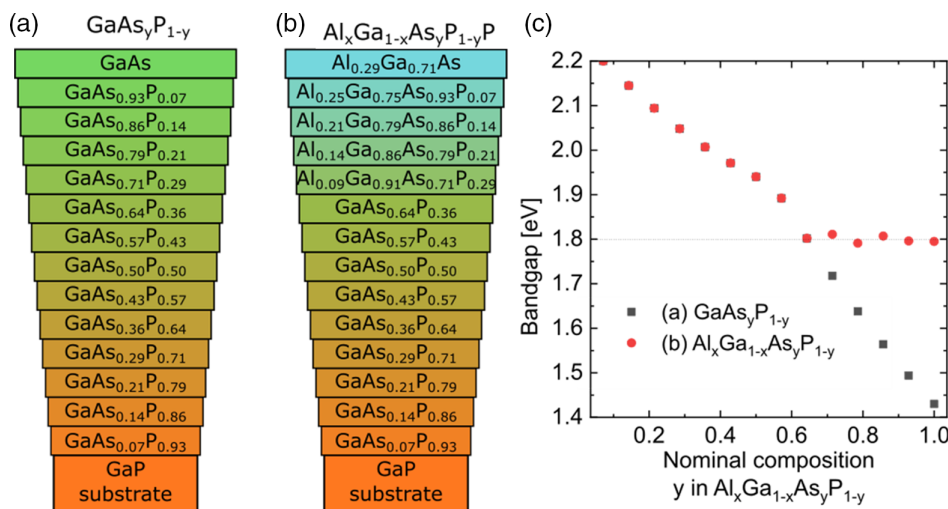
Figure 3. Structure of the a) absorbing $GaAs_yP_{1-y}$ and b) transparent $Al_xGa_{1-x}As_yP_{1-y}$ step-graded buffer on GaP substrates. The given compositions are nominal values. c) The nominal bandgap in dependence of the composition is plotted for (a) and (b).

For wavelengths above 900 nm, a negative slope is observable for both structures which is attributed to free-carrier absorption within the 300 μm-thick GaP substrates.[16] We assume that the slight difference between (a) and (b) originates from differences in the doping levels of the GaP substrates in the range of 5×10^{17} to 2×10^{18} cm^{-3}.

For the GaAs$_y$P$_{1-y}$ buffer structure (a), a continuous increase in transmittance is observed from 600 to 870 nm. The oscillating shape of the increase originates from the onset (or rather end) of absorption in the various GaAs$_y$P$_{1-y}$ layers with different bandgaps below the crossover point from an indirect to a direct bandgap at approximately 2.0 eV–620 nm. In contrast, the Al$_x$Ga$_{1-x}$As$_y$P$_{1-y}$ buffer structure (b) shows a rather steep increase in transmittance starting from 640 nm. The full transmittance (highest point) is reached at (a) 880 nm–1.41 eV and (b) 700 nm–1.77 eV. The results clearly show that the AlGaAsP buffer structure (b) has a higher transmittance in the spectral range, which shows the prominent dip in the total external quenatum efficiency (EQE) in the gen II triple-junction cell in Figure 2. At the same time, the results confirm that the real incorporation of Al is close to the expected compositions of the individual Al$_x$Ga$_{1-x}$As$_y$P$_{1-y}$ layers. The slight difference between the target value (1.8 eV) and the real value of 1.77 eV results from small incorporation uncertainties as the compositions of the quaternary material have not been determined separately for each layer but rather have been extrapolated from the incorporation of Al in AlGaAs.

The incorporation of Al up to a concentration of Al$_{0.29}$Ga$_{0.71}$As did not show any detrimental impact on the surface morphology and atomic force microscopy scans revealed similar root mean square roughness values of (a) 5.6 nm and (b) 4.3 nm on a 20×20 μm^2 area. Regarding the dislocation density, no significant influence of the Al was observed and similar values of $\approx 1.5 \times 10^7$ cm^{-2} were found on an area of >2000 μm^2 for both samples (a) and (b).

4. Solar Cell Results

By implementing the transparent AlGaAsP step-graded buffer structure into the gen IV GaInP/GaAs/Si triple-junction solar cell, the parasitic absorption could be reduced to a large extent. This is reflected in the EQE characteristics of the Si bottom cell in Figure 2 in the range from 670 to 870 nm. Compared with gen II, its current density is improved by +2.1 to 12.1 mA cm^{-2}. A small contribution to the increased current density, however, can also be attributed to better light trapping characteristics in the long-wavelength regime with $\lambda > 1050$ nm. This is the effect of a different morphology and thus different scattering characteristics of the as-received backside of the Si bottom cell, being a bright etched surface for gen II and an acid saw-damage etch for gen IV.

The total EQE data of gen IV in Figure 2, represented by the solid red line, does not show any pronounced dip between 670 and 870 nm, confirming the successful avoidance of parasitic absorption in the metamorphic buffer. The improvement in the short wavelength region of the GaInP top cell (350–450 nm) is caused by an improved design of the ARC and by the reduced thickness of the emitter. The plotted 1–R data in Figure 2 shows a significant reduction of the reflectance in this region for
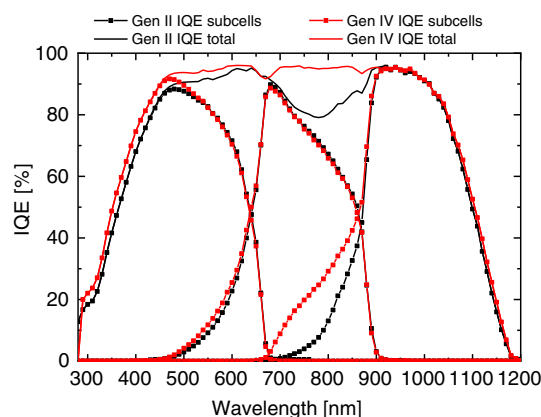
Figure 5. Calculated internal quantum efficiencies of the gen II[6] and gen IV triple-junction solar cells.

the optimized ARC layer thicknesses in the gen IV device. To address the impact of the reduced emitter thicknesses in the III–V subcells, the internal quantum efficiencies (IQE) have been calculated, as shown in **Figure 5**. In the gen IV device, the IQE of the GaInP top cell is significantly higher for $\lambda < 500$ nm, confirming the beneficial impact of the reduced emitter thickness. The same is observable for the GaAs middle cell for $\lambda < 650$ nm. As the GaInP cell thickness is not reduced from gen II to gen IV, the observed increase in IQE for the GaAs middle cell is caused by the change in emitter thickness and not by a higher transparency of the layers above. The small dip at 670 nm in the total IQE (Figure 5) and EQE (Figure 2) of the gen IV device is caused by parasitic absorption in the tunnel junction between the GaInP top and GaAs middle cell.

The IV data in **Figure 6** shows a 27 mV increase in open-circuit voltage from gen II to gen IV. This difference is within the variation of the V_{OC} across different cells on the wafer in the order of 100 mV which is caused by inhomogeneities during the epitaxy and the microfabrication process. As the silicon bottom cell was current limiting in the gen II device, an increase in the short-circuit current to a value of 12.2 mA cm^{-2} is achieved for

|	Gen II	Gen IV
V_{OC} [V]	2.619	2.646
J_{SC} [mA/cm²]	10.0	12.2
FF [%]	85.0	80.2
η [%]	22.3	25.9
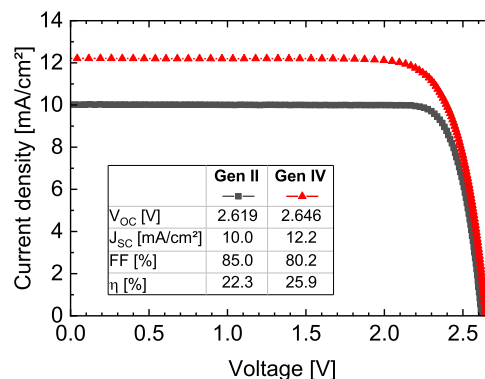
Figure 6. IV characteristics of the GaInP/GaAs/Si triple-junction cells under calibrated AM1.5g conditions, measured with an aperture mask to avoid contribution of current in the Si bottom cell from outside the dedicated cell area. The data of our previous gen II device have been presented in the work by Feifel et al.[6] and are inserted for comparison.

the complete triple-junction device. The fill factor, however, decreased significantly from 85.0% to 80.2%. This is caused by the much more homogeneous distribution of the subcell currents. In the gen II device, there was a substantial current mismatch of $2.8\,\text{mA\,cm}^{-2}$, whereas it is only $1.1\,\text{mA\,cm}^{-2}$ for the recent cell structure. The IV characteristics result in an AM1.5g conversion efficiency of 25.9% for this $4\,\text{cm}^2$ sized triple-junction solar cell which is currently the highest published value for an epitaxial III–V/Si tandem cell. The III–V subcells still have an excess current density over the Si bottom cell and a redistribution of the currents can easily lead to conversion efficiencies beyond 26% in the near future.

Overall, the EQE shows high values above 90% in the relevant wavelength region and is very similar to the EQE of the wafer-bonded GaInP/GaAs//Si triple-junction cell of Cariou et al. with an AM1.5g efficiency of 33.3%,[17] as shown in **Figure 7**. Only in the long-wavelength regime with $\lambda > 1000\,\text{nm}$, the wafer-bonded device shows an increased quantum efficiency which can be attributed to a better passivation quality of the backside of the Si bottom cell and a more effective light-trapping structure which was realized by a diffractive grating. This comparison shows that the current densities of $38.2\,\text{mA\,cm}^{-2}$ for the wafer bonded and $38.0\,\text{mA\,cm}^{-2}$ for the direct growth are nearly the same and that the lower voltage of $2.619\,\text{V}$ compared with $3.127\,\text{V}$[17] is the main limiting factor of the epitaxial structure in the current state. As a consequence, future efforts have to focus on the reduction of threading dislocation densities in the III–V subcells as these defects severely limit the voltage.[18]

Boyer et al. have already demonstrated a threading dislocation density of $3 \times 10^6\,\text{cm}^{-2}$ for a composition of $\text{GaAs}_{0.75}\text{P}_{0.25}$ on Si substrates.[19] Although this step-graded buffer covers only three quarters of the lattice mismatch necessary for the triple-junction devices presented herein, it is a very encouraging result and we expect that similar defect densities can be reached on the GaAs lattice constant in the near future. With threading dislocation densities in the low $10^6\,\text{cm}^{-2}$ regime, a significant boost in open-circuit voltage of above 200 mV can be expected[18] which would, in combination with perfect current matching, enable an efficiency of close to 30%.
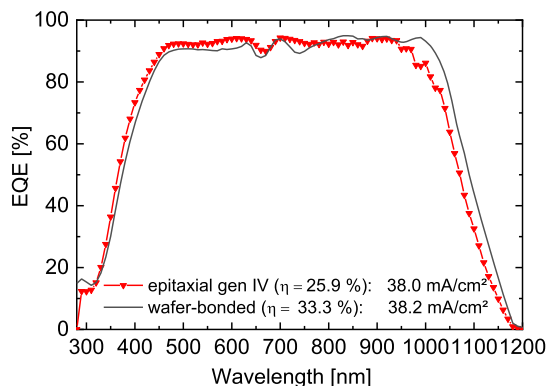
Figure 7. EQE (total) comparison of the epitaxial gen IV and the wafer-bonded GaInP/GaAs/Si triple-junction cells with conversion efficiencies of 25.9% (epitaxial) and 33.3%[17] (wafer-bonded). The integrated total current densities have been calculated under AM1.5g spectral conditions.

5. Conclusions

Based on the previous results, a new generation of GaInP/GaAs/Si triple-junction solar cells grown directly onto silicon has been developed. In our previous gen II device, light was parasitically absorbed within the step-graded metamorphic $\text{GaAs}_y\text{P}_{1-y}$ buffer structure which led to a limitation of the overall current density by the Si bottom cell. By increasing the bandgaps of the individual buffer layers through the use of $\text{Al}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$, the transmittance of the buffer was increased between 670 and 870 nm. Implemented into the gen IV triple-junction solar cell, an increase in short-circuit current density from 10.0 to $12.2\,\text{mA\,cm}^{-2}$ was observed, proving the transparency of the developed buffer structure and enabling an AM1.5g conversion efficiency of 25.9% for this $4\,\text{cm}^2$ GaInP/GaAs/Si triple-junction solar cell. As the current density is already similar to nominally defect-free wafer-bonded GaInP/GaAs/Si cells, future efforts have to focus on reducing the threading dislocation density which is severely limiting the voltage in our device in the current state.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

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Frank Dimroth is heading the department "III–V Photovoltaics and Concentrator Technology" at the Fraunhofer Institute for Solar Energy Systems (ISE). His main fields of research are epitaxial growth of arsenides, phosphides, and antimonides for next-generation multi-junction solar cells. Within the last 20 years he performed applied research in the fields of space and concentrator photovoltaics for electricity and hydrogen production. He was cofounder of the CPV company Concentrix Solar in 2005. He serves as editor of the *IEEE Journal of Photovoltaics* in the area of "III–V, Concentrator and Space PV."

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