

III-V on silicon solar cells reaching 33% photoconversion efficiency in 2-terminal configuration

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Silicon is the predominant semiconductor in photovoltaics. However, the conversion efficiency of silicon single junction solar cells is intrinsically constrained to 29.4%, and practically limited around 27%. It is nonetheless possible to overcome this limit by combining silicon with high bandgap materials, such as III-V semiconductors, in a multi-junction device. Despite numerous studies tackling III-V/Si integration, the significant challenges associated with this material combination has hindered the development of highly efficient III-V/Si solar cells. Here we demonstrate for the first time a III-V/Si cell reaching similar performances than standard III-V/Ge triple-junctions solar cells. This device is fabricated using wafer bonding to permanently join a GaInP/GaAs top cell with a silicon bottom cell. The key issues of III-V/Si interface recombination and silicon weak absorption are addressed using poly-silicon/SiO_x passivating contacts and a novel rear side diffraction grating for the silicon bottom cell. With these combined features, we demonstrate a 2-terminal GaInP/GaAs//Si solar cell reaching a 1-sun AM1.5g conversion efficiency of 33.3%.

Crystalline silicon solar cells have been dominating the photovoltaic market for decades. Today, the overall cost of photovoltaics is driven by system components such as installation, cabling and inverters. Since most of these costs are area-dependent, for a further reduction of the levelized cost of electricity, it is crucial to improve the conversion efficiency. State-of-the-art industrial crystalline silicon solar cells have conversion efficiencies in the range of 20-21% while a few lab-type champion devices reach more than 25%¹⁻⁹, with 26.7%¹⁰ being the current record efficiency. The theoretical Shockley and Queisser radiative efficiency limit¹¹ for silicon solar cells with a band gap of 1.12 eV is 33%. However, due to silicon's indirect bandgap, Auger-recombination becomes the dominant intrinsic loss channel, which reduces the theoretical upper limit to 29.4%¹². Realistic boundary conditions such as the necessity to attach contacts to the cell and incomplete light harvesting reduce the practical efficiency limit to around 27%³. Thus, pure crystalline silicon solar cells are extremely close to their performance limit; new concepts are becoming crucial.

A well-known strategy for increasing solar cell conversion efficiency is the multi-junction architecture in which a set of semiconductor absorbers with appropriate bandgaps are used. This approach reduces thermalization losses arising from the absorption of photons with excess energy compared to the semiconductor bandgap, as well as transmission losses of photons with insufficient energy. Various multi-junction approaches are found in literature. First, solar cells can be integrated in an optical system, splitting the light into different wavelength bands which then are redirected onto solar cells with appropriate bandgap¹³⁻¹⁶. Or alternatively, individual solar cells can be mechanically stacked with separate contacts on each cell, referred as multi-terminal approach^{17,18}. By doing so, no subcells current matching is required if every cell has its own electric circuit throughout the photovoltaic module and its own inverter. An efficiency of 35.9% was recently reported for a mechanically stacked 4-terminal device (GaInP/GaAs on silicon, 1 cm², AM1.5g); by connecting all subcells in series, this device reaches 30.9%¹⁹.

However, all industrially scaled multi-junction cell architectures so far (space application, concentrating photovoltaics or thin film cells) use a 2-terminal approach. This is due to the lower complexity of producing these devices and implementing them into photovoltaic modules. 2-terminal cells can be connected by standard series- or parallel connection with little space between the cells and with only one electric circuit. Moreover, the parasitic absorption in non-photoactive layers is reduced (no intermediate electrodes in the device). Thus, it is expected that 2-terminal cell will also be favourable for future applications of high performance III-V on silicon (III-V//Si – Double slash symbol refers to monolithic 2-terminal integration hereafter) tandem solar cells. Though, it should be mentioned that micro-inverters with high reliability and low cost may enable new architectures for multi-terminal devices in the future. Two material systems are currently discussed as high bandgap absorbers on Silicon: the perovskites²⁰⁻²² and the III-V materials²³⁻²⁶. While the first approach has a clear low-cost potential, its stability and reproducibility are still major issues. In contrast, III-V photovoltaics, while being more expensive, is a proven high efficiency technology, already used in space satellites and concentrating photovoltaics, with champion cell efficiencies up to 38.8% for a 5-junctions solar cell measured at 1 sun and 46% for a 4-junctions devices measured at 508-suns¹⁰. Experimentally, III-V solar cells achieve the highest spectral efficiency among the high bandgap materials and thus appear as ideal tandem partners for silicon, efficiency-wise²⁷. In order to apply III-V on silicon, strategies to grow epitaxial III-V layers directly on silicon have been investigated by generations of scientists²⁸. However, best in class direct grown III-V//Si solar cells with this approach are still limited to ~ 20% efficiency^{29,30}. Indeed, the different lattice constant and thermal expansion

coefficient, but also the combination of polar and non-polar materials and the high sensitivity of silicon to low levels of impurities, remain significant challenges³¹ which require further research and development.

In this work we choose a different approach inspired by the microelectronics sector: surface-activated wafer bonding. While being difficult to scale to high throughput GW manufacturing, this technique bypasses many of the above-mentioned constraints. Thus we use surface-activated wafer bonding to join an independently prepared silicon bottom cell with a GaInP/GaAs top cell, thus forming a monolithic 2-terminal device with three series-connected pn-junctions²⁶. For the silicon bottom cell, we use an advanced architecture with two innovative features. First silicon passivating contacts^{32,33} to enhance the open-circuit voltage of the silicon bottom cell and second a diffraction grating to enhance the internal light trapping of the indirect bandgap semiconductor silicon. The doped poly-silicon/ultra-thin SiO_x contact stack provides an excellent surface passivation for planar surfaces, which prevents recombination at the III-V//Si interface and remains unaltered during the III-V top cell processing. Applying a rear side diffraction grating enables an infrared-optimized design while preserving flat surfaces for the silicon cell^{34,35}. Thus the silicon cell is still fully compatible with the wafer bonding process and the surface area is not enlarged, which would increase effective surface recombination. With this electrically flat and optically structured bottom silicon cell design we demonstrate a 2-terminal 4 cm² III-V//Si triple-junction solar cell reaching a 1-sun AM1.5g efficiency of 33.3%.

III-V//Si solar cell design

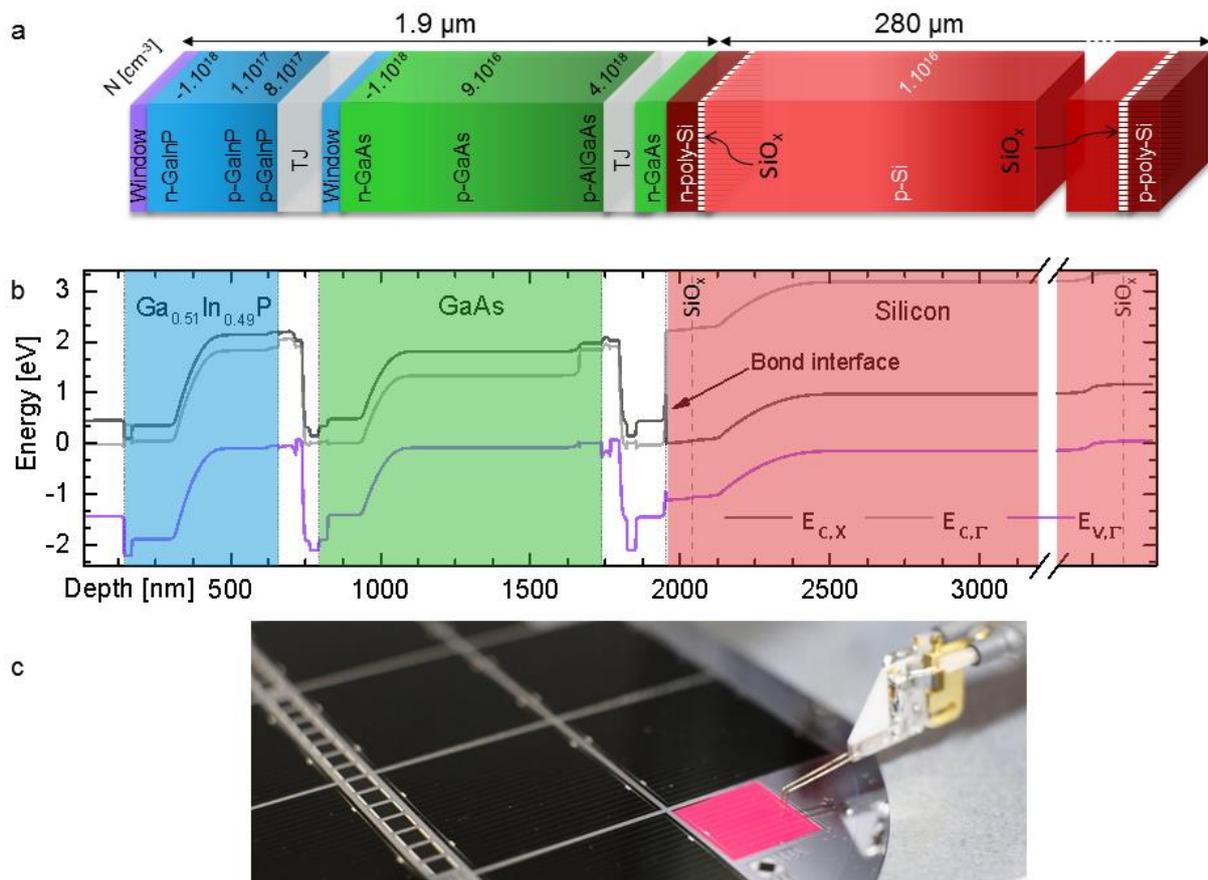


Figure 1 | Structure of the 2-terminal wafer bonded III-V//Si triple-junction cell. **a**, Layer stack (not to scale) of the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{GaAs}/\text{Si}$ solar cell. Subcells are connected by tunnel-junctions (TJ) to form a series-connected 2-terminal device. The light enters the device (left side) through the anti-reflection coating, passes the AlInP window before reaching the 490 nm thick first $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ absorber (1.90 eV direct bandgap). Photons transmitted through the top cell are absorbed in the 880 nm thick GaAs cell beneath (bandgap 1.43 eV) and those transmitted also through the middle cell reach the silicon bottom solar cells (bandgap 1.12 eV). **b**, The semiconductor band structure is shown under open-circuit condition without illumination for the valence band $E_{v,\Gamma}$ (purple line) and the two lowest conduction bands at the Γ (direct transition, grey line) and X (indirect transition, black line) symmetry points of the crystal ($E_{c,\Gamma}$ and $E_{c,X}$ respectively). The $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$, GaAs and Si materials are represented by coloured blue, green and red areas respectively, while the white areas in-between represent tunnel-junction materials. Vertical dashed lines in the silicon area represent ultra-thin SiO_x layers. **c**, Photograph of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{GaAs}/\text{Si}$ triple-junction solar cells (4 cm^2 and 1 cm^2) on a 4 inch wafer. A forward bias applied on the contacted cell results in emission of red light (≈ 650 nm) from the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ top cell.

The layer stack and band structure of the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{GaAs}/\text{Si}$ solar cell fabricated in this study are shown in Fig. 1a,b, while a picture of the final device with bright red electroluminescence (EL) from the GaInP top cell is displayed in Fig. 1c. Both $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ and GaAs are direct semiconductors with the lowest transition energy at the Γ point. This leads to high absorption and allows the III-V layers to have a total thickness of 1.9 μm only.

Photons which are transmitted through the GaAs reach the silicon bottom cell. We use here an advanced p-type silicon solar cell, featuring passivating contacts based on doped poly-silicon layers (90 nm thick) with ultra-thin (~ 1.2 nm) SiO_x on both sides^{32,33}. This architecture, inspired from bipolar junction transistors, was early identified as a promising approach for solar cells^{36,37}. Indeed, the stack of ultra-thin full area interfacial oxides with a doped poly-silicon layer suppresses the recombination of minority carriers while permitting majority carrier extraction from the silicon wafer^{32,38,39}. Due to the fact that silicon is an indirect semiconductor (lowest transition energy at the X point), the absorption of photons near the band edge is significantly lower compared to the III-V top cells. However, as described further in this paper, the optical light path, and thus absorption of long wavelength photons (≥ 1000 nm), can be effectively increased by applying back side diffraction structures on top of the bottom passivating hole contact. Details about the cell fabrication processes are reported in the methods section.

III-V//Si bond interface microstructure

A key point of our approach is the direct crystal connection between the III-V top cells and the silicon bottom cell. Reaching a high performance device in 2-terminal configuration requires a mechanically stable and optically transparent low resistance path for majority carriers at the III-V//Si interface. As shown in Fig. 1a, we connect a n-GaAs 1×10^{19} at./ cm^3 layer directly to the poly-Si bottom cell emitter, with a doping level of 1×10^{20} at./ cm^3 , by means of direct semiconductor bonding⁴⁰ (see method section for process details). Fig. 2a,b,c show schematics of the device; a low magnification GaInP/GaAs//Si cross section scanning transmission electron microscope high-angle annular dark-field image (STEM-HAADF), and a high resolution transmission electron microscope (HRTEM) zoom on the cross section of the GaAs//poly-Si interface are displayed. At the micrometer scale, a sharp III-V//Si interface is visible, but the nanometer scale reveals nonetheless a ~ 1 -2 nm thick amorphous interlayer, which results from the surface sputtering prior to bonding⁴¹. This interlayer enables the transition between the silicon and GaAs crystalline lattices (mismatch of 4 %) and obviates the formation of misfit/threading dislocations which would alter the device performance. Fig. 2d,e,f show a STEM-HAADF zoom on the interface and the corresponding STEM-EDXS silicon and oxygen maps of the area. The ultra-thin tunnel SiO_x appears clearly at the c-Si/poly-Si interface, as well as some remaining oxide from the cleaning procedure at the GaAs//poly-Si interface. Similar interface was reported in the case of GaAs//c-Si bond, which was found to be transparent for photons below the GaAs bandgap and with a low interface resistance²⁶ of only a few $\text{m}\Omega\cdot\text{cm}^2$. Additional STEM-HAADF and STEM-EDXS maps of In, As, P, Al, Ga and Si elements measured on GaInP/GaAs//Si solar cell cross section are shown in supplementary Figure 1.

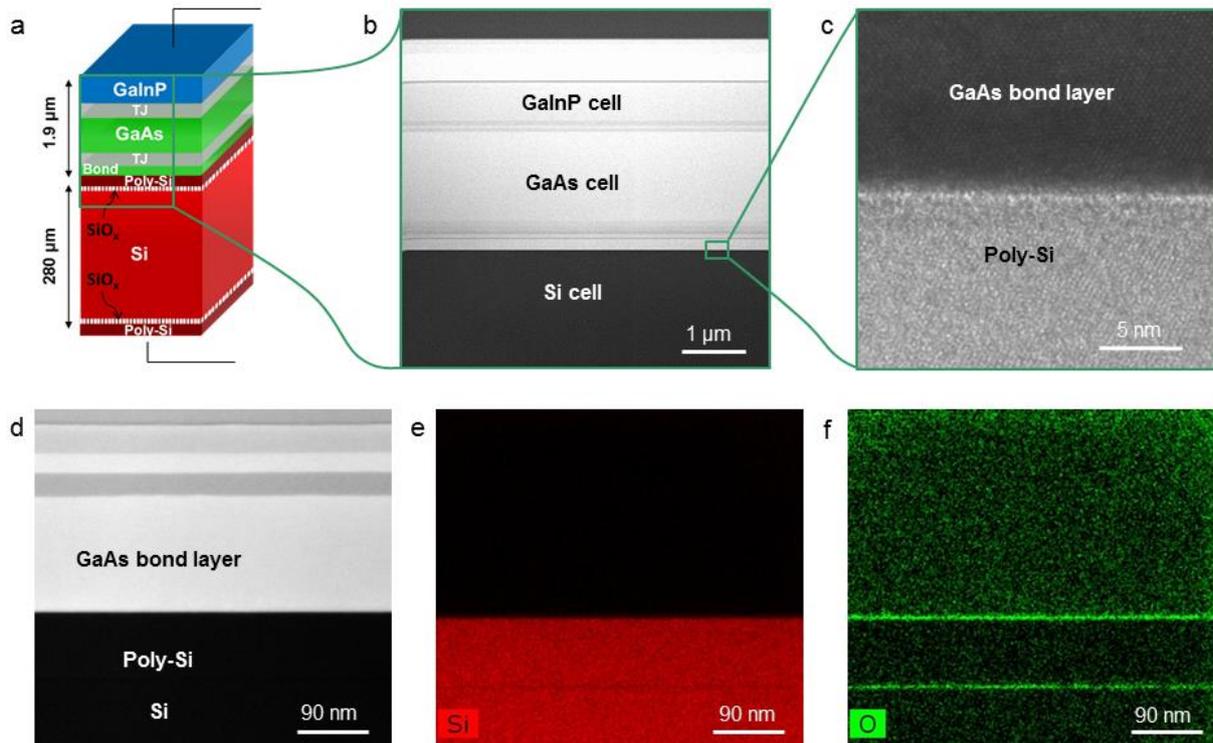


Figure 2 | Characteristics of the III-V//Si wafer bonded interface. **a**, Schematic of the monolithic wafer bonded III-V//Si cell: from top to bottom: GaInP (blue), tunnel junction - TJ (grey), GaAs (green), TJ (grey), bond layer (Green), poly-Si (dark red), SiOx (white dash), Si wafer (red) and SiOx/poly-Si layer back contact. **b**, Cross section STEM-HAADF image of the GaInP/GaAs top cells and the upper part of the Si bottom cell. **c**, HRTEM zoom on the GaAs//poly-Si bond interface. **d**, STEM-HAADF zoom on the GaAs//poly-Si/Si interface; **e**, **f**, STEM-EDX silicon cross section map (red color for Si), respectively oxygen map (green color for O), of the same cross section area.

Planar III-V//Si 2-terminal solar cell performance

A picture of the final solar cell wafer is shown in Fig. 3a: our design features twelve 4 cm² cells and four 1 cm² cells, separated by etched trenches (6 μm into the silicon wafer). The double layer anti-reflection coating results in the general dark appearance of the cells. The distribution of open-circuit voltage (V_{oc}), fill factor (FF) and short-circuit current density (J_{sc}), summarized in Fig. 3c,d,e, has a relatively small spreading with a limited number of outliers. The V_{oc} map, normalized to the best cell voltage (see Fig. 3b), demonstrates the good performance homogeneity. Interestingly, cells with de-bonded areas suffer from strong series resistance but still have high V_{oc} thanks to the effective passivation of the silicon cell. The best cell of the wafer, highlighted on the picture, was measured at Fraunhofer ISE Callab. Fig. 3f shows the External Quantum Efficiency (EQE) of the device which reaches an EQE between 90 and 95% in the 470–1010 nm wavelength range, for a weighted reflection of 2.3% (front metal grid included). From top to bottom, the photo-generated current densities for each junction calculated with the AM1.5g spectrum are 12.7 mA/cm², 13.1 mA/cm² and 11.6 mA/cm². While the GaInP/GaAs top cells are relatively close to current-matching, the planar silicon cell, with weak near infra-red absorption, limits the whole series-connected device. The calibrated IV-curve and cell parameters are displayed in Fig. 3g. With a FF of 0.865 and a V_{oc} of 3.125 V, the cell reaches 31.4% efficiency. With additional electro-luminescence measurements (see methods and supplementary Figure 2 and supplementary Figure 3), we could extract the voltages of the individual subcells: 1.412 V, 1.024 V and 0.692 V from top to bottom. Thus, using the silicon passivating contact approach allows a significant V_{oc} gain of 65 mV compared to a silicon bottom cell with a non-passivated phosphorus doped emitter²⁶. This high voltage demonstrates that the passivating contact architecture is extremely

relevant for silicon-based multi-junctions. However, for this current design, optical simulations clearly reveal that the short circuit current density is limited by the poor light trapping in the double side polished silicon bottom solar cell. Thus, light trapping structures are clearly needed to enhance near bandgap absorption.

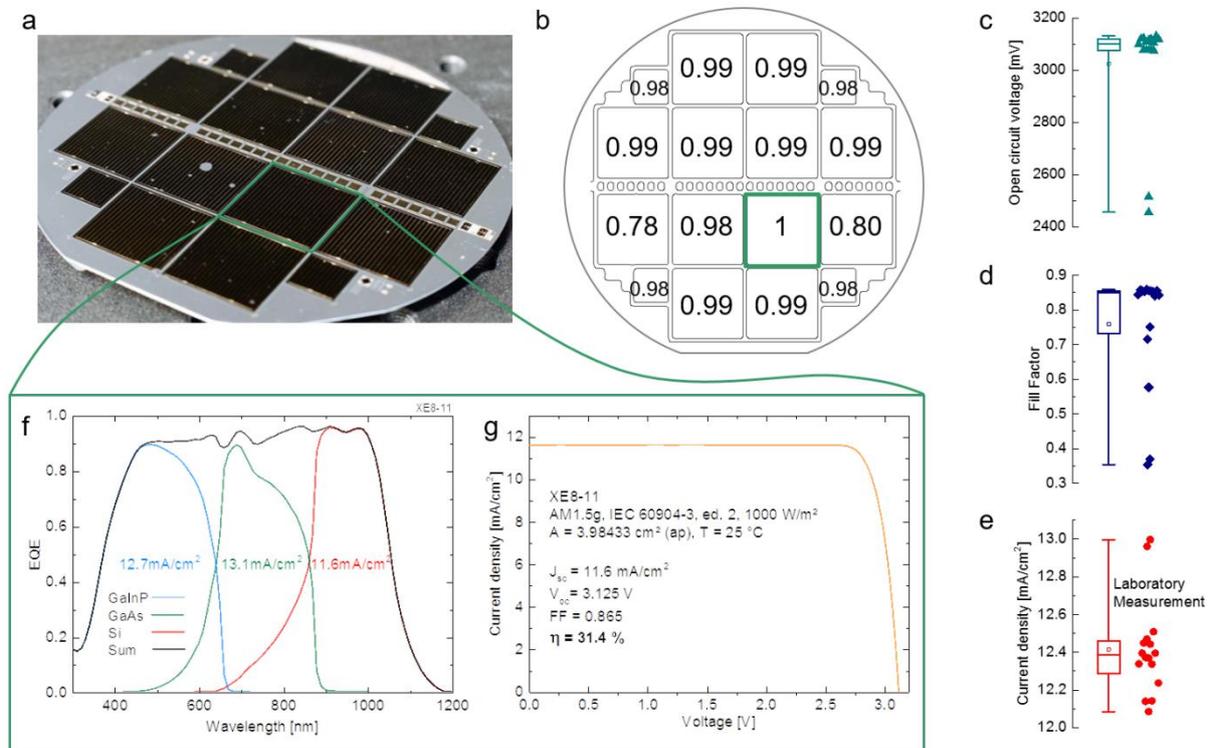


Figure 3 | Performance and statistics of GaInP/GaAs/Si cells without light trapping. **a**, Photo of the 4-inch solar cell wafer with twelve 4 cm² cells and four 1 cm² cells. **b**, Voltage map of the 16 cells, after normalization with the best cell voltage 3.125V. **c,d,e**, Box plots (min-max, 25-75%, mean: open square symbol, median: solid line) showing the statistical distributions of the parameters of the 16 solar cells measured without shading mask (laboratory measurement). **f** External Quantum Efficiency (EQE) of the three subcells as well as the sum of the EQEs, measured at Fraunhofer ISE CalLab. **g**, IV-characteristics measured using a spectrally adjustable solar simulator in the Fraunhofer ISE CalLab, with an aperture of 3.984cm²; the spectrum was adjusted to match the photo-generated current density of each subcell under AM1.5g.

Boosting Si infrared response with photonic light trapping structure

High efficiency silicon solar cells commonly use light trapping features, such as random pyramids on the front (and sometimes rear) side, to compensate for the weak near-bandgap absorption. A structured front side leads to an oblique light incidence inside of the silicon wafer which increases the path length and the probability for total internal reflections in the wafer. However, structuring the front side is not compatible with the bonding process or with direct growth. Integrating random pyramids on the rear side of a silicon solar cell offers efficient light trapping⁴², however passivation of such textured surfaces with p-type poly-Si, as applied at the back side of our device, remains challenging⁴³. Also inverted pyramids and the corresponding passivation/contact structure may degrade during the direct wafer bonding which requires several kN of pressure. Furthermore, the rear texturing and contacting increases the complexity of the overall process flow. Solutions for alternative light trapping concepts based on near field effects, resonances and wave guide modes, which are more relevant for planar and/or thin absorbers are discussed in the literature^{14,44}. As a matter of fact, it is

possible to combine electrically flat interfaces with optically structured rear side designs, to benefit from both: high voltage (low effective surface recombination) and high current. For wafer based silicon solar cells, the effectiveness of this approach was proven with planar single-junction cells having optimized rear side diffraction gratings⁴⁵⁻⁴⁷. As shown, in Fig. 4a, we have developed an optically structured back side beneath the p⁺ passivating contact: it features a diffractive crossed grating made of a polymeric resist, covered with silver that is evaporated on top. We used the nanoimprint lithography technique^{34,35,48} to pattern the diffractive structure at the rear side of our III-V//Si tandem device (details in methods section). The cross section scanning electron microscope (SEM) image of such a poly-Si/resist/silver back side is displayed in Fig. 4b, as well as a SEM tilted view of the grating before metal evaporation (Fig. 4c). The implemented grating goes beyond the state of the art in various respects: the grating consists of a low refractive index epoxy material. Due to the etching step for the removal of the resist residual layer, the epoxy surfaces features a stochastic nanostructure which introduces additional scattering. The silver layer itself is modulated and therefore plays a strong active role in the light trapping. Finally, this photonic light trapping structure acts at the same time as the electrical contact, thus forming a metallic photonic contact layer. The picture of the full wafer back side (Fig. 4d) illuminated with white light confirms the diffractive behaviour of this new back side. This beneficial effect is also confirmed at the cell level (see Fig. 4e). The reflectivity beyond 1000 nm strongly decreases after applying the nanoimprinted grating, reducing the escape loss from light not absorbed in the device by 2.1 mA/cm². This enhanced absorption leads to a 1.1 mA/cm² increase of the photocurrent in the silicon cell as extracted from the EQE. The current increase is lower than the gain in absorption which is attributed to parasitic absorption for example at the interface between rear side resist and metal which turns out to be slightly roughened in the nm scale. The additional current generated by the silicon bottom cell directly improves the triple-junction cell as the silicon subcell was limiting the overall current flow in the series-connected device.

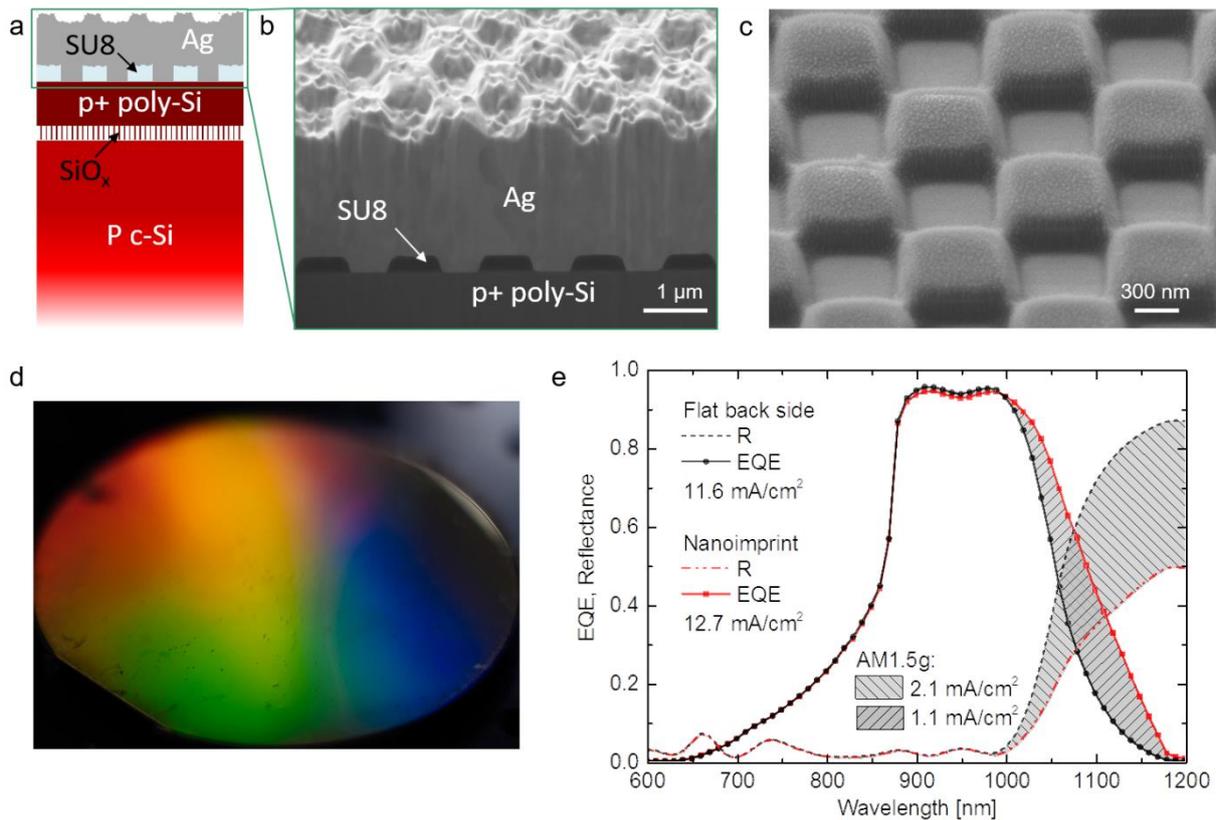


Figure 4 | Enhancing silicon infrared response with photonic light trapping structure. **a**, Schematics of electrically flat (poly-Si back side contact) but optically structured Si back side, with nanoimprinted diffraction grating. **b**, Cross section SEM picture of the Si solar cell with passivated contact and nanoimprint grating (SU8 resist) covered by evaporated metal (Ag). **c**, Tilted SEM view of the nanoimprinted SU8 resist grating before metal evaporation. **d**, Photograph of the 4 inch GaInP/GaAs//Si triple-junction solar cell back side with nanoimprinted grating diffracting the incident light. **e**, Comparison of triple-junction solar cell reflectance (R) and silicon subcell EQE for the same cell before (see Fig. 3f) and after implementing the back side nanoimprint grating.

III-V//Si harvesting one third of the AM1.5g energy

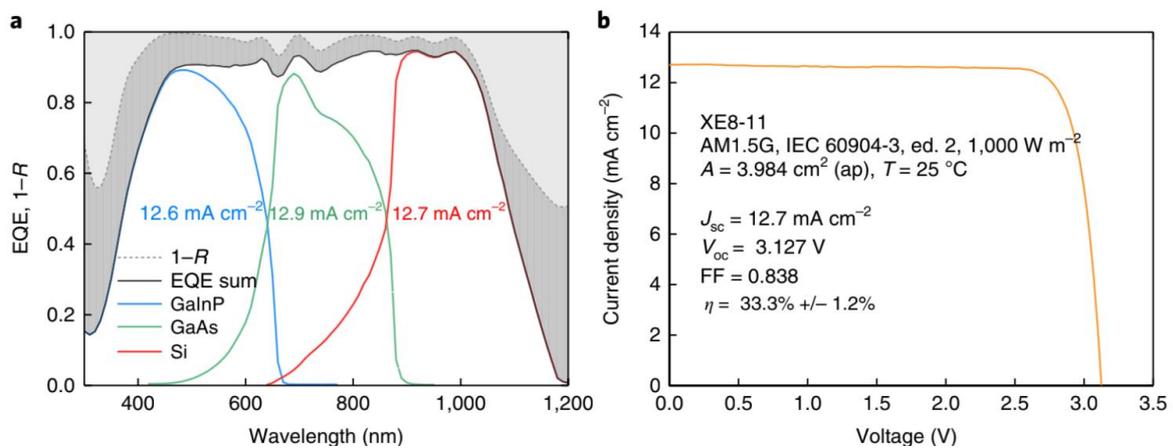


Figure 5 | Performance of best 2-terminal III-V//Si cell with passivating contacts and photonic light trapping structure. **a**, EQE of the three subcells as well as their sum and 1-reflectance (1-R). Escape losses (grey area above 1-R) sum up to 3.8 mA/cm², and recombination and parasitic absorption result in 4.7 mA/cm² losses (hatched grey area). **b**, IV-characteristics measured under a spectrally adjustable solar simulator in the Fraunhofer ISE CalLab, under an aperture of 3.984cm² (see methods for uncertainties); the spectrum was adjusted to match the photo-generated current density of each subcell under AM1.5g.

The planar III-V//Si solar cell wafer shown in Fig. 3 was re-processed, to replace the flat back side silver contact by the above-mentioned diffraction grating. The near-bandgap boost in the silicon bottom cell brings the best device close to current matching: 12.6 mA/cm², 12.9 mA/cm² and 12.7 mA/cm² (from top to bottom) as calculated from EQE measurements (Fig. 5a). Escape losses (area above 1-R in Fig. 5a) sum up to 3.8 mA/cm², and additional losses of 4.7 mA/cm² results from recombination and parasitic absorption (see hatched area in Fig. 5a). The calibrated efficiency of the best solar cell with back side grating reaches 33.3%, as shown in Fig. 5b, thanks to enhanced light trapping in the silicon bottom solar cell which brings the device close to current-matching. The voltage remains unchanged (within measurement uncertainties) and the fill factor decreases slightly due to the better current matching and a small shunt which has been introduced during the rework of the rear side contact. The low shunt resistance of the current limiting GaInP cell allows a higher current to flow at J_{sc} where the GaInP cell is in reverse bias. This explains the difference between the measured current of 12.7 mA/cm² at zero volts compared to 12.6 mA/cm² calculated from the EQE of the current limiting top cell.

The subcell voltages, 1.412 V 1.027 V and 0.689 V (see methods and supplementary Figure 2 and Supplementary Figure 3), are benchmarked against the theoretical Shockley and Queisser limit as well as literature values¹⁰ in Fig. 6a. While just assuming the Shockley and Queisser limit is not sufficient, the comparison with best in class single junction voltages is more relevant, especially when the spectrum filtering from the top cells is taken into account (see Supplementary Table I). Using the bandgap-voltage offset W_{oc} figure of merit⁴⁹, our silicon bottom cell generates a voltage which is only 30 mV lower than the best reported silicon cell after spectrum filtering ($W_{oc} \sim 400$ mV)⁵⁰. The GaAs cell with W_{oc} of 400 mV and the GaInP cell with W_{oc} of 490 mV leave further room for improvements. This underlines the need for better top cell material quality.

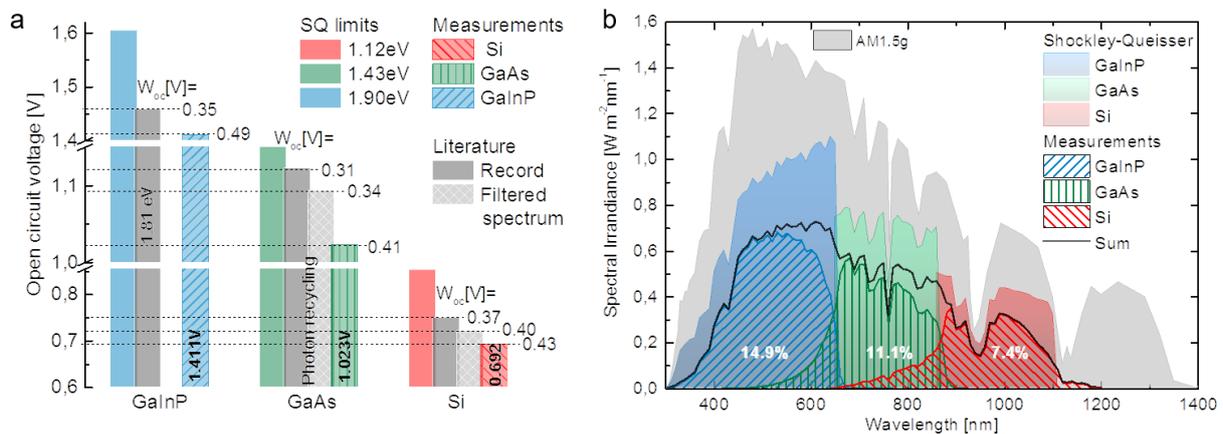


Figure 6 | Benchmarking of 2-terminal III-V//Si cell subcells V_{oc} & spectrum utilization plot. **a**, Benchmark of our subcells open circuit voltages (V_{oc}) with theoretical Shockley-Queisser limit, literature values¹⁰ under 1-sun (1000 W/m²) and filtered spectrum by the corresponding upper cells (333 W/m²). **d**, Utilisation of the 1-sun AM1.5g spectrum by GaInP/GaAs//Si individual subcells in our device. The filled and dashed areas indicate respectively the theoretical (Shockley-Queisser) and measured contributions (using EQE, EL, V_{oc} and FF) of each subcell, and the black line refers to their sum. The absolute efficiency contribution by each subcell to the triple-junction device is: 14.9% Ga_{0.51}In_{0.49}P, 11.1% GaAs and 7.3% Si.

Finally, we evaluate the contribution of each subcell to the power conversion efficiency, using the product $J_{sc}(\lambda) \cdot V_{oc} \cdot FF$ where J_{sc} is extracted from the EQE measurements, FF is the measured value from

the 2-terminal triple-junction IV-characteristics and V_{oc} corresponds to the calculated subcell voltage (see methods section). This calculation leads to the hashed areas in Fig. 6b. The diagram reveals significant losses compared to the idealised Shockley-Queisser (colored areas), which arise from non-radiative recombination and partial transparency of the absorber materials. The total extracted power, i.e. the sum of the three individual curves, corresponds to the black line. Note that the spectrum utilization by the silicon cell beyond 1107 nm is explained by the indirect transitions allowing sub-bandgap absorption. From top to bottom, the absolute efficiency contribution to the triple-junction cell device is: 14.9% $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$, 11.1% GaAs and 7.3% Si respectively.

Conclusion

In conclusion, we have fabricated monolithic 2-terminal III-V//Si triple-junction wafer bonded solar cells featuring an innovative silicon bottom cell design. Highly doped poly-Si/SiO_x passivating and carrier selective contacts were used on both sides of a monocrystalline p-Si wafer. This design was shown to be compatible with wafer bonding and III-V tandem solar cell processing, with the passivation quality remaining un-altered throughout the fabrication process. A silicon subcell open-circuit voltage > 690 mV was achieved under the AM1.5 spectrum filtered by GaInP/GaAs top cells. In addition, we have fabricated a back side diffraction grating, with a nanoimprint technique, which results in an electrically flat but optically structured rear side and strongly enhances the internal light trapping. This leads to a short-circuit current density gain of 1.1 mA/cm² due to near-bandgap absorption enhancement. Our best 2-terminal III-V//Si cell, with a silicon bottom cell featuring passivating, carrier selective contacts and back side diffraction grating, converts 33.3% of the AM1.5g photon energy into electricity. This is a significant improvement beyond the state of art for 2-terminal silicon-based solar cells. The path towards higher performances will be continued by implementing higher bandgap top cells and material quality improvements for the GaInP cell. Then efficiencies in the range of 35% are realistically achievable with a wafer bonded III-V//Si 2-terminal device. Finding a way to scale up this approach and bring the cost down remains an important challenge.

Methods

III-V solar cells epitaxial growth

An inverted $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ (GaInP hereafter)/GaAs dual-junction solar cell structure was grown by metal-organic vapour phase epitaxy onto a (100) GaAs substrate with 6° offcut towards <111> B. The reactor was an AIX2800-G4-TM with an 8x100 mm substrate configuration. The growth was based on Arsine, Phosphine, Trimethylgallium, Trimethylindium, Trimethylaluminium, diluted in hydrogen carrier gas. The pressure during growth was 50 mbar and process temperatures varied between 500 and 700 °C, V/III ratios between 2 and 142. The layer structure starts with a GaAs buffer followed by an n-GaInP etch stop layer and an n-GaAs cap layer which is introduced to form ohmic contacts to the front surface of the solar cell. This layer is selectively removed between the metal grid fingers during device processing. The next layer is an n-AlInP window (indirect bandgap of 2.3 eV) which serves as the front surface field of the top cell. The $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ cell has a p-AlGaInP back surface field followed by a first p⁺-AlGaAs/n⁺-GaInP tunnel diode which changes the polarity from p-type to n-type and allows the series-connection with the GaAs middle cell. The middle cell uses n-GaInP as front-surface field and p-AlGaAs as back surface field and is followed by a second tunnel diode which is composed of p⁺-AlGaAs and n⁺-GaAs. The last layer of the inverted top tandem structure is a n-GaAs bond layer with a high

doping level of 10^{19} cm^{-3} . Chemical mechanical polishing of the last layer was performed at the company III-V Reclaim and resulted in a RMS roughness of $< 0.5 \text{ nm}$. Such a low surface roughness is a requirement for achieving good bond quality.

Silicon solar cell fabrication

Double side polished p-type FZ c-Si wafers ($4 \text{ } \Omega\text{cm}$, $280 \text{ } \mu\text{m}$) were used for the silicon bottom cell. In order to form the poly-Si/SiO_x carrier selective contacts³³, the wafers were dipped in HF followed by an immersion in boiling nitric acid (68 wt%, 110°C) thereby growing a thin tunnel oxide layer. Intrinsic a-Si was then deposited on both sides, in a LPCVD reactor. Thereafter, the n- respectively p-contact layer were formed by phosphorus (P) respectively boron-monofluoride (BF) implantation at low energy. Finally, subsequent to a cleaning step, the wafers received an annealing step in a tube furnace at 850°C (N_2), to activate the implanted species, to remove damage introduced during the implantation step and to recrystallize the a-Si layer. To further improve the surface passivation, the samples were subjected to a remote plasma hydrogen passivation process (RPHP) at 400°C for 30 min. The following doping levels were measured in poly-Si layers: $N_{\text{D,poly}} \sim 1.5 \times 10^{20} \text{ cm}^{-3}$ and $N_{\text{A,poly}} \sim 3 \times 10^{19} \text{ cm}^{-3}$. Prior to wafer bonding, the front n-type poly-Si received chemical mechanical polishing to achieve a low surface particle contamination and RMS roughness; the CMP step removed $\sim 20 \text{ nm}$ of the poly-Si layer thickness, and the resulting RMS roughness was $< 0.5 \text{ nm}$.

Surface activated wafer bonding

Direct semiconductor bonding of the GaInP/GaAs tandem structure to the Si bottom cell was performed at the company EVG in Austria using the EVG580[®] ComBond[®] cluster tool. The process included the transfer of the wafers into a high vacuum ambient ($\sim 10^{-8} \text{ mbar}$), the removal of oxides and hydrocarbons by Combond surface activation (ion beam process) and the room-temperature bonding of the samples under a mechanical pressure of 2.5 kN. A post bonding annealing step at 290°C was performed to enhance bond strength between GaAs and silicon. The bonded wafer pairs revealed low void densities and high bond strengths which was compatible with further cell processing.

III-V//Si Solar cells processing

The GaAs growth substrate was subsequently etched away using a solution of $\text{NH}_3/\text{H}_2\text{O}_2$ which selectively stops on the first GaInP layer. The GaInP etch stop was then removed in HCl giving access to the n-GaAs cap layer. Front side processing followed a sequence of GaAs cap removal between the grid fingers, evaporation and lift-off of a $65 \text{ nm Ta}_2\text{O}_5 / 110 \text{ nm MgF}_2$ double-layer anti-reflection coating, evaporation and lift-off of a metal sequence of Pd/Au/Ge/Ti/Pd/Ag with a total thickness of 2200 nm for the front contact. The contact was annealed at 290°C for 1 minute and the process continued by mesa etching of the cell structure with a depth of $\sim 6 \text{ } \mu\text{m}$ into the silicon wafer to separate adjacent solar cell devices. As a result, on one 4 inch wafer, 12 solar cells with an area of 4.028 cm^2 and 4 cells with area of 1.014 cm^2 were defined. The big cells (respectively small cells) have 4 contact pads (2, respectively) and $5 \text{ } \mu\text{m}$ wide fingers resulting in nominal $\sim 0.8\%$ (1.1%) front side shading. As a last step, silver was evaporated on the Si back side after a short HF-dip.

Rear side light trapping

In order to implement back side light trapping, the Ag back side metal contact was mechanically removed, after solar cell characterizations. In the successive step, a photonic metal structure was realized via nanoimprint lithography (NIL). The master structure, from which the PDMS stamp for NIL was replicated, was realized using interference lithography⁵¹. SU8 photoresist⁵² was directly spin coated on the back side poly-Si, and thermally assisted roller-UV-NIL was used to transfer the pattern

(square pads, pitch 1 μm , depth 250 nm, fill factor 60 %) from the PDMS stamp to the SU8^{34,35,48}. A RIE oxygen/argon plasma step was performed to remove any SU8 photoresist residuals between the pads that additionally implements a scattering nanostructure on top of the grating. This was followed by an HF-dip and Ag evaporation, thus ensuring a good ohmic contact at the poly-Si/Ag interface between the SU8 photoresist pads.

III-V//Si device characterization

Detailed structural and chemical composition of the III-V//Si wafer bonded interface region was studied by transmission electron microscopy at Fraunhofer IMWS. The experiments were conducted on a cross-section lamella prepared by a standard FIB procedure and ex-situ lift out. TEM/STEM studies were performed using a TITAN³ G2 80-300 microscope with X-FEG electron gun at 300 keV, featuring a spherical-aberration corrector, a superX EDXS analyser and a STEM HAADF detector.

The screening of all solar cell performances on the wafer was done with a class A solar simulator from Oriel Corporation equipped with a Xenon lamp. The most promising cells were then characterized in the Fraunhofer ISE calibration laboratory. External Quantum efficiencies (EQE) were measured using a grating monochromator setup with adjustable bias voltage and bias spectrum^{53,54}. Reflection measurements were performed on an integrated LOANA measurement device. 1-sun IV-characteristics were measured under a spectrally adjustable sun simulator with one xenon lamp and two halogen lamp fields which are adjusted in intensity independently of each other in order to generate exactly the same current densities in each subcell as under illumination with the AM1.5g spectrum (IEC 90604-3, ed. 2 with 1000 W/m²). The spectral correction procedure was based on a linear equation system and is equivalent to a generalized mismatch correction procedure⁵⁵. The cell temperature was held at 25°C during the measurement. An aperture mask with an area of 3.984 cm² was placed on top of the III-V-Si solar cell to avoid any contribution of photo-generated carriers from outside the defined cell area. The solar cell results were therefore referring as aperture area measurements, which include shading by the busbars and metal fingers on the front surface of the III-V//Si solar cell. An electroluminescence spectrum was measured by applying a bias voltage to the III-V//Si solar cell and measuring both the resulting forward current density and the emission spectrum between 600 and 1400 nm. Three distinct peaks were observed at 1.90 eV for the disordered GaInP top cell, 1.43 eV for the GaAs middle cell and 1.09 eV for the bottom Si cell. The last value is below the indirect bandgap of silicon of 1.12 eV and correlates with the extended absorption seen in EQE measurements. The spectral electroluminescence together with the EQE and the overall open-circuit voltage of the monolithic device were used to separate the voltage contribution of each of the individual subcells following the procedure in the references⁵⁶⁻⁵⁸. This led to the $V_{oc,meas}$ values for each of the junctions in Figure 6a and supplementary Table 1. The error bar on the efficiency number of the best device is the result of uncertainty analysis taking into account different elements, such as uncertainty of the reference cell, non-uniformity of the illumination of the sun simulator, uncertainty in the measurement of the spectral distribution of the sun simulator, uncertainty in the device area and EQE, adjustment for thickness difference between reference cell and the device under test, adjustment of temperature, etc.

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Author contributions

R.C. carried out experiments in the lab, theoretical modelling and evaluation of the data; together with J.B., they lead the process development and optimization. F.F., M.H. and S.W.G. developed the passivating and carrier selective contact Si bottom cell; S.W.G. also performed the analysis of spectrum utilisation in Fig 5,d. P.B. improved the III-V layer structure and performed the epitaxy growth. D.L. performed band structure simulations and coordinated the epitaxy research. N.R. performed the wafer bonding and coordinated the TEM analysis; M.W. supervised the wafer bonding collaboration and led the design of the EVG580[®] ComBond[®] cluster tool. O.H. and H.H. proposed the idea of the specific rear side diffraction grating and developed and fabricated the crossed grating together. B.B. supported understanding and fine-tuning of the rear side grating and coordinated the photonic light trapping research. G. Siefer supervised the cell calibration and ensured accurateness of the measurements. A.W.B. supported discussions and editing of the manuscript and F.D. developed the concept of 2-terminal III-V-Si tandem cells by direct wafer bonding and he contributed to many aspects of the cell design and process optimization. All co-authors participated in the discussions and improvements of this manuscript.

Data Availability Statement

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Competing interests

The authors N. Razek and M. Wimplinger are employed by EV Group E. Thallner GmbH, 4782 St. Florian am Inn, Austria, which produce the wafer bonding machine used in this study.

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