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Suppression of parasitic electron injection in SONOS-type memory cells using high-*k* capping layers

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Abstract

In this paper the application of thin high-k dielectrics as capping layers on oxide/nitride/oxide memory stacks with respect to suppression of electron injection from the gate electrode during erase operation is investigated. We demonstrate that hafnium silicate layers, with a dielectric constant of 17, as thin as 1nm of physical thickness can clearly reduce electron injection and thereby prevent erase saturation. In theory, tunneling currents will be more strongly suppressed with increasing k values when keeping the equivalent oxide thickness constant. Therefore, the prevention of erase saturation will be further improved. However, titanium oxide as capping layer, which has a dielectric constant of 60, exhibits inferior erase performance due to a strong electron injection by field-enhanced thermal emission of electrons. This Poole-Frenkel conduction mechanism takes place along trapping sites 0.32eV below the conduction band in the titanium dioxide. While the application of high-k materials can efficiently suppress erase saturation due to tunneling currents, this effect can be diminished by leakage currents along shallow trapping sites which occur in high-k dielectrics.

Keywords: hafnium silicate; high-k; SONOS; non-volatile memory

1. Introduction

Scaling of Flash memory devices with charge storage on floating gates is approaching physical limits due to inference between neighboring floating gates. Additionally, inter-poly dielectric and word line have to physically fit between two floating gates to achieve an acceptable gate coupling ratio [1]. Accomplishing this task is becoming more and more difficult using state-of-the-art technology [2]. An approach for scaling beyond these physical limits is the replacement of the floating gate by a charge trapping layer in silicon-oxide-nitride-oxide-silicon (SONOS) memory stacks [1]. These charge trapping devices exhibit fast programming, high reliability and high-density integration [5-6]. However, charge removal during erase operation is severely hampered by electron injection from the gate electrode [3]. Recent approaches to reduce this charge injection from the gate include the application of a metal gate electrode with an adjusted work function. It was demonstrated that for memory stacks with a control oxide of aluminum oxide (Al_2O_3), a work function beyond 5.1eV is required to prevent erase saturation [4]. This restriction regarding the metal work function, however, strongly limits the number of available elements. To allow for a more versatile selection of metals, this paper investigates the application of different high-*k* dielectrics as capping layers on top of the ONO memory stack in order to prevent erase saturation.

2. Experimental

SONOS-type memory capacitors were fabricated on p-type (4-6Ωcm) silicon substrates. First, tunnel oxides of 5nm thickness were grown by dry thermal oxidation. A silicon nitride trapping layer (5nm) was deposited by low pressure chemical vapor deposition (LPCVD) at 790°C. Then, blocking oxides of thicknesses between 3nm and 7nm (as indicated in the discussion) were formed from tetraethyl orthosilicate at 710°C. These SiO_2 layers ensure data retention by

preventing charge loss from the trapping layer. Next, high-*k* capping layers of hafnium silicate ($Hf_xSi_yO_4$) and titanium oxide (TiO_2) were deposited by metal organic chemical vapor deposition from a single source precursor at 550°C or by reactive sputtering at 300°C, respectively. Both types of capping layers were treated by rapid thermal annealing at 900°C for 10s in oxygen ambient to reduce defects in the material. Metal electrodes consisting of 20nm titanium nitride (work function of 4.6eV) and 300nm aluminum were deposited on top of the dielectric gate stacks by sputtering and were patterned by lithography and dry etching. Finally, all samples received a forming gas anneal at 430°C for 30 minutes. Dielectric constants were evaluated by comparison of ellipsometry and CV measurements, and verified by TEM imaging.

3. Results and Discussion

Charge injection experiments were carried out to investigate the impact of capping layers on the control oxide with respect to electron injection from the gate electrode. Figure 1 shows the flatband voltage shift for unstressed memory cells with different control oxides of comparable equivalent oxide thicknesses when applying negative gate bias (erase condition).

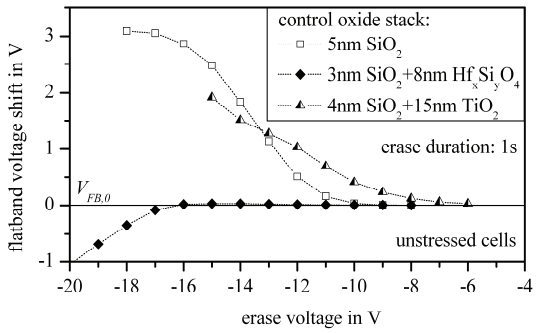

Figure 1: Impact of charge injection under negative gate bias on the flatband voltage shift of SONOS-type memory cells with different control oxide stacks

Although erase voltages are applied, the memory cells with a control oxide of pure SiO_2 (no capping layer) are programmed to more positive flatband voltages (V_{FB}). This so-called "electron back tunneling" effect [4] can be explained from the band-bending diagram in Figure 2 for the case of a control oxide of SiO_2 (without capping). Under high electric fields, a significant Fowler-Nordheim (FN) tunneling current $J_{FN,e}$ of electrons occurs from the gate electrode for negative gate biases.

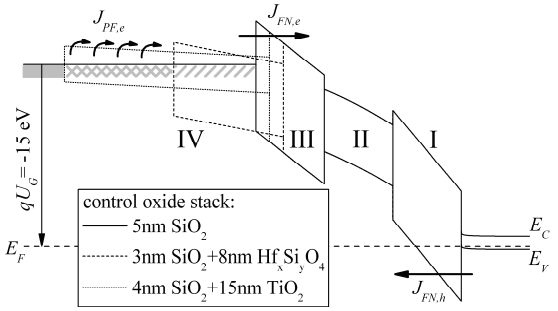

Figure 2: Band bending diagrams of charge-trapping memory gate stacks (I: tunnel oxide, II: trapping layer, III: blocking oxide, IV: capping layer) with different control oxide layers (equivalent oxide thicknesses) under erase condition

Besides the electric field, this tunneling current also depends on the band offset between the gate electrode material and the dielectric in direct contact. Hence, a gate electrode material with a low work function will result in a higher leakage current than a high work function material. The electrons that are injected into the dielectric gate stack become trapped in the memory layer (silicon nitride) shifting the flatband voltage to more positive voltages.

For comparable equivalent oxide thickness (EOT), samples with a capping layer of 8nm hafnium silicate ($k \approx 17$) show negligible V_{FB} shifts for erase voltages up to -16V. This behavior indicates that electron injection resulting from FN tunneling is efficiently suppressed. The reduction of V_{FB} for even higher erase voltages occurs due to a significant FN injection of holes from the substrate $J_{FN,h}$. These holes recombine with electrons in the trapping layer resulting in a flatband voltage shift towards more negative values.

It is very presumable that this hole current also occurs for samples without capping layer. The hole current density injected from the substrate, however, is orders of magnitude smaller than the electron current density injected from the gate. Hence, charge trapping dominates in the samples without capping layer.

In contrast to the samples with $Hf_xSi_yO_4$, the use of 15nm titanium oxide ($k \approx 60$) as a capping layer of the ONO memory stack leads to increased electron trapping in the memory cell as shown in Figure 1. A TiO_2 layer of this thickness efficiently suppresses any tunneling current due to the low electric fields in the di-

electric layer. Therefore, the electron injection responsible for the observed V_{FB} shifts must have another reason. IV measurements indicate that massive electron injection $J_{PF,e}$ takes place due to field-enhanced thermal emission (Poole-Frenkel effect) from trapping sites in the TiO_2. We consider this charge transport mechanism in TiO_2, because current densities through our TiO_2 thin films significantly varied under different annealing conditions prior to metal gate deposition. This observation suggests that trapping sites in the TiO_2 play a major role in current conduction under the investigated conditions. Figure 3 shows a Poole-Frenkel plot for measurements taken between 60°C and 180°C for a TiO_2 thin film of 15nm thickness. Poole-Frenkel conduction occurs via trapping sites located 0.32eV below the TiO_2 conduction band.

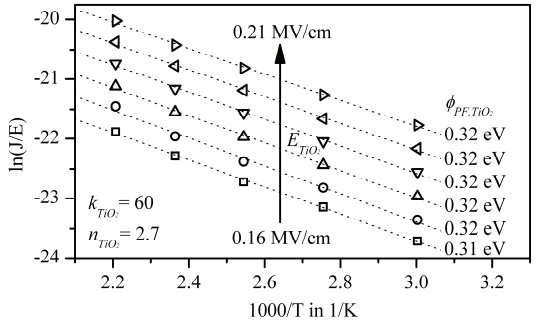

Figure 3: Evaluation of energetic trap depth (Poole-Frenkel plot) of 15 nm TiO_2 layer measured between 60 °C and 180 °C

Electrons trapped in these sites can be easily emitted into the conduction band and drift towards the silicon nitride layer even at room temperature. Eventually, this leads to an undesired trapping of charges in the memory layer. Note that the work function of the gate electrode has little impact on the current density in the case of Poole-Frenkel conduction. Thus, the use of a metal gate with a high work function (e.g. platinum) will not enhance erase performance for these titanium oxide layers.

Even though hafnium silicates are known to have a high density of trapping sites [7], charge trapping during erase operation due to Poole-Frenkel conduction of electrons is not observed for the $Hf_xSi_yO_4$ capping layers. These trapping sites are located 0.80eV below the conduction band as depicted in Figure 4.

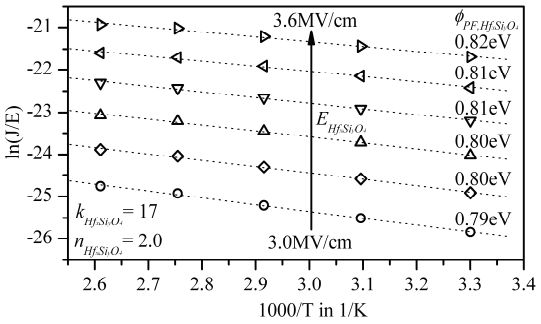

Figure 4: Evaluation of energetic trap depth (Poole-Frenkel plot) of 8 nm $Hf_xSi_yO_4$ layer measured at temperatures between 30 °C and 110 °C

These traps are energetically so deep that current conduction at room temperature is very limited and erase saturation is not observed. For higher electric fields (resulting from erase voltages beyond -16V), the electron current density through the $Hf_xSi_yO_4$ layer is even smaller than the hole current density injected from the substrate and enhanced erase performance is observed as described above.

While the implementation of dielectrics with high dielectric constant reduces electron back tunneling, our measurements show that capping layers with a very high dielectric constant suffer from trap-assisted electron injection from the gate during erase operation. Thus, care must be taken regarding the trapping sites, when choosing a high-*k* dielectric as the capping layer for SONOS-type memory cells.

Next, the scalability of the capping layer is investigated. Erase properties for programmed memory cells with capping layers of 1 nm and 8nm $Hf_xSi_yO_4$ are displayed in Figure 5.

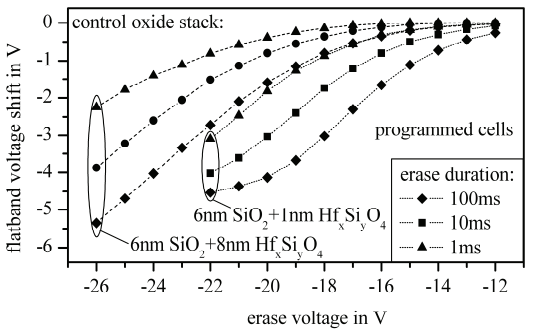

Figure 5: Erase properties of programmed SONOS-type memory cells with hafnium silicate as a capping layers of different thicknesses on top of the control oxide

Application of a thinner capping layer results in a smaller EOT of the memory stack. Hence, a comparable V_{FB} shift already occurs in these devices at lower erase voltages. In fact, a physically 1nm thin capping layer of $Hf_xSi_yO_4$ can sufficiently suppress electron injection compared to ONO stacks without capping, as it is indicated in Figure 6, even though erase saturation is visible to a small extend for U_{FB} shifts beyond -3V. Again, the source of this erase saturation is parasitic tunneling from the gate electrode. In this case, a significant amount of electrons tunnels through the whole $Hf_xSi_yO_4$ layer (1nm) and the triangular barrier of the adjacent SiO_2 blocking oxide (modified Fowler-Nordheim tunneling). Further improvement of erase characteristics using hafnium silicate capping layers may be achieved by the additional application of a metal gate electrode with a work function higher than 4.6eV (e.g., from palladium, gold or platinum).

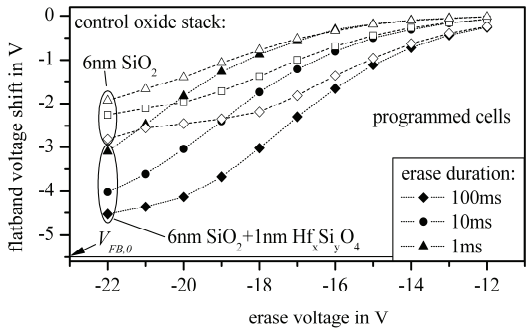

Figure 6: Comparison of erase properties for programmed SONOS-type memory cells with and without a thin hafnium silicate as a capping layer on top of the control oxide

However, noble materials may severely degrade MOS device performance when diffusing into the bulk silicon [4].

4. Conclusion

We have demonstrated that parasitic injection of electrons from the gate during erase operation by FN tunneling can be efficiently suppressed by a thin layer of hafnium silicate even if a gate electrode material with a (low) work function of 4.6eV (TiN) is used.

Charge injection by Poole-Frenkel conduction, however, becomes an issue when a high-*k* material with very shallow trapping sites like TiO_2 is used. Here, major electron injection occurs into the trapping layer, even though tunneling currents are negligible. Therefore, capping layers with very high *k* values do not necessarily suppress electron injection more efficiently than materials with a moderate *k* value do.

Acknowledgements

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References

[1] T.Mikolajick, M.Specht, N.Nagel, T.Mueller, S.Riedel, F.Beug, T.Melde, K.-H.Kusters, *The Future of Charge Trapping Memories*, VLSI Technology, Systems and Applications, 2007, pp.1-4, 23-25 April 2007

[2] International Technology Roadmap for Semiconductors (ITRS), Front End Processes, 2005

[3] T.Erlbacher, A.J.Bauer, H.Ryssel, *Hafnium Silicate as control oxide in non-volatile memories*, Microelectron. Eng. **84**, 2007, pp.2239-2242

[4] S.Jeon, J.H.Han, J.Lee, S.Choi, H.Hwang, C.Kim, Impact of Metal Work Function on Memory Properties of Charge-Trap Flash Memory Devices Using Fowler-Nordheim P/E Mode, IEEE Electron. Dev. Lett. **27**, 2006, pp.486-488

[5] M.H.White, D.A.Adams, J.Bu, *On the go with SONOS*, IEEE Circuits Dev. Mag. **16**, 2000, pp.22-31

[6] C.W.Oh, S.D.Suk, Y.K.Lee, S.K.Sung, J.-D.Choe, S.-Y.Lee, D.U.Choi, K.H.Yeo, M.S.Kim, S.-M.Kim, M.Li, S.H.Kim, E.-J.Yoon, D.-W.Kim, D.Park, K.Kim, B.-I.Ryu, *Damascene gate FinFET SONOS memory implemented on bulk silicon wafer*, IEDM Tech. Dig., Dec. 2004, pp.893-896

[7] T.Erlbacher, M.P.M. Jank, M. Lemberger, A.J. Bauer, H. Ryssel, *HfSiO/SiO$_2$- and SiO$_2$/HfSiO/SiO$_2$-Gate Stacks for Non-Volatile Memories*, Thin Solid Films, In Press, 2008