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Design and Characterization of Highly-Efficient GaN-HEMTs for Power Applications

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Zusammenfassung

Die hervorragenden physikalischen Eigenschaften des Halbleiters Galliumnitrid (GaN) und der darauf basierenden AlGaN/GaN Heterostrukturen eignen sich besonders zur Prozessierung von leistungselektronischen Bauelementen. Die hohe Durchbruchsfeldstärke von GaN in Kombination mit der hohen elektrischen Leitfähigkeit eines polarisations-induzierten zweidimensionalen Elektronengases ermöglicht die Entwicklung von Transistoren mit hoher Sperrspannung, kleinem Durchlasswiderstand und kleinen Schaltladungen. Während die Materialeigenschaften und Technologien kontinuierlich verbessert werden, sollen auch beim Bauteilentwurf Fortschritte erzielt werden.

Diese Arbeit soll durch neue Ansätze beim Entwurf und bei der Charakterisierung von hocheffizienten GaN-Transistoren das enorme Potential dieser Technologie nutzbar machen.

Dazu werden „High-Electron-Mobility Transistors” (HEMTs) in ihren Betriebszuständen untersucht und ihr Verhalten in Bezug zu ihrer Bauteilstruktur analysiert. Hieraus ergeben sich neue Ansätze für den Entwurf dieser Leistungsbauelemente, die hier vorgestellt werden.

Ein Schwerpunkt liegt auf dem flächeneffizienten Entwurf von sehr niederohmigen GaN-Bauelementen. Auf der Basis eines analytischen Modells werden Konstruktionsmethoden für die Entwicklung hocheffizienter GaN-HEMTs abgeleitet. Neben dem Entwurf von interdigitalen Kamm-Strukturen werden neue Layouts für sehr großflächige Bauelemente vorgestellt. Die Layouts sind durch natürliche Flusssysteme inspiriert, wie eine fraktale Kamm-Struktur oder eine Kleeblatt-Struktur.

In vielen leistungselektronischen Anwendungen ist der rückleitende Zustand ebenfalls relevant. Da GaN-HEMTs keine intrinsischen „Body-Dioden” enthalten unterscheidet sich das Verhalten deutlich von herkömmlichen Leistungstransistoren. Diese Arbeit untersucht das Rückflussverhalten einer konventionellen HEMT-Struktur und stellt eine neue, verbesserte HEMT-Struktur mit integrierter Freilaufdiode vor.

Aufgrund kleiner Schaltladungen zeichnen sich GaN-HEMTs durch kleine Schaltverluste aus. Diese Arbeit stellt die messtechnische Charakterisierung von GaN-Transistoren mit sehr kleinen Gate-Ladungen vor. Darüber hinaus wurde in einem eigens dafür entwickelten Pulsmessplatz der Effekt des dynamischen Durchlasswiderstands in einer anwendungsnahen Umgebung bestimmt.

Die gewonnenen Erkenntnisse dieser Arbeit wurden in einem Bauelement-Demonstrator zur Anwendung gebracht. Der GaN-Transistor wurde charakterisiert und seine Eigenschaften mit dem Stand der Technik verglichen. Das Bauelement erzielt den kleinsten flächenspezifischen Widerstand, kleinste Schaltladungen und enthält eine integrierte Freilaufdiode.

Damit trägt diese Arbeit zum Fortschritt und der Entwicklung von noch effizienteren und leistungsfähigeren Transistoren für die Anwendung in der Leistungselektronik bei.

Abstract

The physical properties of gallium nitride (GaN) and the related AlGaN/GaN heterojunctions are ideally suited for the fabrication of power semiconductor devices. The high electrical breakdown field strength of GaN in combination with high conductivity due to a two-dimensional electron gas by induced polarization enables the development of transistors with high off-state voltages, low on-state resistances and low switching charges. While material quality and process technology are continuously improved, also progress in layout developments is required with the same degree of care.

This work wants to push the GaN-technology by new approaches in design and characterization of highly-efficient GaN transistors in order to release its full potential.

High-electron-mobility transistors (HEMT) are investigated in its operating-states and the characteristics are analyzed with regards to the related designs issues. This leads to new design approaches and methods, which are presented in this work.

Particular emphasis is placed on the development of chip area-efficient designs of GaN-HEMTs with very low on-state resistance. Design methods are derived by an analytical on-state model, which was developed in this work. These proceedings are applied to develop highly-efficient GaN-HEMT devices, which generate low on-state losses. Beside the development of interdigital comb-layouts, also new structures suited for very large chips are introduced, as a fractal comb-structure or a clover-structure. These structures are inspired by natural flow systems.

In many applications GaN-HEMTs are operated in the reverse conduction state. A GaN-HEMT can generate significant reverse conduction losses, because GaN-HEMTs do not feature an intrinsic body diode as it is known in conventional power transistors. This work investigates the reverse-state of ordinary HEMT-structures. Furthermore a new improved HEMT-structure with integrated free-wheeling diodes is introduced.

GaN-HEMTs demonstrate low switching losses due to low switching charges. This requires highly sensitive measurement methods and setups. This work presents the characterization of devices with very low gate charges in an advanced measurement environment. Furthermore the developed pulse measurement setup is suited to characterize the degradation-effect of the dynamic on-state resistance.

The findings and design methods are applied to a high-performance demonstrator device. The transistor is characterized in terms of its static and dynamic parameters. In comparison to state-of-the-art power devices the GaN-HEMT achieves the lowest area-specific on-state resistance, lowest switching charges and it features an integrated free-wheeling diode.

This work contributes substantially to the progress and development of highly-efficient high-performance transistors for power applications.

Table of Content

List of Abbreviations

Symbol	**Unit**	**Meaning**
d	[m]	Length of the depletion region
f_{SW}	[Hz]	Switching frequency
f_{T}	[Hz]	Transit frequency
g_{m}	[S], [A/V]	Transconductance
h	[µm]	Height
k	[J/K]	Boltzmann's constant $1.38064852 \times 10^{-23}$ J/K
l_{A}	[µm]	Anode length
l_{AC}	[µm]	Distance between anode and cathode
l_{Ax}	[µm]	Length of an active area with index x (e.g. in fractals)
l_{Bl}	[µm]	Blech length
l_{ch}	[µm]	Channel length
l_{DS}	[µm]	Channel length. The distance between drain and source
l_{G}	[µm]	Gate length
l_{GD}	[µm]	Drain to gate distance
l_{GS}	[µm]	Gate to source distance
l_{MET}	[µm]	Length of a metallization
$l_{\mathrm{MET,crit}}$	[µm]	Critical metallization length
l_{OHM}	[m]	Length of a ohmic contact
l_{SC}	[µm]	Length of a Schottky contact
$l_{\mathrm{SC\text{-}D}}$	[µm]	Length between Schottky contact and drain
$l_{\mathrm{SC\text{-}G}}$	[µm]	Length between Schottky contact and gate
l_{SH}	[µm]	Length of a 2DEG channel segment
l_{XN}	[µm]	Total length of the multi-finger structure in x-direction
m	[1/V]	Gradient at the inflection point of a non-linear capacitance model
n		Exponent of the current density in "Black's equation"
n_{i}	[cm^{-3}], [cm^{-2}]	Carrier density per volume [cm^{-3}] or per area [cm^{-2}]
q	[C]	Elementary charge $1.60217662 \times 10^{-19}$ C
t	[s]	Time
t_{OFF}	[s]	Off-state time
$t_{\mathrm{OFF,STRESS}}$	[s]	Off-state stress voltage time
t_{ON}	[s]	On-state time
$t_{\mathrm{ON,SAMPLE}}$	[s]	Sample time after turn-on
t_{PLS}	[s]	Pulse width
t_{SW}	[s]	Switching time

v_{sat}	[cm/s]	Saturation velocity
x		Index
x	[m]	Dimension or a location
y	[m]	Dimension or a location
z	[m]	Dimension or a location
A	[mm²]	Area
A		Material dependent constant in “Black’s equation”
A_{Active}	[mm²]	Active area on the chip
A_{SC}	[µm]	Width of Schottky contacts
B	[T], [H·A/m²]	Magnetic flux density
B_{SC}	[µm]	Contact to contact distance for GaN-HEMT structures with integrated Schottky contacts
C	[F]	Capacitance
C_{C}	[F]	Coupling capacities, DC-block
C_{DS}	[F]	Drain-source capacitance
C_{GD}	[F]	Gate-drain capacitance
C_{GS}	[F]	Gate-source capacitance
C_{iss}	[F]	Input capacitance
C_{oss}	[F]	Output capacitance
C_{rss}	[F]	Reverse capacitance
E	[V/m]	Electric field
E_{a}	[J], [eV]	Activation energy
E_{C}	[MV/cm], [V/µm]	Critical field strength
E_{g}	[eV]	Bandgap
E_{LOSS}	[J], [Ws]	Energy loss
G'	[S/mm]	Conductance per unit length
I	[A]	Current
I_{CONT}	[A]	Constant current
I_{D}	[A]	Dain current
$I_{\mathrm{D,LEAK}}$	[A]	Drain leakage current
$I_{\mathrm{D,MAX}}$	[A]	Maximum drain current
$I_{\mathrm{D,ON}}$	[A]	Dain current in the on-state
$I_{\mathrm{D,rms}}$	[A]	Root mean square value of the drain current
I_{G}	[A]	Gate current
$I_{\mathrm{G,LEAK}}$	[A]	Gate leakage current
$I_{\mathrm{G,av}}$	[A]	Average gate current
I_{Total}	[A]	Total Current
J	[A/mm²]	Current density
J_{MELT}	[kA/mm²]	Destructive meld current density
J_{S}	[A/mm]	Surface current density

K		Magnetic coupling factor
K_{Bl}	[A/mm]	Critical product of the current density and the “Blech length”
L_{B}	[H]	Inductor as AC-block
L_{D}	[H]	Drain-inductance
L_{DS}, L_{SD}	[H]	Mutual-inductances between drain-source
L_{G}	[H]	Gate-inductance
L_{GD}, L_{DG}	[H]	Mutual-inductances between gate-drain
L_{GS}, L_{SG}	[H]	Mutual-inductances between gate-source
L_{S}	[H]	Source-inductance
N		Number of transistor fingers
P	[W]	Power
P_{A}	[kW/mm^2]	Power density
$P_{\mathrm{A,MELT}}$	[kW/mm^2]	Destructive meld power density
P_{LOSS}	[W]	Static losses
P_{PLS}	[W]	Pulse power
Q_{G}	[C]	Gate charge
Q_{GD}	[C]	Miller plateau charge as part of the gate charge
Q_{RR}	[C]	Reverse recovery charge
Q_{SW}	[C]	General switching charge
R	[Ω]	Resistance
R'	[Ω mm]	Resistance per unit length
R'_{OHM}	[Ω mm]	Ohmic contact resistance
R_{fwrd}	[Ω]	Forward resistance
R_{G}	[Ω]	Gate resistor or resistance between gate and gate-driver
R_{L}	[Ω]	Resistive load
R_{ON}	[Ω]	On-state resistance
$R_{\mathrm{ON,00}}$	[Ω]	On-state resistance assuming no impact of metallization
$R_{\mathrm{ON,DYN}}$	[Ω]	Dynamic on-state resistance
$R_{\mathrm{ON,RVS}}$	[Ω]	On-state resistance in reverse direction
$R_{\mathrm{ON,STATIC}}$	[Ω]	Initial on-state resistance without high off-state stress voltage
$R_{\mathrm{ON}}\cdot A$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance
$R_{\mathrm{ON}}\cdot A_{\mathrm{2D}}$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance of a device with 2-dimensional channel
$R_{\mathrm{ON}}\cdot A_{\mathrm{3D}}$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance of a device with 3-dimensional channel
$R_{\mathrm{ON}}\cdot A_{\mathrm{3D,SJ}}$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance of a device with 3-dimensional channel with homogeneous field shaping
$R_{\mathrm{ON}}\cdot A_{\mathrm{Active}}$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance of active area
$R_{\mathrm{ON}}\cdot A_{\mathrm{Chip}}$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance calculated

		using total chip area
$R_{\mathrm{ON}}{\cdot}A_{\mathrm{MIN}}$	[m$\Omega\cdot$cm^2]	Area-specific on-state resistance assuming no impact of metallization
$R_{\mathrm{ON}}{\cdot}Q$	[m$\Omega\cdot$nC]	Figure-of-merit of efficient, fast-switching semiconductors
$R_{\mathrm{ON}}{\cdot}Q_{\mathrm{G}}$	[m$\Omega\cdot$nC]	Figure-of-merit of efficient, fast-switching semiconductors between off- and on-state
$R_{\mathrm{ON}}{\cdot}Q_{\mathrm{RR}}$	[m$\Omega\cdot$nC]	Figure-of-merit of efficient, fast-switching semiconductors between off- and reverse on-state
R_{SH}	[$\Omega/\square$]	Sheet resistance
$R_{\mathrm{SH,A}}$	[$\Omega/\square$]	Sheet resistance of the active area
$R_{\mathrm{SH,MET}}$	[$\Omega/\square$]	Sheet resistance of the metallization
T	[s]	Cycle time
T	[m]	Thickness
T	[°C]	Temperature
T_{MET}	[µm]	Thickness of the metallization in z-direction
V	[V]	Voltage
V_{++}	[V]	Supply voltage
V_{BD}	[V]	Breakdown voltage
V_{C}	[V]	Cathode voltage
$V_{\mathrm{DR-}}$	[V]	Negative gate driver supply voltage
$V_{\mathrm{DR,OUT}}$	[V]	Driver output voltage
$V_{\mathrm{DR,OUT,OFF}}$	[V]	Low level voltage of the gate driver output
$V_{\mathrm{DR,OUT,ON}}$	[V]	High level voltage of the gate driver output
$V_{\mathrm{DR+}}$	[V]	Positive gate driver supply voltage
$V_{\mathrm{DS,OFF,STRESS}}$	[V]	Off-state stress voltage
$V_{\mathrm{DS,OFF}}$	[V]	Off-state voltage
$V_{\mathrm{DS,ON}}$	[V]	Drain-source voltage in the on-state
V_{fwrd}	[V]	Forward voltage
V_{PLS}	[V]	Input signal of the gate driver
V_{Px}	[V]	Voltage between a field plate $\mathrm{P_x}$ and ground
V_{STEP}	[V]	Lowest level and resolution of a direct voltage
V_{Strip}	[V]	Applied voltage on a metallization test structure
V_{TH}	[V]	Threshold voltage
V_{Total}	[V]	Total voltage
W	[mm]	Finger gate width
W_{crit}	[mm]	Critical gate width
W_{total}	[mm]	Total gate width
X_{CHIP}	[mm]	Chip length in x-direction
X_{periph}	[mm]	Length for peripheral area in x-direction
Y	[S]	Admittance
Y_{CHIP}	[mm]	Chip length in y-direction

Y_{periph}	[mm]	Length for peripheral area in y-direction
Z	[Ω]	Impedance
γ		Propagation constant
ε	[F/m]	Permittivity or dielectric constant
ε_0	[F/m]	Permittivity of free space or the electric constant $\varepsilon_0 = 8.854187817$ pF/m
ε_{i}		Permittivity of the insulator
ε_{r}		Relative permittivity
ε_{s}		Permittivity of the semiconductor
λ	[W/(m·K)]	Thermal conductivity
μ	[cm²/(V·s)]	Mobility of the carriers
μ_{r}		Relative permeability
ρ	[Ω·m]	Electrical resistivity or specific electrical resistance
τ_{RC}	[s]	Time constant of the input -resistance and -capacitance
φ	[V]	Electric potential
Φ	[Wb], [H·A]	Magnetic flux
´		Value per unit length
Ø	[µm]	Diameter

2DEG	Two-dimensional electron gas
4H-SiC	Silicon carbide (4H polytype)
AC	Alternating current
Al	Aluminum (chemical element)
AlGaN	Aluminum gallium nitride
AlN	Aluminum nitride
Au	Gold (chemical element)
BFOM	Baliga’s figure-of-merit
CMOS	Complementary metal oxide semiconductor
CTE	Coefficient of thermal expansion
D	Drain
DC	Direct current
DUT	Device under test
FEM	Finite element simulation
FEMM	Software name: "Finite Element Method Magnetics"
FET	Field effect transistor
G	Gate
GaAs	Gallium arsenide
GaN	Gallium nitride
GATE	Gate metallization
GND	Ground
HEMT	High-electron-mobility transistors
IAF	Fraunhofer Institute for Applied Solid State Physics IAF

IGBT	Insulated-gate bipolar transistor
JFET	Junction field effect transistor
JFOM	Johnson's figure-of-merit (JFOM = $E_C \cdot v_{sat}/(2\pi)$)
$\log_e$	Natural logarithm
LED	Light-emitting diode
MEA	More electric aircraft
MET1	Interconnection metallization
METFP	Gate- and field plate metallization
METG	Electro-plating metallization
MIS	Metal on insulator
MOCVD	Metal organic chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
MTTF	Mean time to failure
Ni	Nickel (chemical element)
OHM	Ohmic contact or ohmic metallization
PAS	Passivation
PCB	Printed circuit board
S	Source
SC	Schottky contact
Si	Silicon (chemical element)
SiC	Silicon carbide
SJ-MOSFET	Super junction metal-oxide-semiconductor field-effect transistor
tanh	Hyperbolic tangent
T	Transistor
TCAD	Technology computer aided design
Ti	Titanium (chemical element)
TLM	Transmission-line-method

1. Introduction

1.1 Motivation

Global concerns such as climate change, overpopulation, and limited resources compel us to make a more sustainable use of the precious energy sources. Advanced ways of savings in the fields of energy generation, conversion, distribution, and consumption are required. In this context electric power is one of the most economical and versatile form of energy and power electronics is its enabling technology. Therefore the demand for advanced power electronic systems is continuously growing.

Power electronic systems cover a wide range of applications and therefore progress in development by means of new key technologies is strongly required:

- The climate change caused by many years of increasing carbon dioxide emissions, the perennial smog alerts in mega-cities, and the limited fossil fuels lead to a rethinking in automotive engineering towards electrical mobility. The electrification of all kinds of vehicles and other former mechanical functions will be enabled by numerous of efficient electronic systems and it will change our understanding of transport and mobility.
- The concept of more electric aircrafts (MEAs) is motivated by the request to improve aircraft performance and to reduce costs. Compact, low-weight power electronic systems will replace conventional, heavy mechanical, hydraulic, or pneumatic systems.
- Rising costs for energy require more and more economical production facilities to stay competitive. Therefore companies invest in efficient industrial plants with advanced power electronics. An energy-efficient and sustainable production saves resources cost and strengthens the company image.
- The energy consumption of the infrastructures for communication- and information-technology, such as network servers or data storage centers, has rapidly grown during the last few years. There is high potential to improve the power supply efficiency up to 50 % for these equipment [1]. In this sector enormous costs and energy can be saved by applying more efficient power converters
- A similar saving potential can be found in the field of solid-state lighting. More than 20 % of the global generated electric power is consumed for lighting [1]. The modern light-emitting diode (LED) technology is efficient but requires also energy efficient voltage converters between power grid and the LED lighting modules. More efficient converters can save large quantities of energy.

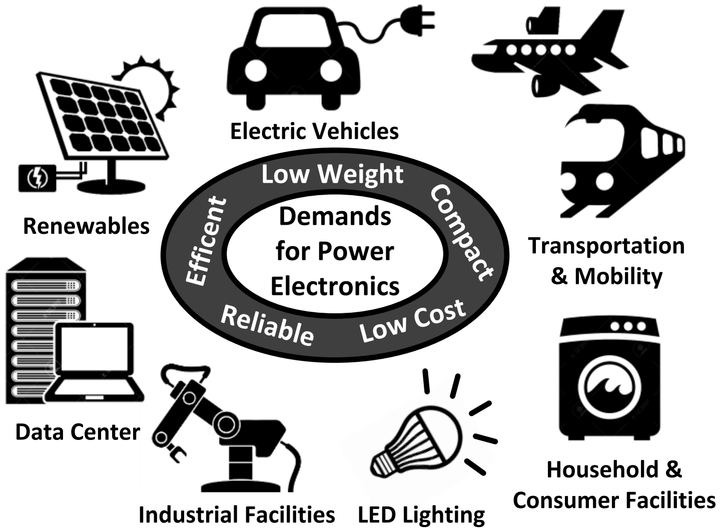

Figure 1: Common demands for prospective power electronics in various applications.

The desires of power electronic systems are recurring. The next generation of power systems has to be high efficient, high compact, with low weight and with low cost. Such developments are only conceivable by new high performance power technologies based on wide bandgap semiconductors, such as silicon carbide (SiC) or gallium nitride (GaN), whereas the conventional technologies based on silicon (Si) are already highly developed and the physical capability is almost exhausted.

SiC components are already established in several market segments, e.g. [1], [2]. In particular SiC Schottky diodes are used as high performance free-wheeling diodes in many power applications. Furthermore SiC field effect transistors (FETs), such as metal-oxide-semiconductor field-effect transistors (MOSFETs) or junction-FETs (JFETs) are applied in several niche markets for high temperature- and high performance applications especially at voltages in the 1200 V class and above. However, high substrate cost and low diameter wafer prevented a widespread introduction in the power device market. It cannot be foreseen that this obstacle can be changed.

Costs are the driving force as well as the barrier in GaN-based technologies. From the technical perspective devices based on GaN-bulk substrate would be very attractive because of low crystal defects by homoepitaxy. But this technology is not marketable due to high wafer cost and low availability.

GaN-on-SiC is established as technology for high frequency high-electron-mobility transistors (HEMT) [3]. SiC carrier substrates feature high isolation, low coefficient of thermal expansion (CTE), low lattice-mismatch and low thermal resistance. These properties are beneficial for power applications. However high wafer cost and low availability of large diameter substrates are barriers to capture high volume markets in power electronics.

A good prospective in the power market has the GaN-on-Si technology. Si carrier substrates are available in high quality at low prices and on large diameter wafers, such as 200 mm and more. Thus the material is compatible to many complementary-metal-oxide-semiconductor (CMOS)-process lines. The epitaxial process for GaN-on-Si is challenging because of the high CTE- and lattice- mismatch, however significant progress has been made such that GaN-on-Si with promising electrical and structural quality became commercially available recently [4], [5]. The thermal resistance of Si is more than 3-times higher compared to SiC. However wafer thinning and advanced packaging can reduce this disadvantage. Thus the GaN-on-Si technology is promised to be a technology with wide bandgap performance (e.g. SiC) at a price in the range of conventional Si technologies today. It's reported in [6] that the market price of a 600 V / 10 A GaN-on-Si device comes down to around 1 $ in the year 2020, which will be in the same range as the price of a Si-SJ-MOSFET at that time. Already today 200 V / 20 A GaN-on-Si devices are commercially available at a price in the range of 6 $. For these reasons GaN-on-Si is a promising technology to conquer many fields in the power market.

Material quality, process technology, and design of GaN-based power devices are still in an early development stage. The existing device designs do not exploit the entire potential of the material and these new technologies. **This work wants to push the GaN-technology by highly-efficient device designs in order to release its full potential.**

1.2 Power Semiconductor Devices in Operation

The design requirements for GaN power devices become apparent in typical applications. Even though such power devices are used in various topologies for different applications, the demands are recurring, and the device performance is determined by the characterization of the different operating states. There are four characteristic operating states for power devices in switching applications:

(1) *Off-state:* The device is non-conductive and no current flows through the switch. Simultaneously the device can block high voltages between drain and source.
(2) *On-state:* The device is conductive and the on-state resistance between drain and source is low. The drain-source voltage is positive and thus high drain currents can flow through the device.
(3) *Switching-state*: The switching-state is a dynamic operating state. During this state the device turns-on or turns-off. This means the device changes between two of the three static states: (1), (2) or (4).
(4) *Reverse-state:* The device is conductive and the reverse on-state resistance is low. The drain-source voltage is negative and high negative drain currents can flow through the device.

In figure 2 the different operating states are illustrated in a typical example of a DC-AC converter application. The topology is connected as half-bridge circuit with differential DC-supplies, two switches with antiparallel free-wheeling diodes, an inductor and a resistive load.

The transistors S_1 and S_2 are switched in a manner that the output voltage above the resistive load obtains a sinusoidal-like shape. The diodes D_1 and D_2 enable a free-wheeling path in case that both transistors S_1 and S_2 are in the off-state and a current is enforced by the inductor. The load current is proportional to the voltage, and it is a sequence of the currents through the switches S_1, S_2, D_1 and D_2. For clarification only the currents of the upper bridge-path are emphasized in figure 2. One is the current in forward direction I_{S1} and the other one is the current in reverse direction I_{D1}. Furthermore the four operating states are denoted with the numbers, which are introduced above. This figure illustrates the time dependent switching behavior and the incidence of each state for a typical application.

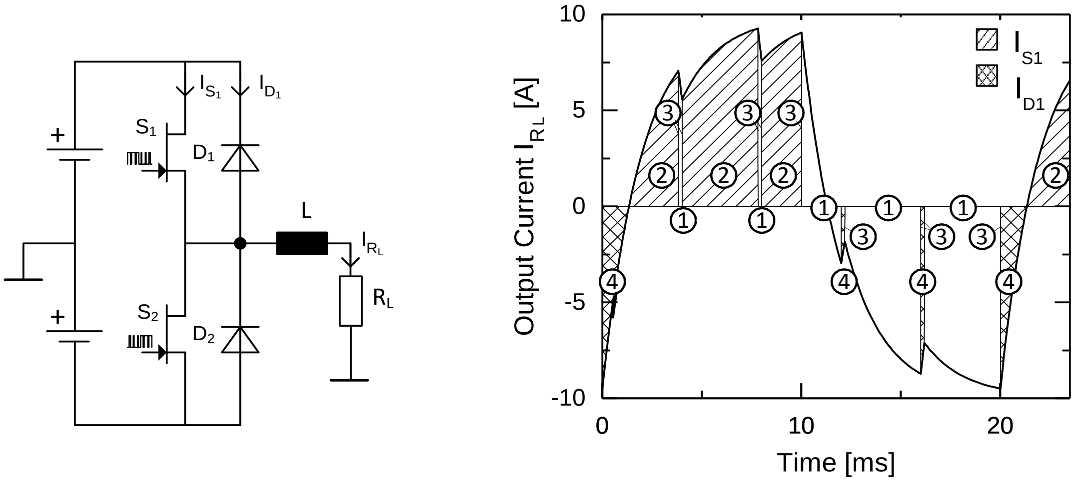

Figure 2: Typical operation and application of power transistors. (Left) Half-bridge circuit with differential voltage sources, two power switches, two reverse diodes, an inductor and a resistive load. (Right) The transient current is monitored through the load. In addition the four operating states are figured and denoted by numbers: (1) off-state, (2) on-state, (3) switching-state, and (4) reverse-state.

The losses in the upper path of S_1 and D_1 can be found by the time signal in figure 2 in combination with the output characteristic of the corresponding power device S_1 and D_1. Such an output characteristic for a GaN-HEMT device is shown in figure 3. Furthermore power hyperbolas are plotted into this graph. In the static-states the operating point is located on these functions (1), (2), and (4) and the corresponding power is dissipated in the devices as heat. The on-state and reverse-state are lossy static operating states, whereas, the leakage current in the off-state is relatively low, and thus the off-state power losses are much lower compared to the losses in the other operating states.

Figure 3 illustrates the output characteristic of a power transistor. The operating point of a devices moves during the switching-state from one static function to another static function. The exact movement of the operating point in the output characteristics depends on the device periphery and parasitics. The difference between a typical load line of a high frequency amplifier and the load line of a converter application with inductive load is illustrated and explained in [7]. In hard-switching applications the load line crosses regions in the output characteristic with very high power. However in efficient hard-switching converters the time of the switching-state is kept small enough such that the switching loss remains small. In this way circuit designers try to minimize the loss energy per switching event. Therewith, the switching losses are a function of the switching frequency of the converter. In many applications high switching frequencies are desirable, because this reduces the volume and weight of energy storage elements, such as inductors or capacitors. This is the motivation to develop fast switching power devices.

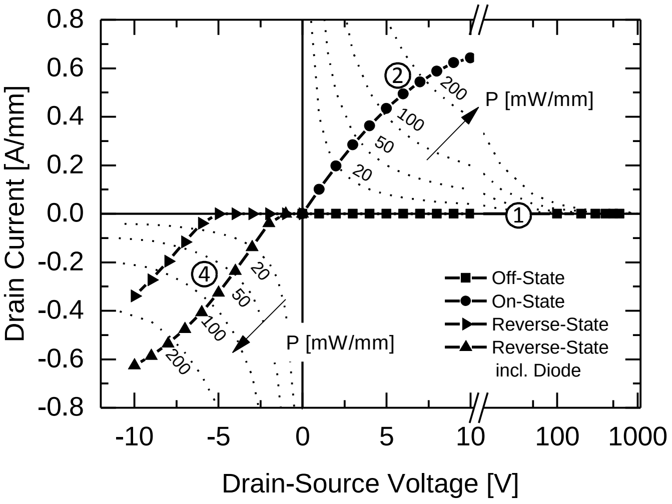

Figure 3: Output characteristic of a high voltage GaN-power device. The different static operating-states are marked by numbers (1, ■) off-state, (2, ●) on-state and (4, ► and ▲) reverse-state. There are two curves shown in the reverse-state. (4, ►) is a typical reverse-behavior of a conventional HEMT. (4, ▲) is a reverse-behavior of a HEMT with integrated free-wheeling diode.

The reverse characteristic of a conventional HEMT without free-wheeling diode depends on the gate-source voltage and it behaves like a JFET, as shown e.g. in [8]. Due to the high forward voltage the conventional HEMT without free-wheeling diode generates high losses in the reverse-state. In order to illustrate the difference there are two functions plotted in the reverse-state of figure 3. The left curve (►) shows the reverse-state for a conventional GaN-HEMT device in the off-state with high forward voltage and high losses, whereas the right (▲) curve shows the reverse-state of a HEMT with free-wheeling diode and low forward voltage.

1.3 What is a Highly-Efficient Power Device?

In general efficiency can be defined as the relation between the output benefit and the input effort or resource. In this context **a highly-efficient power device design performs the appropriate functionality for its application with lowest losses on the given chip area.** In this section the relevant device related figure-of-merits are introduced to allow an evaluation of different devices and designs.

1.3 What is a Highly-Efficient Power Device?

Semiconductor switching devices are affected by several loss mechanisms. These losses can be classified into the static conduction losses and into the dynamic switching losses.

The static losses $P_{\mathrm{LOSS,static}}$ are independent of the switching frequency. These losses are mainly generated in the on-state and determined by the on-state resistance and on-state drain current: $P_{\mathrm{LOSS,static}} = R_{\mathrm{ON}} \cdot I^2_{\mathrm{D,rms}}$. The losses in the off-state caused by leakage currents are relatively low and can be neglected. Thus, a challenge for a chip designer is to achieve a low on-state resistance R_{ON} on a certain chip area A. Therefore the figure-of-merit $R_{\mathrm{ON}} \cdot A$ has been defined to evaluate the chip area-efficiency of a power device. A low value of $R_{\mathrm{ON}} \cdot A$ indicates a high efficiency in the on-state operation with low static losses per chip area.

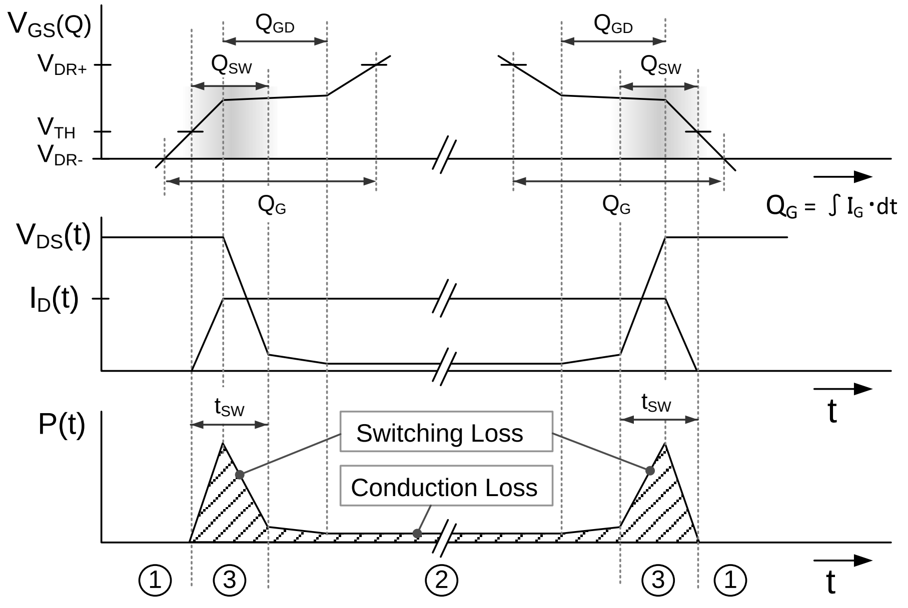

Figure 4: Schematic illustration of the relationship between gate-charge and switching loss-generation in case of a topology with an inductive load.

The switching losses are proportional to the switching frequency f_{SW}, because turn-on and turn-off losses are generated at each switching cycle $T = 1/f_{\mathrm{SW}}$. Thus, if the frequency is increased, there are more switching events and consequently more losses. However as discussed above, high switching frequencies are desired to build compact converter applications. Figure 4 illustrates the switching events of the off-state into the on-state and vice versa. The diagrams show the typical switching behavior of a topology with an inductive load. The drain current rises to its maximum after the gate-source voltage exceeds the transistor threshold-voltage. Afterwards the drain-source voltage decreases from the off-state into the on-state. Switching losses are mainly generated during the switching time t_{SW}. The loss energies for turn-on and turn-off can be approximated by:

$$E_{\mathrm{LOSS,Turn\text{-}On}} \approx V_{\mathrm{DS,OFF}} \cdot I_{\mathrm{D,ON}} \cdot \frac{t_{\mathrm{SW}}}{2}, \text{ and}$$
$$E_{\mathrm{LOSS,Turn\text{-}Off}} \approx V_{\mathrm{DS,OFF}} \cdot I_{\mathrm{D,ON}} \cdot \frac{t_{\mathrm{SW}}}{2}. \qquad \mathbf{(1.1)}$$

Consequently the total losses for such a switching sequence can be written as the sum of static and switching losses:

$$P_{\mathrm{LOSS}} \approx R_{\mathrm{ON}} \cdot I_{\mathrm{D,rms}}^{2} + V_{\mathrm{DS,OFF}} \cdot I_{\mathrm{D,ON}} \cdot t_{\mathrm{SW}} \cdot f_{\mathrm{SW}}. \qquad \mathbf{(1.2)}$$

The first term of this equation represents the static-conduction losses and the second term represents the switching losses. Now the loss relevant device parameters can be determined. The on-state resistance is the device parameter which is responsible for the static losses, whereas the so-called gate charge Q_G is the parameter which is responsible for the switching losses. The losses are generated during the switching time t_{SW} when the channel is charged or discharged by the gate current I_G. The switching time can be written as $t_{SW} = Q_{SW}/I_{G,av}$, whereas the switching charge Q_{SW} is the loss relevant part of the gate-charge Q_G and $I_{G,av}$ is the average gate current during charging time and discharging time. Thus the term of the switching losses can be expressed as:

$$P_{\mathrm{LOSS,SW}} \approx V_{\mathrm{DS,OFF}} \cdot I_{\mathrm{D,ON}} \cdot Q_{\mathrm{SW}} \cdot f_{\mathrm{SW}}/I_{\mathrm{G,av}}. \qquad \mathbf{(1.3)}$$

In literature mostly the total gate-charge Q_G is used as parameter to compare switching losses. Analogous to the area-specific on-state resistance $R_{ON}\cdot A$ the area specific charge Q_{SW}/A can be used as figure-of-merit for power devices.

Even more meaningful is the product of the specific on-state resistance and the specific switching charge $R_{ON}\cdot A \cdot Q_{SW}/A = R_{ON}\cdot Q_{SW}$. The reason is derived in the publication of A. Q. Huang in [9]. Huang has derived the minimal possible power loss per area by minimizing equation (1.2) by assuming $\partial P_{LOSS}/\partial A = 0$. The minimal loss per chip areas is given by:

$$P_{\mathrm{LOSS,min}} = \left\{2 \cdot I_{\mathrm{D,rms}}\sqrt{\frac{V_{\mathrm{DS,OFF}} \cdot I_{\mathrm{D,ON}} \cdot f_{\mathrm{SW}}}{I_{\mathrm{G,av}}}}\right\} \cdot \sqrt{R_{\mathrm{ON}} \cdot Q_{\mathrm{SW}}}. \qquad \mathbf{(1.4)}$$

The first term in the bracket contains the parameter related to the circuit operating conditions. Whereas the second term represents the device related parameters. Thus it is shown that power devices with low $R_{ON}\cdot Q_{SW}$ generated low losses and provide high efficiency. Therefore the product of the on-state resistance and the switching charge $R_{ON}\cdot Q_{SW}$ is known to be a figure-of-merit of power devices for efficient and compact power applications.

This loss model is derived for the switching operation between off-state and on-state. Thus the on-state resistance and gate charge $R_{ON}{\cdot}Q_G$ are the relevant parameter. However as shown in section 1.2 also the reverse-state plays an important role in many power applications and contributes losses which cannot be ignored. Therefore the product of the reverse recovery charge and the on-state resistance in reverse direction $R_{ON,RVS}{\cdot}Q_{RR}$ can be defined as figure-of-merit for the efficient devices between off-state and reverse-state operations. In many conventional power semiconductors the on-state resistance in reverse direction $R_{ON,RVS}$ is equal to the on-state resistance in forward direction thus $R_{ON,RVS} = R_{ON}$. However GaN-HEMT and JFETs can be affected by high forward voltage in reverse direction as shown in figure 3. In this case the on-state resistance in reverse direction $R_{ON,RVS}$ is much higher than on-state resistance in forward direction $R_{ON,RVS} > R_{ON}$ and this operating point generate high losses in the reverse-state.

1.4 Purpose of the Work

The present GaN-heterojunction technologies offer a great potential to replace the currently dominating power device technologies, as the Si-based Power-MOSFETs or the IGBTs. The material quality and process technology is continuously improved. But also the development of device design has to make progress.

This work investigates the potential of the new GaN-heterojunction technologies by introducing advanced design approaches for the development of highly-efficient power devices for the next generation of power electronic systems. The following objectives are the focus of this work:

- Analysis and characterization of the design related behavior of GaN-heterojunction power devices in different operating states. Based on these characteristics new models can be developed and advanced designs can be derived.
- Improving the area-efficiency to enter into competition with the highly-developed, established and inexpensive Si-based power device technologies, as Power-MOSFETs and IGBTs.
- Development of suitable measurement setups to investigate the device specific properties in an environment which is close to the behavior in converter applications.
- Demonstration of outstanding device parameter to enable the development of compact and highly-efficient next generation power electronic systems.
- Improving the device functionality with regard to reverse-state operation adapted to the requirements of the power applications.
- Development of an advanced device performance demonstrator, which is benchmarked against state-of-the-art power device counterparts.

This work significantly contributes to the progress of highly-efficient GaN-based power devices for the next generation power electronic systems.

1.5 Structure and Content of the Work

This work is separated into seven chapters, which are illustrated in a schematic diagram in figure 5. There are two inertial chapters to introduce the topic and the technology. The wide range of the topic of this work: “design and characterization of highly-efficient GaN-power devices” is separated in four subject chapters. The subjects of these chapters are derived by the four operating states of a GaN-HEMT device: off-state, on-state, switching-state, and reverse-state. These four operating states are already introduced in section 1.2. Finally, the derived design methods are applied on a demonstrator device and compared to state-of-the-art power devices. A short description of each chapter is given in the following section.

The introduction in chapter 1 opens up the topic. It points out the motivation, the purpose, and the structure of this work. Furthermore, the scientific questions are derived, explained and posed.

The initial conditions to perform this work are reviewed in chapter 2. At first the theoretical limits for highly efficient power devices are derived. These are used as reference values for the later achieved development results. Subsequently the physical properties of different power semiconductor materials are opposed and discussed. Furthermore, the used process-technology is briefly introduced and its properties are presented. Some experiments expand the standard technology characterization by further power-device-specific parameters. These are required fundamentals to realize the new design approaches, which are presented in the later chapters.

The behavior in the device off-state is mainly determined by the design of the intrinsic HEMT structure, as well as the properties and quality of the technology. In chapter 3 the relevant breakdown mechanisms are discussed. The design and characterization of conventional and new field shaping strategies are presented. These approaches are developed to reduce high electrical field peaks in the HEMT-structure, to improve the device breakdown voltage and the device reliability.

Chapter 4 presents a comprehensive design guide for the development of highly area-efficient GaN-HEMT devices. The design strategies are derived by analytic methods. Origin is the development of an on-state model for lateral finger structures. The theoretical results are verified by experiments and applied to designs from practice. Thus measurement and simulation results are compared with the analytic models. Furthermore, the design and characterization of familiar and new highly-efficient chip layouts are presented, such as the conventional comb-structure, the new clover- and the new fractal-structure. In addition, different on-state specific behaviors are characterized and discussed, such as the effect of self-heating or electromigration.

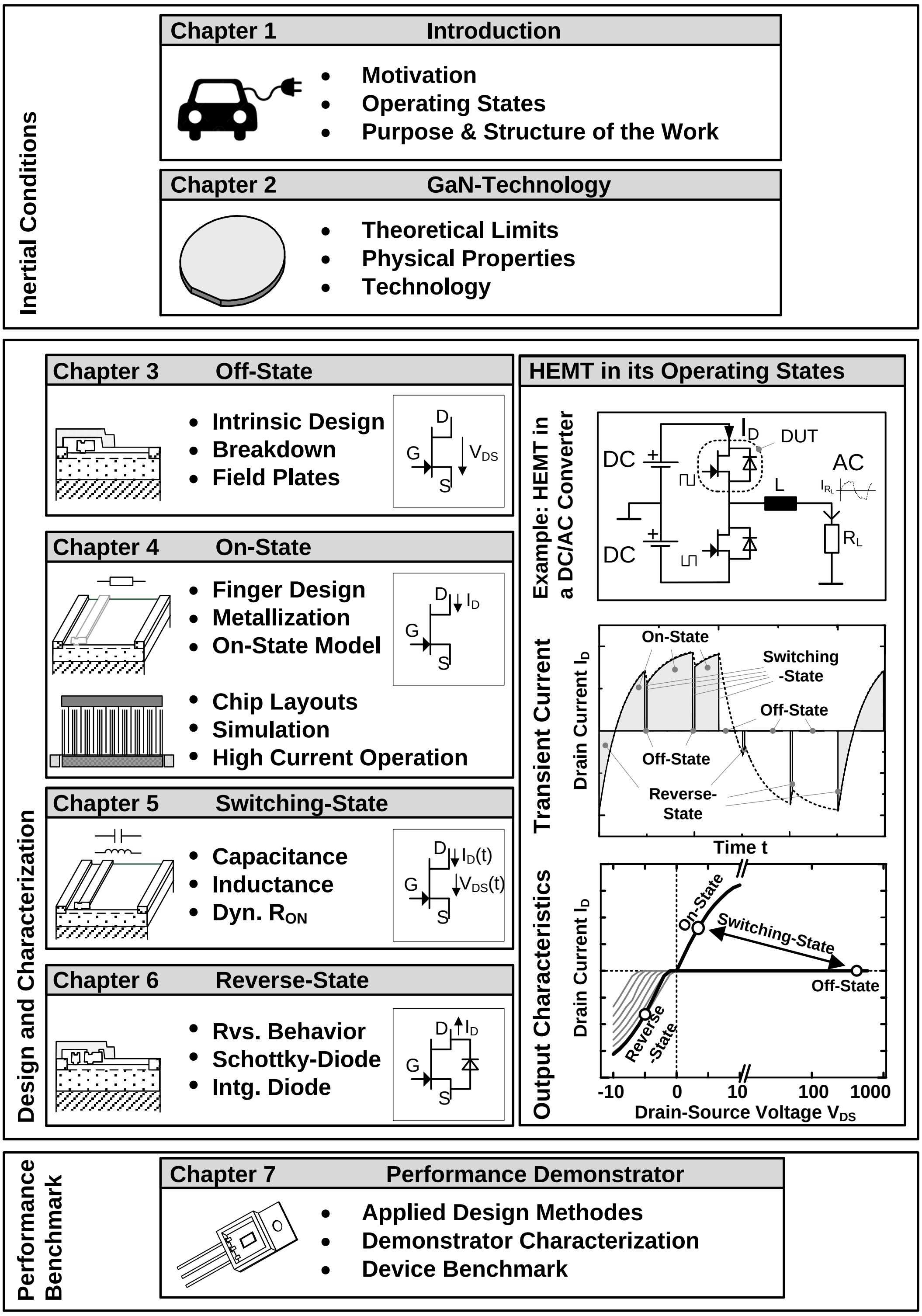

Figure 5 Schematic illustration of the structure of this work. The topic is separated in seven chapters. In the beginning there are two inertial chapters to introduce the topic and the technology. The main chapters about the design and characterization of power HEMTs are categorized by the four operating states of a power transistor. In the final chapter the derived design methods are applied to a demonstrator device. It is characterized and benchmarked to state-of-the-art power transistors.

The characterization of the switching-state is presented in chapter 5. The most relevant dynamic parameters are introduced and discussed. The characteristics were determined using advanced measurement methods, as shown for the parameters dynamic on-state resistance or the nonlinear capacitances. Furthermore the inductive behavior was analyzed by simulations. Finally, the differential equations for an extended small-signal are derived in the general form for a three wire structure in analogy to the static large gate width model in chapter 4.

The reverse-state of GaN-HEMTs is investigated in chapter 0. Conventional GaN-HEMT does not have an intrinsic body-diode as it is known from Si-Power-MOSFETs. Therefore this chapter begins with characterization of the reverse behavior of a conventional GaN-HEMT. An antiparallel diode behavior can be realized by a GaN-Schottky diode. For this reason the intrinsic structure and characteristic of a high voltage diode is investigated and presented. Furthermore, this work introduces a new intrinsic HEMT structure with integrated free-wheeling diodes. Finally, all approaches are summarized and directly compared to measurement results which have been characterized on test structures.

In chapter 7 the findings of the previous chapters are applied to a large-area HEMT layout. This device was fabricated in the presented GaN-on-Si technology and characterized with the methods shown in this work. Finally, the measurement results of the highly-efficient device are compared to other state-of-the-art power devices found in literature.

2. The Fundamentals of the GaN-Technology

2.1 Theoretical Limits

2.1.1 Area-Specific On-State Resistance vs. Breakdown Voltage

A key work regarding the benchmarking of semiconductor materials for power devices is shown in 1982 in B. J. Baliga's publication [10] and later supplementary contributions in [11]. He has shown the limits of the area specific on-state resistance as a function of the breakdown voltage for 3-dimensional channel devices. His findings can be well understood on a simple diode structure as shown in figure 6. The structure consists of a 3-dimensional semiconductor realized as p^+n-diode or Schottky diode device. The chip of this device has a cross-section area, which is the product of the channel width W in y-direction and channel length l_{ch} in z-direction, given by $A = W \cdot l_{ch}$ as shown in figure 6. B. J. Baliga has stated in his work, that the length d of the drift region should be equal to the length of the depletion zone at the breakdown voltage, in order to achieve the lowest drift resistance R_{ON} for the breakdown voltage V_{BD}. The resistance of the drift zone is $R_{ON} = \rho \cdot d/A$, where ρ denotes the resistivity coefficient given by $\rho = 1/(q \cdot n_i \cdot \mu)$.

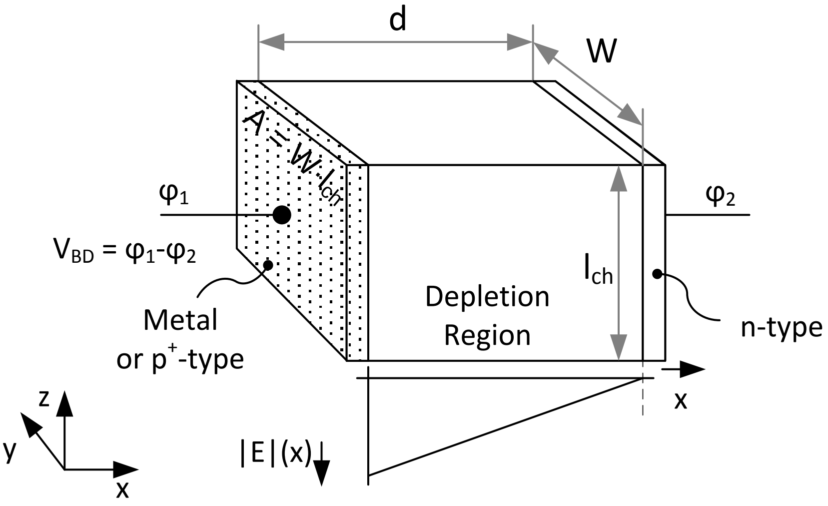

Figure 6: Semiconductor as p$^+$n- or Schottky device with 3-dimensional channel.

The constant of the elementary charge is denoted by q, in semiconductors the carrier density per volume is denoted as n_i with the unit [cm^{-3}] and μ is mobility of the carriers. In the off-state the length of the depletion zone is given by (as shown in literature, e.g. in [12]):

$$d = \sqrt{\frac{2\varepsilon \cdot V_{\mathrm{BD}}}{q \cdot n_{\mathrm{i}}}}, \tag{2.1}$$

where, ε is the dielectric constant. For an abrupt junction as shown in figure 6 the breakdown voltage is given as: [13]

$$V_{\mathrm{BD}} = \int_0^d E(x)\mathrm{dx} = \frac{d \cdot E_C}{2}. \tag{2.2}$$

E_C is the material constant of the critical field strength. With these equations (2.1), (2.2) and with the equation for the drift resistance in a 3-dimensional channel the area specific resistance can be shown as

$$R_{\mathrm{ON}} \cdot A_{\mathrm{3D}} = \frac{d}{q \cdot \mu \cdot n_i} = \frac{4}{\varepsilon \cdot \mu \cdot E_C^3} V_{\mathrm{BD}}^2. \tag{2.3}$$

This formula can be used as theoretical limit for the lowest possible chip area specific on-state resistance as a function of the breakdown voltage, and by using the physical constants the specific on-state resistance can be investigated for several semiconductors. The denominator is known as Baliga's figure-of-merit $BFOM = \varepsilon \cdot \mu \cdot E_C^3$. This value is usually normalized by the value for Si. Baliga's figure-of-merit outlines the potential for different semiconductor materials and is one of the main arguments to push the research and development of wide bandgap semiconductor devices. It will be discussed below in section 2.2 and shown in table 1 that wide bandgap materials, as SiC or GaN, have high critical field strength E_C and high μ carrier mobility. Thus, these materials achieve a low specific on-state resistance as shown in equation (2.3). The theoretical limit, which is derived by Baliga is valid for 3-dimensional channel structures without field shaping. A number of state-of-the-art power semiconductor devices, such as Si SJ-MOSFETs, perform lower specific on-state resistances than predicted by Baliga's limit. This is possible due to field shaping by vertical p-doped trenches. With this approach a homogeneous electric field can be achieved and breakdown voltage shown in equation (2.2) can be increased by factor 2. Thus the breakdown voltage of an ideal field shaped device (e.g. SJ-MOSFET) is given by: $V_{BD} = d \cdot E_C$. With this new condition the area specific resistance can be shown as:

$$R_{\mathrm{ON}} \cdot A_{\mathrm{3D,SJ}} = \frac{1}{2 \cdot \varepsilon \cdot \mu \cdot E_C^3} V_{\mathrm{BD}}^2. \qquad \textbf{(2.4)}$$

The limits in equation (2.3) and (2.4) are valid for devices with 3-dimensional channel, whereas GaN-HEMTs are realized by lateral heterojunction structures with a 2-dimensional channel. W. Saito has shown the theoretical limit of 2-dimensional devices [14] in 2004. He considered the depletion zone with a 2-dimensional channel structure as shown in figure 7. The breakdown voltage of a lateral device is strongly dependent on the shape of the electric field in the depletion zone. To find a theoretical limit for lateral, 2-dimensional devices he assumes a device structure with a slanted field plate.

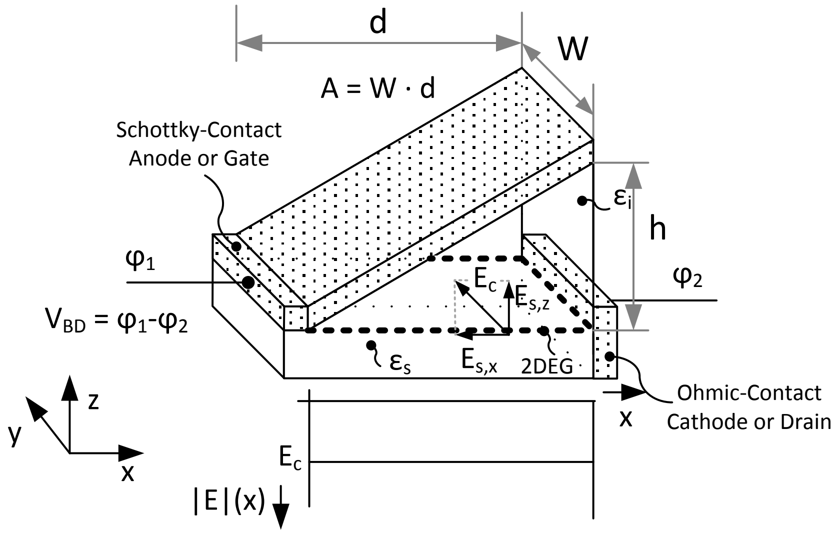

Figure 7: Semiconductor device with 2-dimensional channel and with a slanted field plate.

The device has a lateral, 2-dimensional channel, which is connected to an ohmic contact on one side. On the other side of the channel is a Schottky contact. In this theoretical model the length of the Schottky contact and the length of the ohmic contact are assumed to be very small compared to the length of the depletion- or drift region *d*. Thus it can be neglected and the chip-area of the device is given by $A = W \cdot d$. The structure can be assumed to be a lateral Schottky diode in a heterojunction technology. In this configuration the drift length corresponds to the distance between anode and cathode $d = l_{AC}$. Or the structure can represent the depletion zone of a HEMT structure. Thus the Schottky contact is a gate and the ohmic contact is the drain, and the length of the depletion zone corresponds to the gate-drain distance $d = l_{\mathrm{GD}}$. However the structure as illustrated in figure 7 does not exhibit a complete HEMT structure. The ohmic contact of the source and the drift zone between gate and source are not shown in figure 7. In this theoretical model is it is assumed that the gate-drain distance dominates the HEMT structure and the gate length and gate-source distance is neglected. It is assumed, that the structure has a slanted field plate, which is connected to the Schottky contact. The slanted field plate shapes the electric field in the channel region to be completely homogeneous, thus $V_{\mathrm{BD}} = E_{\mathrm{x}} \cdot d$. According to W. Saito in [14] the lowest drift length for a certain breakdown voltage is achieved, if the electric field in x-direction is equal to the field in z-direction and the magnitude corresponds to the critical electric field strength of the semiconductor, thus $E_{\mathrm{x}} = E_{\mathrm{z}} = E_{\mathrm{C}}/\sqrt{2}$. Under these conditions the breakdown voltage is

$$V_{\mathrm{BD}} = \frac{d \cdot E_C}{\sqrt{2}}. \tag{2.5}$$

In this case the charge of the drift layer is compensated by the field plate charge. This can be expressed by

$$q \cdot n_i = \frac{\varepsilon_0 \varepsilon_i}{h} V_{\mathrm{BD}} = \varepsilon_0 \varepsilon_i E_{\mathrm{z,i}} = \varepsilon_0 \varepsilon_s E_{\mathrm{z,s}}. \tag{2.6}$$

The product of the permittivity and electric field in z-direction in the insulator $\varepsilon_{\mathrm{i}} \cdot E_{\mathrm{z,i}}$ has the same value as the product in the semiconductor $\varepsilon_{\mathrm{s}} \cdot E_{\mathrm{z,s}}$.

In analogy to the area specific on-state resistance for a 3-dimensional channel in equation (2.3), the lowest area specific on-state resistance $R_{\mathrm{ON}} \cdot A$ can be shown for a device with 2-dimensional channel according to [14], to be

$$R_{\mathrm{ON}} \cdot A_{\mathrm{2D}} = R_{\mathrm{SH,A}} \cdot d^2 = \frac{d^2}{q \cdot \mu \cdot n_{\mathrm{i}}} = \frac{2\sqrt{2}}{\varepsilon_S \cdot \mu \cdot E_C^3} V_{\mathrm{BD}}^2. \tag{2.7}$$

It is remarkable the Baliga’s theoretical limit for vertical devices in equation (2.3) and Saito’s theoretical limit for lateral devices in equation (2.7) are nearly the same. Even the lateral limit is slightly lower. However Saito’s limit is a very theoretical limit under ideal electrical field conditions. Such an ideal slanted field plate as shown in figure 7 over the entire channel length is difficult to realize in practice. However, the gate is often processed with slanted side walls as shown e.g. in [15] to reduce field peaks. But such a slanted metallization usually covers only few tens or hundreds of nanometers. Furthermore gate head metallization and other metallizations can be used to build field plates in order to reduce the critical fields. However each abrupt ending plate above the cannel creates new field peaks, which can become critical as well. This topic will be focused in more detail in chapter 3 and chapter 5.

Furthermore, the theoretical model device in figure 7 and in equation (2.7) neglects a number of resistive and area-consuming contributions. A real HEMT structure is shown in figure 8. There are the resistive parasitics of the ohmic contacts of drain- and source metallization, and there is the drift resistance of gate-source channel as well as the channel resistance under the gate. In addition, there are further area consuming contributions. There are the lengths of ohmic contacts for the drain- and source, the distance between gate source and the gate length. The shorter the length of the depletion zones the higher the impact of these additional contributions. Nevertheless, the limit of equation (2.2) is commonly used in literature to illustrate the theoretical limit and compared to the performance of GaN-HEMT devices.

2.1.2 Figure-of-Merit: $R_{\mathrm{ON}}\cdot Q$ vs. Breakdown Voltage

The derivation of the lowest possible area-specific on-state resistance as a function of the breakdown voltage is shown above. The impact of relevant material parameters in terms of area-efficient power devices are stated in equations (2.3) and (2.7). Compared to Si with wideband gap materials it is possible to reduce the on-state resistance per chip area. This feature reduces the on-state losses in power applications. However as Si-chip area is inexpensive, this disadvantage can be compensated by spending more area. But large area devices have higher switching losses, because the larger channel width has to be charged and discharged. In case of a power transistor the switching time is increased by the time constant of the gate resistance and the input capacitance. A low switching charge allows fast switching events with low switching losses. As shown above in section 1.3, the product of the channel charge together with on-state resistance $R_{\mathrm{ON}}\cdot Q$ is considered as figure-of-merit of efficient, fast-switching semiconductors [9].

In this part the theoretical limit of the $R_{\mathrm{ON}}\cdot Q$ product is derived as an extension of Baliga's model. This investigation can be understood by considering the cubical model in figure 6. It was shown that the drift length d is adapted to the breakdown voltage V_{BR} in equation (2.2). Thus the charge of this cubical device is given by $Q = C\cdot V_{\mathrm{BD}}$, and the depletion capacitance C of a Schottky or pn-junction can approximated by the parallel plate capacitor equation $C = \varepsilon\cdot A/d$. This assumption is often found in literature e.g. [16] or [17]. The diffusion capacitor is neglected. With these contributions and equation (2.2) the device charge can be written as

$$Q = C \cdot V_{\mathrm{BR}} = \varepsilon \frac{A}{d} V_{\mathrm{BD}} = \varepsilon \frac{A\cdot E_C}{2}. \qquad \textbf{(2.8)}$$

Now this equation can easily combined with equation (2.3) and the theoretical limit for $R_{\mathrm{ON}}\cdot Q$ is found to be

$$R_{\mathrm{ON}} \cdot Q = \frac{2}{\mu\cdot E_C^2} V_{\mathrm{BD}}^2. \qquad \textbf{(2.9)}$$

This limit is valid for 3-dimensional devices. But the same result can also be derived for the 2-dimensional model by using the equations (2.5) and (2.7) and the charge Q of the 2-dimensional channel, which is calculated by $Q = q \cdot n_\mathrm{i} \cdot A$.

A deviating result is published by A. Nakagawa in [18] and [19]. The result for $R_\mathrm{ON} \cdot Q$ is by factor 2 higher than in equation (2.9). This factor 2 may result from a negligence of the inhomogeneous electric field in the depletion region, which is considered and modelled in this work by equation (2.2). Unfortunately there is no derivation in these two publications of A. Nakagawa.

2.1.3 Power-Frequency Limit

Due to the relatively large channel width and therewith high switching charge in high power devices the switching speed is limited by the time constant of the input -resistance and -capacitance $\tau_\mathrm{RC} = R_\mathrm{G} \cdot C_\mathrm{iss}$. But if we assume an ideal gate driver and this constant is not the bottleneck, then there is another switching speed limit, which is related to the v_sat saturation velocity and the critical field strength E_C. In a drift region homogeneous field the breakdown voltage is given by $V_\mathrm{BD} = E_\mathrm{C} \cdot d$. Furthermore the maximal transit frequency is limited by the v_sat saturation velocity given by $f_\mathrm{T} \leq v_\mathrm{sat}/(\pi \cdot d)$. In combination maximal possible product of transit frequency and breakdown voltage is given by:

$$f_T \cdot V_\mathrm{BD} \leq \frac{E_C \cdot v_\mathrm{sat}}{\pi}. \tag{2.10}$$

This power frequency limit is shown in [12]. In similar form this condition is known as Johnson's figure-of-merit, which is defined as $\mathrm{JFOM} = E_\mathrm{C} \cdot v_\mathrm{sat}/(2\pi)$. Johnson has published this limit in the year 1966 in [20].

2.2 Physical Properties

Different semiconductors are suitable for application as material for high power devices. But power devices based on Si dominate the market today. Si is well investigated, the technology is highly developed and the fabrication is optimized and the costs are low due to large diameter wafer fabrication and mass production. If another semiconductor technology wants to conquer a market it has to prove its benefits beyond Si. Since several decades it is known that there are other semiconductor materials which are better suited for the use in power applications. A path breaking work was published by Baliga [10]. Especially wide bandgap semiconductors are promised to be excellent candidates as materials for power devices. Table 1 presents a comparison of the most important physical material properties for power semiconductor devices. Strong atomic bonds in a crystal structure lead to a wide bandgap between valence- and conduction- band. These materials withstand high electric fields and high temperatures. The high critical electrical field strength is the most important material parameter to develop devices with high breakdown voltage with a short depletion length, and this advantage leads to high power density devices. This point will be discussed in more detail in section 2.1. Furthermore the high melting temperature of the material enables the operation at higher temperatures. In the device on-state high carrier density and high electron mobility are needed for a low channel resistance.

Table 1: Physical material properties of power semiconductors [21].

			Si	GaAs	4H-SiC	GaN	Diamond
Bandgap	E_g	[eV]	1.1	1.42	3.26	3.39	5.45
Intrinsic Carrier Density	n_i	[cm^{-3}]	$1.5 \cdot 10^{10}$	$1.5 \cdot 10^{6}$	$8.2 \cdot 10^{-9}$	$1.9 \cdot 10^{-10}$	$1.6 \cdot 10^{-27}$
Rel. Dielectric Constant	ε_r		11.8	13.1	10	9	5.5
Electron Mobility	μ	[cm²/Vs]	1350	8500	700	1200 (Bulk) 2000 (2DEG)	1900
Saturation Velocity	v_{sat}	[10^7 cm/s]	1	1	2	2.5	2.7
Critical Electric Field	E_C	[MV/cm]	0.3	0.4	3	3.3	5.6
Thermal Conductivity	κ	[W/ cm·K]	1.5	0.43	3.3-4.5	1.3	20

It can be found in table 1 that SiC, GaN, and diamond features promising physical parameters for the development of power devices. A suitable device layout and a suitable process technology are necessary to benefit from these parameters. The next section 2.3 will introduce the GaN-technology, which has been used in this work. Subsequently the following chapters as main part of the work will show how to design advanced GaN-devices in this technology for the use in power applications.

2.3 Technology

2.3.1 Process Technology

The basis of HEMT -development and -fabrication is an advanced high voltage technology. However, this thesis has not the main focus to improve or characterize the technology. This work considers the technology more as an existing framework. In this work the question to be answered is: How should designers apply the given technology to achieve best results? What is the best chip design in terms of efficiency and functionality for the application as switch in high performance voltage converters? None the less, the starting point to achieve these targets is the understanding of the given technology and the relevant technology parameters have to be figured out. This part wants to give a short introduction and a short overview on the used technology. Further details are published in [22], [23], [24], [25].

2.3 Technology

The devices used in this work are fabricated on two different carrier substrates: GaN-on-Si and GaN-on-SiC. SiC carrier substrates have a good thermal conductivity with 3.7 W/cm·K and relatively low lattice mismatch to GaN of 3.1% compared to Si substrates. Si carrier substrates are available in good quality, at low cost and on large diameter wafers. However the lattice mismatch is around 17% and the thermal conductivity of Si is worse with 1.5 W/cm·K. The challenge for the development of a high voltage heterojunction structure is to grow GaN layers with low defect density, high thickness, high isolation and low tensile stress. In this work the technology of the Fraunhofer IAF was used. The epitaxial growth is carried out in an 11×4-inch multi wafer metal organic chemical vapor deposition (MOCVD) reactor. The structure consist of several layers starting with AlN nucleation- and transition layers, a high voltage isolating GaN-buffer, with a total thickness in the range of 2-6 µm, an AlGaN barrier layer and a 3 nm thin GaN-cap layer. The $Al_xGa_{1-x}N$ barrier layer has typically a thickness around 25 nm and an Al-content of around $x = 25\%$. A two-dimensional electron gas (2DEG) with high electron carrier density with high electron mobility is formed at the heterojunction of the GaN buffer and the AlGaN barrier layer due to the piezoelectric and spontaneous polarization effects, which have been analyzed and explained in by O. Ambacher in [26]. This 2DEG is used as conducting channel for the heterojunction power devices. The channel in this work has a sheet resistances as low as $R_{\mathrm{SH,A}} = 500\ \Omega/\square$, with carrier motilities around $\mu = 1500\ \mathrm{cm^2/Vs}$ [25] and sheet carrier concentrations are around $8\times10^{12}\ \mathrm{cm^{-2}}$. Suchlike wafers including the epitaxial grown heterojunction structure are the base material for the further batch-process technology.

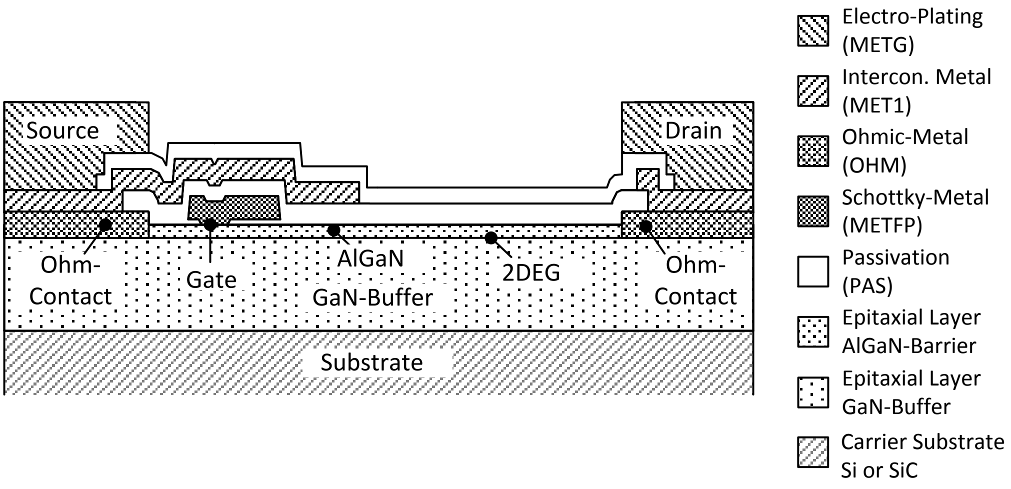

Figure 8: Cross-section of the intrinsic layout of a conventional HEMT-structure in a GaN technology. The device features a Schottky contact as gate, a gate connected field plate, and source connected field plate.

A multi batch-process run contain a series of different treatments with more than 130 single process steps. Typical process steps are fabrication steps like, cleaning, deposition, lithography and etching. A cross-section of a typical high voltage HEMT structure is shown in figure 8. It consists of several metallization and passivation layers, ohmic contacts and Schottky contacts, which will be explained in more detail below. The sheet resistances of the channel and the metallization are of higher importance in this work. Therefore especially the metallization layers are named by abbreviation, as shown on the right side in figure 8. Furthermore the metallization and its resistive behavior will be introduced in this section.

The batch process starts with the realization of the ohmic contacts. The ohmic contacts are realized by a Ti/Al/Ni/Au metal stack, which is annealed at a temperature of around 825°C. These contacts create an electrical connection between a metallization and the 2DEG channel and are mainly used for drain and source contacts in GaN-HEMT structures. A typical value of the contact resistance between channel and metallization is around $R'_{\mathrm{OHM}} = 0.2\ \Omega\ \mathrm{mm}$ as shown in [24] and [25]. Furthermore an ohmic contact can be used as lateral conductor. However the ohmic contact metallization (OHM) is thin and it has a relatively high sheet resistance in the range of $R_{\mathrm{SH\ OHM}} = 2\ \Omega/\square$. After the fabrication of the ohmic contacts the wafer has still a connecting heterojunction (2DEG) on the entire wafer area. The 2DEG is primarily used as active channel for HEMT structures or diodes. All other areas have to be isolated. This isolation of these passive regions is achieved by Argon ion implantation. The value of carrier density in the heterojunction is very sensitive to the charges on top of the wafer, which can modify the surface potential and this changes the carrier density in the channel. Thus the semiconductor surface has to be passivated on top of the wafer by a SiN layer to stabilize the surface potential. A Schottky contact can be realized by opening this passivation layer and by processing a metallization-semiconductor interface using a Ni/Au-based metal stack. Such Schottky contacts are used as gate-contacts for the HEMT devices in this work. Furthermore, Schottky contacts are used as free-wheeling diode contacts as shown in chapter 0. The smallest length dimensions of the structure are mainly limited by the lithography equipment used. The gate metallization (METFP) overlaps the Schottky contact opening of the SiN passivation. Such a metallization overlap can be used as a field plate. The functions and the different designs of field plates will be explained in chapter 3. The so-called field plate metallization (METFP) has a sheet resistance in the range of $R_{\mathrm{SH,METFP}} = 0.1\ \Omega/\square$. This metallization (Ni/Au-based) is typically used as gate-metallization as well as for the gate-connected field plate (as shown in figure 8), and in this work it is often used as one of the interconnection metallizations. Subsequently a further SiN passivation layer is deposited on top of this metallization. Thus the field plate metallization (METFP) is isolated to the next following interconnection metallization layer above (MET1). This Au-based metallization layer can be connected vertically by a via-process with the ohmic metallization (OHM) or the (METFP) below. The sheet resistance of this interconnection metallization layer (MET1) is in the same range as for the field plate metallization (METFP). It has a value in the range of $R_{\mathrm{SH,MET1}} = 0.1\ \Omega/\square$. The metallization (MET1) is used for a wide range of purposes. It is mainly used as metallization for interconnections. But it is also used as source connected field plate as shown in figure 8. In the next process steps the metallization (MET1) is coated by a further SiN-passivation (PAS) layer. Finally, there is a fourth low resistive Au-based metallization (METG) processed by electro-plating on top of this passivation. This metallization is able to carry high currents because of its high thickness in the range between

5-10 µm and it has a low sheet-resistance with a value of $R_{\mathrm{SH,METG}} = 0.002\ \Omega/\square$. It can be vertically connected by a second via-process to the interconnection metallization (MET1). This metallization (METG) is used for bond pads as well as for low resistive, high current interconnections. In this manner the metallization (METG) is used as drain- and source-finger metallization to carry the drain- and source currents in the on-state along a HEMT finger structure. A protecting final SiN passivation is deposited on top of the (METG) metallization and opened only at the bond pads.

2.3.2 Characterization of Capacitive Structures

Capacitive test structures have been developed in this work to characterize the field dependent behavior of the different channel segments of the used GaN-technology. The results of this characterization are a basis for understanding the design of field plate structures in section 3.3.

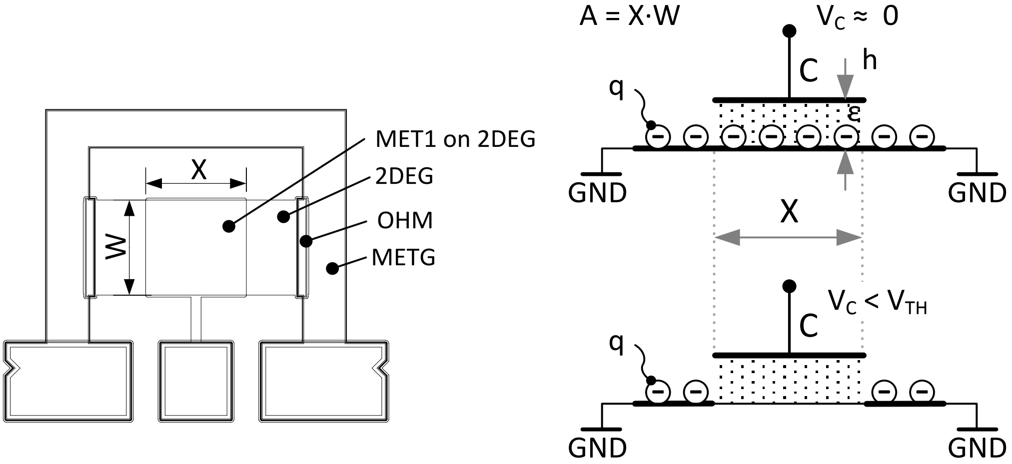

Figure 9: Experiment of the capacitance behavior of different metallization-plates over the 2DEG channel. (Left) Top view of the test structure. (Right Top) Channel segment with a metallization electrode on top without an applied voltage. Carriers are in the channel. (Right Bottom) Same setup as shown above, with a negative voltage, which is applied on the electrode. Carriers under the plate are removed, due to a negative voltage $V_C < V_{TH}$.

The left side of figure 9 shows the layout of such capacitive test structure. The structure consists of a rectangular metallization over a 2DEG channel area. The metallization has an area of $A = 0.1 \times 0.1\ \mathrm{mm}^2$. The channel area with the 2DEG has a larger area compared to the metallization area and it is connected to a metallization via ohmic contacts. The height h of the isolation between the channel and metallization is much smaller compared to the length X and width W. There are carriers in the channel due to the heterojunction in case that no voltage is applied on the metal plate. The channel area $A = X \cdot W$ under the plate has the charge $Q = q \cdot n_i \cdot A$. As long as there are carriers in the channel, the channel is conductive. Together with the metallization it can be seen as a parallel plate capacitance. Thus the structure can be treated like a parallel-plate capacitor, with $C = \varepsilon_0 \cdot \varepsilon_r \cdot A/d$. This capacitance can be measured by a capacitance meter. If the voltage is decreased on the plate the carriers will start to deplete under the plate. The charge in the channel under the electrode will be completely removed, when the product of the capacitance and the voltage is equal to the initial charge $Q = C \cdot V$. This voltage is the corresponding threshold voltage V_{TH} for the tested metallization. If the carriers are removed, then the channel area is an isolator and the parallel-plate behavior is disappeared. The value of the capacitance will decrease drastically. This experiment has been made for different metallization layers. The results are shown in figure 10. Four different structures have been realized in the layout, which is shown in figure 9.

One segment is realized with a Schottky contact area by using the gate metallization (GATE). The others test structures are realized as metal on insulator (MIS) contacts by using the gate metallization (METFP), the first metallization layer (MET1), and the electroplating metallization (METG). As discussed above each metallization type has a different dielectric condition between channel and metal. The capacitance remains constant until all carriers are removed. If the threshold voltage is exceeded, then the channel segment is nonconductive and the capacitance falls by more than a decade.

The determined values are and listed in table 2. As one might expect, the larger the separation between channel and metallization, the lower is the threshold voltage of the structure and the lower is the capacitance.

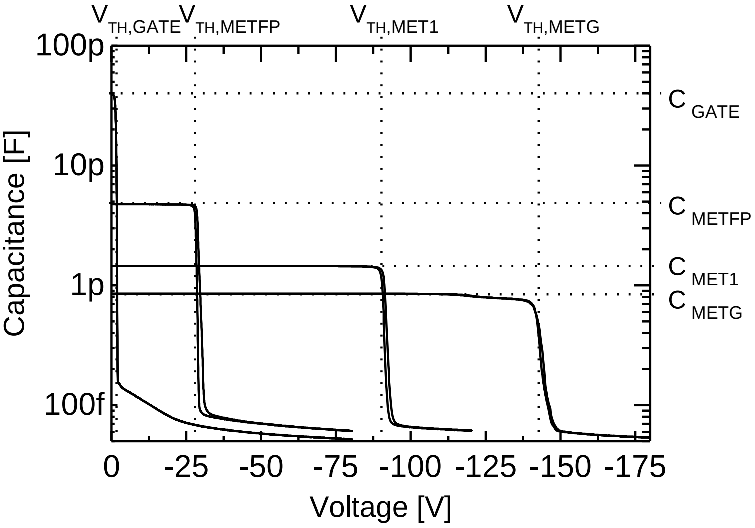

Figure 10: Measurement results of the capacitance behavior of metallization plates over the 2DEG channel. The parallel-plate capacitors area is $A = 0.1 \times 0.1$ mm². The measurement results are shown for different metallization layers as a function of the voltage.

The determined charge values for the different MIS-structures are very similar, whereas the metal-semiconductor Schottky contact is slightly depleted. The test structure with the Schottky contact has a channel charge value which is about factor 2 smaller compared to the MIS-structures. The stack of dielectric isolators between metallization and channel is not uniform. It consists of different layers and it has several interfaces. Thus the dielectric constant, which was found in this experiment, is partly related to the physical material dielectric constant, as well as partly related to the technology-specific properties. It may behave non-linear due to complex interface states and trapping effects.

Table 2: Structure dimensions and determined values extracted by the measurement results on Schottky and MIS-capacitance structures.

Structure			Schottky	METFP	MET1	METG
Area	A	[mm²]	0.1×0.1	0.1×0.1	0.1×0.1	0.1×0.1
Dielectric Height	h	[nm]	25	100	400	700
Threshold Voltage	V_{TH}	[V]	-1.8	-28.5	-91	-145
Capacitance	C	[pF]	39	4.7	1.5	0.9
Charge	Q	[pC]	70	135	132	124
Carrier Density	n_i	[cm^{-2}]	$4.4 \cdot 10^{12}$	$8.4 \cdot 10^{12}$	$8.2 \cdot 10^{12}$	$7.7 \cdot 10^{12}$
rel. Dielectric Const.	ε_r		11.0	5.4	6.6	6.7

The parameters, which have been found in this experiment, and listed in table 1, are used later in this work to explain and to estimate the behavior of more complex HEMT structures. However interface states can influence the dielectric layers and change its ideal behavior. Additional investigations regarding capacitance-voltage profiling for this technology can be found in [27].

2.3.3 Characterization of the Metallization

Characterization of the different metallizations is of particular importance in this work. It will be shown in chapter 4 that the non-ideal properties of the metallization layers and the interconnections play a primary role for high efficient GaN-transistors. The standard low power characterization values of process monitor measurements are not sufficient to predict and design power devices capable of carrying high currents. Therefore characterization structures have been developed to investigate the properties under high current pulse conditions.

Different metallization strips have been measured in pulsed mode ($t_{PLS} = 0.1$ ms) on-wafer in a four-point measurement setup. The different test structures are investigated for different metallization layers, the metallization of the ohmic contacts (OHM), the metallization of the gate metallization (METFP), the first metallization layer (MET1), which is used for field plates and interconnections, and the electroplating metallization (METG) which is used for low resistive, high current-carrying interconnections. Furthermore the investigations were made on two different carrier substrates: GaN-on-Si and GaN-on-SiC. Wafers were processed in the same batch under the same conditions.

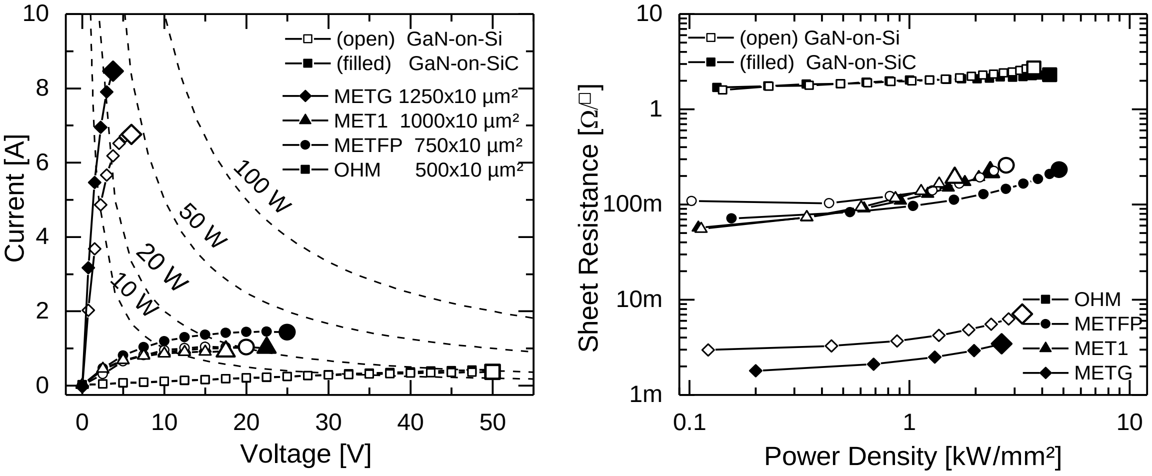

Figure 11: Measurement results of high current pulse tests on metallization strips with $l_{\mathrm{MET}} = 10$ µm. (Left) Total pulse current as function of the voltage. (Right) Sheet resistances as a function of the power per unit length are shown for the different metallization strips. (Conditions) on-wafer 4-point measurement under pulsed conditions with $t_{\mathrm{PLS}} = 0.1$ ms. The wafers are unthinned and at room temperature.

The measurement results are shown in figure 11. Compared to the other metallizations the electro plating metallization (METG) has the lowest sheet resistance. It has a thickness in the range of 5-7 µm and thus this metallization-strip carries high currents with more than 5 A. However due to the high power pulse it already melts at low voltages below 5 V, whereas the ohmic contact metallization (OHM) has the highest sheet resistance. On this metallization structure the destruction due to melting occurs at low currents but at high voltage in the range of 50 V. Thus the failures are power dependent. Both technologies, GaN-on-Si and GaN-on-SiC achieve a similar performance. In direct comparison GaN-on-SiC seems to be a bit more robust. This was expected because of the lower thermal resistance of SiC, such that the metallization is better cooled and it can withstand high power pulses.

Table 3: Measurement results of the short pulse stability test of passive metallization strips with $l_{\mathrm{MET}} = 10$ µm. The sheet resistance of different metallization strips is performed. Furthermore, destructive melt power density was determined and the melt current density was calculated.

	$W \times x$	$R_{\mathrm{SH,Strip}}$	$P_{\mathrm{A,MELT}}$	$P_{\mathrm{A,MELT}}$	J_{MELT}	J_{MELT}
Unit	[µm × µm]	[Ω/□]	[kW/mm²]	[kW/mm²]	[kA/mm²]	[kA/mm²]
Conditions		1kW/mm²	GaN-on-Si	GaN-on-SiC	GaN-on-Si	GaN-on-SiC
OHM	500×10	2	3.6	4.3	736	714
METFP	750×10	0.1	2.8	4.8	257.5	254.75
MET1	1000×10	0.1	1.6	2.3	206	287.6
METG	1250×10	0.002	3.2	2.6	97	121

$T = 20$ °C, $t_{\mathrm{PLS}} = 0.1$ ms

Another representation of the measurement results is shown in figure 11 (Right). The results are plotted as sheet resistance as a function of the power per unit length. In this diagram it can be shown that all metallization strips meld in the range of $P_A \approx 3$ kW/mm². This value is independent of sheet resistance or metal thickness. But it needs to be considered that these measurement are pulsed with a pulse time of $t_{PLS} = 0.1$ ms. Under continuous conditions the strip would melt earlier. The over current time and short circuit robustness time for power devices in other technologies, as Power-MOSFETs or IGBT is in the range of 5-10 µs, which is 10 time shorter than the pulse time used in this experiment.

The sheet resistances for the different metal layers are given in table 3. The measurements are made at a high power density at $P_A = 1$ kW/mm². Furthermore destructive meld power per unit length is given as meld current density.

Table 4: Measurement results of high current pulse stability test of passive metallization strips with a length of $l_{MET} = 10$ µm and a width of $W = 1250$ µm. The influence of measure pulse time and wafer temperature on the sheet resistance is determined.

T	t_{PLS}	$R_{SH,Strip}$	$R_{SH,Strip}$
[°C]	[ms]	[Ω/□]	[Ω/□]
		GaN-on-SiC	GaN-on-Si
20	0.1	0.0016	0.0020
20	1.0	0.0017	0.0021
100	0.1	0.0020	0.0024
100	1.0	0.0020	0.0025

METG, $R_{SH,Strip}$ at $V_{Strip} = 1$V

In table 4 the temperature behavior has been characterized for the electroplating metallization (METG). The sheet resistance is measured for different wafer temperatures and different pulse times. An increased sheet resistance for higher temperatures and for longer pulse times is observable. However this increase is not significant and it will rarely affect the power device performance.

2.3.4 Characterization of Short-Length Ohmic Contacts

The quality of the ohmic contacts is essential for each HEMT-technology. Therefore the characterization of the ohmic contact resistance is part of the standard process monitoring and is automatically measured on each wafer. However because of ambitious layout variants with very short-length ohmic contacts it was necessary to extend the standard characterization to the particular demands of these structures. The results of this characterization are a basis of very chip area-efficient designs with short-length ohmic contacts, which are introduced in section 4.3.3. In this work a number of transmission-line-method (TLM) test structures have been developed to characterize the influence of the reduction of the ohmic contact length l_{OHM} on the ohmic contact resistance R'_{OHM}. The TLM is a common known method to measure the sheet resistance $R_{SH,A}$ and the ohmic contact resistance R'_{OHM}. The method was introduced by Shockley [28]. A detailed description can be found in [28].

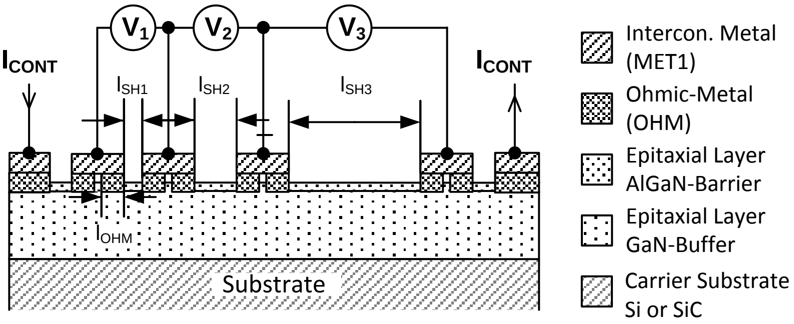

Figure 12: Structure cross section and measurement setup of the transmission line method (TLM) used for the characterization of the sheet resistance $R_{\mathrm{SH,A}}$ and the ohmic contact resistance R'_{OHM}. A constant current I_{CONT} is applied through a chain consisting of ohmic contacts and 2DEG channel segments with different spacings. The potentials are measured at each metal-interconnection above the ohmic contacts. With constant current and differential voltages the sheet resistance $R_{\mathrm{SH,A}}$ and the ohmic contact resistance R'_{OHM} can be calculated.

The test structure used in this experiment is shown in figure 12. A constant current I_{CONT} is applied through a chain consisting of ohmic contacts and 2DEG channel segments with different spacings. The potentials are measured between the channel segments. With the constant current I_{CONT}, and the differential potentials V_{x}, the values for the sheet resistance $R_{\mathrm{SH,A}}$ and the ohmic contact resistance R'_{OHM} can be calculated by using the equation:

$$R'_{\mathrm{TLM,x}} = \frac{V_x}{I'_{\mathrm{CONT}}} = 2R'_{\mathrm{OHM}} + l_{\mathrm{SH,x}}\frac{R_{\mathrm{SH,A}}}{W}. \tag{2.11}$$

Four TLM structures with different ohmic contact lengths have been fabricated and characterized. The results are shown in figure 13. The left plot show the results of the TLM resistance elements as a function of the spacing. The results are fitted with a linear function. In the ideal case with no contact resistance the total resistance would be zero for $l_{\mathrm{SH}} = 0$. However in real measurement there is a remaining resistance at $l_{\mathrm{SH}} = 0$. This value corresponds to the double ohmic contact resistance as shown in equation (4.9). The results of all fabricated TLM structures are plotted in figure 13 on the right side. The experiment demonstrates that the ohmic contact resistances are not increased by the reduction of the contact length. The ohmic contacts have been tested for contact lengths between $l_{\mathrm{OHM}} = 8$ µm and $l_{\mathrm{OHM}} = 3$ µm. Measurements have been made for two technologies variants with different carrier substrates: GaN-on-Si and GaN-on-SiC. The ohmic contacts of both technologies show no degradation caused by reduction of the contact length. These results will be used in section 4.3.3. The short contact length helps to increase the area-efficiency of large area GaN-HEMT structures.

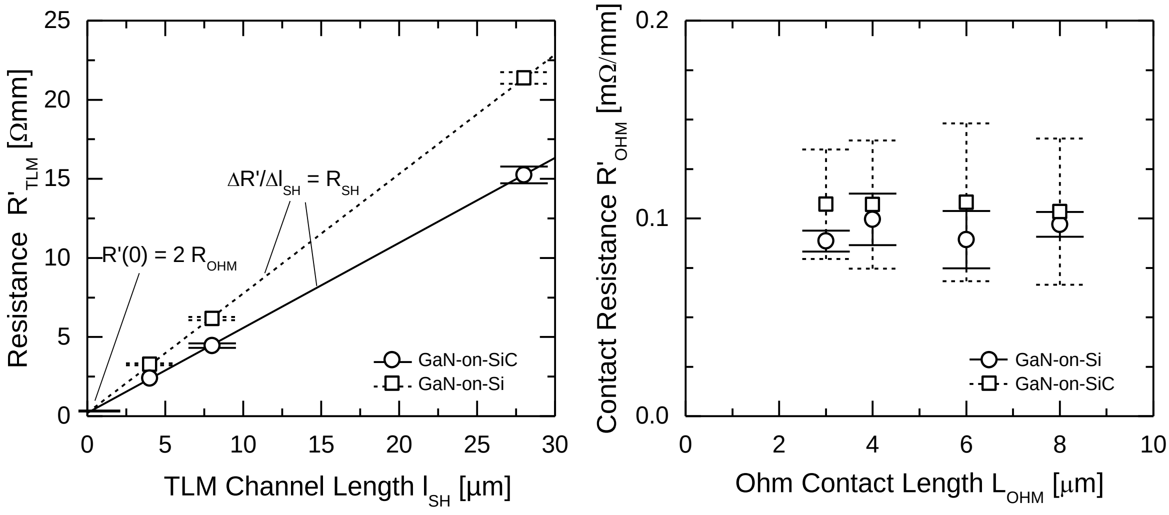

Figure 13: Measurement results of the transmission-line-method (TLM) for the characterization of the sheet resistance $R_{SH,A}$ and the ohmic contact resistance R'_{OHM}. (Left) The specific resistance elements $R'_{TLM,x} = V_x/I'_{CONT}$ are plotted as a function of the TLM channel length l_{SH}. The gradient of the linear fit correspond to the value of the sheet resistance R_{SH} and the resistance at $l_{SH} = 0$ correspond to twice the ohmic contact resistance $R'(0) = 2 \cdot R'_{OHM}$. (Right) values of the ohmic contact R'_{OHM} as a function of the ohmic contact length.

These are relevant technology properties and its characterization belongs to the initial background to design highly efficient HEMT structures. The following four chapters contain the design and the characterization of HEMT structures. The considerations start with the intrinsic structure with regards to the device off-state.

3. Off-State-Specific Device Design and Characterization

3.1 Introduction: Off-State

One might think that the off-state has less importance in terms of efficiency. Because, as discussed in section 1.2 and 1.3 the off-state generates very low losses compared to the other operating states. However, the off-state-specific design has high influence on the losses in the on-state. As already shown in section 2.1 high voltage devices require high depletion length (see equation (2.2) or (2.5)), therefore this length should be chosen with caution. The depletion zone in the off-state is concurrently the most dominant part of the drift zone in the on-state, and the drift length between drain and source l_{DS} is proportional to the on-state resistance $R'_{ON} \approx R_{SH,A} \cdot l_{DS}$ and therewith the dominating design parameter. Thus the depletion length should only be made as long as required, because an oversized length increases the on-state losses and leads to inefficient designs.

The GaN technology is still in an early development state and the defect density is still a more determining factor for the off-state performance than the layout related issues. This becomes evident by a comparison of the off-state performance between small gate-width devices and large gate-width devices, which are based on the same intrinsic design. The yield of functioning high voltage GaN-devices on a fabricated wafer decreases with increasing chip area due to the impact of critical defects in material and technology. Nevertheless the technology is continuously improved and layout-related issues, such as field plate optimization will become more important. A suitable field plate design can improve breakdown voltage, reliability, and the dynamic switching behavior.

This chapter considers the most relevant design parameter for the dimensioning of an intrinsic HEMT structure regarding the device off-state. The breakdown behavior and field plate configurations are experimentally investigated and a new concept of field shaping by using multi-gate-cascades is briefly introduced.

3.2 Breakdown in GaN-HEMT Devices

3.2.1 Lateral Breakdown

The choice of a suitable gate-drain distance l_{GD} is crucial for an efficient GaN-device design. In high voltage HEMTs the gate-drain distance is the dominating distance of the total channel length between drain and source l_{DS}. It is disadvantageous to select too long gate-drain distances, because then the structure features a too high on-state resistance due to the long drift region, and if the gate-drain distance is selected too small then the depletion length is too small and the device has an early breakdown. Thus it is important to characterize the lateral dielectric strength of a technology.

The dielectric properties of the technology used for this thesis have been characterized by a number of small gate width devices. These devices have been measured on wafer with statistically significant numbers of cells. The test devices have been designed with a gate width of $W = 50$ µm, a gate length of $l_G = 1$ µm, and a gate-source distance of $l_{GS} = 2$ µm. The gate-drain distance l_{GD} was incremented by 2 µm for each structure. The structure has been designed without field plates. The currents are the average of more than 5 devices per structure. All devices in this experiment have been measured with floating substrate to prevent a vertical breakdown.

The results of the measurements are shown in figure 14. The left plot shows the drain leakage currents $I_{D,LEAK}$ for each structure as a function of the drain-source voltage. In this experiment the breakdown voltage V_{BD} of each structure was defined at a value of $I_{D,BD} = 10$ µA/mm. On the right plot the breakdown voltages are plotted as function of the corresponding gate-drain distances l_{GD}. A linear behavior can be observed between the gate-drain distance l_{GD} and the breakdown voltage V_{BD}, which is typical for this experiment and can be also observed in other

HEMT technologies in literature [30], [31], [32], or [33]. The gradient shows the lateral dielectric strength of this technology with a value of 105 V/µm. This is a high dielectric strength compared to values in the literature. Typical values are in the range between 50-100 V/µm. In the previous years the lateral isolation of the technology was continuously improved. The isolation was starting with a value of 55 V/µm [22] in the year 2013 and improved to a value of 105 V/µm in this experiment in the year 2016.

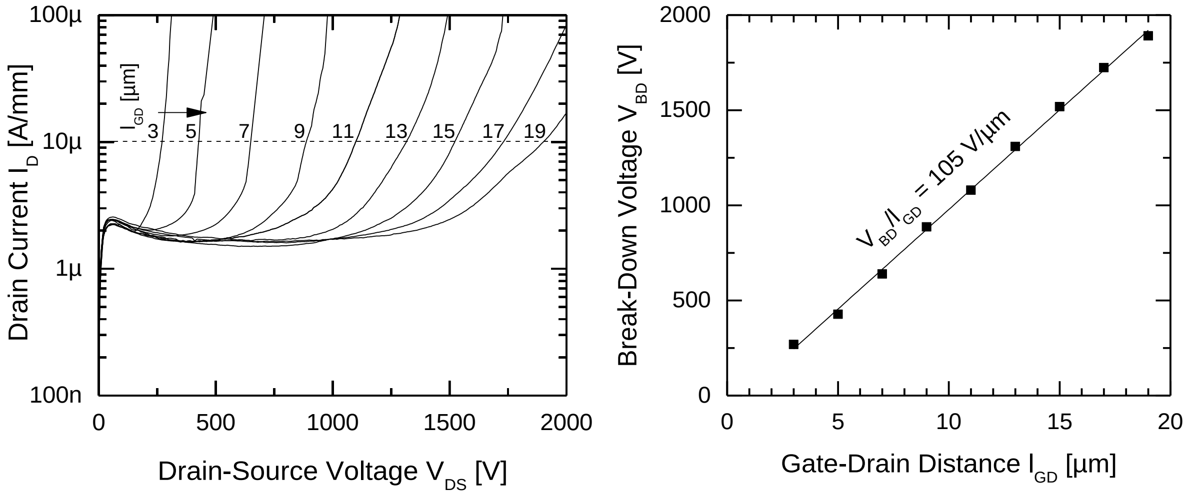

Figure 14: Lateral breakdown as a function of the gate-drain distance (average of at least 5 devices) for transistors having a gate width of 50 µm. (Left) Drain leakage currents as a function of the drain-source voltage measured on small device HEMTs with different gate-drain distances. (Right) Breakdown voltage as a function of the gate-drain distance defined at a drain leakage current of I_D = 10 µA/mm.

The lateral dielectric strength which was found in this experiment is an important reference value to evaluate a technology. However the result of figure 14 should not be transferred one-by-one to choose the drain-gate distance of a large gate width GaN-HEMT power device. Safety margins are required. The experiment has been made on small test devices. Large gate width devices suffer from defects in the structure material by epitaxy as well as by process technology. Furthermore, low gate-drain distances cause high electric field strengths at drain and gate edges. These high fields affect dynamic properties just as the reliability of the device.

3.2.2 Vertical Breakdown

Figure 14 illustrates a linear behavior between breakdown voltage V_{BD} and the gate-drain distance l_{GD}. The lateral component of the electrical field at the gate is the reason for this breakdown. However, breakdown can also occur vertically between the HEMT structure and the carrier-substrate through the GaN-buffer layer. Thus GaN-buffer thickness and the differential potentials between surface and backside are important. Due to the lattice and thermal expansion mismatches between the GaN-based epitaxial layer and the Si-substrate it is challenging to grow GaN-buffers with high thickness, low defect density and low tensile stress. Thicknesses in the range between 3-7 µm are used to achieve the required vertical dielectric strength for high voltage devices [34], [35], [36]. Because of dynamic reasons it is required to apply a fixed potential on the substrate [37]. This is especially important in case that the substrate is conductive, as the Si-carrier-substrate which is used in this work. Often the source potential is connected with the substrate on the backside of the chip to enable a fixed potential under the GaN-buffer. Consequently the buffer has to isolate the full off-state potential between drain-contact and carrier substrate.

3.3 Field Shaping

The purpose of field plates is the reduction of high electric fields in GaN-HEMT structures. With a suitable field plate design the breakdown voltage can be increased, the dynamic behavior can be improved, and the device reliability can be increased. The ideal field plate for lateral devices is a slanted field plate, as shown above in section 2.1.1. With an optimal angle and an optimal adapted dielectric material a slanted field plate shapes the electric field homogeneously in the channel along the *x*-axis, as shown in figure 7. The practical realization of such an ideal field plate along the full channel length in a GaN-HEMT technology is complicated and hardly feasible. However field shaping by slanted gate side walls, which can be considered as a partly executed slanted field plate, is successfully used in many technologies e.g. in [15]. Furthermore GaN HEMTs often contain planar field plates for field shaping, as shown e.g. in [38]. These field plates are usually connected to the gate- or source-potential. Such a field plate can be easily realized by using a metallization, which is deposited on top of a passivation layer. The field plate configuration which is mainly used in this work is shown in the cross section in figure 8. The technology has slanted gate-side walls, a gate connected field plate realized by the metallization (METFP) and a source connected field plate which is realized by the metallization (MET1).

3.3.1 Multiple Field Plates

The behavior of multiple field plates shall be clarified in the following example. Figure 15 illustrates the relationship between field plates and the electric field along the *x*-axis in the channel with help of an example. Three planar plates are arranged above a heterojunction channel. The left plate P1 represents a Schottky gate (Schottky), the middle plate P2 represents a first field plate on top of the first passivation (METFP), and the right plate P3 represents a second field plate on top of the second metallization (MET1). In an initial state all voltages at the field plates are zero and the channel is filled with charge carriers. Each field plate can be considered as separate gate and the properties of these gates are determined in the experiment in figure 9 and shown in figure 10 and table 2, and thus each gate has its threshold voltage and the channel segment can be depleted if the corresponding threshold voltage is applied at its terminals. If we consider the field plate configuration of figure 8 the right field plate is connected to source $V_{P3} = 0 = \mathrm{GND}$, the middle field plate is connected to the gate voltage $V_{P2} = V_{P1} = V_{GS}$, and the left field plate is the Schottky gate, itself. If $V_{GS} = -7$ V the channel segment between x_0 and x_1 is depleted, since $V_{P1}-V_1 < V_{TH1}$. Thus the channel between source and drain is blocked by the left segment. If the drain-source voltage is increased to V_{GS}-$V_{DS} < V_{TH2,}$ than the middle segment between x_1 and x_2 is depleted as well, and if the drain-source voltage is increased to -$V_{DS} < V_{TH3}$ than the next segment x_2 and x_3 is depleted. An inhomogeneous electric field is formed in the depleted channel regions. In particular high peaks arise at the positions x_1, x_2, and $x_{3,}$ as shown in figure 15. The electric field peak $E(x_1)$ is formed by the high differential voltage, which can be found between V_1 and V_{P1}, at x-position x_1. Furthermore there is a small distance h_1 between these potentials, which leads to a high electric field. Comparable circumstances exist at locations x_2 and x_3, and this is the reason for the further electric field peaks $E(x_2)$ and $E(x_3)$ at these locations.

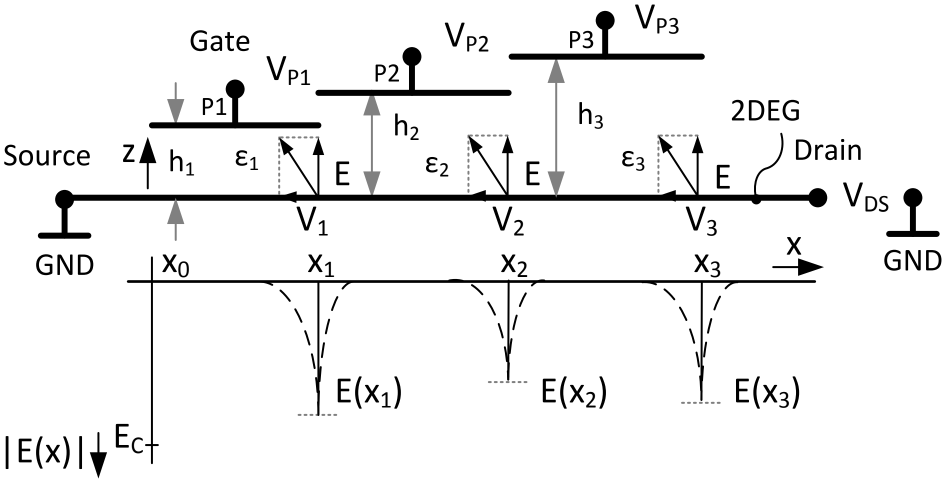

Figure 15: Schematic drawing of a HEMT structure with multiple field plates, and schematic electric field distribution in the channel during the off-state and high positive drain-source voltage.

The electric field distribution in the devices used in this thesis was indirectly characterized by electroluminescence investigation [39]. The dimensions of the structure are shown in figure 16, and it corresponds to the field plate layout T17 (shown below in figure 16). The electroluminescence investigation was made on small test structures with a gate width of $W = 200$ µm. The field distribution is investigated for off-state voltages V_{DS} up to 100 V. The electric field peaks for the Schottky gate edge, for gate-connected field plate (METFP) and for source-connected field plate (MET1) are characterized. The highest electric field peak at gate-edge $E(x_1)$ has a maximal value of 0.9 MV/cm at a corresponding off-state voltage of $V_{DS} = 100$ V. These investigations can be used to match these measurement results with simulation models as well as analytic assumptions.

As shown above field plate structures have many degrees of freedom. Important parameters are the field plate length, the field plate distance to the channel, the dielectric properties of the materials between field plate and channel, the potential of the field plate, the angle of the field plate edge, interface-states, the drain-gate distance, off-state voltage, and in case of multiple field plates the interaction of the field plates, because of this complexity an analytic treatment is rarely published [40]. Therefore field plate optimization is very often assisted by 2-

dimensional Technology Computer Aided Design (TCAD) simulations [38], [41]. The most common used software tools are Silvaco Atlas^{TM}, and Synopsys TCAD^{TM}. Simulation results of field plate structure in this technology are found in [27], [41], [42]. In this work HEMT structures has been evaluated in experimental investigations by comparison of different field plate layouts.

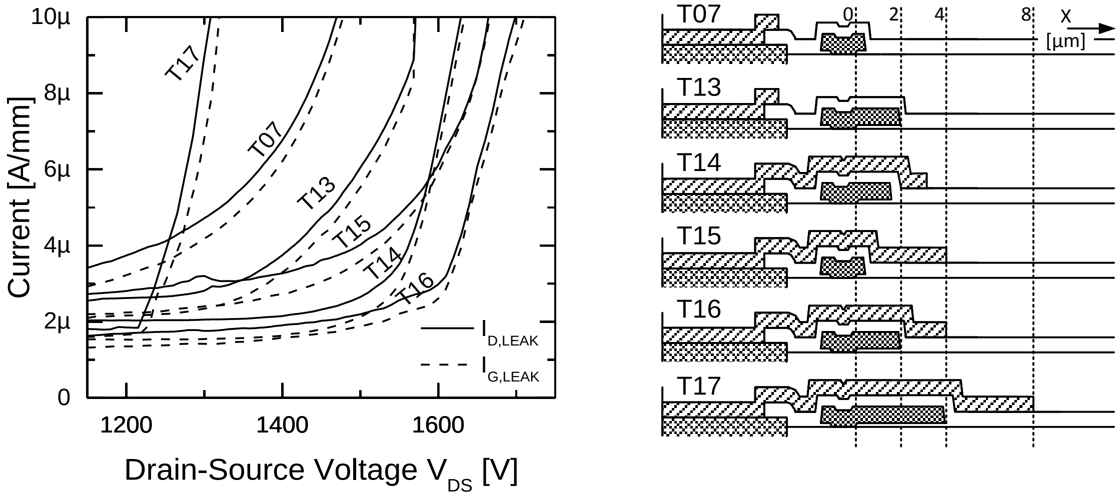

Figure 16: Breakdown behavior of HEMT devices with different field plate configurations. (Left) Measurement results of breakdown leakage currents as a function of the drain-source voltage plotted for different structures. (Right) Cross-sections of the tested field plate configurations.

Small device test structures with different field plate layouts have been designed with a gate width of $W = 50$ µm, a gate-drain distance of $l_{GS} = 15$ µm, a gate length of $l_G = 1$ µm and gate source distance of $l_{GS} = 2$ µm. The test devices with six different field plate layouts have been measured under same conditions. The cross-sections of the different field plate configurations (T07, T13, T14, T15, T16, and T17) are illustrated in figure 16 on the right side. There are length variations of the gate-head, which represent the gate-connected field plate (METFP), and length variations of the source-connected field plate (MET1). The measurement results are shown on the left side of figure 16. Plotted are the gate leakage currents $-I_{G,LEAK}$ as well as the source leakage currents $I_{D,LEAK}$ in the breakdown region as a function of the drain-source voltage. The measurements have been performed semi-automatically on a wafer prober. The current curve is the average of a least 5 measurements. It can be seen that the breakdown voltage can be increased by using field plates. It is shown that the layout T16 achieves a breakdown which is increase by 200 V compared to the layout T07 without field plates. However the structure with the longest field plates achieves the lowest breakdown. The shape of the breakdown is remarkable. The gradients of the breakdown currents change for longer field plates, which indicated that type of the breakdown location is different. From the early breakdowns of devices with layout T17 it can be concluded that the structures with the longer field plates break due to the high critical field peak located close to one of the field plates and not the high electric field close to the gate foot.

An increased breakdown voltage is one criterion to choose a field plate layout. However there are further important issues which have to be considered. Reliability and dynamic switching properties are also important to evaluate a field plate design. Fortunately a suitable field structure improves all three issues. In this manner a reference is also made to the thesis of M. Wespel, which was performed during the same time period. His work includes detailed investigations on different field plate structures with regard to dynamic performance and reliability.

3.3.2 Multi-Gate Cascade

A different and new approach of field shaping for GaN-devices has been introduced in this work by a multi-gate-cascade structure and published in [43]. The new approach proposes a separation of the channel in multiple-segments. Each channel segment has a field plate, which acts like a normally-on gate with a highly negative threshold voltage. The field distribution along the channel is similar to multiple field plates with rising, uniformly distributed steps. The field peaks are formed under the gate of each segment. The distribution of the potentials can be understood in the equivalent circuit model, which is shown on the left side in figure 17.

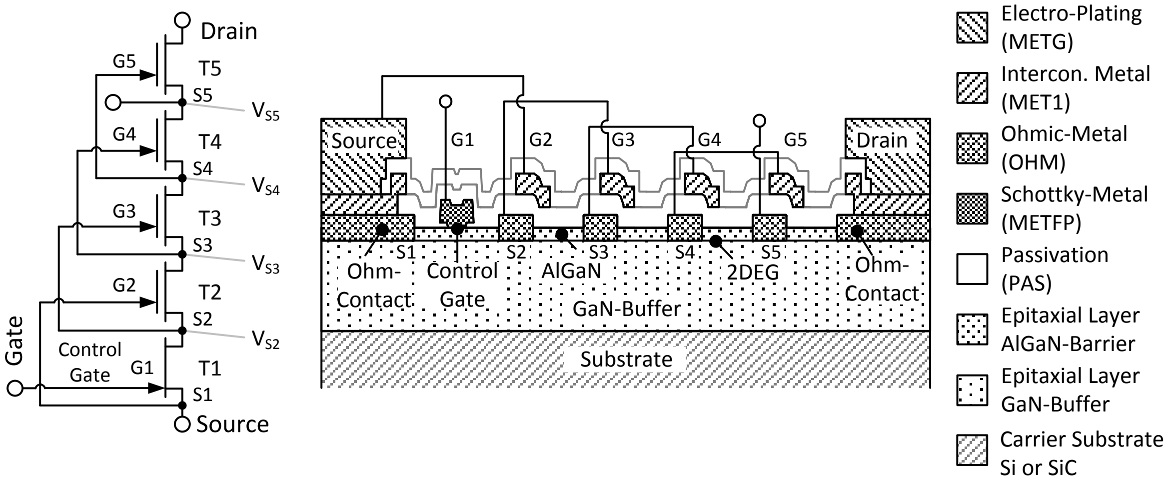

Figure 17: Multi-gate cascade as field shaping approach. (Left) Multi-gate cascade as equivalent circuit. (Right) Cross-section of a multi-gate cascade structure.

A number of normally-on transistors with high negative threshold voltage are stacked over a control transistor. The gates of the normally-on transistors are connected to the sources of the transistors below. In the off-state the blocking voltage of each transistor is limited by the threshold voltage of the transistor above. Thus the drain-source voltage of each transistor segment is equal to the threshold voltage of the transistor segment above $V_{DS}(x) = V_{TH}(x+1)$. Consequently the potentials of the ohmic contacts are related to the threshold voltages such that the voltage blocking capability increases with threshold voltage of the cascade transistors. If the multi-gates are realized in the same metallization, then the potentials on the nodes are incremented by the common threshold voltage: $V_{S2} = V_{TH2}$, $V_{S3} = V_{TH2} + V_{TH3} = 2\cdot V_{TH2}$,

$V_{S4} = 3 \cdot V_{TH2}$ and $V_{S5} = 4 \cdot V_{TH2}$. For these high voltage cascades it is advantageous if the upper gates have a high negative threshold voltage, because then the number of segments in order to reach a given breakdown voltage can be decreased. The control transistor T1 in the bottom of the cascade determines the state of the cascaded transistors above. In the on-state the gate voltages of the stacked normally-on transistors are higher than its threshold voltages. Thus all transistors are in the on-state. The threshold voltages of the control transistor T1 can be chosen completely independent from the other transistor in the cascade. It can be normally-on or normally-off. If the transistor T1 has a normally-off behavior the entire cascade behaves like a normally-off transistor.

A multi gate cascade has been realized using the technology shown in section 2.3.1. The cross section of the intrinsic layout is shown on the right side in figure 17. The control gate is realized by a Schottky contact and the gates of the upper transistor segments are realized by the interconnection metallization (MET1). The threshold voltage of these upper gates is in the range of $V_{TH,MET1} = 91$ V, as shown in table 2. The segments are separated by ohmic contacts (OHM). These contacts are the source contacts of the cascade segments and connected to gates of the upper segments, as shown in the equivalent circuit as well as in the cross section in figure 17. The interconnections of this structure have been realized as shown in the publication in [43]. The structure has been developed with the following dimensions: the control transistor segment has a gate-drain distance of $l_{GD,T1} = 2$ µm, a gate length of $l_{G,T1} = 1$ µm, and a gate-source distance of $l_{GS} = 2$ µm. The upper segments have source-overlapping gates. Thus the gate-source distance is negative to reduce channel length and to meet the design rules of the interconnection metallization (MET1) with a value of $l_{GS} = -1$ µm. The gate length is $l_G = 2$ µm, however only 1 µm covers the channel. The gate-drain distance of the upper segment is $l_{GD} = 2$ µm. The cascade includes 4 upper segments and one control segment. The gate width of the small device test structure is $W = 50$ µm.

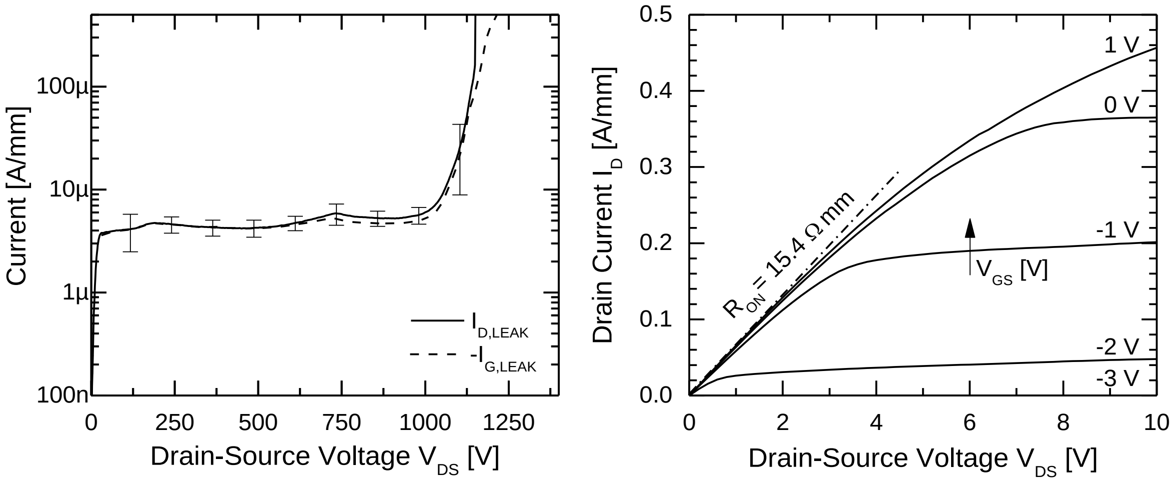

Figure 18: Measurement results of a multi-gate cascade structure. (Left) The leakage currents in the off-state at drain and gate. (Right) The output characteristic of the device.

The test structures have been measured using a semiautomatic on-wafer prober station. The results of the static measurements are shown in figure 18. The left plot shows the off-state leakage currents of gate and drain. The curves are averaged by calculating the mean of more than 5 tested devices. The leakage current is in the same range as for conventional HEMT structures with Schottky gate. Furthermore the drain leakage current is dominated by the Schottky gate leakage. The breakdown voltage is around $V_{\mathrm{BD}} = 1100$ V, which is much higher than the breakdown of a single segment with $V_{\mathrm{BD}} \approx 100$ V/µm·2 µm = 200 V. This states that the cascade divides the total off-state voltage into lower voltages and these lower voltages are separated on the cascade segments. Thus it can withstand high off-state voltages and it is demonstrated that the principle of the multi-gate cascade is working. The results are shown in figure 18. It is shown that the behavior of the Schottky gate determines the behavior of the overall cascade. The threshold voltage is about a $V_{\mathrm{TH}} = -3$ V and the on-state resistance corresponds with the channel length and the sheet resistance.

The concept of multi-gate field plates has been introduced in this section as new field shaping approach. The total voltage between drain and source is split by segments into smaller voltages. These segments can be spatially separated and this enables a distribution of the electric field along the structure similar to a multi-field plate. The experiment above proves the concept. However due to the expense of the additional ohmic contacts and the unoptimized segment dimensions the area-efficiency of the concept is low compared to a conventional structure. This work has its focus on area-efficient device designs. Therefore further investigations are not elaborated in this work.

3.4 Conclusion: Off-State

This chapter has briefly discussed the off-state characteristics of high voltage HEMT structures for power applications. The off-state performance is mainly determined by the intrinsic HEMT-layout. The dimensioning of the depletion length between drain and gate and a suitable epitaxial buffer thickness are the most important parameters to achieve a desired breakdown voltage. Furthermore, because of the early development stage of the GaN-technology the defect density lead to early breakdown especially on large-area devices. Therefore the material quality and defect density have to be further improved. Nevertheless for small devices the lateral isolation of an advanced GaN-technology is in the range of 50-100 V/µm, whereas the vertical isolation is about 150 V/µm. Thus it approaching the half of the theoretical value 330 V/µm = 3.3 MV/cm, which is given in table 1.

Field plate structures reduce high critical electrical field peaks in the HEMT structure and thus breakdown and reliability of devices can be improved. An experimental investigation in section 3.3.1 has shown that a suitable field plate layout increases breakdown and reduces the leakage currents at high voltages. In the experiment the breakdown voltage has been increased from 1400 V without any field plates up to 1600 V with a gate- and a source connected field plate. However it is also shown that inappropriate field plates lead to early breakdown and worsen the performance.

Section 3.3.2 introduces a new concept of field shaping by using a multi-gate cascade design. The electric field can be distributed on multiple segments along the structure. Thus the total off-state voltage is separated in a number of segments. However, due to new additional ohmic contacts the structure requires more chip area compared to a conventional structure. Therefore multi-gate cascades fail the objective of this thesis in terms of area efficiency. However the approach offers other new interesting opportunities for the use in high voltage power applications. The approach enables a spatial separation of the total off-state voltage on a number of segments, which can be used to design very high voltage devices. However this approach was not pursued further in the work.

On one hand the dimensioning of the depletion length defines the maximum off-state voltage and on the other hand the depletion length is directly coupled with the drift length, which determines the on-state resistance. Thus in terms of efficiency the off-state related design should not be overdimensioned. It should be adapted to the requirements of the application. The considerations in following chapter presume a given intrinsic structure with a chosen drain-source length. It will be shown how the intrinsic layout is embedded into extrinsic finger structures in order to achieve highly efficient power devices with low on-state resistance per chip-area as well as high on-state currents.

4. On-State-Specific Device Design and Characterization

4.1 Introduction: On-State

The static losses of a power device are mainly determined by the on-state resistance R_{ON}. Certainly, to achieve lower losses a designer could spend more gate width to reduce the on-state resistance. But an increase of gate-width requires more chip area, which lead to higher device cost. An appropriate chip-layout features low on-state resistance in relation to the used chip-area. This chapter develops the fundamentals to achieve highly area-efficient GaN-HEMT layouts.

The challenge in an efficient layout design is the suitable dimensioning of the HEMT structure. Some inertial parameters are given by technology properties as the sheet resistances of the 2-DEG or the metallization layers, which was characterized in chapter 2. Another important parameter is the channel length between drain and source l_{DS}. This length is predefined by the intrinsic layout of the HEMT structure, and mainly determined by the off-state voltage class. Especially in high voltage devices the depletion length between gate and drain l_{GD} is a dominate length of the structure. Intrinsic layouts were investigated and discussed in chapter 3. In the following section an analytically on-state model is developed. This is the fundamental of the understanding of area-efficient layouts.

4.2 Development of an On-State Model

The understanding of current-, voltage-, and power-density-distributions in HEMT finger structures are important fundamentals for the design of suitable layout structures for high power GaN-HEMTs. Besides the sheet resistance of the semiconductor appropriate dimensions of the metallization determine the on-state performance and the chip area-efficiency. Therefore an electrical model is advantageous for an analysis of the on-state behavior in terms of the area consumption and the performance consideration. For this purpose a static electrical model of GaN-HEMT finger structures is developed in this work. Critical design parameters are analytically derived and discussed. The electrical model can be used to predict the chip-area-specific on-state performance.

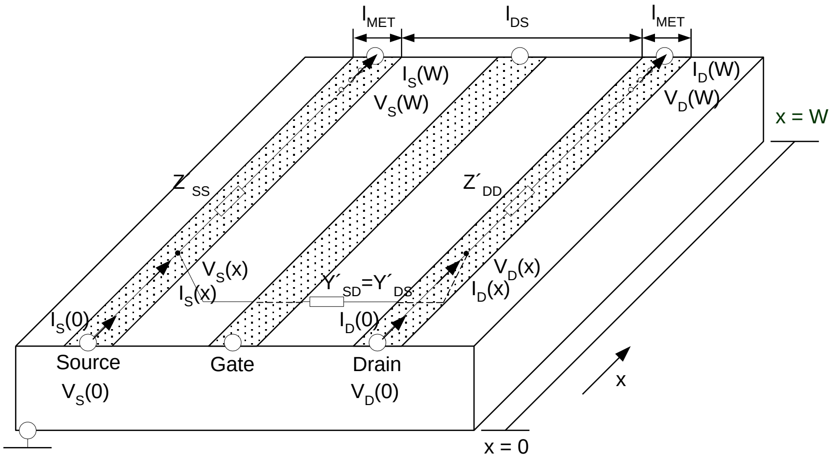

Figure 19: Model of a GaN-HEMT finger structure in the static on-state

A GaN-HEMT structure is a three-wire system with drain, gate and source as shown in figure 19. In the following consideration it is assumed, that the gate voltage V_{GS} is constant and it is higher than the threshold voltage V_{TH}. Furthermore it is assumed that the transistor channel is completely open, and the currents and voltages are static. The gate contact is static and it has no influence on the on-state model, and therefore it can be ignored. Consequently it is enough to consider the model of a two-wire system with drain, conducting channel and source. The currents and voltages in the structure can be written as a differential-equation-system by using Kirchhoff's laws. The voltages and currents are given by the following equations:

$$\frac{\partial}{\partial x}V(x) = -Z' \cdot I(x), \text{ and} \tag{4.1}$$

$$\frac{\partial}{\partial x}I(x) = -Y' \cdot V(x) \text{ with} \tag{4.2}$$

$$I(x) = \begin{bmatrix} I_S(x) \\ I_D(x) \end{bmatrix}, V(x) = \begin{bmatrix} V_S(x) \\ V_D(x) \end{bmatrix}, Z' = \begin{bmatrix} Z'_{\mathrm{SS}} & Z'_{\mathrm{SD}} \\ Z'_{\mathrm{DS}} & Z'_{\mathrm{DD}} \end{bmatrix}, \text{ and } Y' = \begin{bmatrix} Y'_{\mathrm{SS}} & Y'_{\mathrm{SD}} \\ Y'_{\mathrm{DS}} & Y'_{\mathrm{DD}} \end{bmatrix}. \tag{4.3}$$

The impedances Z'_{SS} and Z'_{DD} are determined by the sheet resistance of the source and drain metallization $R_{\mathrm{SH,MET}}$. Usually the length of the source metallization is equal to the length of the drain metallization l_{MET}. With this assumption the impedances Z'_{SS} and Z'_{DD} are given by the resistance per unit length as: $Z'_{\mathrm{SS}} = Z'_{\mathrm{DD}} = R' = R_{\mathrm{SH,MET}}/l_{\mathrm{MET}}$. In the static case there is no coupling between the two lines. Therefore Z_{DS} and Z_{SD} are zero. The admittances Y_{SD} and Y_{DS} describe the conductance per unit length from drain to source and backwards from source to drain. In the static on-state both values are equal. The conductance values are determined by the channel resistance and both ohmic contact resistances at drain and source, the conductance values per unit lengths are given by: $Y'_{\mathrm{SD}} = Y'_{\mathrm{DS}} = G' = 1/(2 \cdot R'_{\mathrm{OHM}} + R_{\mathrm{SH,A}} \cdot l_{\mathrm{DS}})$. The channel resistance in the static on-state is assumed to be homogeneous and it is determined by the sheet resistance of the active area $R_{\mathrm{SH,A}}$ and the length of the channel l_{DS}. Typical values for ohmic contact resistances for GaN-HEMT technologies are in the range of $R'_{\mathrm{OHM}} = 0.1$-0.5 Ωmm, while a typical on-state resistance per unit length for a high voltage GaN-HEMT is in the range of $R'_{\mathrm{ON}} = 10$-16 Ω mm. These on-state values correspond to a sheet resistance of the active area in the range of $R_{\mathrm{SH,A}} = 500$-800 Ω/□ and a typical channel length of $l_{\mathrm{DS}} = 20$ µm. Consequently the channel resistance is usually much higher than the ohmic contact resistance $R_{\mathrm{SH,A}} \cdot l_{\mathrm{DS}} >> R'_{\mathrm{OHM}}$. Therefore in high voltage HEMTs the conductance is mainly determined by sheet resistance and the channel length. The ohmic contact resistance can be neglected, and the channel conductance can be given as $G' \approx 1/(R_{\mathrm{SH,A}} \cdot l_{\mathrm{DS}})$.

The conventionally used layout structure for power GaN-HEMTs is the comb layout. This structure in figure 26 and will be explained in more detail in section 4.4.2. In this structure the source interface is connected to a source bus metal at location $x = 0$ and the drain interface is connected to the drain bus metal at location $x = W$. Drain metallization at location $x = 0$ and source metallization at location $x = W$ are not connected. Thus these ends are open and the currents at these positions are zero. With these information the states at all interconnections of the system are known, and the boundary conditions for the differential-equation-system (4.1) to (4.3) are given by the expressions: $I_S(0) = I_{\mathrm{Total}}$, $I_D(W) = I_{\mathrm{Total}}$, $I_S(W) = 0$, $I_D(0) = 0$, $V_S(0) = 0$, and $V_D(W) = V_{\mathrm{DS}}$. Variable $\gamma = \sqrt{2R'G'}$ is used as propagation constant. Equation (4.1) can be inserted in the second derivative of equation (4.2) to get:

$$\frac{\partial^2}{\partial x^2} I(x) = Y'Z' \cdot I(x). \tag{4.4}$$

The resulting differential equation system which is given in equation (4.4) can be solved in order to find the current and the voltage distributions as a function of the location. The solutions for the currents $I_S(x)$, $I_D(x)$, and $I_{\mathrm{DS}}(x)$ are shown below. Because of the unhandy equations the solutions of voltages $V_S(x)$ and $V_D(x)$ are shown in the appendix I. Furthermore only the currents results are used for further analysis in this work.

4.2.1 Currents on GaN-HEMT Finger Structures

The currents along the source and the drain metallization are solved to be:

$$I_S(x) = -I_{\text{Total}} \frac{e^{-x\gamma}(e^{x\gamma}+1)(e^{x\gamma}-e^{W\gamma})}{2(e^{W\gamma}-1)}, \tag{4.5}$$

$$I_D(x) = I_{\text{Total}} \frac{e^{-x\gamma}(e^{x\gamma}-1)(e^{x\gamma}+e^{W\gamma})}{2(e^{W\gamma}-1)}. \tag{4.6}$$

The current per unit length through the channel along the x-axis between drain- and source-metallization is given by:

$$I'_{\text{D}}(x) = \frac{\partial I_D}{\partial x} = I_{\text{Total}} \frac{\gamma e^{-x\gamma}(e^{2x\gamma}-e^{W\gamma})}{2(e^{W\gamma}-1)}. \tag{4.7}$$

The result in equation (4.7) shows that the current through the channel has an inhomogeneous behavior because of the influence of the resistive metallization. This effect is called current crowding effect and can affect performance. The solution for the impedance and the current in the channel was shown before by G. Simin and published in [44]. However, the current distributions for different finger structures and different boundary conditions are analyzed and solved in this work and the detailed derivation has been published in [45].

4.2.2 Resistance of a GaN-HEMT Finger Structure

The resistance of a GaN-HEMT structure with an idealized, non-resistive metallization is given by $R_{\text{ON,00}} = 1/(G'\cdot W)$. This equation can be used for HEMT structures with low gate width, whereas in large area GaN-HEMT with large gate width finger structures the influence of resistive metallization has to be considered. Furthermore the effect of current crowding can affect performance and increase the static on-state resistance.

The on-state resistance R_{ON} is not a direct result of the solution of the differential-equation-system (4.1) to (4.3). But the solution of the total finger resistance R_{ON} can be found by using the first derivation of the source current. This is a part of the equation (4.2) and given by:

$$-\frac{\partial}{\partial x} I_D(x) = G'(V_D(x) - V_S(x)). \tag{4.8}$$

The expressions $\partial I_D(x)/\partial x$, $V_D(x)$ are $V_S(x)$ are present as solution of differential equation system (4.1) to (4.3), and with the equation $R_{\text{ON}} = V_{\text{Total}}/I_{\text{Total}}$ the total resistance of the finger structure can found to be

$$R_{\mathrm{ON}} = \frac{\gamma}{2G'}\left(\frac{\gamma W}{2} + \frac{e^{\gamma W}+1}{e^{\gamma W}-1}\right). \tag{4.9}$$

The on-state resistance R_{ON} is determined by the gate width W, the sheet resistance of the active area $R_{\mathrm{SH,A}}$, the channel length l_{DS}, the metallization length l_{MET}, and the sheet resistance of the metallization $R_{\mathrm{SH,MET}}$.

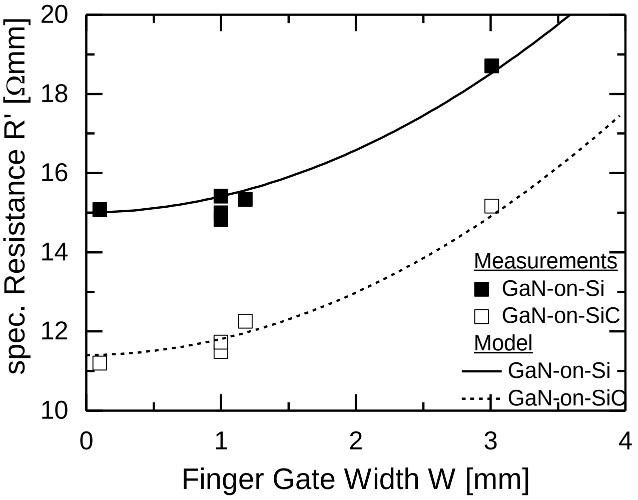

Figure 20: The on-state resistance per unit length R' is shown as a function of the finger gate width W. The curves are calculated by using the model given in equation (4.9). The measurements are made on different HEMT structures with same cross-section design and different finger gate width. The parameter for calculation are found in process monitor measurements: $R_{\mathrm{SH,MET}} = 0.003\ \Omega/\square$, $R_{\mathrm{SH,A}} = 750\ \Omega/\square$ for GaN-on-Si, $R_{\mathrm{SH,A}} = 550\ \Omega/\square$ for GaN-on-SiC, and given by cross-section layout: $l_{\mathrm{MET}} = 4\ \mu\mathrm{m}$ and $l_{\mathrm{DS}} = 19\ \mu\mathrm{m}$.

An experiment was made to determine the practical relevance and correspondence of the on-state model compared to measurement results. The on-state resistance per unit length R' of different HEMT structures with the same cross-section design and different gate widths was measured and compared to the calculated model-function given by equation (4.9). The on-state resistance per unit length is calculated by $R' = R_{\mathrm{ON}} \cdot W$, with the unit [Ω mm]. The results of measurement and model are shown in figure 20. The technology parameters for the calculation are extracted from process-monitor measurements. The results in figure 20 illustrate the significant increase of the on-state resistance R' per unit length as a function of the finger gate width W. Model- and measurements- results show a good agreement. Thus the experiment demonstrates the suitability of the model. The specific on-state resistance R' for large gate width finger structures can be predicted by using this model.

As shown in figure 20 the specific on-state resistance R' increases with the gate width W, whereas the total on-state resistance R_{ON} decreases to a minimum value. The influence of the resistive metallization becomes dominant by exceeding this minimum point and the total resistance increasing with the gate width W. The particular gate width for which the minimum value of the on-state resistance is reached can be found by $\partial R_{\mathrm{ON}}/\partial W = 0$. The minimum of the on-state resistance R_{ON} is a critical gate width value W_{crit}, which is given by:

$$W_{\mathrm{crit}} = \log_e(3 + 2\sqrt{2})/\gamma. \tag{4.10}$$

Thus this is the gate width with the lowest possible on-state resistance for the given technology-parameters R' and G'. It has to be considered that this gate width W_{crit} does not lead to the lowest on-state resistance per chip area $R_{\mathrm{ON}}\cdot A$. Issues regarding chip area-efficiency are discussed below in the next section 4.3.

4.3 Highly Area-Efficient GaN-HEMT Finger Structures

4.3.1 Area-Efficient GaN-HEMT Finger Design

In terms of device costs and on-state performance one of the most important objectives in power device design is to get a low on-state resistance per chip area. A finger with a large gate width leads to a low on-state resistance. However on large gate width finger structures current crowding can occur and this can affect the on-state performance. A finger metallization with more chip-area would be necessary to decrease this effect. The question is: which are sufficient finger parameters to get an area efficient GaN-HEMT finger structure design? A well-known figure-of-merit for area-efficient power devices is the product of the on-state resistance R_{ON} and the used area A, the so-called area specific on-state resistance $R_{\mathrm{ON}}\cdot A$. The lowest possible value for $R_{\mathrm{ON}}\cdot A$ for a certain channel length l_{DS} is the on-state resistance calculated without the influence of the resistive metallization and without the influence of the metallization area $\mathrm{MIN}(R_{\mathrm{ON}}\cdot A) = R_{\mathrm{ON}}\cdot A_{\mathrm{MIN}} = l_{\mathrm{DS}}/G' = l_{\mathrm{DS}}^2\cdot R_{\mathrm{SH,A}}$. Certainly, this value is just a theoretical value, but it can be used as a reference to evaluate finger designs. For designs with high gate width the area specific on-state resistance $R_{\mathrm{ON}}\cdot A$ can be calculated by the product of the resistances in the on-state R_{ON}, which is given in equation (4.9), and the total area A of a GaN-HEMT finger structure.

The relation between the finger parameters and the relation to the area specific on-state resistance $R_{\mathrm{ON}}\cdot A$ can be demonstrated in an example. The following parameters are given as typical values to calculate the following example: $R_{\mathrm{SH,A}} = 500\ \Omega/\square$, $R_{\mathrm{SH,MET}} = 0.002\ \Omega/\square$, and $l_{\mathrm{DS}} = 10\ \mu\mathrm{m}$. Furthermore two assumptions are made for simplification. In conventional HEMT finger structures the metallization length l_{MET} is as long as the ohmic contact length l_{OHM}. Therefore it is assumed that: $l_{\mathrm{MET}} = l_{\mathrm{OHM}}$. Thus the total area is calculated by: $A = (2l_{\mathrm{MET}}+l_{\mathrm{DS}})W$. Furthermore, in high voltage structures the channel resistance per unit length R' is much higher than the ohmic contact resistance R'_{OHM}, therefore the ohmic contact resistance is neglected in this example, $R'_{\mathrm{OHM}} = 0$. With this information it is possible to create a contour plot of the area specific on-state resistance as a function of metallization length l_{MET} and the gate width W.

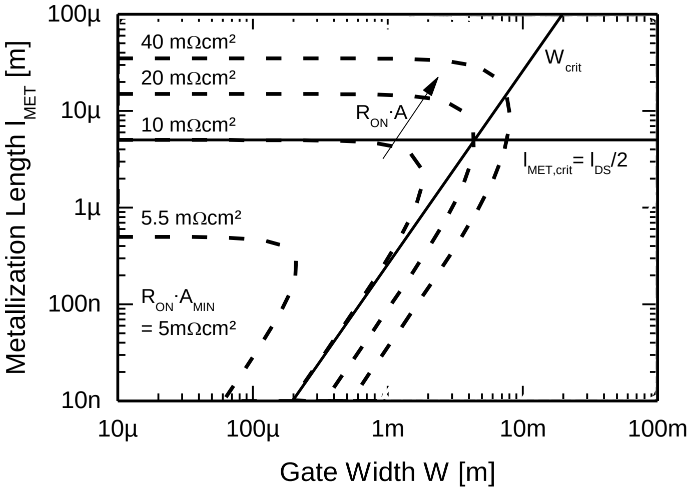

Figure 21: Area specific on-state resistance $R_{ON} \cdot A$ plotted versus the gate width W and the length of the metallization l_{MET}. The value of $R_{ON} \cdot A$ can be seen as a figure-of-merit for the area-efficiency. In this example a drain-source distance of $l_{DS} = 10$ µm is given. The sheet resistance of the metallization is $R_{SH,MET} = 0.002$ Ω/□ and the sheet resistance of the active area is $R_{SH,A} = 500$ Ω/□.

The result is shown in figure 21. There is a parameter region where the specific on-state resistance is close to the lowest possible value $R_{ON} \cdot A_{MIN}$ in the lower left corner of the diagram. This parameter region is enclosed by two borders. The layouts with parameters which exceed these critical borders are area-inefficient. The first border is given by the critical gate width W_{crit}, which is given in equation (4.10). This is the gate width W at which the resistance of metallization begins to be dominant. This critical value W_{crit} is plotted as line into figure 21. This is the line where the specific sheet resistance is increased to more than twice the value of the lowest possible value $R_{ON} \cdot A \geq 2\ R_{ON} \cdot A_{MIN}$.

The second border is a critical metallization length $l_{MET,crit}$. In this case the area of the metallization begins to be higher than the area of the active region, thus the area specific on-state resistance begin to increase significantly as well. The critical metallization length is given by:

$$l_{MET,crit} = l_{DS}/2. \tag{4.11}$$

This is the second critical parameter. In case that this critical value is exceeded the specific on-state resistance becomes more than twice the value of the lowest possible area specific on-state resistance $R_{ON} \cdot A \geq 2\ R_{ON} \cdot A_{MIN}$. Consequently these two critical values $l_{MET,crit}$ and W_{crit} should not be exceeded in an area efficient GaN-HEMT design.

In practice the minimal metallization length l_{MET} is given by the minimal technological metallization lengths, which are given by the limits of the electroplating process, as well as the minimal possible ohmic contacts. A strip realized in electroplating metallization (METG) should not be smaller than 10 µm in the given technology as otherwise the reproducibility cannot be ensured. Since finger structures in comb layouts are connected in parallel the metallization length of 10 µm can be used as drain- or source metallization for two channels. Consequently a finger structure with one channel has a minimal drain metallization length of $l_{\mathrm{MET}} = 5$ µm and a minimal source metallization length of $l_{\mathrm{MET}} = 5$ µm. A GaN-HEMT with a breakdown voltage of 200V has a typical channel length in the range of $l_{\mathrm{DS}} = 10$ µm. In this case the critical metallization length given in equation (4.11) is reached. The area for metallization is equal to the active area. A GaN-HEMT with a breakdown voltage of 600 V has a typical channel length in the range of $l_{\mathrm{DS}} = 20$ µm. The area for metallization is still a half of the active area.

These two examples demonstrate the high impact of metallization area on the value of the area specific on-state resistance. With the plot as shown in figure 21 the designer is able to choose more sufficient layout parameters.

4.3.2 Analysis of Tapered Finger Structures

The examples and discussion in section 4.3.1 demonstrate the impact of the metallization area on the chip area-efficiency for GaN-HEMT finger structures. Furthermore the problem of current crowding and the inhomogeneous current distribution in conventional GaN-HEMT finger structures can be analyzed with the solutions of the static on-state model in equations (4.5) - (4.7). This section introduces a HEMT-finger layout with a tapered drain- and source-metallization. The electrical properties of this layout are investigated in the same way as for the layout with a conventional structure, which was shown in section 4.2. Thus the results of the general equation (4.4) are solved for this layout type as well. Some results of this work are published in [45].

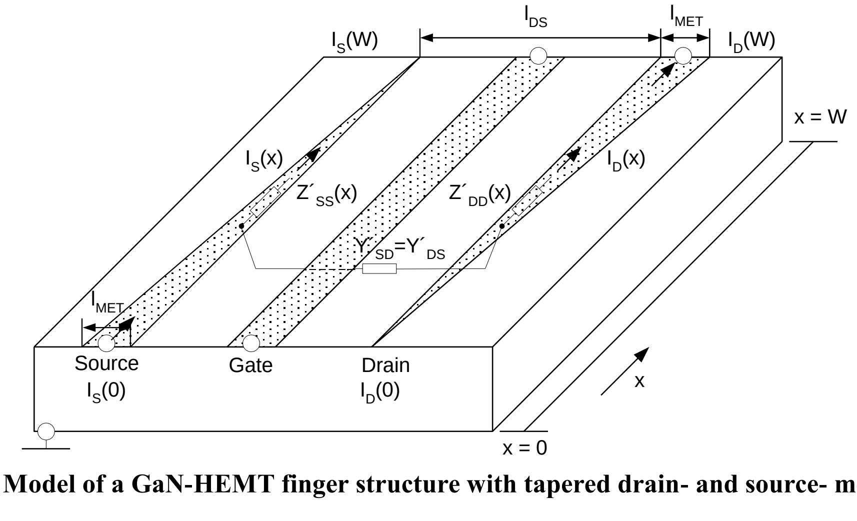

Figure 22: Model of a GaN-HEMT finger structure with tapered drain- and source- metallization.

An important difference in the analysis between conventional, rectangular fingers and tapered fingers is the inhomogeneous metallization-resistance per unit length. Rectangular structures have a constant resistance per unit length $Z' = R' = R_{\mathrm{SH,MET}}/l_{\mathrm{MET}}$ as shown in equation (4.1), whereas the resistance per unit length of a tapered structure is a function of the finger position *x*, thus $Z'_{SS}(x) = R'_S(x) \neq Z'_{DD}(x) = R'_D(x)$. The source metallization resistance per unit length is calculated by $R'_S(x) = R_{SH,MET}/(-l_{MET} \cdot x/W + l_{MET})$, and the drain metallization resistance per unit length is calculated by $R'_D(x) = R_{SH,MET}/(l_{MET} \cdot x/W)$. In analogy to the results in section 4.2.1 the currents for tapered finger structures can be written as

$$I_S(x) = -\frac{I_{\text{Total}}}{W} x + I_{\text{Total}}, \text{ and} \tag{4.12}$$

$$I_D(x) = \frac{I_{\text{Total}}}{W} x. \tag{4.13}$$

The current per unit length through the channel along the *x*-axis between source and drain is given by

$$I'_{\text{DS}}(x) = \frac{\partial I_D}{\partial x} = \frac{I_{\text{Total}}}{W} = \text{const.} \tag{4.14}$$

The results of the currents feature a remarkable property of such a tapered layout. The current per unit length I'_{DS} through the channel along the *x*-axis is constant. This structure has a constant current density along the channel and no current crowding effect occurs in contrast to the conventional structure, as shown in equation (4.7). Furthermore the current density in the metallization is constant as well. The current density in the metallization is calculated with equation $J(x) = I(x)/(l_{MET}(x) \cdot T_{MET})$, where the thickness of the metallization in *z* direction is denoted with T_{MET}. Since the current $I(x)$ and the metallization length $l_{MET}(x)$ are linear functions of the location *x* the current density is constant $J(x) = const$. The current density in drain- and source- metallization is given by $J(x) = I_{Total}/(l_{MET} \cdot T_{MET})$.

The influence of resistive metallization on the on-state resistance R_{ON} can be found in the equation:

$$R_{\text{ON}} = \frac{R_{\text{SH,A}} \cdot l_{\text{DS}}}{W} + \frac{R_{\text{SH,MET}} \cdot W}{l_{\text{MET}}}. \tag{4.15}$$

Equation (4.15) consists of two terms. The first term represent the resistance of a GaN-HEMT structure with an idealized, non-resistive metallization $R_{ON,00}$. This expression was already introduced above in section 4.2.2. The second term describes the resistive contribution of the metallization. The resistance R_{ON} will reach its minimum value when both terms become equal as will be shown below. The corresponding gate width W_{crit} of the on-state resistance can be found by zeroing the first derivate of the on-state resistance $\partial R_{ON}/\partial W$, as done before for the conventional layout in equation (4.10). The gate width with the lowest on-state resistance is given by

$$W_{\text{crit}} = \sqrt{\frac{R_{\text{SH,A}}}{R_{\text{SH,MET}}} l_{\text{DS}} \cdot l_{\text{MET}}}. \tag{4.16}$$

At this critical gate width W_{crit} the area specific on-state resistance $R_{\mathrm{ON}}{\cdot}A = R_{\mathrm{ON}}{\cdot}W(l_{\mathrm{DS}}+l_{\mathrm{MET}})$ has reached more than double the value of the lowest possible area specific on-state resistance $R_{\mathrm{ON}}{\cdot}A_{\mathrm{MIN}}$. Consequently the design becomes area-inefficient by exceeding this critical value. In analogy to the considerations in section 4.3.1 there is a critical value for a metallization length, defined as

$$l_{\text{MET,crit}} = l_{\text{DS}}/4. \tag{4.17}$$

This is the critical metallization length, where the active area of the HEMT-structure has the same value as the metallization area. Accordingly, at this length the figure-of-merit $R_{\mathrm{ON}}{\cdot}A$ has increased to more than double the value of the lowest possible area specific on-state resistance $R_{\mathrm{ON}}{\cdot}A_{\mathrm{MIN}}$ and such a design gets area-inefficient as well. Thus, with these equations a designer can generate a contour plot as shown for a conventional design in figure 21 and determine suitable design parameters for an area-efficient HEMT design a with tapered metallization.

The different on-state behaviors of finger structures with rectangular shape metallization and finger structures with tapered shape metallization can be demonstrated by observing the surface power density. Since the considerations in this section are made in the static-state the power is fully dissipated into heat. These locations on the structure with high power density are hot spots. The power density is calculated by the surface power per area $P_{\mathrm{A}} = \partial P/\partial A$. The power is calculated by the well-known equation $P = I^2{\cdot}R$, where R is the resistance of area A. At large gate width finger structures the dissipated power on metallization can get considerable. It is shown above that both terms of equation (4.15) become equal when the gate width is close to the critical gate width W_{crit}. The last term represent the resistive metallization, thus a structure with the critical gate width W_{crit} dissipates half of the power in the metallization.

A direct comparison between a conventional finger structure and a tapered finger structure is illustrated in figure 23. The power density distribution as a function of the finger position x is plotted for both structures. On the left side the power density is calculated with the current equations (4.5)-(4.7) for conventional finger structures with rectangular shaped metallization. In contrast to that, on the right side the power density is calculated with the current equations (4.12)-(4.14), which are derived for tapered finger structures. Typical design- and technology parameter of a large area power transistor are used for calculating this example. A large gate width is chosen with a value of $W = 3$ mm per finger. The area of the conventional structure, with $l_{\mathrm{MET,Rect}} = 5$ µm is equal to the area of the tapered structure with $l_{\mathrm{MET,Tapered}} = 10$ µm. Both structures have a channel length of $l_{\mathrm{DS}} = 20$ µm, which is a typical value for a HEMT devices with a breakdown voltage higher than 600 V.

The conventional structure with rectangular shaped metallization which is shown on the left side in figure 23 features high power densities at the source interface at position $x = 0$ and at the drain interface at position $x = W$. The total finger current has to pass these interfaces. The metallization length of the tapered structure is adapted to this total current. As the surface current density and the sheet resistance are both homogeneous for the tapered structure. The surface power density is homogeneous as well as shown in figure 23 (Right). The power densities at the interface positions can be calculated for both structures with equation $P_{\mathrm{A,IF}} = R_{\mathrm{SH,MET}} \cdot (I_{\mathrm{Total}}/l_{\mathrm{MET}})^2$. Because the surface power density of the tapered structure is homogeneous this formula is also valid for any position on the metallization. The power density of the active area of the tapered structure is given by $P_{\mathrm{A,2DEG,Tapered}} = R_{\mathrm{SH,A}}(I_{\mathrm{Total}}/W)^2$.

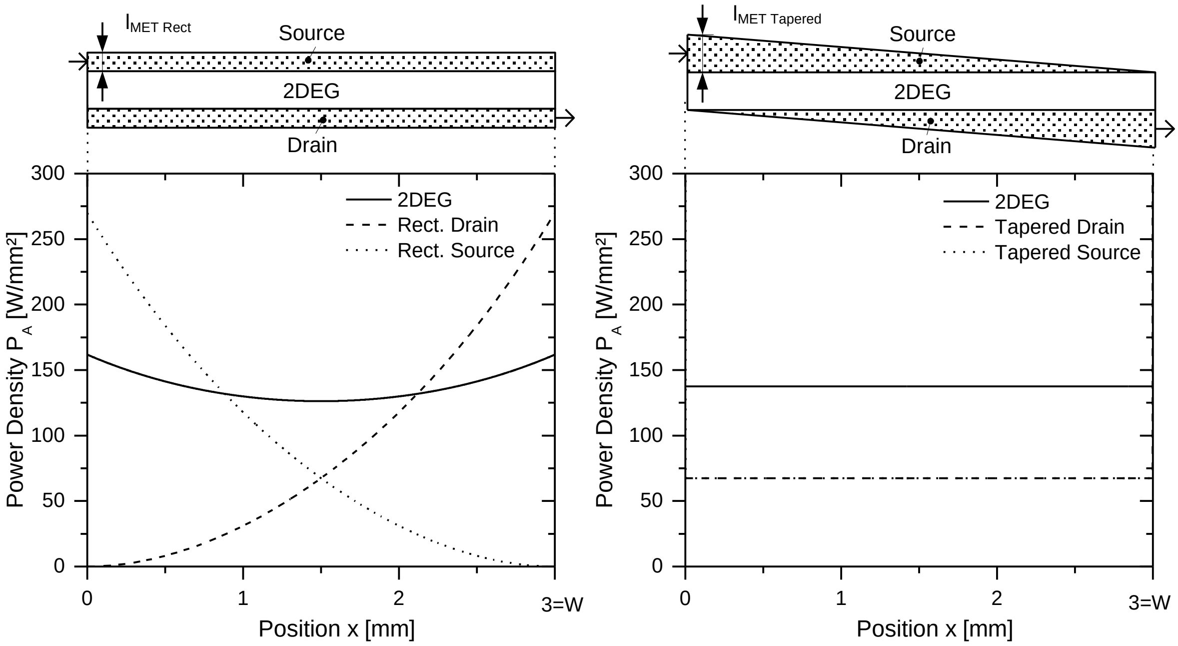

Figure 23: Comparison of the power density distribution along the x-axis on two different finger layouts. (Left) The power density on a conventional finger structure with rectangular shape drain- and source- metallization. (Right) The power density on a finger structure with tapered shaped drain- and- source metallization. Both layout are calculated with the same gate width $W = 3$ mm and area $A = 0.09$ mm². In addition typical technology- and design parameter are used for this calculation: $R_{\mathrm{SH,MET}} = 0.002\ \Omega$, $R_{\mathrm{SH,A}} = 500\ \Omega$, $l_{\mathrm{DS}} = 20\ \mu\mathrm{m}$, $I_{\mathrm{D}} = 1.5$ A, $l_{\mathrm{MET,Rect}} = 5\ \mu\mathrm{m}$ for conventional metallization, and $l_{\mathrm{MET,Tapered}} = 10\ \mu\mathrm{m}$ for tapered metallization.

As mentioned above both structures have the same area. The on-state resistances are determined with equation (4.9) for the conventional structure and with equation (4.15) for the tapered structure. The conventional structure with rectangular shaped metallization has an on-state resistance of $R_{\mathrm{ON,Rect}} = 4.1\ \Omega$ and the tapered structure a resistance of $R_{\mathrm{ON,Tapered}} = 3.9\ \Omega$. The values correspond to an area-specific on-state resistance of $R_{\mathrm{ON}} \cdot A_{\mathrm{Rect}} = 3.7\ \mathrm{m}\Omega \cdot \mathrm{cm}^2$ and an on-state resistance of $R_{\mathrm{ON}} \cdot A_{\mathrm{Tapered}} = 3.5\ \mathrm{m}\Omega \cdot \mathrm{cm}^2$.

In summary, tapered HEMT structures feature many advantages compared to a conational HEMT-finger layout with rectangular shaped metallization. Tapered HEMT structures have no current crowding in the active area. The current density is homogeneous along the fingers in the active area and in the drain- and the source-metallization. Thus there are no local thermal hot spots such that performance and reliability are improved. In direct comparison to a conventional finger layout a tapered layout features a low area-specific on-state resistance. However in practice the technological realization of tapered metallizations is challenging. The minimum possible lengths of the electro plating metallization and the ohmic contact limit the possibilities to realize such tapered finger metallizations. Nevertheless the advantages of tapered structures can be used for drain and source bus metallization of large area GaN-HEMT structures.

4.3.3 HEMT Structures with Short Ohmic Contact Length

The discussion in the sections above demonstrates the high impact of metallization on chip-area-efficiency. The drain- and source-metallizations are realized by a metallization stack, which consists of the electro plating metallization (METG), the metallization (MET1) and the ohmic contact (OHM). The electro plating metallization carries the drain- and source–currents along the finger structure. A conventional design is shown in figure 8 and such an arrangement is commonly used in literature, e.g. in [46], [47], or [48]. The length of metallization is in the range of the length of the ohmic contact $l_{\mathrm{MET}} \approx l_{\mathrm{OHM}}$. As discussed above the length of the metallization l_{MET} is often determined by the minimum possible dimensions of electroplating. In this technology the minimum dimension for metal strips made by electroplating is in the range of 10 µm. Consequently a significant part of area is consumed by drain- and source-metallization. As a consequence of the analytic results in section 4.3.1 a new intrinsic structure with reduced ohmic contacts was investigated in this work.

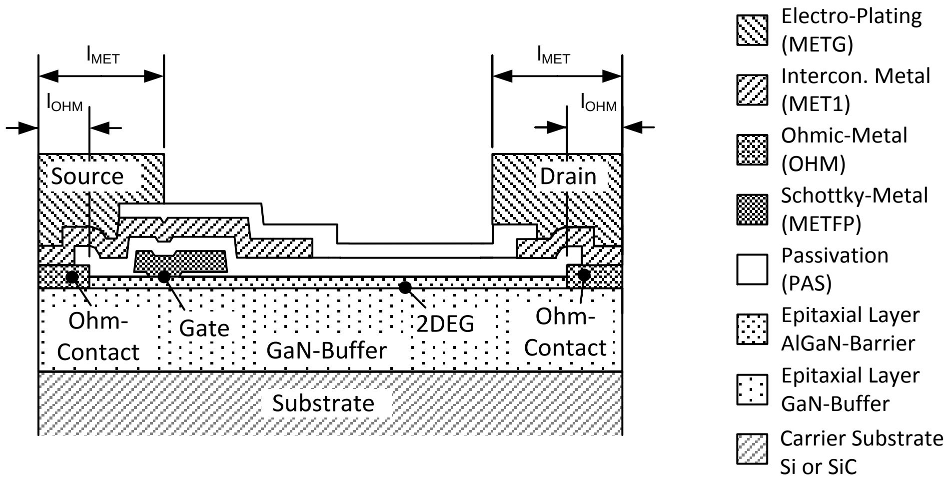

Figure 24: Cross-section of a HEMT in GaN technology with short ohmic contacts.

The length of the ohmic contact can be realized shorter than the length of the drain- and source- metallization such that $l_{\mathrm{MET}} > l_{\mathrm{OHM}}$. Such a design is shown in figure 24. The electroplating metallization can cover the passivation above the active area. Thus the total area is reduced to $A = (2 \cdot l_{\mathrm{OHM}} + l_{\mathrm{DS}}) \cdot W$, whereas the metallization resistance per unit length remains $R' = R_{SH,MET}/l_{MET}$. The ohmic contact can be shrunk to the technological minimum. Special TLM structures have been designed to characterize the short length ohmic contacts of this technology. The results are performed in section 2.3.4. The reduction of the ohmic contacts does not show degradation on the resistive performance. This is a value of about 3 µm for this technology. In multi-finger comb-structures the drain- and source metallization is used for two channels. Thus, the ohmic contact length can be reduced from $l_{OHM} = 5$ µm to $l_{OHM} = 1.5$ µm. The gain of area-efficiency can be demonstrated by the following design examples. The shrinking of the ohmic contact reduces the area-consumption for a 600 V device by a factor of about $(2\cdot l_{MET}+l_{DS})/(2\cdot l_{OHM}+l_{DS})$ = (10µm+20µm)/(3µm+20µm) = 0.76. The area-consumption of a 200 V devices is reduced by the factor of about (10µm+10µm)/(3µm+10µm) = 0.65. Thus with this reduction of the ohmic contact length the area-efficiency of a chip can be considerably improved.

4.4 Large Area Structures

4.4.1 Design of Bond-Pads

A suitable bond-pad layout is crucial for a high performance GaN-chip. An undersized interconnection technology due to small bond-pads can be the bottleneck of the device: the on-current capability will be reduced, the on-state resistance increased and the reliability of the device degraded. On the other hand an oversized layout reduces the chip-area-efficiency of a device. GaN-heterojunction devices are realized in a lateral technology such that the drain-, source- and gate-contacts are located on the top side. The area which is used for bond-pads cannot be used for active HEMT-structures. Therefore a suitable trade-off is needed. There is no generally valid solution, such that interconnection solutions have to be adapted to chip-size, package- or module environment, or other application issues. Interconnection technologies are well investigated, a good overview can be found in the literature, e.g. in [49]. Hence this work will not go into details. However because of the high relevance some layout specific issues are discussed in this section.

Conventional power technologies, as IGBTs or Power-MOSFETs are vertical devices. Such devices have a large source bond-pad on the top, as well as a smaller gate bond-pad on the topside and the drain-contact on the chip backside is directly connected with a package- or module- contact. The topside bond-pads are interconnected by large diameter bond wires (usually Ø ≥ 150 µm). Typically the interconnections are made by using round aluminum wires with copper core in wedge-wedge bond technology. These large diameter bond technologies are not suitable for the GaN-HEMT technology, which is used in this work. The bonds would cover too much pad area. Furthermore, these bond technologies feature high push- and pull-forces during the bond-process, which can destroy or lift-up the relatively thin pad-metallization. Therefore large diameter bonds with Ø > 100 µm are inconvenient for a conventional GaN-technology.

The devices which are fabricated in this work are interconnected by a high number of short length, low diameter wedge-wedge bonds (Ø = 50 µm). The high number of bonds results in a low inductive connection, which is advantageous for fast switching. Low diameter bond wires are more flexible, thus smaller bond loops with shorter bond lengths are possible. On the one hand a large diameter bond has a high cross-section area and is low resistive, on the other hand a low diameter bond can be realized with a much shorter length and thus it is low-resistive as well.

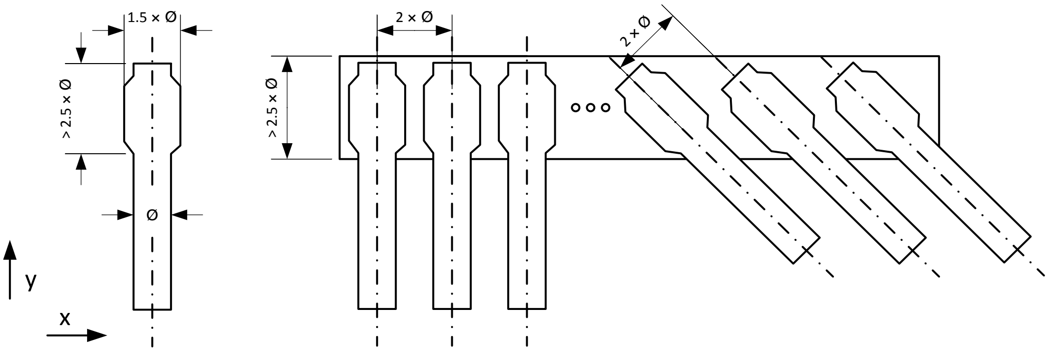

Figure 25: (Left) Typical bond-foot dimensions of a round wire in wedge-wedge bond technology. An arrangement of multi-wire bonds with a pitch in *x*-direction, and minimal pad-dimensions in *y*-direction. (Right) An angular arrangement of multi-wire bonds in a 45° angle.

The following rules for a bond pad design were used in this work: The bond foot of a round wire wedge-wedge bond is typically shaped to around 1.5 times of the wire diameter [49]. Therefore the pitches of two bond wire should be in the range of more than two times of the wire diameter. The weld-length of the bond food depends on the bond tool. With conventional tools a pad length of > 2.5 times of the wire diameter should be used in account for a bond pad. In case the pad length in *y*-direction is to low, the bond can be place with an angle of around 45° as shown in figure 25 on the right side. For power devices it is important that all bonds have similar shape, connection and length to achieve a similar resistance. If the bond resistances vary too much, the bond with the lowest resistance carry the highest current and may fuse. A chain reaction can occur, and all bonds can fuse one after the other.

4.4.2 Design of Area-Efficient-Comb-Layouts

The conventional structure for large-area GaN-HEMTs is the comb-layout. The design is simple and often used, but with inconvenient dimensions a comb-layout becomes inefficient. This section introduces design methods to develop area-efficient comb-designs. The comb-layout consists of a high number of single transistor fingers as shown in figure 19. The fingers are connected in parallel to build an interdigital structure as shown in figure 26. Two HEMT-finger structures share a drain contact in a way that the fingers are mirrored along the *y*-axis. As a consequence in multi-finger comb-structures the source contacts are shared as well. All drain contacts are connected together in parallel by a drain-bus line, which is also used as drain-bond-pad. In a similar way the source contacts are connected to a source-bus-line on the other side of the chip. The source bond-pad area is smaller because on this chip-side there are also the gate-pads. In contrast to the high drain potential in the off-state the source potential is similar to the gate potential. Thus between gate and source pads there are no high electric field and an early breakdown is avoided.

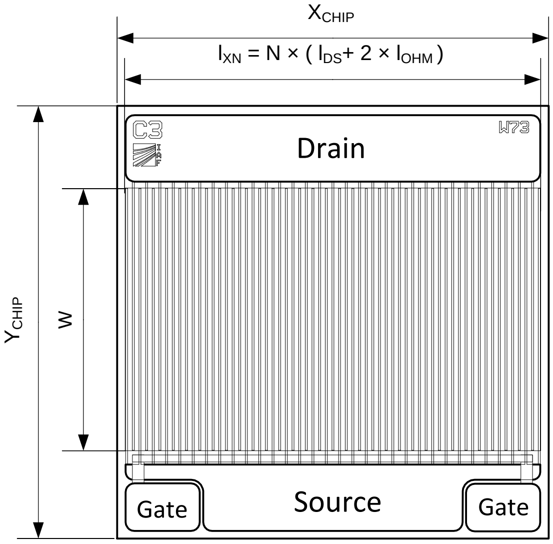

Figure 26: Multi-finger comb-layout for large area GaN-HEMT structures. The chip has an area of $A = 2{\times}2\ \text{mm}^2 = 4\ \text{mm}^2$, a channel length of $l_{DS} = 20\ \mu\text{m}$, finger gate width of $W = 1277.5\ \mu\text{m}$ and with a number of $N = 62$ fingers a total gate width of $W_{Total} = 73$ mm.

In the design in figure 26 there are two gate-pads at the outsides of the source-pad. Only one gate-pad has to be connected as both are connected to a common gate-bus line. There are gate-pads on both sides for reasons of flexibility for the packaging. The bus-line is realized on a different metallization layer than the source-bus. Thus it is possible to cross the source-metallization without short circuits between gate- and source- metallization. The minimum design dimensions for bond-pads are described above in the section 4.4.1. The gate carries only leakage currents. Therefore the gate-pad design has to be large enough for at least one bond, whereas the source-pad and the drain-pad have to be large enough for multi-bonds. The drain- and source-pads have to carry the total current of the chip. The example in figure 26 demonstrates the high amount of area for bond-pads. The chips has a total area of $A = 2{\times}2\ \text{mm}^2 = 4\ \text{mm}^2$, whereas the actual multi-finger area is given by $A_{Active} = W{\cdot}N{\cdot}(l_{DS}+2{\cdot}l_{OHM}) = 2.2\ \text{mm}^2$. Thus in this case around 45 % of the chip area is used for bond-pads and safety-distances. In terms of area-efficiency such a relatively small chip area with 4 mm² is inconvenient because of relatively large bond pads due to minimal safety margins for bond tools. For higher area chips the relation of multi-finger area to chip area is higher. But in general, an important question for a designer is: what is the best aspect ratio for a certain chip area? In this case a quadratic chip was chosen. The following section will introduce a method to analyze and determine a suitable aspect ratio with regards to area-efficiency.

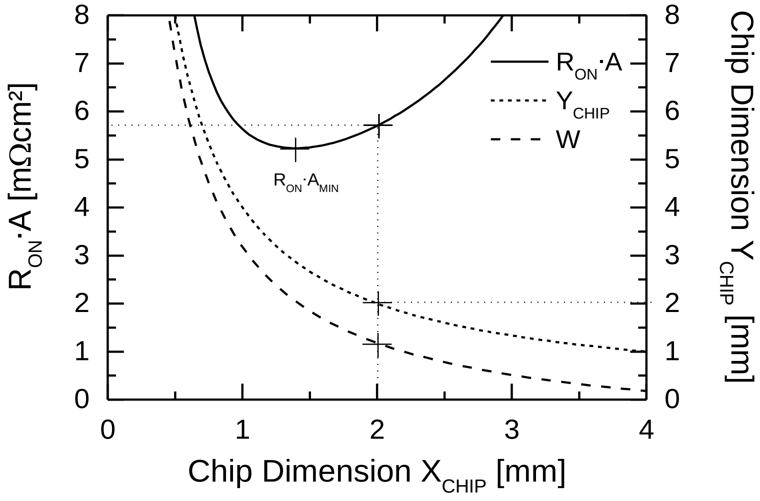

Figure 27: Area-specific on-state resistance as a function of the chip length X_{CHIP} (see equation (4.18)). On the right *y*-axis the chip dimensions in *y*-direction are shown (see equation (4.19)). With this graph the aspect-ratios $X_{\mathrm{CHIP}}/Y_{\mathrm{CHIP}}$ of a chip with a total area of $A = 4$ mm² can be analyzed. The following values are used for calculation: $l_{\mathrm{DS}} = 20$ µm, $l_{\mathrm{OHM}} = 5$ µm, $R_{\mathrm{SH,MET}} = 0.002$ Ω, $R_{\mathrm{SH}} = 500$ Ω, $Y_{\mathrm{periph}} = 0.82$ mm, $X_{\mathrm{periph}} = 0.15$ mm.

The analysis is demonstrated for a GaN-chip with a conventional comb-structure as shown in figure 26. The aim of this analysis is to determine an area-efficient aspect ratio for a chip with a total area of $A = 4$ mm². Some new dimensions are introduced for this calculation: the chip - length and -width are denoted by X_{CHIP} and Y_{CHIP}. As discussed above there is area needed for the pads, the gate-bus, and the safety-distances. The length, which is needed for this peripheral area in *x*-direction is denoted by $X_{\mathrm{periph}} = X_{\mathrm{CHIP}}\text{-}l_{\mathrm{XN}}$ and in *y*-direction by $Y_{\mathrm{periph}} = Y_{\mathrm{CHIP}}\text{-}W$. The total length of the multi-finger structure in *x*-direction is given by the expression $l_{\mathrm{XN}} = N\cdot(l_{\mathrm{DS}}+2\cdot l_{\mathrm{OHM}})$ and N is the number of fingers. The remaining area is calculated by:

$$W = \frac{A}{X_{\mathrm{CHIP}}} - Y_{\mathrm{periph}} = \frac{A}{N(l_{\mathrm{DS}}+2l_{\mathrm{OHM}})+X_{\mathrm{periph}}} - Y_{\mathrm{periph}}. \quad (4.18)$$

The total area-specific on-state resistance can be found by using equation (4.9), the target chip area A, and the total number of fingers N:

$$R_{\mathrm{ON}} \cdot A = \frac{\gamma A}{2G'N}\left(\frac{\gamma W}{2} + \frac{e^{\gamma W}+1}{e^{\gamma W}-1}\right). \quad (4.19)$$

It is enlightening to investigate the behavior of these two equations in a diagram. The area-specific on-state resistance, as a function of the chip dimension in *x*-direction and in combination with the chip dimension in *y*-direction, is shown in figure 27. The lowest value for area specific on-state resistance is calculated to be $R_{\mathrm{ON}}\cdot A = 5.2$ mΩcm² at a multi-finger length of $l_{\mathrm{XN}} = 2.1$ mm. With a corresponding finger gate width of $W = 2.16$ mm. The total chip dimensions would result in $A = 1.37\times2.92$ mm²= 4 mm². For some reasons a chip would not be practicable. Chips with rounded dimensions are easier to place on process masks without leaving a residue. Furthermore, the wafer dicing can easier performed due to coherent dicing streets and standardized picking tools. In addition such a power chip with less than 1.5 mm would have a relatively small source-pad. It would be challenging for an interconnection technology to interface the currents.

The design with aspect ratio of $X_{\mathrm{CHIP}}/Y_{\mathrm{CHIP}} = 2$ mm / 2mm = 1, is marked with dotted lines in figure 27. The specific on-state resistance is found to be $R_{\mathrm{ON}}{\cdot}A = 5.7$ mΩcm^2. Thus the on-state performance is slightly reduced compared to the lowest value $R_{\mathrm{ON}}{\cdot}A_{\mathrm{MIN}}$. But rounded dimensions are more reasonable as discussed above. The multi-finger length is $l_{\mathrm{XN}} = 1.85$ mm. With a corresponding finger gate width of $W = 1.18$ mm. The chip-dimensions are $A = 2{\times}2$ mm^2 = 4mm^2 as mentioned before. However, it is shown in figure 27 that a further increase of the chip size in x-direction would worsen the area-efficiency clearly. Consequently, the chip dimensions of the design in figure 26 are a suitable trade-off for a chip in the used technology and for the required chip-area in this example.

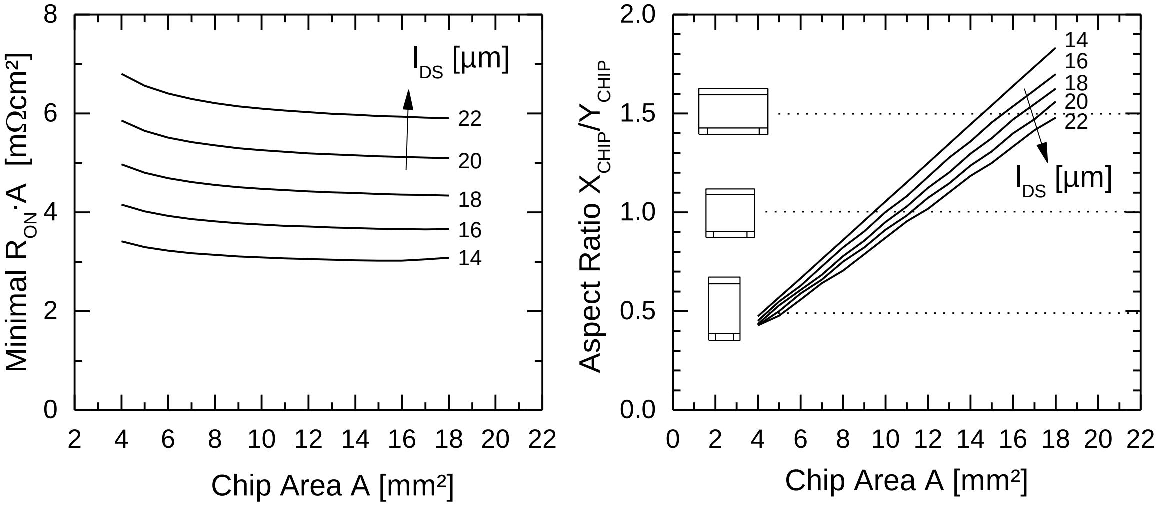

Figure 28: (Left) The minimal achievable area-specific on-state resistance $R_{\mathrm{ON}}{\cdot}A$ for a given chip-area A in case that a comb-structure is used. (Right) Plotted is the aspect ratio $X_{\mathrm{CHIP}}/Y_{\mathrm{CHIP}}$, which is required to achieve the lowest area-specific on-state resistance $R_{\mathrm{ON}}{\cdot}A$ for a certain area A. The following values are used for calculation: $l_{\mathrm{OHM}} = 5$ µm, $R_{\mathrm{SH,MET}} = 0.002\ \Omega$, $R_{\mathrm{SH}} = 500\ \Omega$, $Y_{\mathrm{periph}} = 1$ mm, $X_{\mathrm{periph}} = 0.2$ mm.

A chip-area of 4mm^2 is relatively small. The calculated curves in figure 28 give designers guidelines to find a suitable aspect ratio for area-efficient comb-designs. Assumed are typical initial parameters for a comb-design as shown in the figure-caption. The right plot shows the minimal achievable area-specific on-state resistance. It is shown, that the peripheral area increases the area-specific on-state resistance for low chip-areas. But this effect is compensated by using a low aspect ratio $X_{\mathrm{CHIP}}/Y_{\mathrm{CHIP}}$. On the right plot the corresponding optimal aspect ratio is given. Thus relative small chips have the best area-efficiency at a low aspect ratio. In contrast to that very large-area chips have a good area-efficiency at aspect ratios higher one. A low aspect ratio for large-area chips would result in high finger gate width and this would cause current crowding, as shown in the example in figure 20. The current crowding is higher for HEMTs with lower drain-source distance l_{DS}, therefore the gradient in figure 28 increases for lower channel lengths l_{DS}.

The calculations to find the lowest area-specific on-state resistance and the corresponding aspect ratio in figure 28 were made with automated algorithms and computed with numerical mathematics-software: GNU Octave [50]. It was examined how the function continues for huge chip-areas, with an area of $A = 100\ \mathrm{mm}^2$, a drain-source distance $l_{\mathrm{DS}} = 20\ \mu\mathrm{m}$ and the electrical parameters, as used for figure 28. The aspect ratio would continue to a value of $X_{\mathrm{CHIP}}/Y_{\mathrm{CHIP}} = 3.5\ \mathrm{mm} / 28.7\ \mathrm{mm} = 8.23$, and the area-specific on-state resistance would slightly decrease to $R_{\mathrm{ON}}{\cdot}A = 4.933\ \mathrm{m\Omega cm}^2$. Thus the chip dimensions approximate the shape of a bar in x-direction with increasing chip area. It is not beneficial to increase the y-dimensions. This would lower the area-specific on-state resistance due to current crowding.

4.4.3 Two-Dimensional Current-Density Simulations

In the sections above the analysis of finger structures and comb-structures were investigated by analytically derived equations. But if designers want to explore more complex shapes an analytic treatment gets extensive or there are no analytic solutions for a certain problem. In this case the finite element simulation is a helpful tool to illustrate the potentials and the current densities in the active area as well as in the metallization layers. With this it is possible to determine bottlenecks in designs. Different layouts can be explored and the simulation results allow a prediction of the performance. Furthermore, with the simulations analytic calculated solutions can be verified. Finite element simulations are often used for different physical problems. In this work the two-dimensional simulation of current densities in lateral HEMT structures was introduced and published at [45]. The software which is used for this finite element simulation is called FEMM. Corresponding information can be found in [51].

Since the GaN-HEMT technology is lateral, the reduction from a 3-dimensional problem to a 2-dimensional problem is possible under certain conditions. Some assumptions are necessary. In case that the length of metallization is in the range of the length of the ohmic contact the assumption can be made that $l_{\mathrm{MET}} = l_{\mathrm{OHM}}$. A further simplification can made in the case, that the ohmic contact resistance is low compared to the channel resistance. Thus the ohmic contact resistance is assumed to be negligible. Furthermore it is assumed that the sheet-resistance in the channel and on the metallization is homogeneously distributed and thermo-electric effects are not considered.

The 2-dimensional simulation results of the comb-structure are shown in figure 29. The structure is analyzed in section 4.4.2 and the layout with the dimensions is illustrated in figure 26. A voltage of 1 V is applied at the bond wire interfaces between drain and source. These are the boundary conditions for this simulation.

On the left side of figure 29 the potentials are plotted as greyscale image. It can be observed that drain metallization is uniformly on the 1 V potential whereas the source is uniformly on ground potential. The potential alteration occurs in the active channel area between the drain- and source- finger metallization.

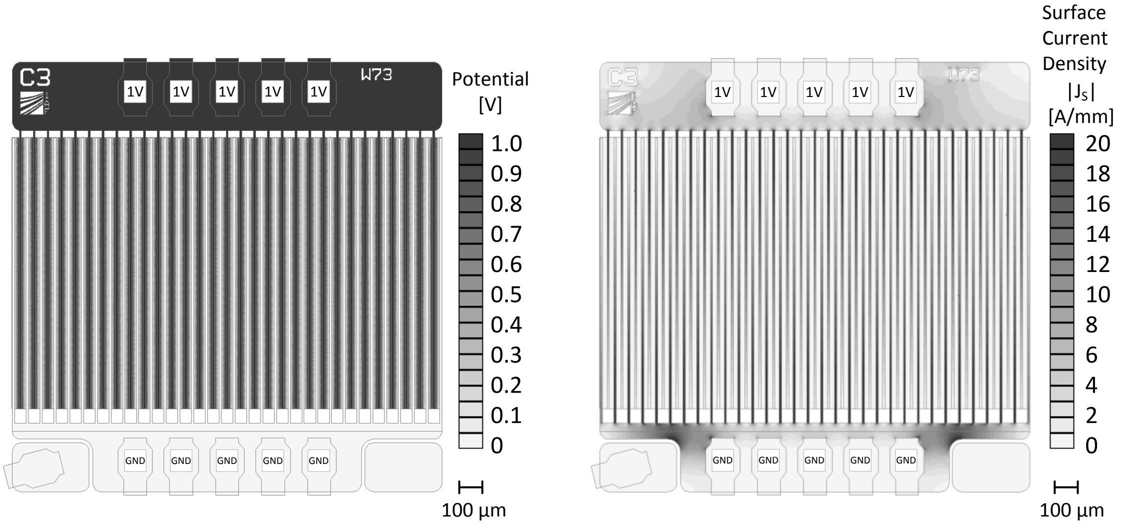

Figure 29: Two-dimensional simulation results of a comb-structure. (Left) The potentials distributed over the structure. (Right) The magnitudes of the current density $|J_S|$ distributed over the structure. (Conditions) The structure was simulated with a voltage of 1V between the boundaries at the bond wires. The sheet resistance of the active area is $R_{SH} = 500\ \Omega$ and the sheet resistance of the metallization is $R_{SH,MET} = 0.002\ \Omega$.

On the right side of figure 29 the magnitude of the surface current density $|J_S|$ is plotted as greyscale image. The bottlenecks of charge flow can be observed as dark regions. These areas with high current densities are located at the interfaces of each finger, or in other words, at each connection of drain-finger metallization and the drain bus, and on the other side on each connection of source-finger metallization and source bus. Furthermore a high current density can be observed close to the gate-pad, because at these locations the source bus metallization is subtracted by the gate-pad area. The highest surface current density in this simulation is in the range of $J_S = 20$ A/mm. An excursus regarding surface current density can be found in the appendix II.

Moreover, it is possible to determine the total on-state resistance of the structure, with the help of the simulation results. Therefore all partial currents across a line have to be integrated to the total current. The line has to cross the entire structure. In this example the line is dragged along the source-bus metallization above the gate pads. Thus all partial currents are included. The total current is found to be $I_{Total} = 6.94$ A. By taking into account the applied voltage of 1 V the simulated on-state resistance equals to $R_{ON,SIM} = 144$ mΩ. By using the parameters found in section 4.4.2 an on-state resistance of $R_{ON,CALC} = 142$ mΩ is calculated Thus the simulation results are in very good agreement with those obtained by the analytic calculation. On other large area structures, this simulation method was compared with measurement results with good agreement. These results are published in [45]. The results demonstrate the suitability of this method to analyze the current density of large area structures and to predict the total on-state resistance by 2-dimensional finite element simulations.

4.4.4 The Clover-Structure

The purpose of a large-area HEMT layout is to route the total current in an efficient way through a certain area. Low resistance, high reliability and a good interfacing to peripheral devices are main targets in design. There are numerous possibilities to arrange the high HEMT channel-width on a given chip area. The design of efficient comb-structures is shown above. But there are other structures with high area-efficiency and beneficial properties. Apart from electrical engineering there are similar matters in other fields. Nature demonstrates a diversity of energy-efficient flow structures in plants. Evolution has optimized plants for efficient energy exchange, and thus also the flow structures in plants are adapted for an efficient fluid exchange. There is an analogy between the flow of fluids-charge and the flow of electrical-charge, known as the electronic-hydraulic analogy. Due to this analogy an electrical current can be imagined as a liquid flow.

In this work a new area-efficient HEMT-layout was developed called clover-structure and shown in figure 30. The archetype for this structure is a four-leaf clover. On one hand the plant needs large-area leafs for photosynthesis, one the other hand an efficient flow-structure to the stipe of the plant is needed to exchange nutrient. Publication [52] shows the measurement results of a fabricated device. This section discusses further aspects found by simulations and it presents a direct performance comparison between a clover-structure and a comb-structure. A clover-structure consists of four large-comb areas. The drain bond-pad is centered, and four hyperbolic-shaped supply-lines are connected to the drain interfaces of the transistor fingers. The source-pad surrounds the chip at the cutting-edges. This source-bus can be used as bond-pad for small-diameter bonds (Ø < 75 µm). For large diameter bond wires a larger bond-pad area is provided in the four chip corners. There are also pads in each corner for connecting the gates. A gate runner is routed close to the source-bus around the chips. Thus only one gate-pad has to be connected. The other three pads are designed for redundancy and they increase the flexibility of the assembly technology. One large-diameter ball-wedge bond [49] can be used to connect the drain to a package pin. Short small-diameter bonds or small ribbon-bonds can be used to connect the source with the ground plate. This layout is well suited for the use in a conventional TO 220 package as shown on the right side in figure 30. This section describes a comparison between the clover-layout and the comb-layout in order to permit an evaluation. A clover structure is shown in figure 30. The chip has a total area of $A = 4\times4\ \text{mm}^2 = 16\ \text{mm}^2$, total gate width is $W_{\text{Total}} = 359$ mm and the drain-source distance is $l_{\text{DS}} = 20\ \mu\text{m}$. Furthermore, a comb-layout with the same chip dimensions and the same intrinsic HEMT-layout was designed as comb-structure. The layout with the comb structure achieves a considerably higher gate width, with a value of $W_{\text{Total}} = 397$ mm.

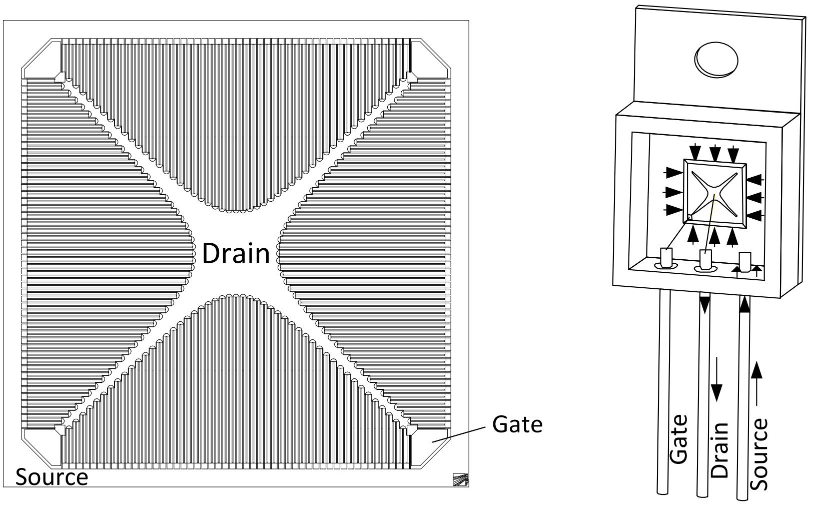

Figure 30: (Left) Large-gate width clover-layout with a chips size of 4×4 mm² and a total gate width of W_{Total} = 359 mm. (Right) Assembly of a GaN-HEMT with clover-layout in a TO 220 packaged.

Both structures have been simulated in a 2-dimensional finite element simulation to investigate the on-state behavior. The boundaries of the clover structure are applied in the center as circle with a potential of 1 V and on the chip-border with ground potential. The boundaries of the comb-structure are applied at the outer edges of the drain- and source-pad with the same drain-source voltage of 1 V. The simulation results are shown in figure 31 as grayscale plots. Illustrated is the magnitude of the surface current density.

Although the clover-layout has a lower total gate-width it achieves a lower on-state resistance compared the comb-structure. The on-state resistance of the clover-structure is simulated to be $R_{\mathrm{ON,Clover}} = 1\ \mathrm{V}/33.28\ \mathrm{A} = 30\ \mathrm{m\Omega}$, whereas the on-state resistance of the comb-structure has a simulated on-state resistance of $R_{\mathrm{ON,Comb}} = 1\ \mathrm{V}/30.59\ \mathrm{A} = 32.7\ \mathrm{m\Omega}$. The reason is the high finger gate-width of the comb structure. The impact of high finger width was introduced in section 4.2.2. With the method of section 4.4.2 the optimal aspect ratio and the lowest possible on-state resistance for a comb-structure can be analyzed. The lowest resistance for such an optimized comb-structure would be $R_{\mathrm{ON,Comb,MIN}} = 32\ \mathrm{m\Omega}$ with a corresponding aspect ratio of $A = X_{\mathrm{CHIP}} \times Y_{\mathrm{CHIP}} = 4.7 \times 3.4\ \mathrm{mm}^2 = 16\ \mathrm{mm}^2$, which is still worse than the resistance of the clover-layout. The gate widths of the comb fingers are $W = 3$ mm, whereas the maximum finger gate widths of the clover structure are $W = 1.38$ mm.

This is an advantage in terms of area-efficiency, but also it reduces the high current densities at the interfaces on drain and source metallization. This will improve reliability and the self-heating. The very high current density can be observed on the right side in figure 31 in the zoomed area. There are surface current densities up to $J_{\mathrm{S}} = 50$ A/mm, whereas on the left side of figure 31 the highest surface current densities are in the range of $J_{\mathrm{S}} = 30$ A/mm.

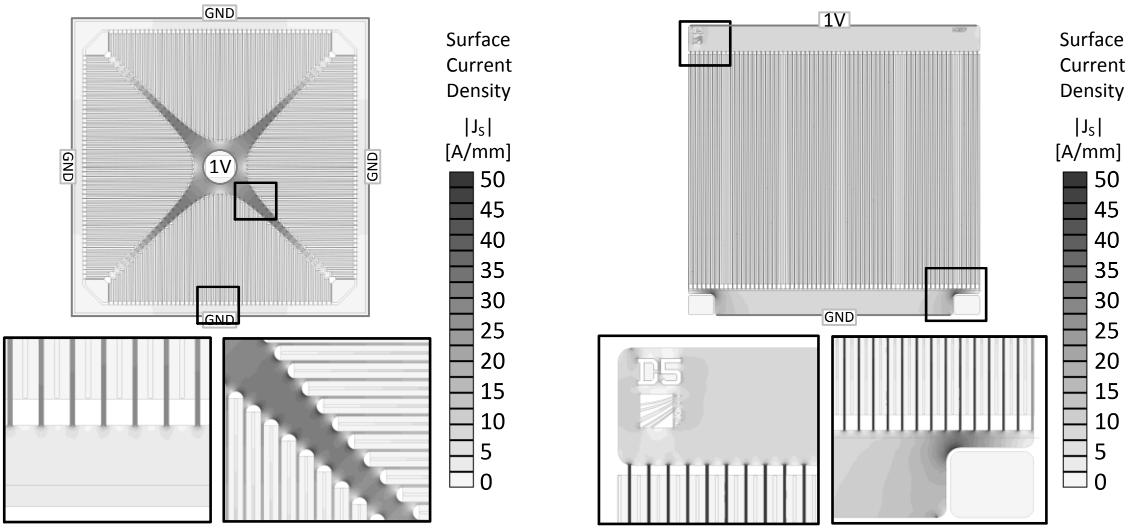

Figure 31: Direct comparison of two large gate width layouts by two-dimensional current density $|J_S|$ simulation. (Left) The simulation results of a clover-structure. (Right) The simulation results of a comb-structure. (Conditions) The area of both layouts is A = 4×4 mm². The sheet resistance of the active area is R_{SH} = 500 Ω and the sheet resistance of the metallization is $R_{SH,MET}$ = 0.002 Ω.

Consequently the clover design in this example has lower current densities compared to any comb-structure of the same size. In comparison a real device in a clover-layout would achieve a higher area-efficiency, a higher reliability, and lower self-heating effects. The fabrication and measurement results of such a GaN-device are shown in [52].

The clover-structure is area-efficient up to a certain area size. At very large areas the critical finger gate width will be exceeded again and the HEMT fingers with higher finger gate width will be inefficient.

4.4.5 Fractal-Structures for Power Devices

The limits of comb- or clover-structures with very large area are discussed above. For comb-structures in figure 28 an appropriate range of areas has been listed between 2 mm² and 20 mm². It is shown that very large area-chips get more and more high aspect ratios to remain area-efficient. However this is only feasible up to a certain size. It is shown in section 4.3.1, that it is not reasonable to increase the gate width W or the metallization length l_{MET}. The example in figure 21 shows that both actions would result in inefficient designs. A solution was found in this work to use a fractal metallization structure. The approach was published in [53] and it was patented in [54] and [55].

The term “fractal structure” has been coined by B. Mandelbrot in [56]. A fractal is a natural or artificial shape, which exhibits self-similar pattern on different orders in scale. A number of natural flow systems appear with fractal shapes, such as in blood circuits, roots, trees, or watershed. In many cases such structures feature energy- and area-efficient properties, optimized by evolution or by the physical principle to find a lower-energy state. Usually such structures are power density adapted. In such fractal flow structures the matching is achieved by branching of the supply line. Fractal flow structures have already found their applications in heat flow or liquid flow structures. However till now fractals have not been consciously used in electrical designs to improve the electric current flow.

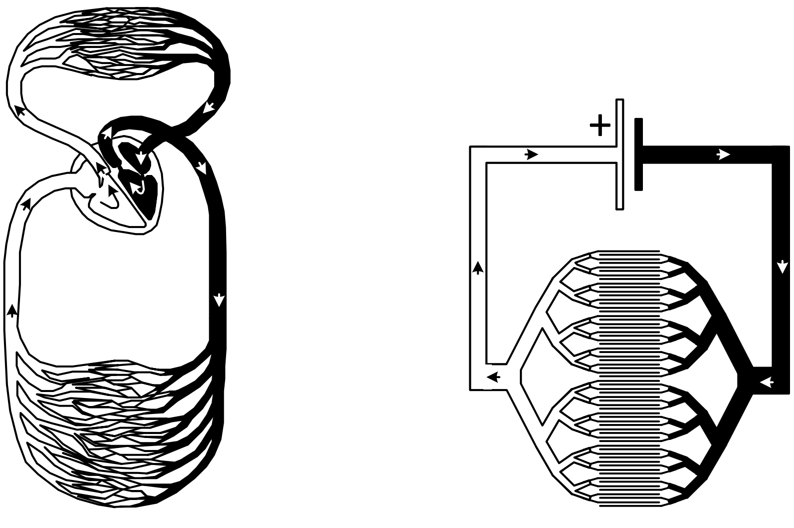

Figure 32: The principle of a natural fractal flow structure and the adaptation to an artificial-designed charge flow structure. (Left) A schematic drawing of a human blood circuit. (Right) a schematic drawing of an electrical circuit with a fractal load.

On the left side in figure 32 an example of the human blood circuit is illustrated. This is a good example for a fractal flow structure with fractal input and output. And thus it can be adapted to electrical structures with in- and outgoing supply lines. On the right side in figure 32 an electrical circuit with arbitrary fractal load is illustrated. However the fractal approach can be applied in various, concrete electrical flow structures, for example as metallization for large area solid-state lighting systems, or for solar cells. This section explains the design of a fractal area-efficient metallization structure for lateral large area power devices, as GaN-diodes or the drain-source metallization of HEMTs.

The design of a fractal metallization structure is shown in figure 33. The design consists of several nested finger structures. The base cell or the lowest order of the fractal structure in figure 33 is a conventional transistor finger as shown in figure 19. The length of drain- and source-metallization is denoted by $l_{\mathrm{MET},1}$, the drain-source distance by $l_{\mathrm{DS}} = l_{\mathrm{A}1}$ and the gate width by W_1. If the sheet resistance of the active area $R_{\mathrm{SH,A},1}$ and metallization $R_{\mathrm{SH,MET},1}$ are known, than the on-state resistance of such a finger $R_{\mathrm{ON},1}$ can be calculated by equation (4.9).

The 2^{nd} order of the structure is a multi-finger structure or comb-structure as shown in section 4.4.2. In case that the interfaces of drain and source are placed in an analogous manner to the interfaces of a single finger, than the dimensioning of a comb bus metallization can be treated equally to a single finger design. Therefore new finger parameters have to be calculated. The drain-bus length and the source-bus length of such a finger are denoted with $l_{\mathrm{MET},2}$. The new width of such a 2nd order finger is $W_2 = N{\cdot}(2{\cdot}\mathrm{l}_{\mathrm{MET1}}+l_{\mathrm{A1}})$. The new channel length correspond to the single finger width, thus $l_{\mathrm{A2}} = W_1$. Furthermore for a comb with a high number of fingers an equivalent active sheet resistance can be defined. This new sheet resistance is given by $R_{\mathrm{SH,A2}} = R_{\mathrm{ON1}}{\cdot}W_1/l_{\mathrm{DS}}$. The sheet resistance of the drain-bus and source-bus metallization is denoted as $R_{\mathrm{SH,MET2}}$. With these new 2nd order parameters the on-state resistance of the 2nd order finger can again be calculated by equation (4.9).

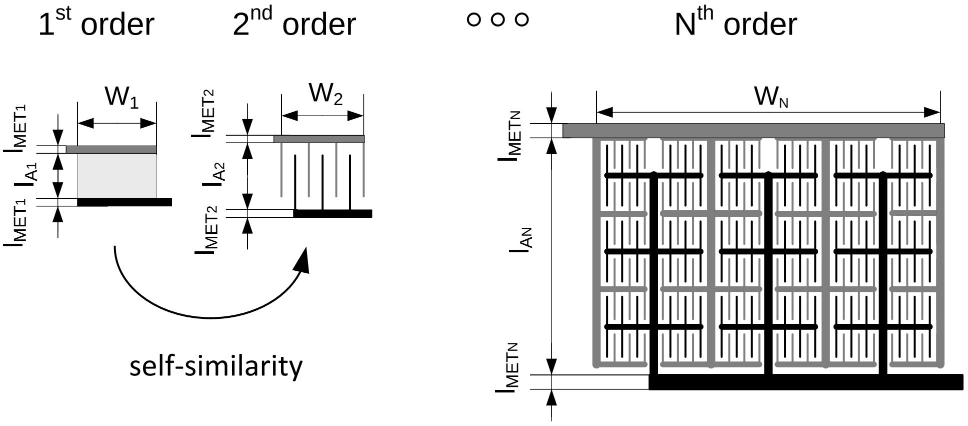

Figure 33: Design of a fractal metallization structure for large-area power devices, e.g. a lateral diode. On the left side a 1st order structure is illustrated. In the middle a 2nd order structure is a multi-finger connection of 1st order structures, and on the right a nth order structure is a multi-structure connection of (n-1)th structures.

The 3rd order of the structure is a multi-finger structure of the 2nd order finger structure. The procedure to calculate the on-state resistance of higher orders is the same as shown for the 2nd order. Thus the complete fractal structure can be designed or analyzed by the theory for comb layouts as shown in this section.

In terms of area-efficiency a designer should apply the insight of section 4.3.1. The equivalent sheet resistance $R_{\mathrm{SH,A,X}}$ is significantly reduced at each order. However a problem is with only one electroplating metallization layer the sheet resistance $R_{\mathrm{SH,MET,X}}$ remains constant for each order. Compensation by enlarging the metallization length $l_{\mathrm{MET,X}}$ is not suitable. This would result in area inefficient higher orders finger designs. Therefore the metallization thicknesses $T_{\mathrm{MET,X}}$ have to be increased at each order. This important issue in design is illustrated in figure 34. It shows a 3-dimentional sketch of a fractal chip metallization. The metallization cross-section dimensions of each order rises not only in length $l_{\mathrm{MET,X}}$, is rises also in the thickness $T_{\mathrm{MET,X}}$.

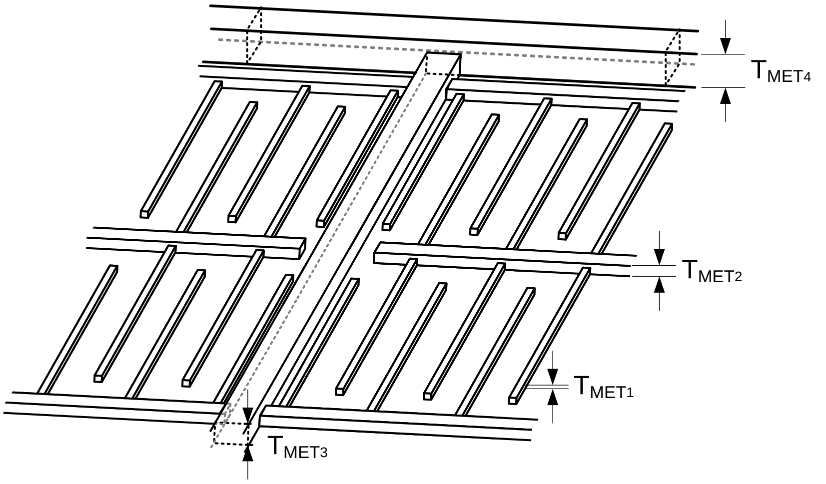

Figure 34: Three-dimensional drawing of the metallization of a fractal structure. The thickness of the metallization rises at each order to achieve a reduction of the metallization sheet resistance of each order.

A fractal layout is shown in figure 35. It is realized on the 4th order and has an area of 4×3 mm². The drain-source distance is relatively high $l_{DS} = 25$ µm and the structure has a total gate width of $W_{Total} = 194$ mm. The fractal structure is based on two metallization layers, MET1 and METG. The metallization of the 1st order fingers are realized on MET1 with a short metallization length $l_{MET} = 4.5$ µm to achieve high area-efficiency. On the left side of figure 35 a 2nd order element is illustrated. It consists of 12 1st order fingers in meander shape. In contrast to a conventional comb-structure the meander shape has the advantage, that no gate bus is needed. Furthermore, there is no isolated zone between the source-finger-end and the drain-metallization, and there is no isolated zone between the drain-finger-end and the source-metallization respectively. These issues save chip area, whereas area is lost caused by the arc-shaped metallization. Furthermore current-crowing occurs in the active area close to the drain- and source-ends caused by high current density. Due to the low sheet resistance of metallization (MET1) with $R_{SH,MET1} = 0.1\ \Omega$ and the short metallization length l_{MET} the gate width of the 1st order finger has to be low. The 2nd order element was simulated and achieves an on-state resistance of 7.04 Ω. It has an area of 0.191×0.354 mm² and achieves an efficient area-specific on-state resistance of $R_{ON} \cdot A = 4.76\ \text{m}\Omega\cdot\text{cm}^2$.

On the right side of figure 35 the entire fractal HEMT layout of drain- and source-metallization is illustrated. The 2nd, the 3rd and the 4th orders of metallization are realized in the same electro plated metallization (METG). As discussed above this is not recommended in terms of area-efficiency. However due to lack of further metallization layer this was the way to proceed. The 2nd order finger structure is designed with a rectangular finger metallization as analyzed in section 4.2.2., whereas the 3rd and the 4th order are designed in tapered shaped metallization. As shown in 4.3.2 a tapered metallization reduces current crowding and saves area. In a 2-dimensional finite element simulation an on-state resistance of $R_{ON} = 86\ \text{m}\Omega$ was simulated for the structure. Combined with the chip size of 4×3 mm² an area-specific on-state resistance of $R_{ON}{\cdot}A = 10.3\ \text{m}\Omega{\cdot}\text{cm}^2$. This value is relatively area-inefficient compared to the value of a well-designed comb-structure. The conventional comb structure can achieve a value of $R_{ON}{\cdot}A = 7.5\ \text{m}\Omega{\cdot}\text{cm}^2$ with these chip dimensions and simulation parameters. This fractal structure was design in the beginning of this work. The theoretical background was not developed at that time. But nevertheless the layout contained a number of new concepts and it has demonstrated the feasibility as structure for large-area HEMT structures.

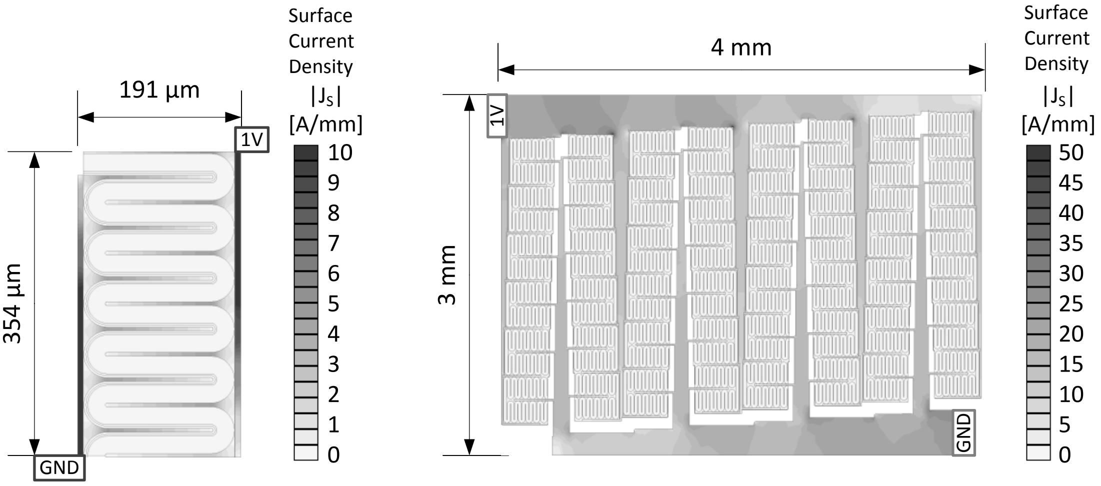

Figure 35: Results of a two-dimensional finite element simulation of a fractal HEMT structure. Illustrated is the current density $|J_S|$. (Left) 2nd order element of the fractal structure. (Right) Complete fractal 4th order layout. (Conditions) The sheet resistance of the active area is $R_{SH,A}$= 500 Ω, the sheet resistance of the first metallization layer is $R_{SH,MET1}$ = 0.1 Ω and the sheet resistance of the electro plated gold metallization is $R_{SH,METG}$ = 0.002 Ω.

A further crucial property of a fractal flow structure is the adapted current density on each new order. This advantage is independent of the issue of area-efficiency. An adapted, more homogeneous current density on large are a power structures lead to reliable designs and it reduces local hot spots. Consequently fractal designs as shown in this section are predestinated for very large chip areas. However for the design of advanced fractal layouts further metallization layers are required, as shown in figure 34.

4.5 High Current Operation

GaN-HEMTs are able to achieve high on-state currents due to a high electron density as well as high carrier mobility in the heterojunction channel. GaN devices carry significant higher on-state currents per chip-area compared to state-of-the-art Si-devices. For example, the results of a benchmark test in [57] demonstrates, that even today the on-state current per chip-area of a GaN-HEMT device is more than two times higher compared to state-of-the-art Si counterpart devices. In this section the high on-state current operation of GaN-HEMTs is experimentally characterized. Furthermore, in this section, the thermal issues of self-heating are qualitatively investigated by experiments to demonstrate the impact on performance. However, it is emphasized that temperature related effects are also closely associated with the assembly technology, which is not in the focus of this work. A suitable thermal management by a novel assembly technology for these GaN-power devices is given in the work of A. A. Bajwa in [58] and [59]. In these publications issues of layout-dependent thermal aspects are discussed.

4.5.1 On-State Current Saturation

As shown above in section 4.2 the sheet resistance of the active area $R_{\mathrm{SH,A}}$ and the channel length l_{DS} are the dominating parameters to determine the channel conductivity by $G' = 1/(2 \cdot R'_{\mathrm{OHM}} + R_{\mathrm{SH,A}} \cdot l_{\mathrm{DS}})$. But this equation is only valid in the range where on-state currents are not saturated. In high current operation the on-state currents saturate at a certain knee voltage. The maximum current decreases by self-heating at higher drain-source voltages. The behavior of current saturation as a function of the channel length l_{DS} is demonstrated in an experiment. The drain current is measured in the on-state with a gate-source voltage of $V_{\mathrm{GS}} = 1$ V, and the channel length is parameterized from $l_{\mathrm{DS}} = 6$-20 µm. The measurements have been made with continued supply voltages without pulsing. The measurement results are shown in figure 36. The saturation characteristics can be modelled by using a hyperbolic tangent function, defined as:

$$G' = \frac{I'_D}{V_{\mathrm{DS}}} = \frac{I_{\mathrm{D,MAX}}}{V_{\mathrm{DS}}} \cdot \tanh\left(\frac{V_{\mathrm{DS}}}{I_{\mathrm{MAX}}\left(2R'_{\mathrm{OHM}} + R_{\mathrm{SH,A}} l_{\mathrm{DS}}\right)}\right). \tag{4.20}$$

A comparison of measurements and results of an empirical model is shown in figure 36.

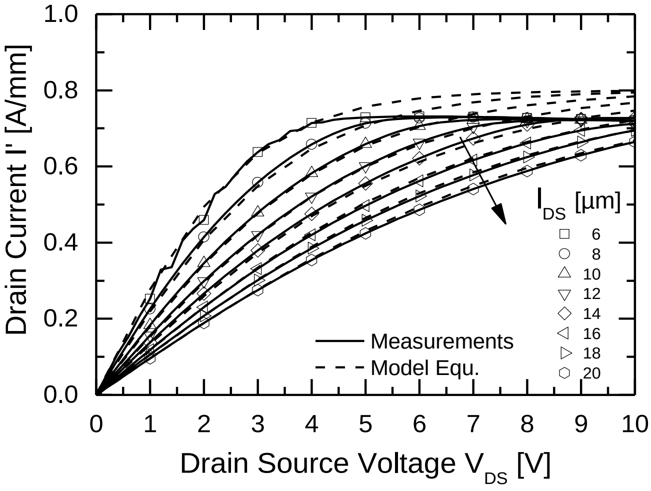

Figure 36: The on-state conductivity is given by $G'=I_{\mathrm{D}}'/V_{\mathrm{DS}}$. The plot shows the on-state current as a function of the drain–source voltage. The channel length is parameterized between: $l_{\mathrm{DS}} = 6$-20 µm. The continuous lines are measurement results measured on $W = 50$ µm GaN-on-SiC HEMTs at a gate voltage of $V_{\mathrm{GS}} = 1$ V. The dashed lines are the model curves given by equation (4.20).

The simple, empirical model describes the saturation behavior with a good agreement. But at higher drain-source voltages the high power density leads to self-heating in the channel and this leads to current degradation. The comparison of the ideal model and the measurement results illustrate the impact of the self-heating. Without this degradation the current would achieve a maximal current $I_{D,MAX}$ and this value is independent of the channel length l_{DS}.

The gate-length of a HEMT-structure is often discussed in terms of high frequency properties, such as the transit frequency. However, the gate-length also has a high impact on the static transfer characteristic. In Schottky devices the gate-length may even affect the maximal drain current. This gate-length dependent behavior is shown in measurement results and illustrated in figure 37.

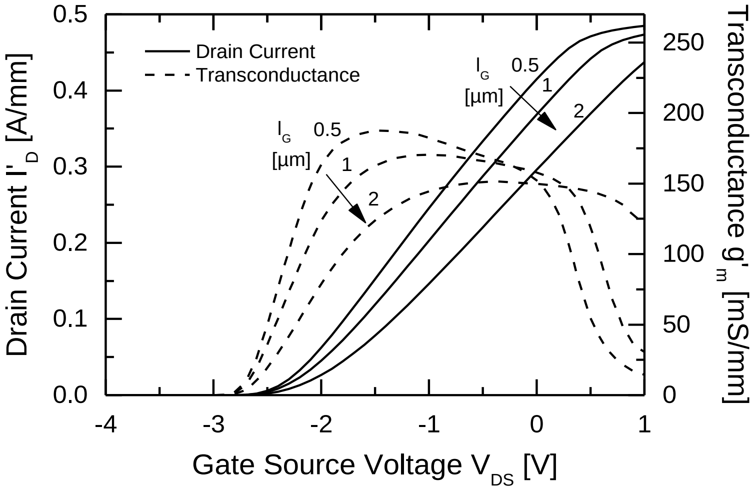

Figure 37: The transfer behavior a high voltage GaN-HEMT. The plot shows the drain current and the resulting transconductance as a function of the gate voltage. The measurement results are shown for three different gate length l_G: 0.5 µm, 1 µm and 2 µm, on small GaN-on-Si HEMTs with $W = 50$ µm and $l_{GD} = 15$ µm. The drain-source voltage is fixed at $V_{DS} = 10$ V.

With rising gate-length the gradient of the drain-current as a function of the gate-voltage decreases. This becomes clear at the transconductance g_m. The transconductance is the derivative of the drain-current given by $g_m = \partial I_D / \partial V_{GS}$. The highest transconductance is achieved with the lowest gate-length. It is shown that the structure with the lowest gate length achieves the highest current at $V_{GS} = 0$ V. The three curves tend to merge again at higher gate-voltages, but this convergence is affected by another property of the Schottky gate. The Schottky contact will become conducting before the maximal drain-current is reached. Furthermore, local heating of the rising gate-current will affect the channel in addition. Therefore, the choice of the gate length should be made with caution. A short gate-length $L_G < 1$ µm leads to a high transconductance and this may causes dynamic instabilities. A long gate-length $L_G > 1.5$ µm may affect the on-state performance as well as shown in this example. In this work a gate-length of $L_G = 1.0$ µm was found to be a good tradeoff.

Low on-state resistances at high drain-currents are desired properties of highly efficient power transistors. The question raises, what is an efficient operating point in the on-state and how are area-efficient HEMT finger designs affected by self-heating? Therefore the self-heating effect, which is already observed in this section, will be characterized in more detail in the following section.

4.5.2 Self-Heating

The case that the dissipated power of a HEMT structure heats up itself is called self-heating. The sheet resistance $R_{\mathrm{SH,A}}$ of the active area (2DEG) is highly dependent on the temperature. The sheet resistance is a function of the carrier density n_{i}, the carrier mobility μ and the elementary charge e. The sheet resistance is calculated by equation $R_{\mathrm{SH,A}} = 1/(e \cdot n_{\mathrm{i}} \cdot \mu)$, and the mobility is reduced at higher temperatures due to phonon scattering, as shown in the literature e.g. in [12]. Thus the on-state performance is strongly influenced by the temperature generated by the dissipated power and the thermal interface to a heat sink. The self-heating behavior is well investigated for high frequency devices as power bars for mobile applications, e.g. as shown in [60] and many others. However, these results can be only partly applied to large area high voltage devices for power applications. Power HEMT devices have a much higher gate-gate pitch compared to power bars. GaN-based power devices are usually realized on Si substrates, and this has a lower thermal conductivity compared to SiC, which is usually used as carrier substrate for high frequency devices. The losses of high frequency transistors are mainly determined by the switching losses, whereas power transistors are mainly determined by the static on-state losses. Only in case of compact and high frequency switching converter applications the losses of a power transistor is determined by both: on-state losses and the switching losses. A detailed analysis is not focused in this work but the impact of self-heating and the influence on the on-state performance is demonstrated in an experiment. For comparison, similar self-heating investigations have been concurrently made by O. Hilt on large area power devices and published in [61].

An experiment was performed in this thesis to discover the self-heating effect of large area GaN-HEMTs with an area of $A = 4\times3\ \mathrm{mm}^2$. The total gate width of the device is $W = 260$ mm. This structure was characterized on GaN-on-Si as well as on GaN-on-SiC. The drain current curves with a corresponding gate-source voltage of $V_{\mathrm{GS}} = 1$ V are measured on-wafer in a four-point measurement setup. The experiment illustrates the degradation of the on-state current I_{D} as a function of drain-source voltage V_{DS} and as a function of the pulse duration t_{PLS}. Furthermore, a comparison of two different substrates was made.

The measurement results are shown in figure 38. A strong degradation of the on-current is demonstrated as a function of the pulse time t_{PLS}. However, the impact is only observable at high power pulses $P_{\mathrm{PLS}} > 50$ W. The degradation is relatively low below a pulse power of $P_{\mathrm{PLS}} < 50$ W, even at a maximal pulse time of $t_{\mathrm{PLS}} = 2$ ms. The degradation of the current I_{D} at a corresponding drain-source voltage $V_{\mathrm{DS}} = 10$ V is significant. The current degrades by 35 %

from $I_D = 76$ A to 50 A on the GaN-on-SiC wafer, and the GaN-on-Si wafer by 43 % from $I_D = 76$ A to 43 A. The lowest possible pulse time in the setup is $t_{PLS} = 100$ µs and the highest possible pulse time with the highest degradation in this setup is $t_{PLS} = 2$ ms. It is remarkable that the difference between GaN-on-SiC and GaN-on-Si is relatively low. The thermal conductivity of SiC is much higher than on Si. SiC has a thermal conductivity of $\lambda_{SiC} = 3.4\text{-}4.5$ W/(cm·K) and Si has a value of $\lambda_{Si} = 1.5$ W/(cm·K), as shown in table 1. Both wafers are unthinned and have a thickness of about 600 µm.

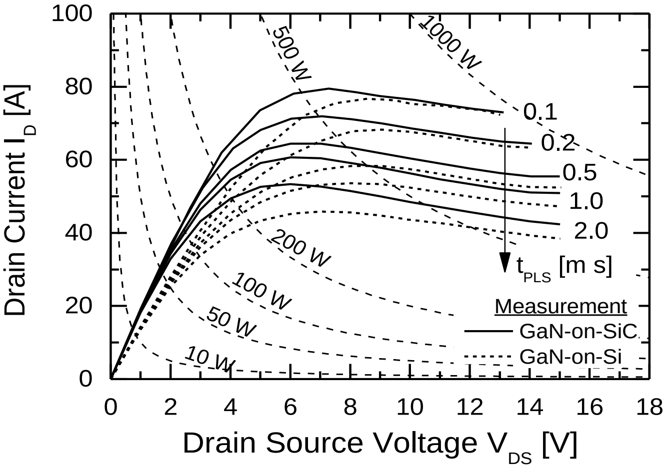

Figure 38: Influence of self-heating in the on-state performance is shown on a large area HEMT structure. The on-state current I_D at a gate voltage of $V_{GS} = 1$ V is measured as a function of the drain-source voltage V_{DS} and as a function of the pulse time t_{PLS}. Measurements are made on-wafer in a four point measurement setup. The device has a gate width of $W = 260$ mm and an area of $A = 4 \times 3$ mm².

The result of this experiment show that self-heating has a high impact and it can lead to strong performance degradation. For high power operation, a suitable assembly technology is necessary, as shown for example in [1]. Another finding of this experiment is that the on-state resistance in the lower power range is not affected by self-heating.

Large area GaN-HEMT devices are typically designed in multi-finger configurations. The parallel connection of several fingers reduces the effect of heat spreading. The following experiment demonstrates the influence of self-heating, in case of multi-finger connections. As shown in figure 20 the increase of the single finger gate width results in a decrease of the specific on-state resistance. In this experiment a number of fingers with a single finger gate width of around 1 mm are connected in parallel to multi-finger structures. The multi-finger structures feature a gate-drain-gate pitch of 44 µm and a gate-source-gate pitch of 14 µm.

The measurement results are shown in figure 39. The experiment illustrates that multi-finger configurations generate heat accumulation and this leads to self-heating and current degradation, whereas at low power the self-heating effect is negligible.

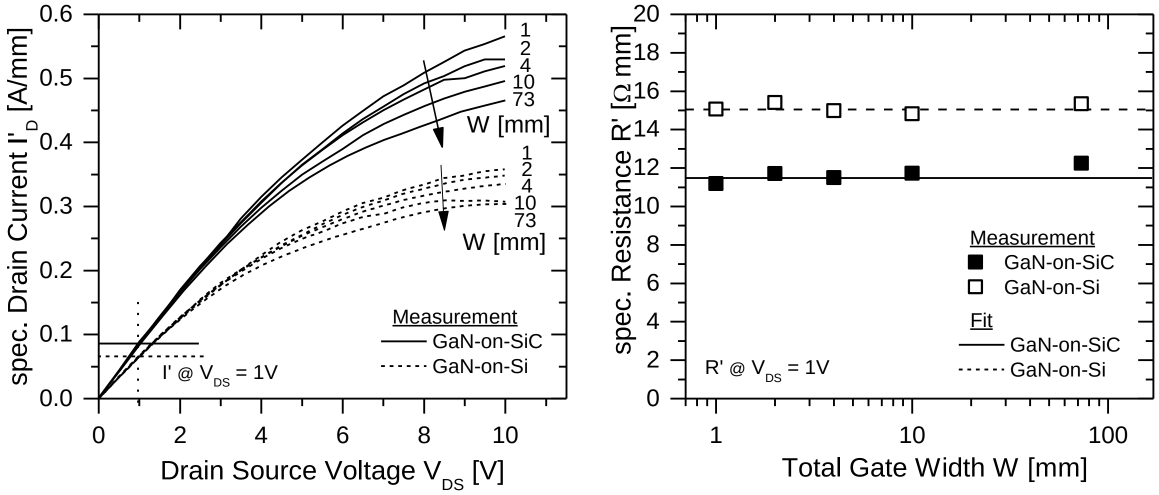

Figure 39: Influence of self-heating on multi-finger structures. A number N of fingers with a gate width around 1 mm^2 is connected in parallel. A pulse time of t_{PLS} = 0.1 ms was chosen. (Left) The current per unit length is measured in the on-state at a corresponding gate-source voltage of V_{GS} = 1 V as a function of drain-source voltage V_{DS}. (Right) The specific on-state resistance measured at a gate source voltage of V_{DS} = 1 V is illustrated as a function of the total gate width.

Self-heating affects the on-state performance, but on the other hand the current degradation has an import advantage. It leads to thermal stability on large area structures with a high number of HEMT-fingers. If the current flow of one transistor finger is higher than on other fingers, the power dissipation will be increased on this finger. This higher power leads to self-heating and reduce the current flow on this finger. This characteristic is very important in power devices. In contrast to this thermal-electric self-stabilization the parallel connection of bipolar transistors can cause a thermal runaway and can result in destruction [62].

4.5.3 Electromigration

A main focus in this work is the design of area-efficient layout structures for large-gate width GaN-HEMT structures. One strategy to achieve area-efficient designs is to reduce the area of metallization. With the analysis of section 4.3 and 4.4 a designer is able to find a good compromise between metallization area-consumption and its resistivity. However reduction of metallization and high current density can cause reliability issues, as the effect of electromigration. The investigation of long term reliability is an important issue for most application areas, especially for safety-relevant applications as automotive or aerospace. Therefore the effect of electromigration is important in terms of reliable high current operation and should be taken into account. This work does not investigate the reliability of GaN-HEMT structures in terms of electromigration, but it will refer to relevant literature in this section.

The effect of electromigration is caused by the movement of ions in a conductor. There are two reasons for this movement. The first and the main reason is a movement of ions due to the momentum of drifting electrons. The second, but less important reason is a movement caused by the electric field. The result is a migration of the conductor material. The reduction of the conductor cross-section increases the current density at the affected location, and thus the electromigration effect is further intensified at that location till the conductor is interrupted. An overview and an introduction to the topic can be found in [63] or in section 2 of [64].

Beside the value of current density the electromigration is influenced by other material properties and structure dimensions. The migration appears primarily at grain boundaries in inhomogeneous crystalline structures. Thus gain size and distribution are relevant. Moreover the dimensions and in particular the length of a metallization is important. I. A. Blech has found a critical structure length l_{Bl} [65]. This so called "Blech length" can be determined by an experiment, as shown in [64] or [65]. Below this critical length l_{Bl} a structure is not affected by electromigration. The product of the current density and the "Blech length" is a constant value $K_{\mathrm{Bl}} = J \cdot l_{\mathrm{Bl}}$. Thus if the current density is decreased the critical "Blech length" is increased. Experimental results of electroplated gold-strips on Si-substrates are shown in [66]. In the experiment the metallization-strips under test have a length of $l_{\mathrm{MET}} = 12.5\ \mu\mathrm{m}$ and the thickness of $T_{\mathrm{MET}} = 4\ \mu\mathrm{m}$. A critical product of the current density and the "Blech length" was found to be $K_{\mathrm{Bl}} = J \cdot l_{\mathrm{Bl}} = 19\ \mathrm{kA/mm^2} \cdot 14.9\ \mu\mathrm{m} = 283\ \mathrm{A/mm}$. The result is not fully applicable to the technology used in this work, but it can be used as comparable reference value. The value shows that most finger structures in this work are exposed by electromigration, if they operate under continuous high current conditions.

An empirical model to estimate mean time to failure (MTTF) of an interconnection is given by "Black's equation" and this was published in [67]. The mean time to failure is the time after 50 percent of the tested interconnections are failed. The equation is expressed by:

$$\mathrm{MTTF} = \frac{A}{J^n} \exp\left(\frac{E_a}{k \cdot T}\right). \tag{4.21}$$

Where A is a material dependent constant, J current density, and n is its exponent. This value is typically between 1 and 2. The activation energy is denoted by E_{a}, k is the Boltzmann's constant and T is the temperature of the metallization. The activation energy of electroplated interconnections was determined in [68]. The metallization-strips had a length of $l_{\mathrm{MET}} = 12.5\ \mu\mathrm{m}$, a thickness of $T_{\mathrm{MET}} = 4\ \mu\mathrm{m}$ and a width of $W = 450\ \mu\mathrm{m}$. The metallization was stressed with a current density of $J = 20\ \mathrm{kA/mm^2}$ and high temperatures (325°C, 350°C and 375°C). Under these conditions an activation energy of $E_{\mathrm{a}} = 0.59$ eV was found.

These results give indications of the electromigration behavior on large gate width finger structures. But further work will be necessary to determine the electromigration under conditions close to the application.

4.6 Conclusion: On-State

The on-state resistance is the most relevant device parameter in terms of static losses. Therefore an economically sensible chip layout features low on-state resistance related to the used chip area. A meaningful parameter to compare the extrinsic layouts is the area-specific on-state resistance $R_{\mathrm{ON}} \cdot A$. This chapter introduces an analysis to design area-efficient HEMT layouts.

Large gate width HEMT structures are affected by the resistance and dimensions of drain and source metallization. A theoretical derived on-state model is developed in this work and describes the impact of the metallization on the performance. Large gate width finger structures with rectangular metallization feature inhomogeneous voltage and current distributions. Furthermore, a critical gate width is defined in equation (4.10) as well as a critical metallization length in equation (4.11). The exceeding of these values leads to inefficient layouts. Many conventional layout structures are designed with an inconvenient metallization length. The area efficiency can be significantly improved by reducing the length of the ohmic contacts.

A similar analysis is made on finger structures with tapered drain and source metallization. Tapered structures feature homogeneous voltage and current distributions on drain, source and active area. Furthermore, in direct comparison a tapered structure achieves a better area-efficiency than a structure with a rectangular shaped metallization. However due to minimal dimension requirements of the process technology tapered structures can only be realized insufficiently.

The most common used extrinsic layout is the comb structure. This work introduces an analytical method to determine a layout with optimal aspect ratio of the chip with taking into account practical matters, as bond pad or dicing requirements.

Furthermore in this chapter two new extrinsic layouts are introduced and analyzed. A clover structure features low current crowding by lower HEMT finger lengths. The on-state resistance of an exemplary clover layout is around 10 % lower compared to a comb layout which was realized on the same chip area. Another fractal structure is suited for very large chip areas. The metallization structure of each self-similar order in the fractal design can be adapted to the required current density. Thus inhomogeneous current distributions due to long finger structures can be reduced. However fractal layouts are complex in design and require a technology with several metallization layers.

Two-dimensional finite element simulations are introduced in this work and suitable to analyze complex layout structures. Current density and potential distributions can be illustrated. Thus bottlenecks in layout can be found. Furthermore the on-state resistance can be approximated by the results of this simulation.

The high current operation of typical GaN-HEMTs is characterized by experimental investigations in section 4.5. A simple empirical on-state model as a function of the channel length is plotted with measurement results and it illustrates the impact of the self-heating. Furthermore the effect of self-heating is characterized for different pulse lengths on a large area GaN-HEMT. The measurements have been made for two different carrier substrates GaN-on-Si and GaN-on-SiC devices. Finally, the high current operation and large gate width HEMT designs are discussed in terms of electromigration.

On one hand power devices with large gate width feature low on-state resistances and high on-state currents, but on the other hand the larger the channel width the larger the parasitics, as capacitances and inductances, which are relevant in the switching state. In the following chapter the dynamic behavior of large area devices is characterized.

5. Characterization of the Switching-State

5.1 Introduction: Switching-State

As shown in the introduction in equation (1.2) the most relevant losses of a power transistor can be separated in two terms. The first term describes the conduction losses and the second term the switching losses. Furthermore in this equation it is shown that the switching losses are proportional to the switching frequency. Consequently at low switching frequencies the static losses are dominant. However it is desirable in most applications to choose a high switching frequency to reduce the values of energy storage elements, as inductors and capacitors. Low value inductors and capacitors lead to lower volume, weight and cost for these components, which are required properties in most applications. For this reason high switching frequencies are needed and the characterization of the switching state has a high relevance for the design of compact and highly-efficient power applications.

An ideal switch would change between the static states instantaneously, whereas a real switch is affected by parasitic inductances, capacitances or other non-idealities. These non-idealities imply a number of time constants, and these time constants delay or slow down the transition between the static states. A power device crosses operating points with high power in the output characteristic during the switching event. Therefore in efficient hard switching applications it is desirable to have short time constants for fast switching to keep the switching energy as low as possible. Moreover it is beneficial to know and to describe the remaining parasitics. In soft switching topologies linear parasitics can be compensated by an advanced system design. In this chapter the relevant dynamic parameters of GaN-HEMTs are characterized and discussed.

5.2 Characterization of Dynamic Parameter

5.2.1 Pulse Characterization

The switching characteristic of power devices is strongly dependent on its periphery. Therefore it was an aim in this work to characterize the dynamic parameters of GaN devices in an application-near environment. A measurement setup has been developed to characterize the dynamic behavior of GaN power devices. The schematic test circuit is shown in figure 40.

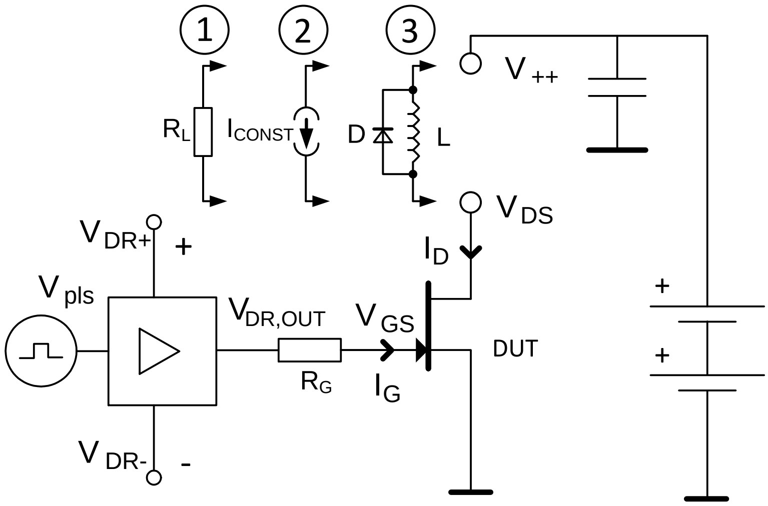

Figure 40: Pulse circuit for power devices to characterize dynamic parameters. There are three different load configurations: (1) real load, (2) constant current compliance as load for dynamic on-state resistance measurements, (3) inductive load for double pulse measurements with free-wheeling diode.

The construction is equal to a switching unit of a power electronic system. The circuit was realized on a printed circuit board (PCB). The device-under-test is driven by a commercial Power-MOSFET gate-driver circuit (Micrel-MIC4452). The gate voltages V_{GS}, the drain voltage V_{DS}, the driver output voltage $V_{DR,OUT}$, and the supply voltage V_{++} are measured by an oscilloscope. The pulse voltage V_{PLS}, the positive driver supply voltage V_{DR+}, and the trigger signal of the oscilloscope are controlled by a crystal clocked microcontroller on the PCB to get reproducible conditions. Thus time-relevant switching operations are executed by the microcontroller. Furthermore the microcontroller is connected via serial interface with a laboratory computer. The laboratory computer manages all time uncritical procedures of the experiment, as the initialization as well as the setup of the supply voltages, the switching unit, and the oscilloscope settings. Subsequently, after the measuring procedure the oscilloscope data are collected on the laboratory computer for signal processing.

According to the requirements it is possible to apply different loads in the setup. The load options are shown in figure 40. Depending on the experiment it is suitable to connect a resistive load, a constant current, or an inductive load. Corresponding examples will be shown below.

The switching event itself is a complex interaction between power device and the connected components at the transistor terminals. In addition in very fast switching applications the influence of parasitic components becomes relevant and the characterization of the behavior becomes even more complicated. A turn-on event will be enabled by the required quantity of charge which is fed into the channel. Conversely, a turn-off event will be enabled by the required quantity of charge which is removed from the channel. This procedure makes a power switch conductive or high resistive. Thus in power devices the switching speed is mainly determined by the quantity of the required switching charge and the circumstance how fast the charge is provided or removed. In addition the highest possible switching speed is derived by Johnson in [20], which is discussed in section 2.1.3. Very fast switching gradients have been shown by S. Mönch in [69], [70] and [71]. He developed advanced push-pull gate drive circuits and power circuits with HEMT devices. The power device of the monolithically integrated circuit has a layout which was developed with the design of this work. Slew rates up to 240 V/ns for turn-on as well as turn-off event have been achieved in a half bridge demonstrator.

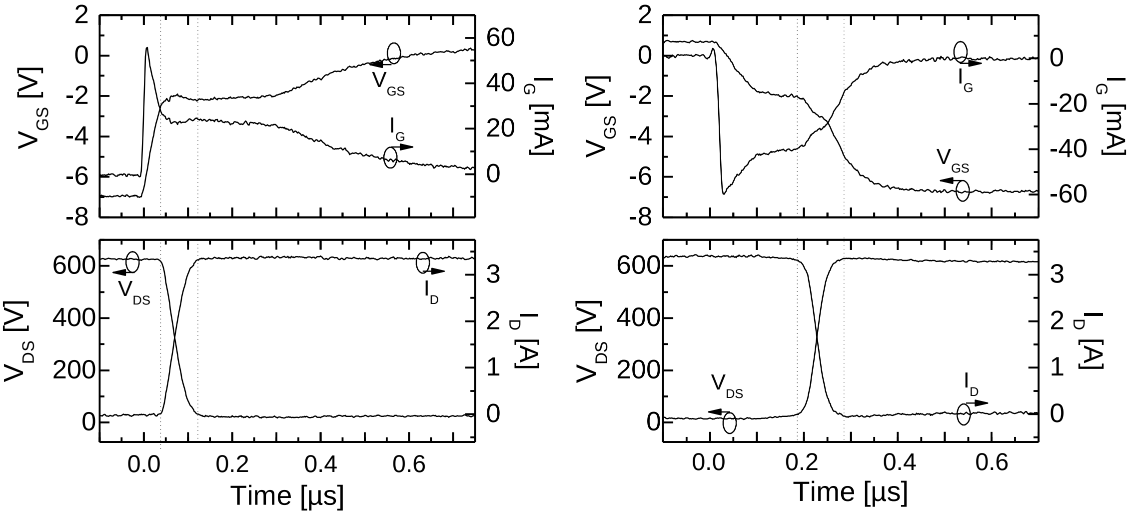

Figure 41: Transient terminal voltages and currents during the switching operation. (Left) Turn-on event of a GaN-HEMT. (Right) Turn-off event of a GaN-HEMT

In this work the turn-on and turn-off events have been measured to analyze a characteristic GaN-HEMT power devices with a gate-width of $W = 248$ mm, a gate-length of $l_G = 1$ µm, a gate-drain distance of $l_{GD} = 15$ µm and a total chip area of $A = 3\times3$ mm². In static measurements the device was characterized. It achieves an on-state resistance of $R_{ON} = 70$ mΩ and an off-state voltage of more than 600 V. The device is tested to determine the dynamic parameters in the setup, which is introduced above and shown in figure 40. This setup is configured by using a resistive load with a value of $R_L = 180$ Ω. Furthermore a gate resistor between gate and driver output is chosen with a value of $R_G = 120$ Ω. The relatively high value of the gate-resistor slows down the charging process. Thus switching events are dominated by the time constant of the gate-resistor R_G and the input capacitance of the transistor and not by inductive parasitics of the test setup and packaging technology. Figure

41 shows the measured transient signals at gate and drain in a GaN-HEMT power device. The voltages V_{DS}, V_{GS}, $V_{\mathrm{DR,OUT}}$, and V_{++} are detected by the four channels of the oscilloscope. The gate current is calculated by $I_{\mathrm{G}} = (V_{\mathrm{DR,OUT}}-V_{\mathrm{GS}})/R_{\mathrm{G}}$ and in the same manner the drain current with $I_{\mathrm{D}} = (V_{++}-V_{\mathrm{DS}})/R_{\mathrm{L}}$. The turn-on event is presented on the left graphs. At $t = 0$ the gate driver output voltage $V_{\mathrm{DR,OUT}}$ steps from an off-state gate voltage of $V_{\mathrm{DR,OUT,OFF}}$= -7 V into an on-state gate voltage of $V_{\mathrm{DR,OUT,ON}}$= 1 V. The input capacitance is charged by the gate current via the resistor R_{G} and the gate drain voltage is rising till the threshold voltage V_{TH} is reached. At this voltage the transistor starts to become conductive. The drain-source voltage falls and the drain current rises along the straight load characteristic of R_{L}. The new operating point is the crossing point between the straight load characteristic of R_{L} and the on-state resistance R_{ON} in the output characteristic. The gate-source voltage remains close to the threshold voltage till the transistor channel is fully charged. Finally, the gate source voltage can reach the value which is applied by the driver $V_{\mathrm{DR,OUT}}$. In a similar way the turn-off event starts with an immediate change of the driver output voltage $V_{\mathrm{DR,OUT}}$ from 1 V to -7 V. The charge is removed though the gate and the gate-source voltage fall till the threshold voltage is reached. Then the drain-source voltage rises and the drain current falls along the load characteristic till the transistor is off. The charge will be removed till the gate-source voltage V_{GS} reaches the negative driver voltage $V_{\mathrm{DR,OUT}}$ with a value of -7 V.

5.2.2 The Gate Charge

It is challenging to evaluate the switching performance of a power device separated from its periphery. The pulse shapes are strongly related to the gate-drive circuit, the load or parasitics of the assembly technology. A parameter which is mainly independent from periphery is the gate charge. The total gate charge is defined as the quantity of charge which is required to switch a power device from on-state to off-state and back. The total gate charge is the time integral of the gate current and can be expressed as

$$Q_G = \int_{t_1}^{t_2} I_G \,\mathrm{d}t. \tag{5.1}$$

The time t_1 represents the moment when the driver output changes its voltage $V_{\mathrm{DR,OUT}}$ and the gate input capacitance is charged. The time t_2 is defined by the moment when the gate-source voltage has reached the value of the driver output voltage $V_{\mathrm{DR,OUT}}$ after the charging process. Thus the total gate-charge also depends on the range of the gate-driver voltage. An important part of the gate-charge represents the Miller plateau [71]. This is the part close to the threshold voltage where the gradient of the gate-source voltage over charge is low. This plateau charge is often denoted with Q_{GD}, and this is charge in the channel area, which changes the state from on-state to off-state and back. The gate-charge is usually plotted as characteristic curve in relation to the gate-source voltage. The gate-source voltage is shown in the y-axis as function of the gate-charge, which is plotted in the x-axis. Such a typical gate-charge curve is shown in figure 42 on the right side.

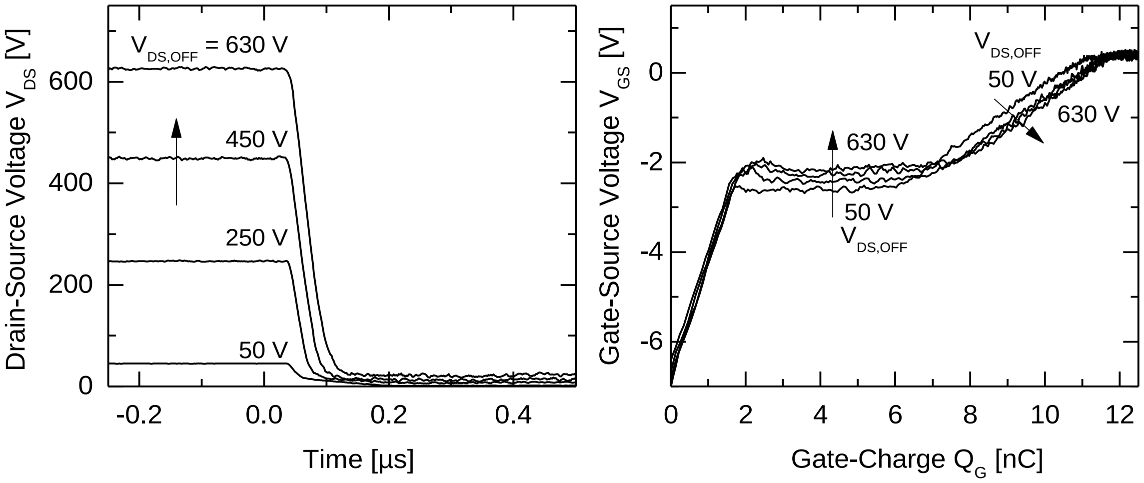

Figure 42: Gate-charge characterization as a function of the drain-source off-state voltage. (Left) Falling edges of the drain-source voltage. (Right) Gate-charge curves show the gate-source voltage as a function of the gate-charge.

The measurements have been performed on the same device and in the same setup as introduced above in section 5.2.1. Furthermore the same setup configuration with $R_L = 180\ \Omega$ and $R_G = 120\ \Omega$ has been used as above.

The gate charge measurements have been made for different off-state drain voltages as shown in figure 42 on the left side. For all of these turn-on events the gate charge has been calculated and plotted in the figure 42 on the right side. The gate charge is nearly independent of the off-state drain voltage in the range between $V_{DS,OFF} = 50$ V and $V_{DS,OFF} = 630$ V. The total gate charge of this device was measured to be $Q_G = 12$ nC within a gate-source voltage swing between -7 V and 1 V. The tested device has a total gate width of $W = 248$ mm. Thus the intrinsic structure of the tested device has a gate charge per unit length of $Q'_G = 50$ pC/mm. GaN devices achieve a relative low gate-charge compared to conventional power devices based on Si. The reason for this can be found in equation (2.9). The excellent isolation properties of GaN allow devices with short depletion lengths. This issue result in short drift length devices with low specific on-state resistances and low specific channel charges. Direct comparisons of fabricated devices will be made below in the benchmark section 7.4. An undesired effect after turn-on is characterized in the next section. Trapped charges in the HEMT structure can affect the drain-source resistance in the on-state.

5.2.3 Dynamic On-State Resistance

The GaN technologies are still in an early stage of development. One of the most frequently investigated topics of international research groups is the current collapse phenomena after electric field stress, e.g. in [33], [41], [42]. This effect is also called the dynamic on-state resistance in contrast to the static on-state resistance, which is measured in setups at low drain-source voltages. An increased dynamic on-state resistance can occur when high electric fields in the off-state charge defects in the transistor structure. These charged defects act like an additional negatively charged gate and thus they constrain the electron flow through the channel in the on-state. The on-state resistance can be increased by orders of magnitudes compared to the static on-state resistance. These undesired charges which are the reasons for the increased dynamic on-state resistance are called traps. Trapping mechanisms are many and varied. It is not the focus of this work to investigate these effects. A detailed analysis of physical and technological reasons of these effects can be found in the work of M. Wespel, which was performed during the same time period at IAF Fraunhofer. Contributions regarding these topics were published in [27], [41], [42]. Nevertheless, in this work measurement equipment has been developed to characterize the dynamic on-state resistance on very low-resistive high power devices. This setup and some measurement results will be introduced in this section.

The characterization of the dynamic on-state resistance requires high demands on the measurement equipment. The setup has to measure fast transient responds with high dynamic resolutions. Commercial pulse measurement equipment is very costly and it often cannot fulfil the requirements for an accurate measurement on high power devices. For this reason the development of equipment for dynamic resistance characterization becomes more and more a research topic itself. Other advanced equipment has been recently introduced in literature and will be referenced and discussed in more detail below.

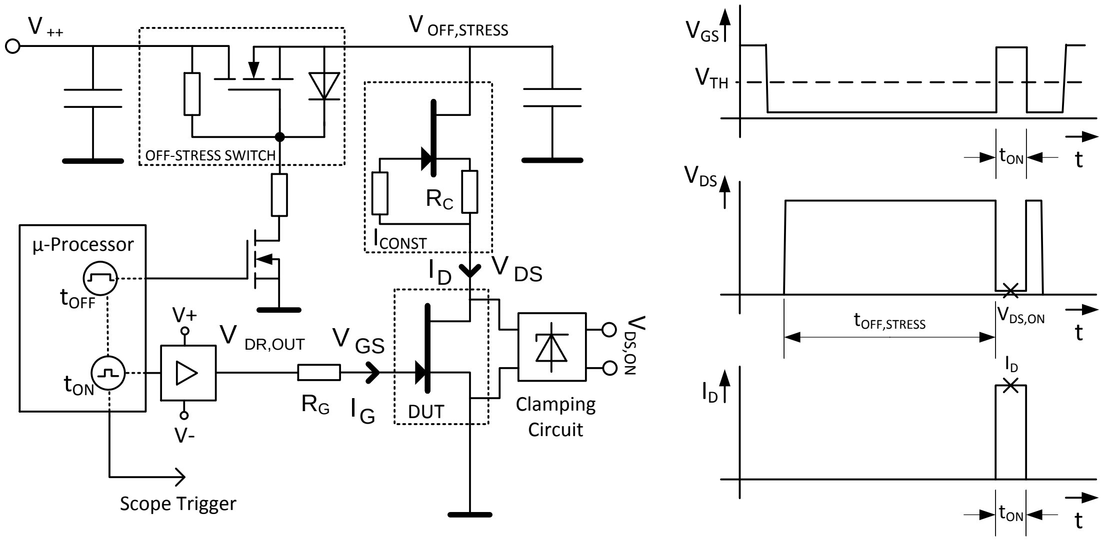

Figure 43: Dynamic on-state characterization. (Left) A measurement circuit to execute the pulse procedure for the dynamic on-state measurement. (Right) Time sequence of signals to measure the dynamic on-state resistance.

The procedure of dynamic on-state measurement is typically executed as shown in the right plot of figure 43. The device-under-test (DUT) is switched into the off-state with $V_{GS} < V_{TH}$. In the next step a defined off-state voltage is applied between drain and source $V_{DS} = V_{OFF,STRESS}$. After a defined off-state-stress-voltage-time $t_{OFF,STRESS}$ the device is turned on ($V_{GS} > V_{TH}$). A few microseconds after turn-on the on-state voltage $V_{DS} = V_{DS,ON}$ and the drain current I_D is measured to determine the dynamic on-state resistance. This measurement has to be done for rising off-stress voltages, whereby the resistance in the on-state should be always characterized under same on-state current conditions. Such a measurement can be realized with a setup as shown in figure 40. The load should act like a current source in the on-state, as shown in load option 2 in figure 40, whereas in the off-state the load should be low-conductive.

A solution which was developed in this work is shown on the left side in figure 43. It contains a high side switch to control the off-state stress voltage time $t_{\mathrm{OFF,STRESS}}$. A constant current circuit represents the load and provides constant on-state conditions as required. A driver circuit is connected to the gate for turn-on and turn-off the on-state event. The time signals are recorded by an oscilloscope. The procedures for all switches and the trigger for the oscilloscope are controlled by a microprocessor (TI-MSP430). The pulse energy for the on-state event is temporarily stored in a capacitor. Thus the energy for the on-state can be provided immediately with low parasitics or delays.

The high-side switch is necessary to ensure an accurate timing of the off-state stress voltage time $t_{\mathrm{OFF,STRESS}}$. Stress times can be adjusted in a range starting from few milliseconds up to minutes. Moreover off-state stress voltages $V_{\mathrm{OFF,STRESS}}$ up to 600 V can be blocked or switched on by a high side switch. The basic concept of this high side switch is based on the circuit of an adjustable voltage regulator, as shown e.g. in [73]. The diode between source and gate is necessary to protect the gate in case that the capacitor at source is charged and the gate of the high-side switch is pulled down to ground.

The current source circuit as load is realized by using a normally-on transistor as current source as shown in figure 43 and the principle is explained e.g. in [74]. A resistor R_C is connected to the source and the gate is connected via a low-ohmic resistor to the other side of the resistor R_C. Thus the constant current can be easily determined by the equation $I_D = I_{\mathrm{CONST}} = |V_{\mathrm{TH}}|/R_C$. The resistor at the gate reduces the switching speed of the current source. Very fast switching may lead to instabilities during the measurement due to parasitics. The breakdown voltage of the transistor should be higher than the off-state stress voltages $V_{\mathrm{OFF,STRESS}}$. The current source has to resist nearly the entire off-state stress voltage $V_{\mathrm{OFF,STRESS}}$ during the on-state of the DUT. At the same time the current source provides a constant drain current $I_D = I_{\mathrm{CONST}}$. Consequently the current source as load has to dissipate a very high power under these conditions. The drain current can be measured by using a fast current clamp or indirect on a shunt-resistor with a differential high voltage probe.

The transient signals are recorded by an oscilloscope. However the dynamic resolution of conventional oscilloscopes is 8-bit with 256 values, and also the dynamic resolution of probes is adapted to this 8-bit. Thus the resolution of the oscilloscope is not accurate enough to detect the off-state voltage and the on-state voltage of a pulse at same channel. If one assumes a maximal off-state voltage of $V_{\mathrm{OFF,STRESS}} = 600$ V the smallest resolution step is about

$V_{\mathrm{STEP,8\text{-}BIT}} \approx 2.3$ V. Therefore it is necessary to record the on-state separately from the off-state with two channels of the oscilloscope. One channel records the total waveform and the second channel focus to the on-state voltage $V_{\mathrm{DS,ON}}$. Thus it is possible to characterize the on-state with high resolution even though the oscilloscope has only 8-bit. However the input of the oscilloscope has to be protected against the high voltages of the off-state. This issue is discussed in literature and different clamping circuit approaches are published in [75], [76], [77], [78] and [79]. In the early state of this work the clamping circuit has been used, which was later published in [75]. Since the year 2013 a commercial product is available, which is described in [80].

The considered power devices feature on-state resistances in the range 100 mΩ and below. Therefore a four-point measurement is crucial to eliminate parasitic influences of the assembly. The four-point measurement can be achieved by tapping the on-state voltage $V_{\mathrm{DS,ON}}$ directly at the drain- and source- pin of the tested device. The clamping circuit should be independent of the setup-ground-potential, as shown in figure 43, and the output of the clamping circuit should be recorded by a differential voltage probe.

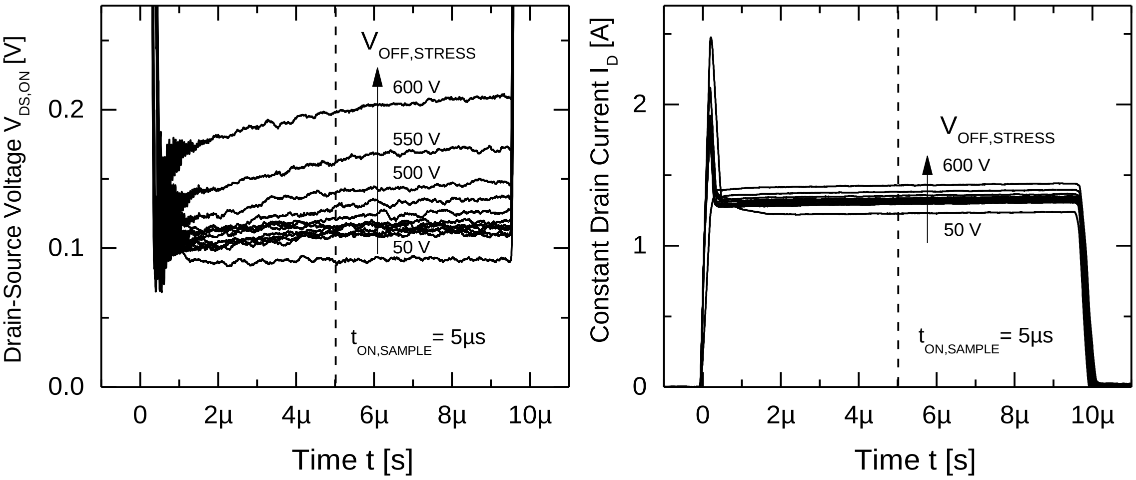

Figure 44: Dynamic on-state pulse measurements on a large power device GaN-HEMT, with gate width of $W = 248$ mm. (Left) Transient on-state voltage curves parameterized as a function of the off-state stress voltage. (Right) Transient on-state current curves parameterized as a function of the off-state stress voltage.

The results of dynamic on-state pulse measurement are shown in figure 44. The transient on-state voltages $V_{\mathrm{DS,ON}}$ and currents I_{D} are shown as a family of curves as a function of the off-state stress voltage $V_{\mathrm{DS,OFF,STRESS}}$. The specification of the DUT has been shown above in section 5.2.1. The GaN-HEMT power device has a gate width of $W = 248$ mm, a gate-length of $l_{\mathrm{G}} = 1$ µm, a gate-drain distance of $l_{\mathrm{GD}} = 15$ µm, total chip area of $A = 3\times3$ mm² and it achieves a static on-state resistance of $R_{\mathrm{ON}} = 70$ mΩ. This device has been characterized in a setup, which is introduced in figure 43. The off-state stress voltage $V_{\mathrm{DS,OFF,STRESS}}$ was increased by around 50 V in each pass. Furthermore each off-state stress voltage $V_{\mathrm{DS,OFF,STRESS}}$ was applied between drain and source for an off-state stress time of $t_{\mathrm{OFF,STRESS}} = 10$ s. After this time the device is switched into the on-state for about $t_{ON} = 10$ µs. The drain current is kept constant by using a current-source with a current of about $I_D = 1.3$ A. This is shown in figure 44 on the right side. The current-source generates an overshoot during the turn-on event. This overshoot is caused during the charging event of the power transistor in the current source, because this device is switched to an operating point with high drain-source voltage. The switching speed of this current source can be increased by reducing the value of the resistor on the gate. However this can also lead to instabilities. On the left side of figure 44 the increase of the dynamic on-state resistance can be observed by the increase of the on-state voltage $V_{DS,ON}$. In this work the dynamic on-state resistance is calculated using the on-state voltage $V_{DS,ON}$ and the on-state current I_D after a time of $t_{ON,SAMPLE} = 5$ µs. These values with $R_{ON,DYN} = V_{DS,ON}/I_D$ are collected and plotted as a function of the off-state stress voltage $V_{DS,OFF,STRESS}$ and shown in figure 45. The interval value $R_{ON,DYN,50V}$= 75 mΩ is closed to the static on-state resistance with a value of $R_{ON} = 70$ mΩ. In the range between 100 V and 400 V the dynamic on-state resistance is increase by about 10%. At 600 V the dynamic on-state resistance is twice the inertial value.

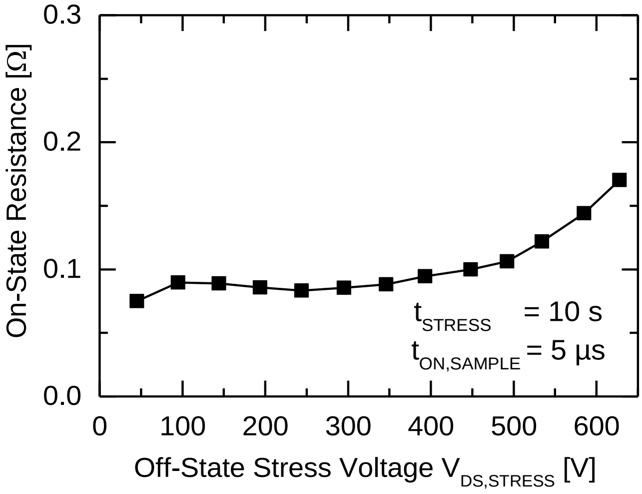

Figure 45: Dynamic on-state resistance $R_{ON,DYN}$ as function of the off-state stress voltage $V_{OFF,STRESS}$ between drain and source of the GaN power device-under-test with $W = 248$ mm

As discussed above the investigation of the dynamic on-state resistance is still a main subject of international research groups. During the last years the behavior was continuously improved by the progresses in epitaxy and process technology. Today in the year 2016, only very few publications show comparable or better results on large gate width devices and at off-state voltages above 600 V, one example is shown in [81].

The transient turn-on and turn-off event, the gate-charge curve, as well as the effect of the dynamic on-state resistance are measured by using a pulse setup, which is presented in this section. In the following sections of this chapter the device is analyzed and modeled in terms of its small signal behavior. Firstly, the non-linear capacitances are determined by measurements as a function of the drain-source voltage. Secondly, the inductances of large gate width HEMT fingers are predicted in simulations. These parameters can be applied in an extended small signal model which is shown at the end of this chapter.

5.2.4 Capacitive Behavior

In the switching time the device capacitances are charged or discharged. During this time the operating point moves between two static states and during this time switching losses are generated in the transistor. The understanding of switching losses requires a previous characterization of the device capacitances. This section investigates the behavior of GaN-HEMT device capacitances and it describes its influence on the switching-state.

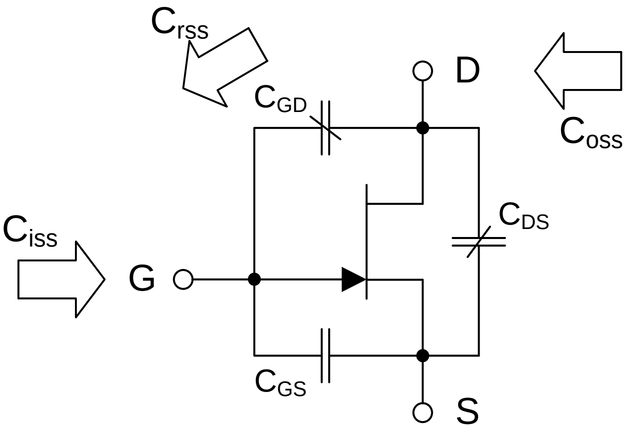

Figure 46: A HEMT symbol with the three terminal capacitances: gate-drain capacitance C_{GD}, drain-source capacitance C_{DS}, and gate-source capacitance C_{GS}. Furthermore the definition of the C_{iss} input-, C_{oss} output- and C_{rss} reverse capacitance is illustrated.

The capacitive behavior of a power transistor is described by three capacitances as shown in figure 46. The gate-drain capacitance C_{GD}, the drain-source capacitance C_{DS}, and the gate-source capacitance C_{GS} are known as the three terminal capacitances of a power field effect transistor. These capacitances are strongly dependent on the terminal voltages. Especially the gate-drain capacitance C_{GD} and the drain-source capacitance C_{DS} have non-linear behavior and dependent on the drain-source voltage. These capacitances are strongly dependent on the drain-source voltage. In particular the gate-drain capacitance C_{GD} has high influence on the switching speed. Early scientific work has been done by J. M. Miller on this topic in 1920. He described the influence of such a feedback capacitance in vacuum tube amplifiers [72]. Therefore the gate-drain capacitance C_{GD} is also known as the Miller-capacitance. The three terminal capacitances can be directly characterized by using the measurement setups which are proposed in [82].

There is a further widely used description of the capacitive behavior: the input capacitance C_{iss}, with shorted drain-source terminal, the output capacitance C_{oss}, with shorted gate-source terminal, and the reverse capacitance C_{rss}, which is equal to the gate-drain capacitance C_{GD}.

This description is often found in application-related descriptions or data-sheets. Because C_{iss} is the input capacitance a driver circuit has to charge and discharge, and C_{oss} is the output capacitance which may have to be matched to load or to a secondary stage. Both descriptions can be easily converted into each other, by using;

$$\begin{aligned} C_{\text{iss}} &= C_{\text{GS}} + C_{\text{GD}}, \\ C_{\text{oss}} &= C_{\text{DS}} + C_{\text{GD}}, \text{ and} \\ C_{\text{rss}} &= C_{\text{GD}}. \end{aligned} \qquad \textbf{(5.2)}$$

The characterization of the drain-source voltage dependent capacitances C_{iss}, C_{oss} and C_{rss}, can be found by using the measurement setups, which are shown in figure 47. The circuits are shown in [83]. The setups consist of a capacitance meter (HP4275A), different AC- or DC-blocking elements, a fixed voltage source to apply the gate-source voltage, an adjustable high voltage source to apply the drain-source voltage and a power transistor under test.

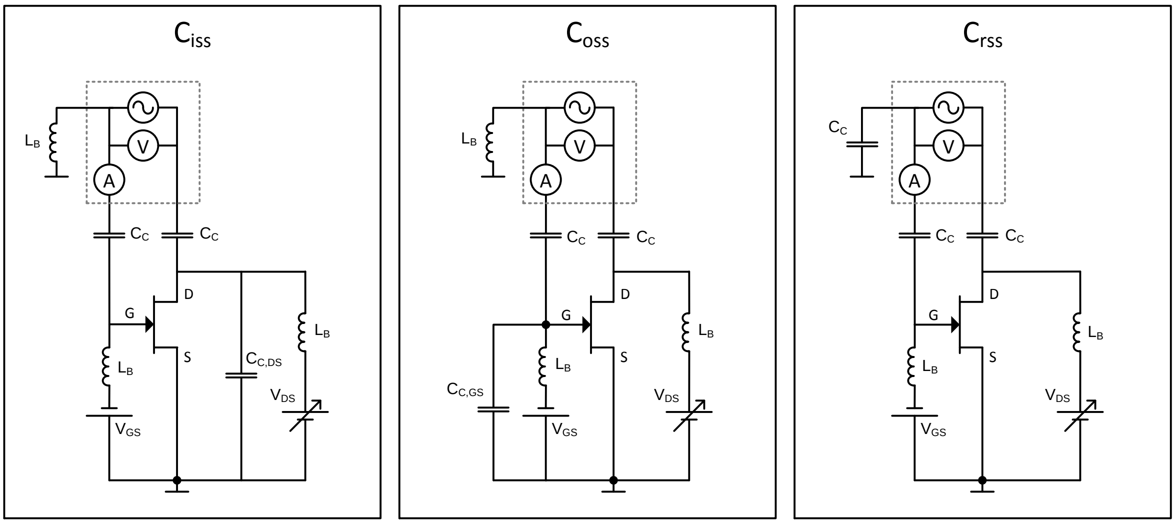

Figure 47: Measurement setups for the characterization of the non-linear parasitic capacitances. Three parameters can be characterized: (Left) C_{iss} input capacitance, (Middle) the C_{oss} output capacitance and (Right) the C_{rss} reverse capacitance.

The measurement circuits in figure 47 can be understood by separating the connections in an AC-equivalent circuit and a DC-equivalent circuit. The capacitance meter is illustrated by an AC-source, a voltage meter and an ampere meter. With the capacitance meter an AC-voltage is applied and the complex current is measured by the measurement unit. Thus it can determine the capacitance. Both measurement inputs of the capacitance meter are DC-blocked, but AC-coupled by the coupling capacities C_{C} and connected between gate and drain, whereas the voltage supplies for gate-source- and drain-source voltage are AC-blocked by the inductors L_{B}. The input capacitance C_{iss} can be measured if the drain-source is AC-short-circuited by $C_{\text{C,DS}}$. Thus the capacitances C_{GD} and C_{GS} are connected in parallel in an AC-point of view. The output capacitance C_{oss} can be measured if the gate-source is AC-short-circuited by $C_{\text{C,GS}}$. Thus the capacitances C_{GD} and C_{DS} are connected in parallel in an AC point of view. For these two setups for C_{iss} and C_{oss} the capacitance meter is AC-blocked to ground by an inductor L_B. An AC-coupling to ground would either short circuit the voltage meter or the ampere meter. In case of measuring the reverse capacitance C_{rss} this point is AC-coupled to ground by a coupling capacitance C_C. Thus only the current through the gate-drain capacitance C_{GD} is measured by the current meter.

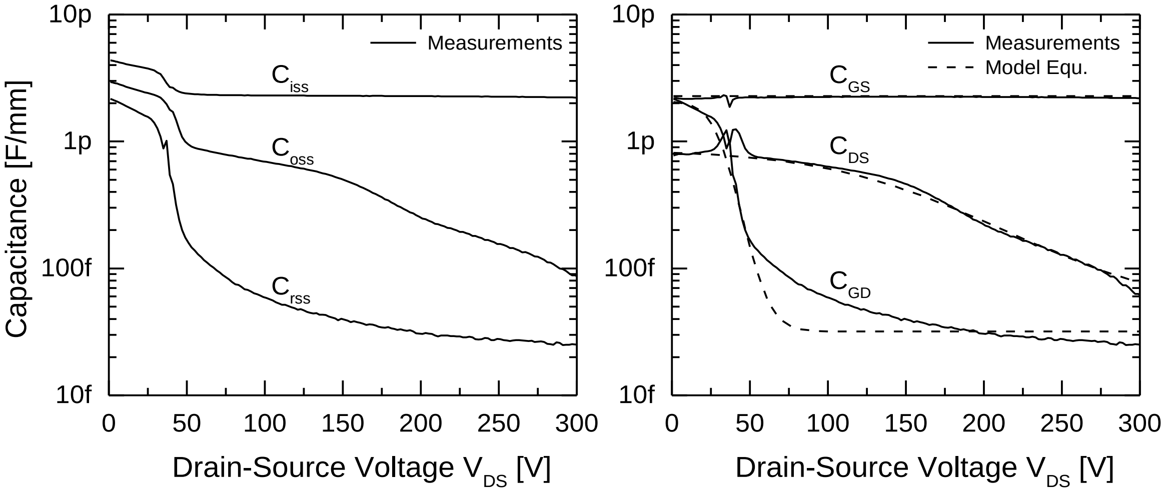

Figure 48: Characterization of the drain-source voltage dependent device capacitances of a large are GaN-HEMT. (Left) The capacitances: C_{iss}, C_{oss}, and C_{rss}. (Right) The three terminal capacitances: C_{GD}, C_{GS} and C_{DS}. The GaN-HEMT-under-test has a total gate width of $W = 220$ mm and a double field plate structure. The test frequency was 1 MHz.

The measurement results of a large area device are shown in figure 48. The DUT is a device with a chips size of $A = 4 \times 3$ mm², a gate width of $W = 220$ mm, a gate length of $l_G = 2$ µm, a gate-drain distance of $l_{GD} = 20$ µm, it has a double field plate structure and the chip layout is realized in a conventional comb-structure. The capacitances to be measured are very small. Therefore it is advantageous to characterize devices with high gate width to achieve a high capacitance and a high resolution. The measurements have been performed using the measurement setup explained above and shown in figure 47. The input capacitance C_{iss}, the output capacitance C_{oss} and the reverse capacitance C_{rss} are plotted on the left. By using these values and the equations (5.2) the terminal capacitances C_{GD}, C_{GS} and C_{DS} are calculated and they are plotted on the right. It can be observed that C_{GS} is nearly independent of the drain-source voltage. Whereas the gate-drain capacitance C_{GD} and drain-source capacitance C_{DS} are strongly dependent on the drain-source voltage. Both capacitances decrease their values by more than one decade for higher drain-source voltages. The physical background will be explained below. The strong voltage depended behavior is important for the analysis of the switching behavior.

In this work a simple empirical model is used to describe the non-linearity. The model function is based on a hyperbolic tangent function. These model functions are used in figure 48 on the right side as fit-functions for C_{GD}, C_{GS} and C_{DS}. The three model functions are given by:

$$\begin{aligned} C_{\mathrm{GS}} &= \mathrm{const}, \\ C_{\mathrm{GD}}(V_{\mathrm{DS}}) &= C_{\mathrm{GD,high}}\left(1-\tanh\left(m_{\mathrm{GD}}\left(V_{\mathrm{DS}}-V_{\mathrm{TH,GD}}\right)\right)\right)/2 + C_{\mathrm{GD,low}}, \text{ and} \\ C_{\mathrm{DS}}(V_{\mathrm{DS}}) &= C_{\mathrm{DS,high}}\left(1-\tanh\left(m_{\mathrm{DS}}\left(V_{\mathrm{DS}}-V_{\mathrm{TH,DS}}\right)\right)\right)/2 + C_{\mathrm{DS,low}}. \end{aligned} \tag{5.3}$$

The non-linear model-function of $C_{\mathrm{GD}}(V_{\mathrm{DS}})$ has a high capacitance value $C_{\mathrm{GD,high}}$ for low drain-source voltage and a low capacitance value $C_{\mathrm{GD,low}}$ for high drain-source voltages. There is a threshold voltage $V_{\mathrm{TH,GD}}$ at the point of inflection and a constant value m_{GD}, which determines the gradient at the inflection point. There are equivalent parameters for the non-linear model function of $C_{\mathrm{DS}}(V_{\mathrm{DS}})$. As mentioned above C_{GS} is not a function of the drain-source voltage in this model.

The shape of the capacitances in figure 48 can thus be understood by considering the cross-section of the corresponding HEMT structure. The device-under-test in figure 48 has a double field plate structure as shown in figure 8. These field plates behave like parallel-plate capacitors in the experiment in figure 10. The reverse capacitance $C_{\mathrm{rss}} = C_{\mathrm{GD}}$ has a step at around $V_{\mathrm{DS}} = 30$ V. This step corresponds to the threshold voltage of the gate connected field plate, also known as Γ-gate overhang. This field plate is realized in the field plate metallization (METFP), and has a threshold voltage in this range as shown in table 2 in section 2.3.2. However the potential of this gate is below the device threshold voltage at $V_{\mathrm{GS}} = -5$ V. Thus the threshold voltage of the step is shifted by $V_{\mathrm{TH,METFP}} = V_{\mathrm{DS}}-V_{\mathrm{GS}}$. The step of the Schottky gate contact cannot be observed in this measurement, because this measurement is made below the Schottky gate threshold voltage. In this characterization the charge below the Schottky contact is already depleted. The next terminal capacitance, the drain-source capacitance C_{DS} has a step a higher voltage. This step is caused by the source-connected field plate. This field plate is realized on the first metallization layer (MET1). Therefore it has a higher threshold voltage at around 90 V, as shown in table 2 in section 2.3.2. The output capacitance C_{oss} has two steps, because C_{oss} is a parallel connection of gate-drain capacitance C_{GD} and drain-source capacitance C_{DS}. The deviations between C_{DS} and the model result from measurement errors caused at the strongly falling terminal capacitances, whereas the deviations between C_{GD} and the model is structure-related and not reproduced by the simple model function.

The behavior of the terminal capacitances can vary for different intrinsic HEMT structures and different technologies. However, by using this method the behavior can be characterized. Furthermore the results, which are shown in figure 48, can be used as an example of a typical characteristic with typical values for conventional HEMT structures.

5.2.5 Inductive Behavior

In chapter 4 different large-area HEMT-structures are discussed in terms of on-state performance. Large-area comb-structures are designed with a high finger gate width and their finger metallization has to carry high currents. Such finger structures contain parasitic inductances. Each conductor has a self-inductance: drain-inductance L_D, gate-inductance L_G and source-inductance L_S, and also each conductor influences its neighbors. This effect cannot be neglected, because these conductors are arranged in parallel and are close together. Thus there are the mutual-inductances between drain-source $L_{DS} = L_{SD}$, gate-drain $L_{GD} = L_{DG}$ and gate-source $L_{GS} = L_{SG}$. The direction of each pair is interchangeable, due to the magnetically reciprocity theorem.

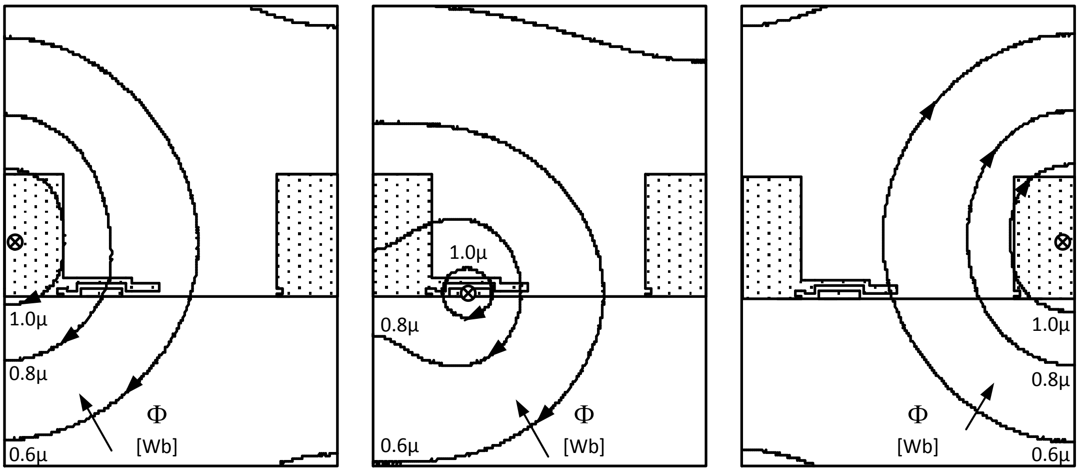

Figure 49: Finite elements simulation of the magnetic flux lines for the determination of the inductances of a GaN-HEMT structure. This example structure has a gate-drain distance of $l_{GD} = 15$ µm. (Left) A constant current of $I = 1$ A is flowing through the source metallization. (Middle) A constant current of $I = 1$ A is flowing through the gate metallization. (Right) A constant current is of $I = 1$ A flowing through the drain metallization.

An illustration of the magnetic flux lines for each conductor is shown in figure 49. It is shown a cross-section of a GaN-HEMT structure with double field plates very similar to figure 8. The magnetic flux lines are found by simulation and shown as contour plot. The device inductance can be determined by using these simulation results. In contrast to the non-linear behavior of the device capacitances, the finger inductances can be treated to be linear. They are not influenced by the charge in the channel. Therefore it is possible to simulate the inductances by a finite elements magnetic flux simulator [51]. For the simulation to find the device inductances the relative permeability of all materials is assumed to be $\mu_r = 1$. A constant current of $I = 1$ A is supplied into the cross-section of each conductor strip: source, gate and drain. This leads to the formation of flux lines around the conductor. The self-inductance of a conductor is found by the calculation of the magnetic flux divided by the current $L = \Phi/I$. Whereas, the magnetic flux is the cross-section surface integral of the magnetic flux density B, given by $\Phi = \int_A \vec{B}(\vec{r}) \cdot \mathrm{d}\vec{A}$. For example the self-inductance of the drain is calculated by using the magnetic flux through the drain cross-section-area divided by the supplied current. Thus the drain inductance is given by $L_D = \Phi_D/I_D = 9$ Wb/1A = 9 µH. The unit of the magnetic flux is Weber [Wb] this corresponds to Henry times Ampere [H·A].

In the simulation calculated with a depth of the structure $W = 1$ m. Consequently the inductance per unit length is $L'_D = 9$ nH/mm for this example.

The calculation of the mutual inductances is very similar. In this case a neighbor conductor generates a magnetic flux, and the mutual inductance is calculated by the magnetic flux in a conductor divided by the current of a neighbor conductor. For example the mutual inductance of the source caused by a drain current is calculated by $L_{SD} = \Phi_S/I_D = 0.3$ µWb/1 A = 0.3 µH. The relation between the self-inductances and the mutual-inductances is expressed by the coupling factor K. It is calculated by using the self-inductance of both concerned conductors e.g. L_1 an L_2 and its mutual inductance $L_{12} = L_{21}$. The factor is calculated by: $K_{12} = K_{21} = L_{12}/\sqrt{L_1 \cdot L_2}$.

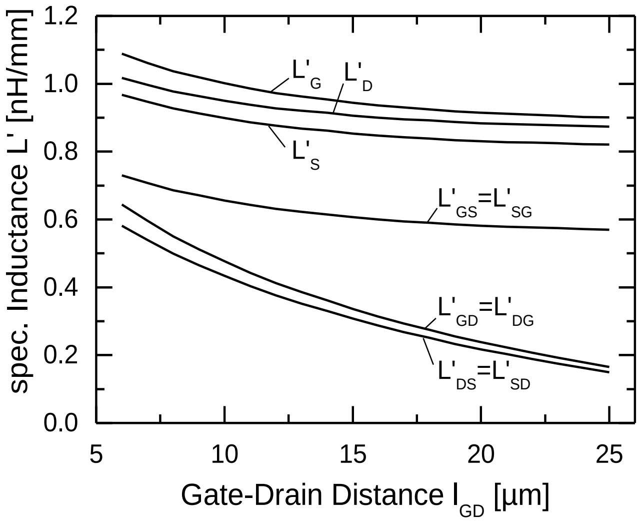

Figure 50: Inductance per unit length of drain-, gate- and source- metallization and its mutual inductances for a GaN-HEMT structure as a function of the gate-drain distance. The values are determined by finite elements simulation.

The simulator has been automatized to get the device inductances for different cross-sections, starting at a gate-drain distance of $l_{GD} = 6$ µm up to $l_{GD} = 25$ µm. The mutual inductances between a gate and source are relatively high, because these two conductors are very close together. The finger inductances are important input parameters for a chip designer to investigate the frequency behavior of large gate width finger structures. This simulation considers a mirrored multi-finger field characteristic with a synchronized operation of all fingers. However this is an idealized approach. In real structures it can happen, that adjacent HEMT finger structures operate asynchronously, which may cause hardly comprehensible dynamic conditions. Designers can use this investigation as a guideline to characterize the inductive behavior of HEMT structures by simulation. The results in figure 50 can be used as typical values for conventional HEMT structures.

The capacitances found in section 5.2.4 and inductances of this section can be used in the small signal model which is introduced in the following sections.

5.3 Development of a Dynamic Model

5.3.1 Small Signal Model

Small signal models are used to analyze the dynamic behavior around a certain DC operating point. Nonlinear behaviors of the transistor are linearized at the operating point. For example the capacities of the GaN-HEMTs have high voltage dependence. This nonlinearity is not recognized in the small signal model. The capacitance is assumed to be constant with the corresponding value at its operating point. A simple and often used small signal model for GaN-HEMTs with low gate width can be found in the path breaking work in [84]. This model is often used for the modelling of the small signal characteristic of an intrinsic HEMT structure and it will be used below as the intrinsic cell for an extended small signal model.

Passives of assembly technology, packaging and circuit interconnection are usually considered as passive networks. Around the intrinsic cells there are passive elements, such as the passive parasitics of the metallization. These passives can be modelled as an extrinsic shell. Additional passives for example caused by packaging parasitics can be modelled as a further extrinsic shell around the inner extrinsic shell, and so on. These models are often used for high frequency modelling. A pioneer work can be found in the work of Dambrine in [85]. An overview on this topic and further references are given in [86].

5.3.2 Large Gate Width Model

As discussed above GaN-HEMT structures for high power application are designed with large gate width finger structures. Dynamic effects like inductive and capacitive coupling, self-resonances, series inductances of drain, gate and source metal strips should be considered. The theory and the treatment of similar issues can be found in previous works for multi-conductor transmission lines e.g. in [87] or [88] for microwave transistors. Especially the theory of distributed traveling wave transistors [89] shows many analogies. Although power GaN-HEMTs work at much lower frequencies the much higher gate widths can cause similar effects as in high frequency transistors. For example the influence of high gate width and gate metal resistance can reduce high frequency operation as shown in [90]. The same effect is discussed and attach to the shell model shown above and can be found in [85]. The model equations are complex and become extensive by considering the parasitics of all metallization strips of drain, gate and source. Analytic considerations of these distributed effects on transistor finger structures can be found in the works of Heinrich e.g. in [91], [92], and [93]. However these publications show special cases of a finger structure, usually with an idealized source metallization. This reduces the complexity from three- to a two- wire system. This is valid for a number of microwave HEMT structures. Because these structures have source vias to the wafer backside to ground or there is a large-area, low-inductive metallization on source side. This is not valid for GaN power devices finger structures. Typically the source metallization length is equal to the drain metallization length. Both are realized as thin metal strips. The parasitics of the source metallization cannot be neglected. But the general analytic solution of this three-wire system is very extensive. A solution for transistor finger structures is found in [94] but due to different interface conditions the solution cannot be applied to the interface configuration which is discussed here in this work. D' Agostino in [95] has shown a way to solve this problem and to get a more general but analytic solution.

In this section in analogy to the calculations in section 4.2 the differential-equation-system of such a three-wire system model is derived and presented. In contrast to the calculations for the static on-state model in the dynamic consideration the gate metal strip cannot be ignored anymore. All three conductors are recognized and described with their matrix of 3×3 parameters Z' and Y'. The system is illustrated in figure 51.

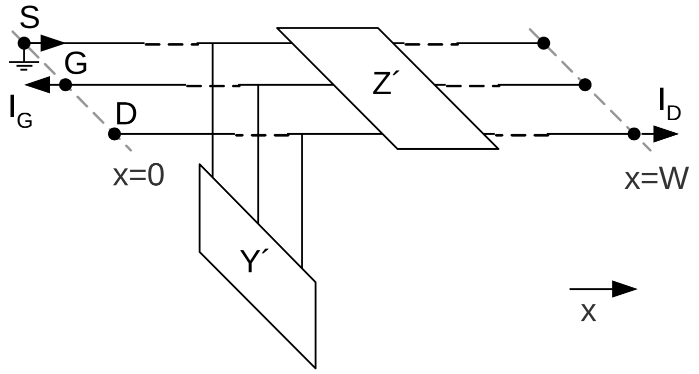

Figure 51: Model of a three-wire GaN-HEMT structure in the general case.

The currents and voltages on the structure can be written as a differential equation system in the same way like in equation (4.1) and equation (4.2), according to $\partial V/\partial x = -Z'\cdot I$, and $\partial I/\partial x = -Y'\cdot V$. The equation is solvable in second derivative of equation (4.2) to get with equation (4.1) the equation (4.4) $\partial^2 I/\partial x^2 = Y'Z'\cdot I$. The matrices for the voltages V, the currents I, the matrix of the impedances per unit length Z', and the matrix of the admittances per unit length Y' are written as:

$$I = \begin{bmatrix} I_S(x) \\ I_G(x) \\ I_D(x) \end{bmatrix}, V = \begin{bmatrix} V_S(x) \\ V_G(x) \\ V_D(x) \end{bmatrix}, Z' = \begin{bmatrix} Z'_{\mathrm{SS}} & Z'_{\mathrm{SG}} & Z'_{\mathrm{SD}} \\ Z'_{\mathrm{GS}} & Z'_{\mathrm{GG}} & Z'_{\mathrm{GD}} \\ Z'_{\mathrm{DS}} & Z'_{\mathrm{DG}} & Z'_{\mathrm{DD}} \end{bmatrix}, \text{ and}$$

$$Y' = \begin{bmatrix} Y'_{\mathrm{SS}} & Y'_{\mathrm{SG}} & Y'_{\mathrm{SD}} \\ Y'_{\mathrm{GS}} & Y'_{\mathrm{GG}} & Y'_{\mathrm{GD}} \\ Y'_{\mathrm{DS}} & Y'_{\mathrm{DG}} & Y'_{\mathrm{DD}} \end{bmatrix}. \tag{5.4}$$

In the typical comb-design the source- and gate- interface is connected at location $x = 0$ to a bus metal-strip and the drain-interface at location $x = W$ is connected to the drain bus metal. In this case the boundary conditions for the currents can by defined as: $I_S(0) = I_D + I_G$, $I_G(0) = -I_G$, $I_D(0) = 0$, $I_S(W) = 0$, $I_G(W) = 0$, $I_D(W) = I_D$. In addition three voltage boundaries are necessary to get a solvable system. Usually the potential at the source interface is defined as ground potential. Consequently the voltage at source can be written as $V_S(0) = 0$. The other voltage boundaries can be found by using two current equations extracted from equation (4.2), e.g. the equations for $\partial I_S(x)/\partial x$, and $\partial I_G(x)/\partial x$. Two boundary equations are found by a mathematical conversion to be:

$$V_G(0) = \frac{Y'_{\mathrm{SD}} I'_G(0) - Y'_{\mathrm{GD}} I'_S(0)}{Y'_{\mathrm{SG}} Y_{\mathrm{GD}} - Y'_{\mathrm{SD}} Y'_{\mathrm{GG}}}, \text{ and } V_D(0) = \frac{Y'_{\mathrm{SG}} I'_G(0) - Y'_{\mathrm{GG}} I'_S(0)}{Y'_{\mathrm{SD}} Y'_{\mathrm{GG}} - Y'_{\mathrm{SG}} Y'_{\mathrm{GD}}}. \qquad \textbf{(5.5)}$$

Voltage boundaries in the equations (5.5) are one possible solution. Others can be found for example on different locations at $x \neq 0$. Other boundaries can be helpful, if there are convergence problems for numerical solutions. For analytic solutions the location x of the boundaries are irrelevant.

As discussed above the general analytic solution is very extensive. But for many considerations a simplified version of the system is enough to get an appropriate solution. For example, the solutions in equation (4.5) and equation (4.6) which can be solved by this general form. Thus this general form can be used as basis for further analytic treatments.

5.3.3 Extended Small Signal Model

In this section the impedance parameters in the Z' matrix and the admittance parameters in the Y' matrix will be derived, in order to find an extended small signal model for large gate width transistor finger structures. The model is illustrated with lumped elements in figure 52. In the cross-section the typical small signal model can be found with the transistor capacities per unit length C'_{DS}, C'_{GD}, C'_{GS}, and the current source given by $V_G(x) \cdot g_m$. Along the x-direction there are the inductances of the metal strips L'_S, L'_G, L'_D, the mutual inductances between the metallization $L'_{\mathrm{SG}} = L'_{\mathrm{SG}}$, $L'_{\mathrm{DG}} = L'_{\mathrm{GD}}$, $L'_{\mathrm{SD}} = L'_{\mathrm{DS}}$, and the parasitic resistances R'_S, R'_G, R'_D. There are different possibilities to connect the interfaces at location $x = 0$ and $x = W$. The typical case of current flow in power GaN-HEMTs are shown in figure 52 and defined above.

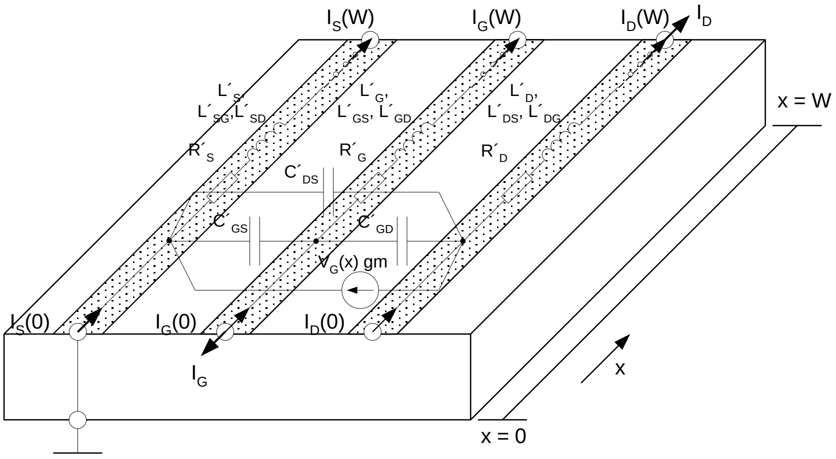

Figure 52: Extended small signal model of a transistor finger structure with large gate width.

In this consideration it is assumed that source at location $x = 0$ is connected to ground. The total current flows at this position into the source metallization strip. The total current is separated into the gate current I_G and the drain current I_D. The gate current flows at gate connection at $x = 0$, and the drain current at drain connection at $x = W$.

The impedance parameters $Z'_{n,m}$ and the admittance parameter $Y'_{n,m}$ can be found by using the rules in equation (5.6). These rules are used in the Z-parameter and Y-parameter theory, as shown e.g. in [96]. The rules are valid for the general case of an N-port network. The rules are defined as:

$$-Z_{n,m} = \frac{V_n'}{I_m}\Big|_{I_k=0 \text{ for } k\neq m}, \text{ and } -Y_{n,m} = \frac{I_n'}{V_m}\Big|_{V_k=0 \text{ for } k\neq m}. \quad \textbf{(5.6)}$$

In contrast to n-port matrices in the ordinary form the impedances and admittances are defined per unit length with the help of equations in (5.6), $Z'_{n,m} = Z_{n,m}/W$, and $Y'_{n,m} = Y_{n,m}/W$ the impedance parameter for the Z' matrix and the admittance parameter in the Y' matrix can be found to be:

$$-Z' = \begin{bmatrix} R_S' + j\omega L_S' & j\omega L_{\mathrm{SG}}' & j\omega L_{\mathrm{SD}}' \\ j\omega L_{\mathrm{GS}}' & R_G' + j\omega L_G' & j\omega L_{\mathrm{GD}}' \\ j\omega L_{\mathrm{DS}}' & j\omega L_{\mathrm{DG}}' & R_D' + j\omega L_D' \end{bmatrix}, \text{ and} \quad \textbf{(5.7)}$$

$$-Y' = \begin{bmatrix} j\omega(C_{\mathrm{GS}}' + C_{\mathrm{DS}}') + g_m & -j\omega C_{\mathrm{GS}}' - g_m & -j\omega C_{\mathrm{DS}}' \\ -j\omega C_{\mathrm{GS}}' & j\omega(C_{\mathrm{GS}}' + C_{\mathrm{GD}}') & -j\omega C_{\mathrm{GD}}' \\ -j\omega C_{\mathrm{DS}}' - g_m & -j\omega C_{\mathrm{GD}}' + g_m & j\omega(C_{\mathrm{DS}}' + C_{\mathrm{GD}}') \end{bmatrix} \quad \textbf{(5.8)}$$

Thus this general form can be used as basis for further analytic treatments. Furthermore, this differential equation system can be used to analyze the behavior of large gate width HEMT structures by numerical solvers, e.g. GNU Octave, which is shown in [50].

5.4 Conclusion: Switching-State

Chapter 5 presents the characterization of the most relevant parameters of a power HEMT in the switching-state. The transient switching behavior of GaN-HEMTs is investigated in a pulse setup, which was developed in this work. The purpose of this measurement setup is to characterize GaN-HEMTs in an application-oriented environment. The used periphery corresponds mostly to conditions in real applications.

The setup is used to characterize the turn-on and turn-off event. These measurements have been used to extract the dynamic device parameters, as the gate-charge, or the dynamic on-state resistance. As shown in section 1.3 the gate-charge is the determining device parameter of the switching losses. The gate-charge measurements on a large-gate width device with

248 mm are investigated as a function of the off-state voltage. The results show low influence of the drain source voltage on the gate charge, and the device achieves a low gate charge value with of 12 nC. Furthermore this chapter presents a description how the dynamic on-state resistance can be characterized in good resolution. The setup is used to characterize the performance demonstrator, which is shown in chapter 7.

In analogy to the on-state model in section 4.2 a three wire model is developed and presented in this chapter. This can be used for analytic investigations of large gate width finger structures. Furthermore the equations can be calculated by numerical solvers to analyze the small signal behavior on large gate width fingers.

The behavior of the three terminal capacitances is an important part of a power device model and should be taken into account in simulation and design of power circuits. These capacitances are highly non-linear due to the stepwise depletion of the channel caused by field plates. In this chapter these terminal capacitances are characterized as a function of the off-state voltage and discussed with respect to the intrinsic HEMT design.

The large gate width finger structures of power HEMTs feature considerable series-inductances and mutual-inductances. These parameters have been determined by two-dimensional finite element simulations. These inductances together with the measured terminal capacitances can be implemented in the extended small signal model which is presented in this chapter. Thus it can be used for further investigations on large gate width fingers.

GaN-HEMTs require low switching charges to turn-on and turn-off the current in the transistor channel. This is valid for forward as well as for reverse currents, and this is not self-evident. The behavior of GaN-HEMTs in the reverse-state differs considerably from the reverse characteristic of conventional power devices. In the following chapter the reverse-state of GaN-HEMTs is investigated and a new improved HEMT structures with integrated freewheeling path is presented.

6. Reverse-State-Specific Device Design and Characterization

6.1 Introduction: Reverse-State

The reverse operation has a high significance in power electronic circuits. In order to achieve an efficient reverse operation, power transistors are often connected in parallel with free-wheeling diodes, as shown in figure 2. Especially in half- and full-bridge topologies this configuration is the usual case. The free-wheeling diodes offer a path for inductive reverse currents. IGBTs are typically connected with additional external free-wheeling diodes. This is an expensive hybrid solution and the additional components have additional parasitic inductive interconnections. But the advantage of external diodes is that the designer is able to select the desired performance of the free-wheeling diode. Si Power-MOSFETs feature an internal body-diode as free-wheeling diode. But the reverse recovery charge of body-diodes is relatively high compared to single device Schottky diodes. This is shown in [97], and another detailed comparison for different types of Si-MOSFETs and SiC-devices in the 600 V / 10 A-class can be found in the book of Baliga [98]. The reverse-characteristic of GaN-HEMTs is rarely noticed in literature. Historically HEMT-devices have been mainly used in high frequency applications. In these applications the operation is usually in the forward direction. The use of GaN-diodes in the reverse-state operation is beneficial for some reasons. Although GaN-based diodes have a relatively high reverse forward voltage, they provide the same advantages as the HEMTs, such as a high breakdown voltage and a high on-state performance, and if a free-wheeling diode is realized as a Schottky contact it features a low reverse recovery charge.

In this chapter the reverse characteristic of conventional GaN-HEMTs is investigated. The performance of a high voltage GaN-based Schottky diode is presented, and a new concept of GaN-HEMTs with integrated Schottky diodes for an improved reverse operation is introduced and explored.

6.2 Reverse-State of conventional GaN-HEMTs

The output characteristic of a transistor is usually shown in forward direction, which is the drain current as a function of the positive drain-source voltage. However in many power applications a power device is also driven in reverse direction, which is the negative drain-current as a function of the negative drain-source voltage. It should be noted that the reverse characteristic of a GaN-HEMT structure is different from the reverse characteristic of conventional power devices. GaN-HEMTs have a diode-like reverse characteristic. However, it is different to conventional body-diodes, because the diode forward voltage V_{fwrd} depends on the gate-source voltage and this circumstance can lead to high reverse conduction losses. A characterization of the reverse characteristic on E-mode GaN-HEMT is shown in [99]. The characteristic is similar to the behavior of a JFET-device. The full output characteristic of a conventional HEMTs structure with forward- and reverse- state is shown in figure 53.

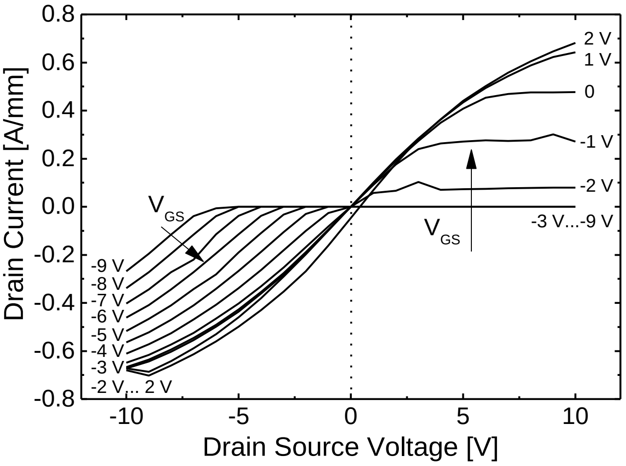

Figure 53: Typical output characteristic of a GaN-HEMT with Schottky gate. Shown is the forward- and reverse behavior for different gate-source voltages. The measurement is stepped beginning with a negative gate-source voltage of V_{GS} = -9 V to a positive voltage of V_{GS} = +2 V. The measured GaN-HEMT has a gate-width of W = 50 µm, a gate-drain distance of l_{GD} = 15 µm, a gate length of l_G = 1 µm, and a gate-sources distance of l_{GS} = 2 µm.

The reason for this reverse characteristic is the bidirectional property of a GaN-HEMT. This can be understood by considering a simple intrinsic HEMT structure, with drain, gate, source and conducting channel. If the structure is not optimized for high off-state voltages, the HEMT can be realized without field plates and the gate can be placed in the center. Such a device would be fully symmetric and drain and source are interchangeable. The device is in the on-state if $V_{GS} > V_{TH}$, and it is in the on-state if $V_{GD} > V_{TH}$. An optimized HEMT is not symmetrical in terms of its breakdown voltages, because of the field plates on source side and because of the asymmetric gate-location. However in terms of threshold voltages it can be treated as symmetrical, thus the device is in the on-state if $V_{GS} > V_{TH,}$ as well as if $V_{GD} > V_{TH}$. Under this condition the device features a reverse-state as shown in figure 53. Therefore, a device is in the on-state, if the negative drain-source voltage is higher than the threshold voltage and the gate source voltage $-V_{DS} > V_{TH} + V_{GS}$. The negative gate voltage is added to the reverse diode forward voltage, and this increases the reverse conduction losses.

6.3 GaN-Schottky Diodes

As discussed above it is advantageous in many power applications to have a diode characteristic in the reverse-state. However as shown in figure 53 the typical reverse characteristic of a GaN-HEMT with Schottky gate is dependent of the potential of the gate voltage. Therefore in many topologies power switches are connected in parallel with free-wheeling diodes, as shown e.g. in [100]. In contrast to vertical power technologies, such as Power-MOSFETs or IGBTs, in the lateral GaN-heterojunction technology Schottky diode-structures can be added in a monolithic design, in case that a free-wheeling diode is necessary in the reverse-state for a certain application. Such a solution was shown in [101]. Fabricated is a full-monolithic GaN-on-Si half-bridge with integrated free-wheeling diodes for a one-phase inverter for automotive applications. The total chip size is about 4×3 mm². Active area of one transistor is about 2×0.5 mm², and a diode has active area of 1×0.5 mm². Another example for such a GaN-on-Si half-bridge can be found in [100] in a hybrid solution. In this module SiC diodes are chosen as free-wheeling diodes in parallel to the two power switches.

In this section the layout and the performance of fabricated heterojunction GaN-Schottky diodes are investigated and presented.

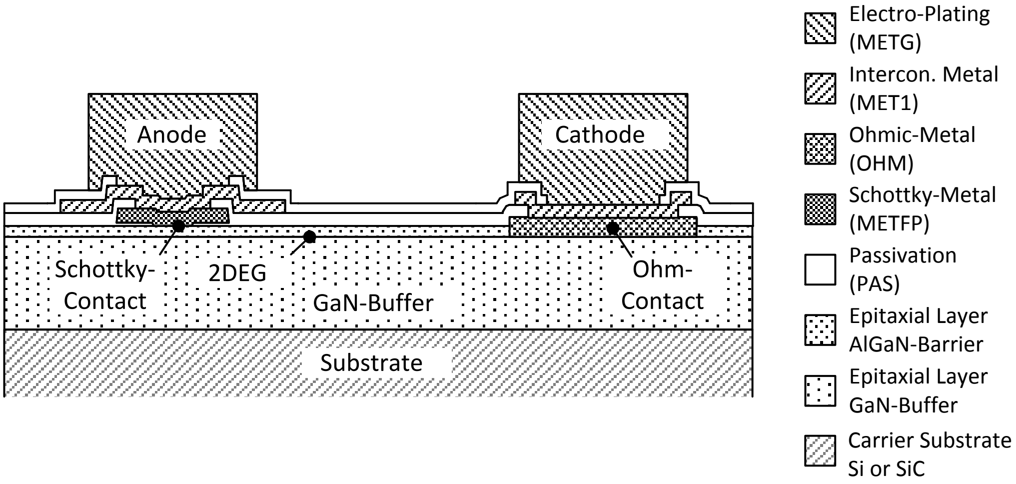

Figure 54: Cross-section of a heterojunction GaN-Schottky diode for high voltage applications

In figure 54 the cross-section of a heterojunction GaN-Schottky diode is shown. On the left there is the anode, which is realized as Schottky contact and on the right there is the cathode, which is realized as ohmic contact. The ohmic contact is connected to the two dimensional electron gas (2DEG), which is used as channel for the diode. Very similar to a GaN-HEMT structure a GaN-diode can be realized with field plates. In the off-state the electrical field is applied between cathode and anode. If there are no field plates the highest field strength appears under the anode at the end of the Schottky contact in cathode direction. Therefore by analogy to the off-state of a GaN-HEMT, the critical field peaks can be reduced by field plates. The Schottky contact head has the same function as a Γ-gate or a T-gate field plate. In this work the Schottky contacts for the anodes are realized with the same metallization as for the HEMT gates (METFP). The passivation on the top of the anode is etched and thus the anode is connected with the interconnection metallization (MET1) and the electroplating metallization (METG). In GaN-HEMT there is a source-connected field plate realized by the interconnection metallization (MET1). The diode has a similar field plate which is realized in this metallization (MET1) but in this case it is connected to the anode Schottky contact. By considering the electric fields this makes only a small difference. The potential difference between gate and source is very low compared to the gate drain voltage. For field considerations the differential voltage between gate and source can be neglected, and thus it is the equal case as for a diode. Thus the lengths of the field plates can be made with the same dimensions as for a HEMT. This is also valid for the anode- to cathode- distance. This distance can be equally chosen as for the gate-drain distance of an HEMT, if the same breakdown voltage is aimed. Thus for high voltage diodes the anode- to cathode- distance is a dominating parameter of the total structure length. The Schottky length is relatively small compare to the channel. The anode is an ohmic contact (OHM) and its length is determined by the electroplated interconnection metallization above. The metallization for the anode and cathode has to carry the on-state current in the same manner as for a power HEMT the drain- and the source- metallization. The analysis for such layouts is given above in chapter 4 and can be applied on diodes in the same way.

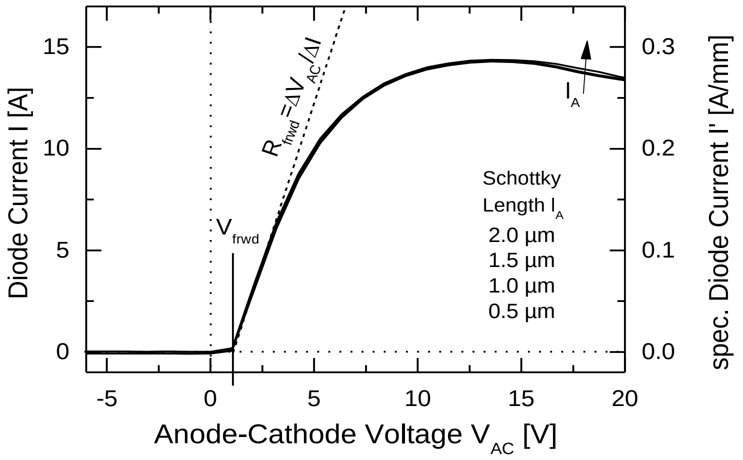

Figure 55: Measurement results of large channel width $W = 48$ mm GaN-on-Si diodes for power applications. The anode-cathode distance of the diode is $l_{AC} = 17$ µm. Measurements are made on-wafer with a four-point measurement setup and in pulse-mode with a pulse time of $t_{PLS} = 0.1$ ms at room temperature.

The measurement results of large gate width GaN-based Schottky diodes are shown in figure 55. The diodes-under-test are realized with different Schottky contact lengths. The Schottky length is scaled from $l_A = 0.5 - 2$ µm, and the anode-cathode distance is $l_{AC} = 17$ µm. Thus these diodes are suitable for off-state voltage up to 600 V. Each diode has been fabricated on a chip size of $A = 2{\times}1$ mm², the total diode channel-widths are $W = 48$ mm. As shown in the measurement results the scaling of the Schottky length l_A from 2 µm to 0.5 µm and has nearly not influence to the forward performance. There is an insignificant difference observable at the saturation currents. Due to technological minimum ratings the anode length cannot be further reduced to see a bottleneck effect. The length of $l_A = 0.5$ µm is the minimum possible Schottky contact length. This limit is caused by the photolithography in this technology. The device has forward voltage of $V_{fwrd} = 1.4$ V. The forward resistance of the devices is calculated to be $R_{\mathrm{fwrd}} = 400\ \mathrm{m\Omega}$. This corresponds to a specific value per unit length of $R'_{\mathrm{fwrd}} = 19.5\ \Omega\mathrm{mm}$.

6.4 GaN-HEMT with Integrated Free-Wheeling Diode

A target of this work is the design of area-efficient, fast switching GaN-HEMTs for power applications and as discussed above in many power applications free-wheeling diodes are necessary for a save and proper operation. Certainly hybrid solutions are possible as shown in [100]. But hybrid solutions are expensive due to the effort of components, assembly and bond wire interconnections. In addition, extensive interconnections introduce wire parasitics, and this reduces switching speed and this may lead to overshoots, due to inductive impedances. For this reason in this section new possibilities and solutions are discussed. Furthermore a new design approach of GaN-HEMTs with integrated free-wheeling diodes is introduced and investigated.

The monolithic integration of free-wheeling diodes is a possibility to reduce the problems of a hybrid solution. Since GaN-HEMTs are lateral power devices the integration of different components is possible. As shown in [101] the full monolithic integration of a GaN half bridge with two HEMTs and two diodes is already realized. As shown in section 6.3 the area for the additional free-wheeling diodes is about 1/3 of the total active area. The free-wheeling diode has to withstand the same off-state voltage as the power switch. Hence the anode-cathode distance should be chosen similar to the gate-drain distance $l_{\mathrm{GD}} \approx l_{\mathrm{AC}}$, and in high voltage devices the gate-drain distance l_{GD} is the dominating distance and thus the relevant area consuming parameter.

In publication [101] the area of the diode finger structure is placed next to the area of the HEMT finger structure. From the thermal point of view this is disadvantageous, and can be easily improved by an alternating structure. Thus HEMT- and diode-fingers are interleaved, so that the thermal cycling can be better distributed on chip area. In such a layout the drain of the HEMT shares the finger metallization strip and ohmic contact with the cathode. The Schottky contact of the anode has a separate metallization strip. Its interface is connected to the source bus. Such an interleaved structure was developed and fabricated in this work on a chip size of $A = 2\times2\ \mathrm{mm}^2$. Due to the additional diode channel length the area-efficiency of this structure was low and such this approach was not pursued any further. However the performance will be discussed and compared below in table 5.

A technologically demanding structure is shown in [102]. The Si carrier bulk material is used to build an integrated Si body-diode to the ground plate of the device. Therefore it is necessary to edge a via-hole through the drain contact. The advantage of this structure is that there is no extra space needed for the realization of the diode. On the other hand the fabrication is more complex, and due to the drain-down-vias through the buffer the back side of the GaN-buffer is on drain potential. This solution can affect the dynamic- and breakdown-properties. Furthermore since large-area buffer backside is on drain potential the sensitive Miller capacitance will be increased.

Another approach which has been developed in this work is the use of a lateral, internal free-wheeling path. The same approach was developed in parallel from B.-R. Park and first published in 2013 in [103] and later in [104]. The principle and function will be explained below.

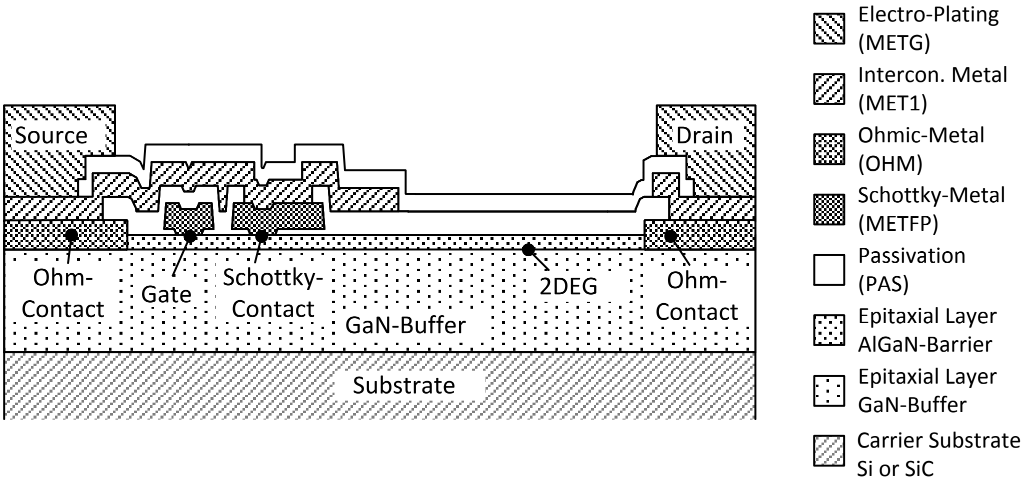

Figure 56: Cross-section of a GaN-HEMT with integrated free-wheeling diode.

The cross-section of such a HEMT structure with an internal Schottky free-wheeling path is shown in figure 56. In front of the gate, on the drain side, there is a Schottky contact connected to the source. This approach can be fabricated in the given technology by placing a second gate in front of the ordinary gate. The passivation over this gate has to be opened and connected to the source connected field plate.

In the reverse-state the source potential is higher than the drain potential, whereas the gate can have any potential. In this solution the current can flow from the source through the source connected field plate, through the Schottky contact into the channel and through the channel into the drain. As mentioned, this path is open independent of the potential and state of the gate. If the gate is open, in the case that $V_{GS} > V_{TH}$, than an additional current can flow from source through the channel below the gate and below the Schottky contact to the drain.

In the off-state the gate is closed $V_{GS} < V_{TH}$, and the drain potential is higher than the source. In this case the Schottky contact is in inverse direction and the current into the Schottky path via the source connected field plate is blocked. Since the gate is in off-state the current flowing below the gate into the source is blocked as well. No current can flow from drain to source. The highest electric field density will appear at the corner of the Schottky contact towards the drain. In this structure the drain-Schottky contact distance determines the lateral breakdown behavior, by analogy to the drain-gate distance of a conventional HEMT structure.

The structure, which is shown in figure 56 has been realized, measured and directly compared to the results of a conventional HEMT structure in the same technology. The measurements have been made on the same wafer and the results are shown in figure 53. The drain-Schottky contact distance is chosen equal to the gate-drain distance of the conventional HEMT structure $l_{\mathrm{SC\text{-}D}} = l_{\mathrm{GD}} = 15\ \mu\mathrm{m}$, as well as the dimensions of the field plates. With this equivalent dimensions very similar breakdown behaviors can be expected and this has been confirmed in break-down measurements and verified for both structures.

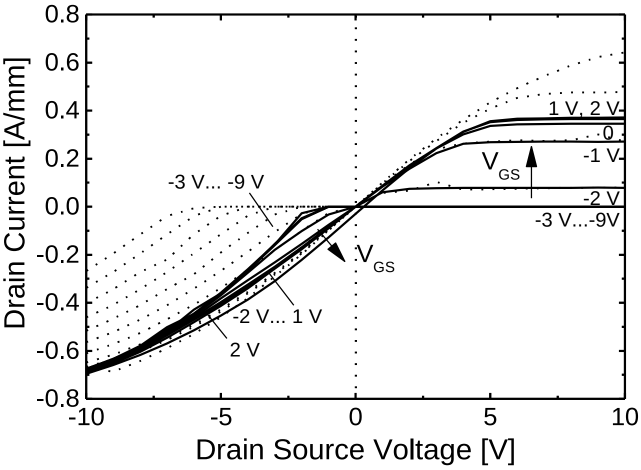

Figure 57: Output characteristic of a GaN-HEMT with integrated Schottky diode as free-wheeling path. The corresponding HEMT design is shown in figure 56. The measured GaN-HEMT has a gate-width of $W = 50\ \mu\mathrm{m}$, a Schottky contact to drain distance of $l_{\mathrm{SC\text{-}D}} = 15\ \mu\mathrm{m}$, a Schottky contact length of $l_{\mathrm{SC}} = 1\ \mu\mathrm{m}$, a Schottky contact-gate distance of $l_{\mathrm{SC\text{-}G}} = 2\mu\mathrm{m}$, a gate length of $l_{\mathrm{G}} = 1\ \mu\mathrm{m}$, and a gate-sources distance of $l_{\mathrm{GS}} = 2\ \mu\mathrm{m}$. The dotted lines show the output characteristic of a conventional HEMT structure with equivalent design parameters. These curves are shown before in figure 53.

The results of the measurement are shown in figure 57. In the reverse-state on the left side of the plot the current shows the desired behavior. If the reverse voltage exceeds the forward voltage of the Schottky contact a reverse current can flow through this path. In addition, the measurement results show the case when the gate is open, for $V_{\mathrm{GS}} > V_{\mathrm{TH}}$. In this case an additional current can flow from source through the channel segment below the gate, and a current flows already before the forward voltage of the Schottky contact is reached. The lowest on-state resistance can be determined by the gradient of a tangent at the point zero. If this on-state resistance is compared to the on-state resistance of the conventional HEMT, it can be shown that the structure with free-wheeling Schottky contact has a slightly higher on-state resistance. This issue has two reasons: on one hand the total channel length $l_{\mathrm{DS}} = l_{\mathrm{SC\text{-}D}}+l_{\mathrm{SC}}+l_{\mathrm{SC\text{-}G}}+l_{\mathrm{G}}+l_{\mathrm{GD}}$ is higher, caused by the Schottky contact to gate distance and the Schottky contact length. In contrast to that, the channel length of the conventional HEMT is slightly shorter and given by $l_{\mathrm{DS}} = l_{\mathrm{GD}}+l_{\mathrm{G}}+l_{\mathrm{GD}}$. On the other hand this Schottky contact acts like a second Schottky gate. This gate is directly connected to the source and thus it has a gate-source voltage of zero. A GaN-HEMT with a gate-source voltage of zero is not fully open. This limits the performance. Furthermore, in the measurement results it can be clearly seen, that the total drain current is much less than the total current of the conventional HEMT. The Schottky contact acts like a second gate and it limits the drain current to the value, which corresponds to a gate-source voltage of zero. A direct comparison of the reduced performance will be shown in the conclusion of this section.

As discussed above the Schottky contact acts like a second Schottky gate, which is connected to the source and this limits the drain current and it resists the current flow as shown in figure 57. In the following an improved concept is introduced, which was developed in this work to eliminate the problems of the approach above. Instead of using a continuous Schottky contact strip, the improved design uses an interrupted Schottky contact strip, as shown in figure 58. This approach was developed in this work and patented in [105], as well as in [106], and later published in [107].

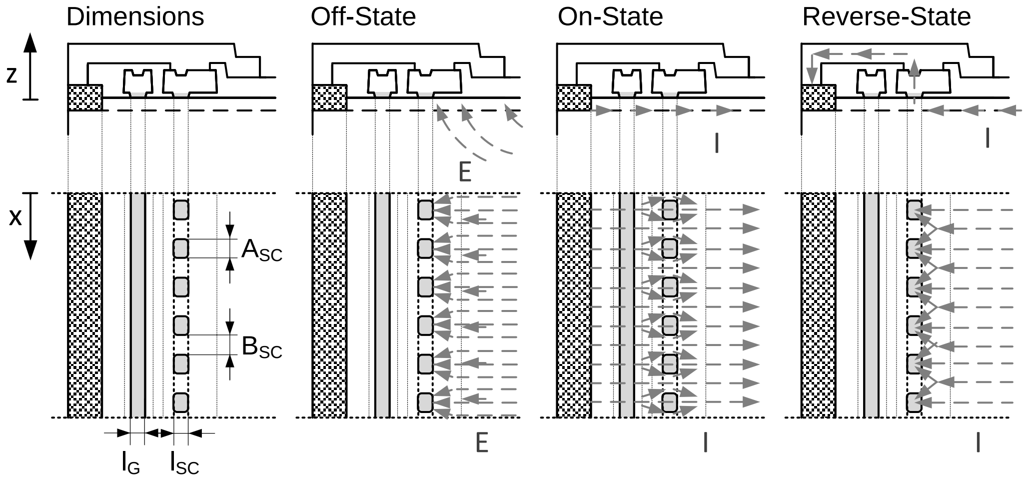

Figure 58: Cross-section and top-view of gate-source region of a GaN-HEMT structure with integrated, separated Schottky contacts as free-wheeling path. The figure is separated in four parts: (Dimensions) The dimensions of the Schottky contacts are defined. (Off-State) Sketch of the electric field lines *E* in the device off-state are illustrated. (On-State) The current flow-lines are shown through the channel in the on-state. (Reverse-State) The electron current flow-lines are illustrated through the Schottky contacts.

The advantage of such a structure is that in the on-state the current has the possibility to flow around the Schottky contacts. Thus the maximum current is not limited by the reverse Schottky contacts. Nevertheless, a part of the current will also flow underneath the Schottky contacts. The Schottky contacts can be realized with a very small contact width A_{SC}, as well as the pitch B_{SC} can be adapted and optimized for best thermal distribution and highest performance. In the off-state the Schottky contacts are in inverse direction. The electric field lines will terminate at the Schottky contacts. The field lines will end below the contacts at the Schottky contact edge at drain side. In the reverse-state the current can flow into the contact and it can flow through the field plate metallization to the source. If the current density in reverse-state at the contacts rises up, than the current can flow around the contact and enter from the sides.

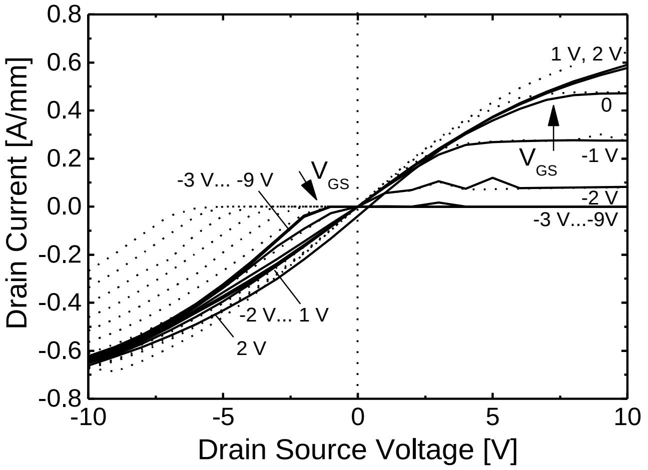

Figure 59: Output characteristic of a GaN-HEMT with separated Schottky diode contacts as free-wheeling path. The corresponding HEMT design is shown in figure 58. The measured GaN-HEMT has the following design parameters: $W = 50$ µm, $l_{SC\text{-}D} = 15$ µm, $l_{SC} = 1$ µm, $l_{SC\text{-}G} = 2$µm, $l_G = 1$ µm, $l_{GS} = 2$ µm, a Schottky contacts width of $A_{SC} = 1$ µm, and a contact to contact pitch of $B_{SC} = 1$ µm. The dotted lines show the output characteristic of a conventional HEMT structure with equivalent design parameters. These curves are shown before in figure 53.

The measurement results are shown in figure 59. It is shown, that the structure with the Schottky contact array reaches a similar reverse-state performance as the structure with the continuous Schottky strip. In on-state the current is not limited due to the potential of the Schottky contacts, and the performance in forward direction is nearly as high as for conventional HEMT structure. A quantitative comparison between the different approaches is made in the next chapter.

6.5 Conclusion: Reverse-State

In many power applications a free-wheeling diode behavior is required, especially in half- and full-bridge topologies, electric machines, or in general applications with inductive loads. Power modules with IGBTs use additional power diodes as hybrid solutions. Power-MOSFETs are often realized with an internal body-diode. The reverse characteristic of GaN-HEMTs with Schottky gate is not suitable for this purpose. The use of additional diodes is required either as hybrid solution or as a monolithic approach. Compared to Si-diodes the GaN-Schottky diodes have a higher forward voltage, but a lower specific forward resistance per area, and a lower diode charge due to the wide bandgap properties. Beside the monolithic integration of GaN-Schottky diodes, there are new concepts investigated and developed in this work, to build a GaN-HEMT structure with integrated free-wheeling Schottky contacts.

A summary of the measurement results is given in table 5. All test structures have equivalent dimensions to be comparable. This means all structures use the same field plate configurations and the same depletion distance of 15 µm. Due to the implemented free-wheeling path the total channel length of the new approach is slightly increase by the additional Schottky contacts. The new approach requires less chip area, compared to a monolithic solution with a separated diode finger structure, because the new approach uses the depletion length $l_{SC\text{-}D} = 15$ µm for both, for the diode and for the HEMT. This saves chip-area, whereas the monolithic solution with separated diode finger requires this distance twice $l_{GD}+l_{AC} = 2\times15$ µm.

Table 5: Summary of measurement results for different approaches for HEMT designs. (Conditions) The specific on-state resistance R' was measured at $V'_{GS} = 1$ V, $V'_{DS} = 1$ V. The specific on-state current $I'_{D,MAX}$ was measured at $V'_{GS} = 1$ V, $V'_{DS} = 10$ V.

		Unit	Conv. HEMT	HEMT + Diode	Rev. HEMT 1	Rev. HEMT 2	Rev. HEMT 3	Rev. HEMT 4
On-State Resistance	R'	[Ωmm]	9.5	9.5	11.1	11.0	11.0	11.0
Maximum Drain Current	$I'_{D,MAX}$	[mA/mm]	689	689	364	619	635	582
Rev. Forward Voltage	V_{fwrd}	[V]	-	1.4	1.4	1.4	1.4	1.4
Rev. Forward Resistance	R_{fwrd}	[Ωmm]	-	8.9	8.9	11.1	12.2	10.0
Channel Length	l_{DS}	[µm]	28	43.5	31	31	31	31
Spec. On-State Resistance	$R_{ON}\cdot A$	[mΩcm²]	2.7	4.1	3.5	3.4	3.4	3.4
Schottky Contact Width	A_{SC}	[µm]	-	-	-	1	0.5	2
Schottky Contact Pitch	B_{SC}	[µm]	-	-	0	2	2	1.75

Different GaN-HEMT structures with integrated free-wheeling Schottky contacts have been investigated. The HEMT with continuous Schottky contact strip (Rev. HEMT 1) has a reduced drain-current, because the Schottky contact acts like a second Schottky gate with a potential of zero. An improved solution is to separate the Schottky contact into a high number of small Schottky contacts, thus the current can flow around the contacts in the on-state. This improves the current flow of the test structure from a value of $I'_{D,MAX} \approx 350$mA/mm up to a values of $I'_{D,MAX} > 600$mA/mm. Test structures with such multi-Schottky contacts have been shown in versions 2-4 (Rev. HEMT 2-4). These designs have various parameters for the contacts width A_{SC} and the contacts pitch B_{SC}. As was to be expected, the design (Rev. HEMT 3) with the lowest width $A_{SC} = 0.5$ and the highest pitch $B_{SC} = 2$ has achieved the highest drain current in forward on-state operation, but the highest forward resistance in the reverse-state. However the best solution depends on the requirements of the application, and can be adjusted by these two parameters.

The new intrinsic HEMT structure with integrated free-wheeling diodes (Rev. HEMT 2) is applied to a performance demonstrator device. Design and characterization is presented in the following chapter.

7. Performance of a Highly-Efficient GaN-Device

The design methods which have been introduced in previous chapters 3-0 are applied to an area-efficient GaN-HEMT demonstrator. In this chapter the layout of this power device is presented with references to the related design approaches presented in the previous chapters. A full device characterization with static- and dynamic- parameters will be performed. Furthermore results are compared to state-of-the-art power devices in different technologies.

7.1 Layout and Packaging

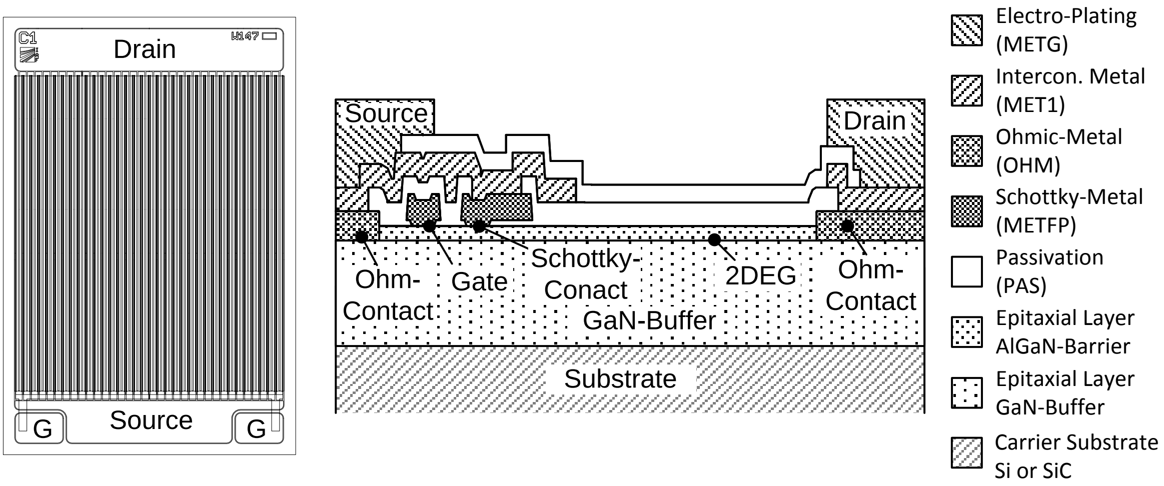

Figure 60: Area efficient GaN-demonstrator with integrated free-wheeling diodes. (Left) Top-view of the layout. (Right) Cross section and intrinsic layout of the demonstrator-device, which is analyzed in this section.

The demonstrator device was designed to achieve the highest static performance on a low chip area, as well as low gate- and reverse-recovery- charges to achieve excellent switching properties. For a robust off-state behavior in the 650 V class a depletion length of 15 µm has been chosen. Thus the chip is able to manage breakdown voltages above > 750 V by using a GaN-technology with lateral isolation properties of ≥ 50 V/µm. As shown in section 3.2.1 the latest technology generation has a lateral isolation of up to 105 V/µm on small area devices. However the derating of about factor two is required for large area devices due to the impact of the defect density on the wafer yield. Furthermore the high depletion reduces the electric field strength in the structure and therefore the reliability and dynamic degradation are improved. In addition a double source-connected field plate structure is designed to reduce high electric field peaks at the gate edge. For an efficient reverse conduction the intrinsic structure features an integrated free-wheeling diode as proposed in chapter 0 and illustrated in figure 60. The total channel length has a value of $l_{\mathrm{DS}} = 20$ µm. The ohmic contact length at drain is equal to the drain metallization $l_{\mathrm{OHM,D}} = l_{\mathrm{MET,D}}$, because of dynamic reasons, as shown in [41], whereas on the source side the ohmic contact is reduced to the technological minimum of $l_{\mathrm{OHM,S}} = 4$ µm to achieve a higher area-efficiency as proposed in section 4.3.3. However the current carrying galvanic metallization (METG) has the same metallization length on source side as on drain side $l_{\mathrm{MET,S}} = l_{\mathrm{MET,D}}$. The cross section of the intrinsic layout is illustrated in figure 60. The aspect ratio of the chip has been found by using the guideline from section 4.4.2 and selected by using figure 28. The drain- and source- pads with 300 µm length each are designed to be connected by 50 µm diameter gold bond wires. Thus a length of $Y_{\mathrm{periph}} = 800$ µm is needed for this peripheral area in y-direction. In x-direction a length of $X_{\mathrm{periph}} = 2\times80$ µm = 160 µm is used as total safety margin between the chip borders and the device structure. With a target chip area of $A = 6$ mm² and drain-source distance of $l_{\mathrm{DS}} = 20$ µm an aspect ratio of $X_{\mathrm{CHIP}}/Y_{\mathrm{CHIP}} = 2$ mm / 3 mm = 0.66 have been chosen.

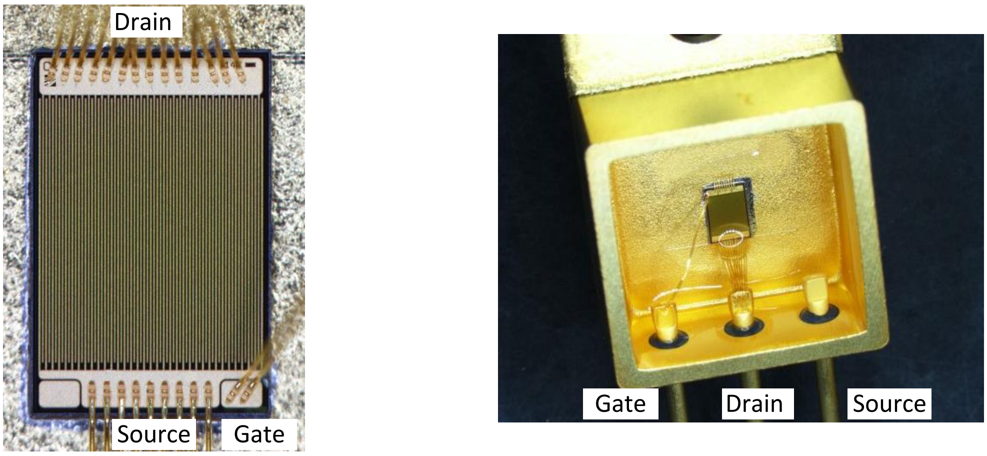

Figure 61: Assembly technology of the device-demonstrator (Left) Chip assembly on the package base plate by gold-tin solder die attachment and with 50 µm diameter bond wires interconnection technology. (Right) The chip is assembled in a TO258 engineering package with conventional pin assignment.

The device has been assembled in a TO258 engineering package. The assembly technology is illustrated in figure 61. The chip is attached on the base plate of a TO258 engineering packages using a gold-tin solder. The wedge-wedge bond wire connections are realized by 50 µm diameter gold wires. The backside of the chip is connected to the source contact with short wire bonds. This source-backside connection is done for dynamic reasons as explained in section 5.2.2. Due to the number of 9 short source bonds the connection is realized with low inductance and low resistance. Thus the backside and frame of this engineering package is at source potential. The source pin is short-circuited by a conduction ring on the outside of the package frame. In figure 61 this connection is hidden by the package frame. The drain pad is directly connected to the drain pin of the package by 14 bond wires. One of the two gate pads is connected to the gate pad by two bond wires. The connections are arranged in a way to achieve the conventional pin configuration for power devices.

7.2 Characterization of the Static Device Performance

7.2.1 Device Performance in the On-State and Reverse-State

The static output characteristic of the device was measured on-wafer as well as in-package. The results of the on-wafer characterization are shown in figure 62. The device was measured in a high current source measurement unit. To avoid self-heating the measurements have been made pulsed with a drain current pulse time of $t_{PLS} = 100\ \mu s$. The influence of parasitic resistances caused by measurement equipment has been excluded by a four-point measurement setup. The on-state resistance is measured to be $R_{ON} = 105\ m\Omega$ at a corresponding drain current of $I_D = 10$ A. At a drain-current of the $I_D = 30$ A the on-state resistance is still low with a value of $R_{ON} = 120\ m\Omega$. The maximum pulse drain current is in the range of $I_{D,MAX} = 43$ A, with an associated gate-source voltage of $V_{GS} = +1$ V, and a dissipated power of $P = 110$ W at this operation point. The threshold voltage is $V_{TH} = -3$ V. In the reverse-state the resistance is measured to be $R_{ON,RVS} = 150\ m\Omega$ at a corresponding drain current of $I_D = -30$ A, and a gate-source voltage of $V_{GS} = -5$ V. Under these conditions the device dissipated power of $P = 135$ W. With such a negative gate voltage the entire reverse current is flowing via the reverse Schottky contacts. The forward voltage of the reverse diode is measured to be $V_{fwrd} = 1.4$ V with a forward resistance gradient of $R_{fwrd} = 104\ m\Omega$ measured at a reverse current of $I_D = -30$ A, and an applied gate-source voltage of $V_{GS} = -5$ V.

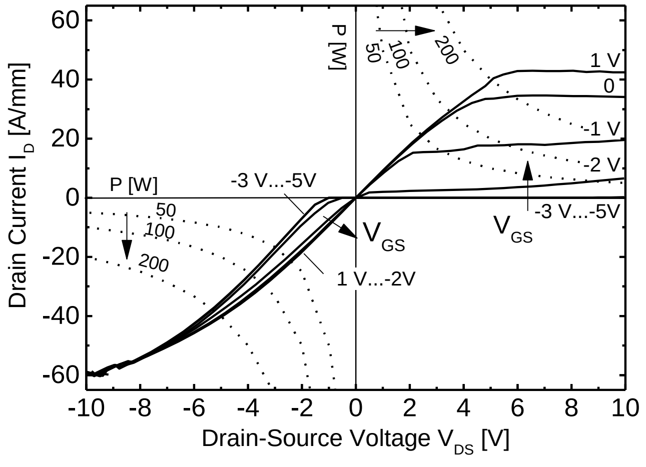

Figure 62: The output characteristics in on-, and in reverse– state measured in pulsed-mode on-wafer four-point measurements with $t_{PLS} = 100\ \mu s$.

7.2.2 Device Performance in the Off-State

Off-state measurements have been performed on a high voltage on-wafer probe station. The results of the leakage currents are shown in figure 63. The gate-source voltage was set to be $V_{GS} = -5$ V. The measurements have been made by semiautomatic measurements on a four inch wafer with 37 devices. About 50% of the devices achieved the breakdown voltage with a value of more than $V_{DS} = 1000$ V without any failure. The device gate-leakage currents are in the range of $I_{G,LEAK} = -0.5$ mA, and the drain leakage currents are in the range of $I_{D,LEAK} = 5$ mA. The drain leakage current is composed of the gate leakage currents and the leakage currents of the reverse diode Schottky contacts. With a gate width of $W = 147$ mm the specific leakage currents are below 50 µA/mm.

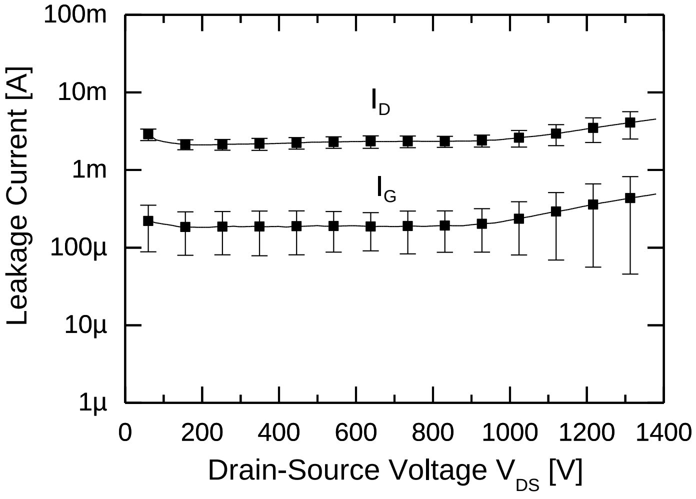

Figure 63: Off-state characterization of leakage currents. Measurements were performed using a high voltage on-wafer prober setup.

7.3 Characterization of the Dynamic Device Performance

7.3.1 Gate-Charge and Reverse Recovery Charge of the Device

One of the most important parameter of fast switching power devices is the gate charge, which is needed to bring the device from off-state into the on-state and vice versa. The procedure and the relevance of this parameter are discussed in section 5.2.2. This section presents the measurement results of the demonstrator device which is shown above. Figure 64 shows the gate charge curves of the device during the turn-on event as a function of the off-state voltage. The curve is plotted by calculating the integral $Q_G = \int I_G(t)\, dt$ and visualized by means of a gate charge curve with gate voltage versus gate charge. The gate charge was measured with a total value of below $Q_G = 4$ nC. The experiment was performed with a resistive load. A value of $R_L = 178\ \Omega$ was used in the setup. Furthermore a gate resistance of $R_G = 120\ \Omega$ was chosen to measure the gate current during the switching operation.

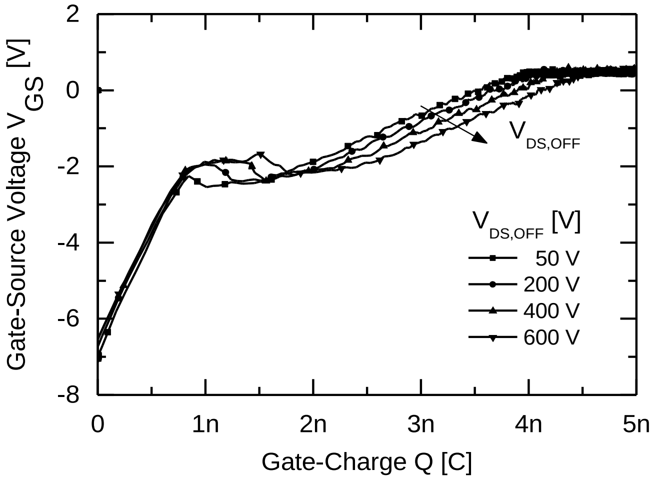

Figure 64: Gate charge curves measured during turn-on as a function of the off-state voltage.

Another important switching charge is the reverse recovery charge Q_{RR}. This charge is required to turn-on the power device from off-state into the reverse-on-state, and the same charge is necessary to turn-off the device from reverse on-state back into the off-state. The reverse recovery charge of the HEMT structure with integrated Schottky contact is much smaller compared to charge of conventional Power-MOSFETs with body-diode.

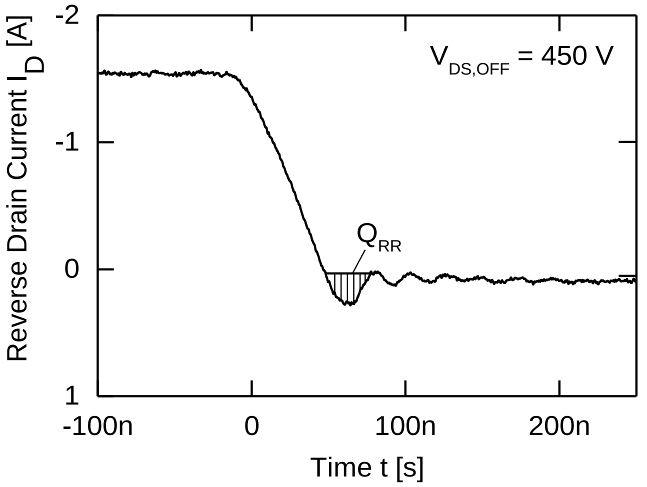

Figure 65 Characterization of the reverse recovery charge in a double pulse measurement setup with $V_{DS,OFF}$ = 450 V.

The reverse recovery charge has been characterized using a double pulse measurement setup which was realized in the work of B. Weiss and published in [108]. The turn-off behavior of the tested freewheeling diode is shown in figure 65. The pinched-off transistor at the high-side is turned-off from reverse-state into the off state, with a voltage of $V_{DS,OFF}$ = 450 V. The calculation of the integral of the current below zero over time results in a reverse recovery charge of around Q_{RR} = 12 nC.

7.3.2 In-Circuit Pulse Characterization

High voltage GaN-HEMT technologies are still in an early stage of development. Especially dynamic drain current degradation effects in pulsed operation are in the focus of international research groups. An inappropriate intrinsic design can affect the dynamic properties as shown in [41] as well as an unsuitable GaN buffer doping can lead the drastic increase of the dynamic on-state resistance caused by traps, as shown e.g. in [33]. As a consequence the GaN-HEMT device is not able to turn-on. Thus in case of driving a resistive load the drain-source voltage will not fall to a low value and the drain current is affected by the influence of the increased dynamic on-state resistance. In this work the switching performance was analyzed in a self-built pulse setup which is introduced in section 5.2.1. A turn-on pulse with a pulse time of about t_{PLS} = 10 µs and voltage between V_{GS} =-7 V and V_{GS} = +1 V was applied at the gate. The drain-source voltage response, as well as the drain current response are shown in figure 66.

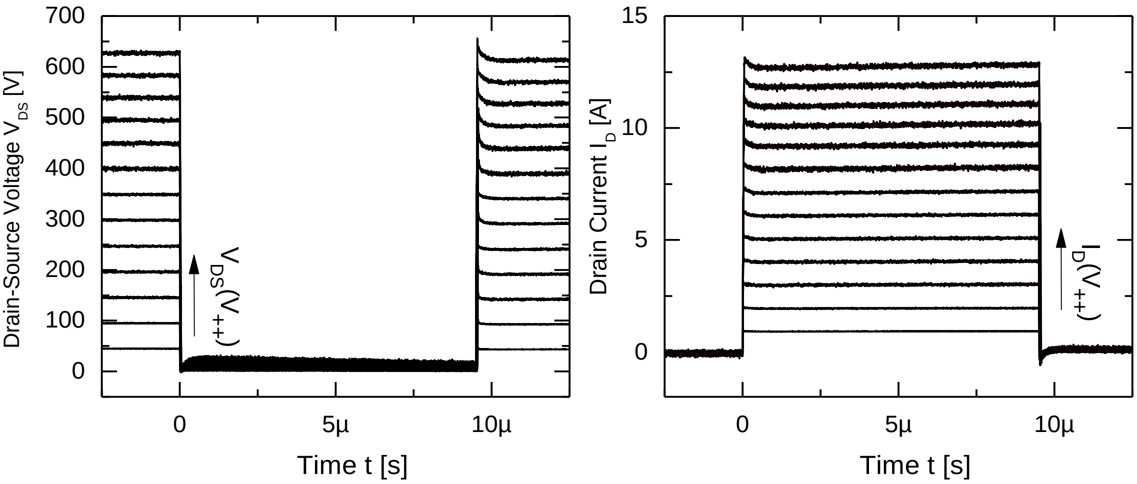

Figure 66: In-circuit pulse responce driving a resistive load R_{L} = 47 Ω at drain. (Left) Transient drain-source voltage with rising voltage supply V_{++}. (Right) Transient drain current response with rising voltage supply V_{++}.

The pulse is performed with rising supply voltage steps starting at V_{++} = 50 V up to a supply voltage of about V_{++} = 630 V. Between supply voltage and drain there is a resistive load with a value of R_{L} = 47 Ω. Thus the current is switched on up to a current of I_{D} = 13 A. The on-state resistance can not be determined due to inappropriate resolution of the oscilloscope with 8-bit analogue-to-digital converter as well as insufficient calibrated voltage probes. A clamping circuit is necessary for this characterization. The gate voltage is switched by a commercially available MOSFET-gate driver circuit (MIC4452). Between gate and driver a gate resistor of R_{G} = 15.2 Ω has been used to suppress instabilities. The characterization of the pulse response by using a resistive load is suitable to analyze turn-on and turn-off. With such a pulse setup driver circuits can be evaluated and gate resistors can be adapted to the gate drive. Furthermore if a device has strong dynamic drain current degradation the effects can be observed at drain-source voltage in the on-state as well as in the drain current response. However a small increase of the dynamic on-state resistance if $R_L >> R_{ON}$ cannot be recognized.

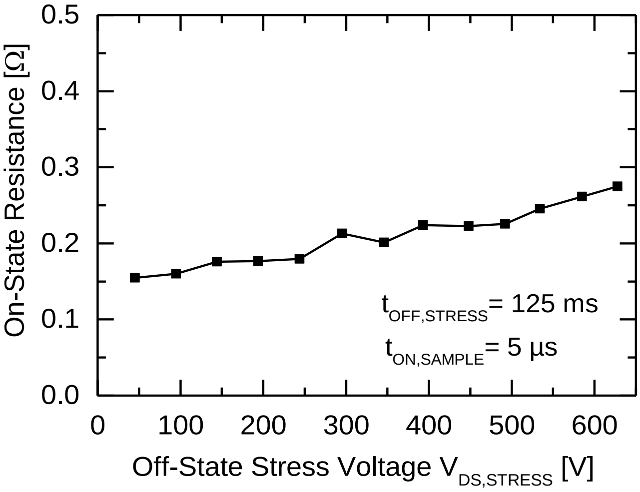

Figure 67: Increase of the dynamic on-state resistances as a function of the off-state stress voltage between drain and source caused by traps.

A suitable measurement setup to characterize the dynamic on-state resistance is introduced in section 5.2.1. A pulse setup with constant current source as load is likely to archive consistent on-state conditions even though the off-state stress voltage is increased during measurement campaign. The dynamic on-state resistance of the demonstrator device has been tested with the setup which was introduced in section 5.2. The device is turn-off and an off-state stress voltage is applied at the drain during a certain stress time. In this experiment the stress time was chosen to be $t_{OFF,STRESS} = 125$ ms. After this duration the device is switched on into the on-state and the current and voltage is measured immediately after turn-on. In this setup the on-state resistance of the device-under-test is measured after $t_{ON,SAMPLE} = 5$ µs. The results of this experiment are shown in figure 67. Compared to the static on-state characterization the dynamic on-state of the device is increased from $R_{ON,STATIC} = 115$ mΩ to $R_{ON,DYN,50V} = 150$ mΩ. The dynamic on-state resistance rise slightly as a function of the off-state stress voltage to a maximum value of $R_{ON,DYN,630V} = 275$ mΩ. Consequently, the relative increase of the on-state resistance is found to be lower than a factor of 2. Calculated by $R_{ON,DYN,630V}$ / $R_{ON,DYN,50V}$ = 275 mΩ / 150 mΩ = 1.83.

7.4 Performance Benchmark

The results of the characterization above are promising. The demonstrator device achieves advance static- and dynamic- transistor parameters: a high off-state voltage up to 1200 V, a low on-state resistance with a value of $R_{ON} = 105$ mΩ, high on-state current with $I_{D,MAX} = 40$ A, a low gate charge with a value of $Q_G = 4$ nC, and a low reverse recovery charge with $Q_{RR} = 12$ nC. The question arises how are these results compared to other state-of-the-art devices? How can this device be classified for the use in high voltage converter applications? A fair an objective comparison is challenging. Devices to compare are built for different voltage classes, power classes, or switching speeds. A classification of the device properties can be made by using figure-of-merits for power devices. This chapter benchmarks the device above to state-of-the-art power devices in GaN-, SiC, and Si-technologies.

7.4.1 Chip Area-Efficiency

Chip area-efficiency, which is valued as the product of the on-state resistance and the device area $R_{ON} \cdot A$ is the most referred figure-of-merit in literature in regards of wide band gap power devices. However $R_{ON} \cdot A$ is used as a broad term and widely varying devices under different initial conditions are compared by this parameter. In literature $R_{ON} \cdot A$ is often applied at very small device with gate widths in the range of $W = 50\text{-}1000\ \mu m$. These results are used to compare the technology parameter of the sheet resistance R_{SH} in the on-state versus the isolations properties. In these cases the area A of a device is determined without metallization for drain and source and without the needed area for bond pad of safety margin, as defined e.g. in [109]. In other publications area A includes the area for drain and source metallization but without bond-pads, as defined in e.g. in [32].

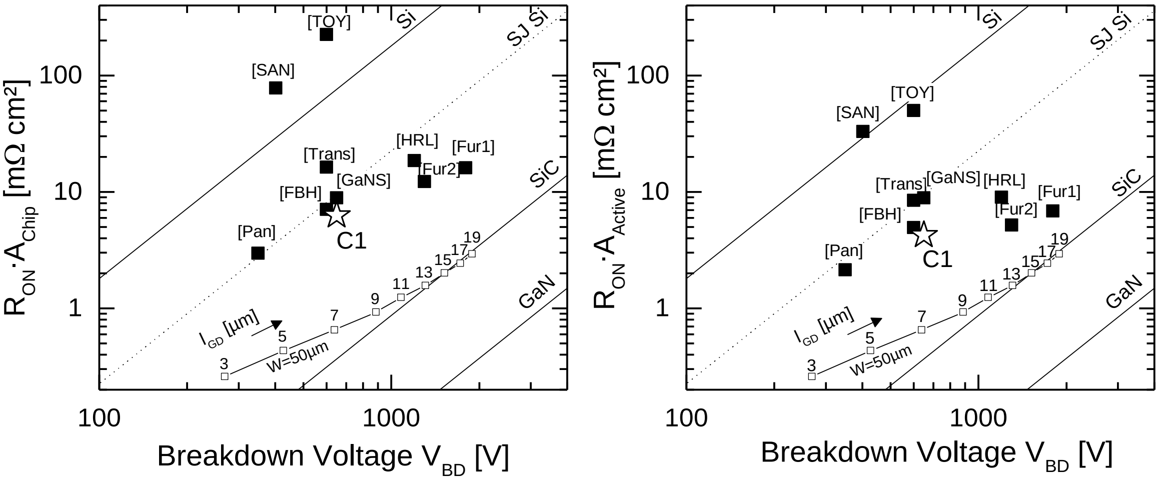

Figure 68: Product of the on-state resistance and device area $R_{ON} \cdot A$ as a function of the breakdown voltage V_{BD}. Values are taken from literature of large area devices in comparison to the GaN-demonstrator device C1, which is analyzed in this chapter. Furthermore Baliga's theoretical limit for the figure-of-merit $R_{ON} \cdot A$ for a vertical depletion zones, which is shown in equation (2.3) are drawn in the plot for comparison. A chain of values from section 3.2.1 are illustrated in the plot. These results are taken from small area devices with $W = 50\ \mu m$ and without pad or metallization periphery area. (Left) The value $R_{ON} \cdot A_{Chip}$ includes the total chip area. (Right) The value $R_{ON} \cdot A_{Active}$ includes the active area without bond pads and safety margin areas. References: [Fur1&Fur2]=[32], [HRL]=[110], [FBH]=[61], [Pan]=[111], [SAN]=[112], [Toy]=[113], [Trans]= [47], [GaNS]=[48].

This work wants to compare less the technology, but rather more the area-efficiency design of large area structure with gate width of more than $W > 100$ mm. Figure 68 shows two plots with large area devices which have been found in literature. The left plot shows $R_{ON}{\cdot}A_{Chip}$ of the devices calculated using the total chip area. Whereas on the right side the $R_{ON}{\cdot}A_{Active}$ values are calculated by using just the active area including drain and source metallization but without bond pads and safety margin areas. It can be shown that the demonstrator device in this work achieves a lower $R_{ON}{\cdot}A$ than all other devices in the same voltage range. This is valid for both definitions for the total chip area with a value of $R_{ON}{\cdot}A_{Chip} = 6.3\ \text{m}\Omega{\cdot}\text{cm}^2$ as well as for active comb area without bond pads with a value of $R_{ON}{\cdot}A_{Active} = 4.25\ \text{m}\Omega{\cdot}\text{cm}^2$.

However the comparison in figure 68 is still strongly related to technology properties. The breakdown voltage V_{BD} of the large area GaN devices is highly dependent on material quality or rather the defect density and isolation of the epitaxial GaN-buffer and the process technology. Therefore in figure 69 large area devices are compared as a function of the drain-source distance l_{DS}, in order to obtain a better evidence of the chip area-efficiency. Nevertheless, the sheet resistance as technology parameter has still an influence on this comparison, but they are comparable to the technology used in this work.

In comparison to the other designs with comparable drain source distance the demonstrator-device in this work achieves a better value of $R_{ON}{\cdot}A$. Only the design in [111] has a low value which is related the very low drain-source distance of $l_{DS} = 8$. Because the low drain-source distance l_{DS} is squared related to the value $R_{ON}{\cdot}A$ as shown in equation $R_{ON}{\cdot}A_{MIN} = R_{SH}{\cdot}l_{DS}^2$.

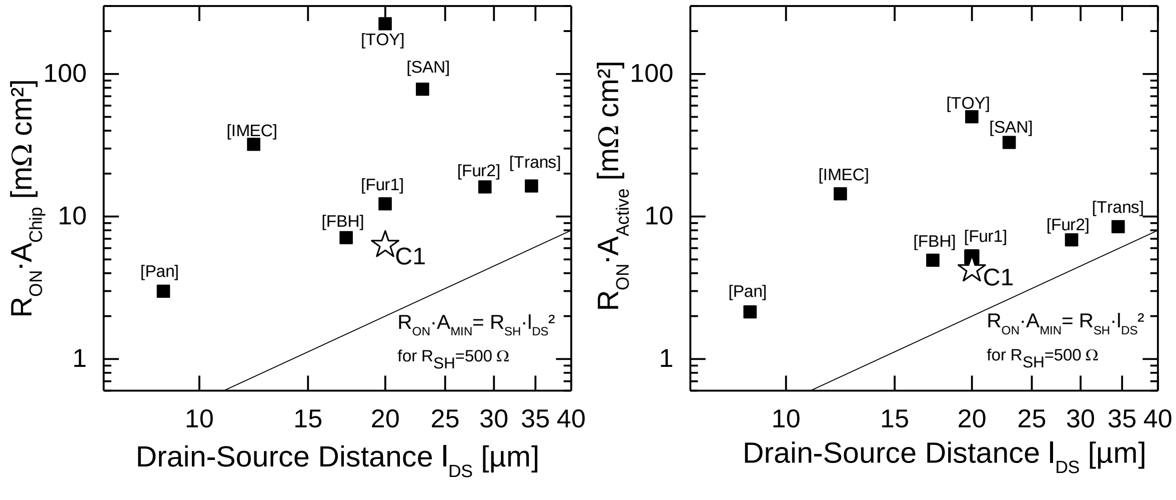

Figure 69: Product of the on-state resistance and device area $R_{ON}{\cdot}A$ as a function of the drain-source distance l_{DS}. Values are taken from literature of large area devices in comparison to the GaN- demonstrator device C1, which is analyzed in this chapter. Furthermore for comparison a line for $R_{ON}{\cdot}A_{MIN} = R_{SH}{\cdot}l_{DS}^2$, with $R_{SH} = 500\ \Omega$ is drawn in the plot. (Left) The value $R_{ON}{\cdot}A_{Chip}$ includes the total chip area. (Right) The value $R_{ON}{\cdot}A_{Active}$ includes the active area without bond pads and safety margin areas. References: [IMEC]=[46] [Fur1&Fur2]=[32], [HRL]=[110] [FBH]=[61], [Pan]= [111], [SAN]=[112], [Toy]=[113], [Trans]=[47], [GaNS]=[48].

The chip area-efficiency $R_{ON}{\cdot}A_{Chip}$ is a parameter which gives a statement about device performance per production cost. But only some percent of performance per chip area would be a too weak argument to change from an established technology as Si to a new barely developed technology as GaN-on-Si. Further convincing properties have to be shown to enable development leap. In this context the switching charges are key-parameters. GaN transistors require low charge quantities to switch the HEMT from the off-state into the on-state and back. Furthermore low charge quantities are necessary to switch the device from off-state into the reverse-state and back. And these low charges enable significant lower switching losses per pulse and therefore GaN-devices enable higher switching frequencies in converter applications. And this is desirable, because power inductors and capacitor in converters, can be designed to be smaller. Thus volume, weight and cost of the application are reduced.

7.4.2 Switching Charges

The most important figure-of-merit for fast and efficient power transistors is the product of the on-state resistance and the switching charge of $R_{ON}{\cdot}Q$. This product is a suitable reference value, because large devices have a low on-state resistance, but a high charge and low devices have a high on-state resistance but a low charge. Primarily the product of the on-state resistance and the gate charge $R_{ON}{\cdot}Q_G$ is considered and often specified in data sheets of power semiconductors.

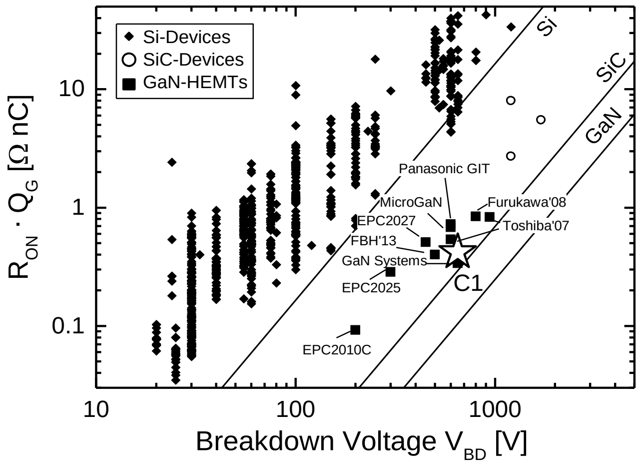

Figure 70: Product of the on-state resistance and gate charge $R_{ON}{\cdot}Q_G$ as a function of the breakdown voltage. GaN-HEMT demonstrator is compared to other state-of-the-art devices in Si-, SiC- and GaN- technologies. Furthermore the theoretical limit for $R_{ON}{\cdot}Q$ for a vertical depletion zones, which is shown in equation (2.9) are drawn in the plot as lines. References: [Furu08]=[113], [FBH]=[115], [Tos]=[116], [MicroGaN]=[117], [Pan]=[118], [GaNSys]=[119], [EPC2010C]=[120], [EPC2025]=[121].

Figure 70 shows the value of $R_{ON}{\cdot}Q_G$ for a large number of different power devices as function of the breakdown voltage. One can notice the similarity to the plot with $R_{ON}{\cdot}A$. Both values are related as shown in section 2.1.2. It is shown that the Si-devices have reached their theoretical limit. Whereas the values of $R_{ON}{\cdot}Q_G$ for GaN-devices are significant lower compared to the Si-devices. The demonstrator device in the work belongs to the devices with the best $R_{ON}{\cdot}Q_G$ in its voltage class.

A similar figure-of-merit is the product of the on-state resistance in reverse direction and the reverse recovery charge $R_{ON}·Q_{RR}$. The reverse recovery charge Q_{RR} is charge quantity, which is needed to switch from off-state into the reverse one-state. The reverse-state is relevant for most power topologies but often treated with little attention. In figure 71 the value of $R_{ON}·Q_{RR}$ of the demonstrator device is compared to other state-of-the-art power transistors with intrinsic free-wheeling diode and single power diode devices. In contrast to IGBTs the conventional Power-MOSFETs included an intrinsic body-diode, which are able to provide the desired reverse-state. However these intrinsic body-diodes feature relative poorly reverse recovery charge properties. This can be observed in left plot in figure 71. The left plot shows the $R_{ON}·Q_{RR}$ of transistors with intrinsic free-wheeling diode. The right plot shows the $R_{ON}·Q_{RR}$ of the diode. Compared to the diodes the intrinsic body-diodes are far away from the theoretical limit for $R_{ON}·Q$, which is also valid in reverse direction and given by equation (2.9). At the moment there are no other GaN-devices with intrinsic freewheeling diode published in literature. Conventional GaN-devices feature a JFET-behavior in reverse direction. This is depending on the gate-source voltage, and it features high reverse-state losses, due to high reverse-forward voltages. Therefore often the reverse-diode path is provided by an external antiparallel connected diode.

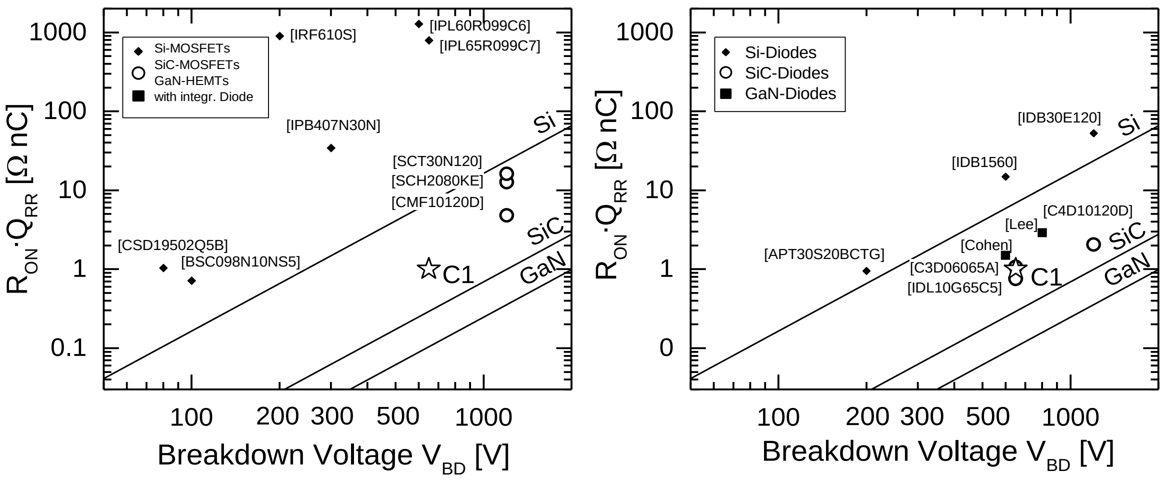

Figure 71: Product of the on-state resistance and reverse recovery charge $R_{ON}·Q_{RR}$ as a function of the breakdown voltage. The GaN-HEMT demonstrator is compared to other state-of-the-art devices in Si-, SiC- and GaN- technologies. Furthermore the theoretical limit for $R_{ON}·Q$ for a vertical depletion zone, which is shown in equation (2.9) are drawn in the plot as lines. (Left) The GaN demonstrator is shown in comparison with body-diodes of Power-MOSFETs. (Right) The GaN demonstrator is shown in comparison with power diodes. References: [Lee]=[122], [Cohen]= [2].

Baliga has compared different power device technologies in terms of its reverse recovery behavior [98]. Baliga has classified devices with a breakdown voltage in the range of $V_{BD} = 600$ V and $I_D = 10$A. In comparison to all other technologies the device with the enhanced HEMT structure with integrated-freewheeling contacts achieves the best value for $R_{ON}·Q_{RR}$.

In comparison to other state-of-the-art power transistors in the 650 V-class the performance demonstrator achieves the lowest area-specific on-state resistance, a very low figure-of-merit for fast and efficient power devices: $R_{ON}{\cdot}Q_G$, and it is the first GaN-based power HEMT with an integrated free-wheeling diode.

Conclusions and Outlook

This work presents the design and the characterization of highly-efficient GaN-HEMT power devices. New advanced design methods and new layout structures are developed to achieve area-efficient power HEMTs. These designs are suited for fabrication in existing AlGaN/GaN-heterojunction technologies. Furthermore the characteristics of GaN-HEMTs in the operating states are investigated with respect to the device designs.

The derived design methods and findings are applied in one large-area device HEMT layout, which was realized and compared to other state-of-the-art devices found in literature. The measurement results demonstrate the outstanding device performance and the benefits of the advanced design approaches.

The 650 V class rated demonstrator device is designed on an chip area of $A = 2\times3\ \text{mm}^2$ and it achieves a maximal voltage up to 1200 V, an on-state resistance of 105 mΩ, maximal current up to 40 A and low gate charges with a value of 4 nC, as well as low reverse recovery charge with $Q_{RR} = 12$ nC. The device has an area specific on-state resistance of $R_{ON}\cdot A_{CHIP} = 6.3\ \text{m}\Omega\cdot\text{cm}^2$. This value is lower than all $R_{ON}\cdot A_{CHIP}$ values of large-area GaN-HEMT devices in this voltage class. The same device achieves a low product of on-state resistance and gate-charge, with a value of $R_{ON}\cdot Q_G = 0.42\ \Omega\cdot\text{nC}$. This is known as the figure-of-merit to realize compact and highly-efficient power applications. Furthermore it is the first GaN-HEMT power device with an integrated free-wheeling diode. It achieves a low figure-of-merit for reverse recovery losses, with a value of $R_{ON}\cdot Q_{RR} = 1.26\ \Omega\cdot\text{nC}$, which is around factor 500 lower compared to state-of-the-art Si-MOSFETs, and in the range of the best GaN- and SiC-Schottky diodes.

A new methodical design approach leads to comb layouts with lowest area-specific on-state resistances. The fundamental of this design method is an analytically derived on-state model, which is presented in this work. The model describes the current and voltage distributions on the active area along the finger structure as well as on drain and source metallization. Furthermore the on-state resistance HEMT finger structures can be determined as function of the gate width and metallization length. A critical gate width as well as a critical metallization length are analytically derived and presented and should not be exceeded to achieve efficient designs.

The analysis on large gate width finger structures reveals the limits of the conventional comb layout. Two new extrinsic chip layouts are inspired by natural flow structures and introduced in this work. The archetype for the first structure is a four-leaf clover. It is suited for the assembly in conventional industrial standard packages (e.g. TO220 or TO258). This clover-structure achieves high chip area efficiencies due to fingers with lower gate width compared to comb-structures realized on same chip area. The second structure introduces a fractal comb design. The fractal approach enables an exceeding of the area-limits for very large gate width comb structures. On each self-similar comb level the metallization design can be adapted to the required current density. Thus very large area designs are possible with highly homogeneous power distributions and high area-efficiencies.

The reverse-state of GaN-HEMTs is hardly investigated in literature, although it is of considerable importance in most power topologies. This work characterizes the reverse-state of conventional HEMT structures and introduces an improved HEMT structure with integrated free-wheeling diodes in combination with high area-efficiency. The new structure enables a low-resistive reverse conduction which is independent of the gate-source voltage. It is especially suited for power topologies with inductive load. By using this structure hybrid-connected freewheeling diodes are not required anymore.

GaN-HEMTs features low switching losses due to the low gate-charges. As shown on the demonstrator device the gate-charge can be reduced by factor 10 compared to best Si-MOSFETs on the market. The very fast switching devices place new demands on measurement equipment. This work presents a new flexible application-oriented pulse setup. Low gate charges and the effect of the dynamic on-state resistance is measured with high resolution and shown in this work.

This work demonstrates the high potential of GaN-based heterojunction technologies by the development of highly-efficient power transistors. In direct comparison to conventional Si-based power devices the GaN-HEMTs achieve a lower area-specific on-state resistance and low switching charges. GaN can be grown by epitaxy on large-diameter low cost Si-substrates. Therefore the GaN-on-Si technology is promised to be a high performance technology at low cost.

However beyond device performance of highly-efficient power HEMTs the GaN-heterojunction technology enables an additional outstanding feature. In contrast to conventional power technologies, such as Power-MOSFETs or IGBTs, the GaN-based heterojunction technology is of lateral nature. This property enables the monolithic integration of several power devices side-by-side on a single GaN-chip. Entire circuits or power topologies can be integrated. Thus the performance of the devices can be further improved by reduced electric parasitics. Furthermore, on-chip interconnections and the related lower effort for assembly technologies improve reliability and reduce costs. Some promising results are achieved already today and realized in context to this work. A monolithic half-bridge circuit with integrated free-wheeling diodes is presented in [128]. Even more complex topologies as a multilevel converter can be integrated as shown in [129]. Furthermore a monolithically integrated power circuit with gate-driver stage combined with a power device demonstrates very fast slew rates, as shown in [70].

Advanced chip-designs in GaN-heterojunction technologies lead to outstanding power performance and higher functionality. These high performance GaN-devices will enable a new generation of power applications.

Appendix

I. Calculation Attachments

Some results of calculation are less important for this work, but may help in further considerations. For this reason and for completeness these results are attached in the appendix.

The equation below is an attachment of the solution of equation (4.1) - (4.3). Depicted is voltages V_S(x) and V_D(x) on source and drain metallization strips in the static on-state.

$$V_D(x) = \frac{\gamma \cdot I_{\text{Total}}}{4 \cdot G'} \cdot \frac{x\gamma + 1 - e^{(W-x)\gamma} - e^{x\gamma} + e^{W\gamma}(1 + W\gamma - x\gamma) - W\gamma}{e^{W\gamma} - 1}, \quad \textbf{(A.1)}$$

$$V_S(x) = V_{\text{Total}} + \frac{\gamma \cdot I_{\text{Total}}}{4 \cdot G'} \cdot \frac{x\gamma - 1 + e^{(W-x)\gamma} + e^{x\gamma} - e^{W\gamma}(1 + x\gamma)}{e^{W\gamma} - 1}. \quad \textbf{(A.2)}$$

II. Surface Current Density and Current Density

Current flow can be investigated by different models. Because of the lateral constitution of the GaN-technology it is often reasonable to use a 2-dimenstional model. Usually the expression of current density is related to a current through a cross-section area and describes the current density in a 3-dimensional conductor. In this work both expression are present. Therefore, this section wants to clarify the different views of current flow through a 2-dimensional and a 3-dimensional conductor.

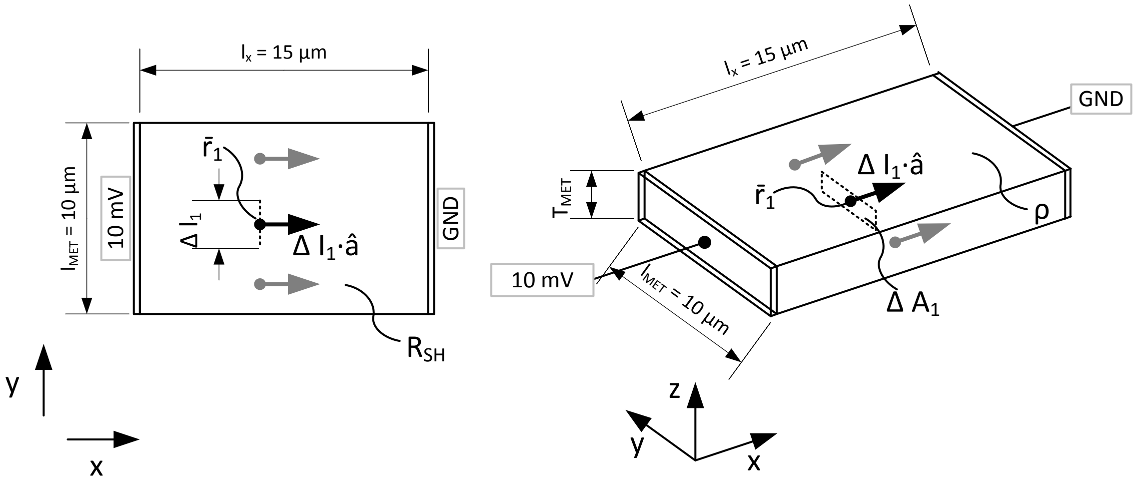

Figure 72: Current density though a conductor. (Left) Current density in 2-dimensional model. (Right) current flow in a 3-dimensional model.

The difference and the terms can be understood by examine an example of a short metallization strip shown in figure 72. This example determines the current density of a strip which is realized in metallization METG. The metal length in y-direction of $l_{\mathrm{MET}} = 10\ \mu\mathrm{m}$, the width in x-direction is $l_x = 15\ \mu\mathrm{m}$. The differential voltage between the interfaces is 10 mV.

First the 2-dimensional current density will be observed. This 2 dimensional charge flow at a point $\bar{r}_1$ is called the surface current density J_S and can be written as:

$$J_S(\bar{r}_1) = \lim_{\Delta 1_1 \to 0} \frac{\Delta I_1 \hat{a}}{\Delta l_1}. \tag{A.3}$$

The vector $\Delta I_1\ \hat{a}$ represents both the current magnitude ΔI_1 and direction $\hat{a}$ of the current flowing across small length Δl_1 at a point $\bar{r}_1$. Thus the unit of the surface current density J_S is ampere divided by meter [A/m] or in terms of smaller dimensions [A/mm]. In this simple example the vector $\hat{a}$ point in x-direction. As shown in table 3 the sheet resistance of metallization METG is in the range of $R_{\mathrm{SH,METG}} = 0.002\ \Omega_{\square}$. Thus the resistance of the structure is $R = R_{\mathrm{SH,METG}} \cdot l_x / l_{\mathrm{MET}} = 3\ \mathrm{m}\Omega$. Consequently a total current of $I = 3.33$ A would flow. Because of a homogeneous sheet resistance and a rectangular strip in this example the current and the length are proportional $I/I_1 = l_{\mathrm{MET}}/l_1$. Equation (A.3) can be simplified to $J_S = I/l_{\mathrm{MET}}$. Thus the surface current density J_S on this structure is $J_S = 3.33\ \mathrm{A}/10\ \mu\mathrm{m} = 333\ \mathrm{A/mm}$.

In the second part of this example the charge flow of a 3-dimensional strip is investigated as shown on the right side of figure 72. The electric current density J is a certain current ΔI_1 per cross-section area ΔA_1, which can be written as:

$$J(\bar{r}_1) = \lim_{\Delta A_1 \to 0} \frac{\Delta I_1 \hat{a}}{\Delta A_1}. \tag{A.4}$$

In analogy to the definition above the vector $\Delta I_1\ \hat{a}$ represents both the current magnitude ΔI_1 and direction $\hat{a}$ of the current flowing across small area ΔA_1 at a point $\bar{r}_1$. The unit of this current density is ampere divided by square meter [A/m²]. Because of small dimensions in this work current refer to millimeter [A/mm²]. The metallization strip is realized in metallization layer METG, thus the resistance, the voltage and the total current is as above. A similar relation as above, namely $I/I_1 = l_{\mathrm{MET}} \cdot T_{\mathrm{MET}} / \Delta A_1$ simplify equation (A.4) to $J = I/(l_{\mathrm{MET}} \cdot T_{\mathrm{MET}})$. Thus the current density across the metallization strip is about $J = 3.33\ \mathrm{A}/(0.01 \cdot 0.007\ \mathrm{mm}^2) = 47.6\ \mathrm{kA/mm}^2$.

The conversion of surface current density into the current density of a 3-dimenstional conductor is simple if the thickness of the conductor is known. In this example expression T_{MET} is the thickness of the conductor. Consequently the relation can be written as: $J = J_S / T_{\mathrm{MET}}$.

III. Surface Power Density and Volume Power Density

The expression power density has different meanings. In general the power density is the amount of power per volume. The general unit is W/m³. This expression is often used in terms of batteries, motors, and so on. Regarding voltage converter the expression is often used different. A voltage converter with a high power density is a compact converter, which is able to convert high power. But the power used for this value is dissipated the load and not in the compact converter. Thus the power density in terms of voltage-converter is a figure-of-merit of the compactness of a voltage in power applications. The typical unit for this value is kW/dm³.

In this work the expression is often used regarding the dissipated power at per chip-area at a certain location on the chip. For example the drain- and source-metallization of a high gate width finger structure has to carry the total current of the finger structure at the interfaces of drain and source. At these locations the metallization has a high surface current density, and thus this is also a location with high surface power density. The surface power density at a point $\bar{r}_1$ can be calculated by:

$$P_A(\bar{r}_1) = |J_S(\bar{r}_1)|^2 \cdot R_{\mathrm{SH}}. \tag{A.5}$$

The surface current density is denoted with J_S and the sheet resistance with R_{SH}. Typical chip-dimensions are in the millimeter range. For a suitable valuation the unit in this work for surface power density is W/mm²

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List of Published Work

First author:

(1) R. Reiner, P. Waltereit, B. Weiss, S. Moench, M. Wespel, S. Müller, R. Quay, and O. Ambacher, "Monolithically-Integrated Power Circuits in High-Voltage GaN-on-Si Heterojunction Technology," invited paper in *Proceedings of the 13th International Seminar on Power Semiconductors (ISPS'16)*, 2016, pp. 29-38, and selected for the *Special Issue on ISPS'16 of the IET Power Electronics Journal,* 2017.

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