TECHNISCHE UNIVERSITÄT DRESDEN

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Fakultät Elektrotechnik und Informationstechnik

Chair of Materials Science and Nanotechnology

Design and Layout of a Transimpedance Amplifier (TIA) at 50 GHz for Optical Receivers in IHP 130nm SiGe BiCMOS Technology

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Task Formulation for a Master Thesis

Student´s Name:	Lavakumar Navilipuri
Matriculation Number:	4821932
Studies:	Nanoelectronic Systems
Subject:	**Design and Layout of a Transimpedance Amplifier (TIA) at 50 GHz for Optical Receivers in IHP 130nm SiGe BiCMOS Technology**

Objectives of work

Optical fiber communication has emerged as a critical contributor to today's industrial development, economic progress, and modern society. Extending the bandwidth of analog front-end circuits for optical communications is critical to cope with the ever-increasing traffic. The transimpedance amplifier (TIA), acting as the electrical front-end of an optical receiver, is an essential block in optical communication systems.

In the Optical receiver, the photodetector converts incident light into a small photocurrent. The transimpedance amplifier (TIA) amplifies the current received from the photodiode to an adequate voltage level for the following stages. Front-end circuits for high-speed applications usually require the characteristics of low-noise and broad-bandwidth. With no exception, the TIA design entails many trade-offs between total input-referred noise, bandwidth, transimpedance gain, supply voltage, and power dissipation, presenting difficult challenges.

Focus of the work

This thesis focuses on the design and layout of a transimpedance amplifier (TIA) for optical receivers in IHP 130nm SiGe BiCMOS technology at a 50 GHz frequency range. The designed TIA should have a minimum transimpedance gain of 60 dBOhms, a minimum bandwidth of 40 GHz, and a maximum input-referred noise of 20 $pA/\sqrt{Hz}$. To achieve this, the following sub-tasks have to be followed:

- Literature review of state-of-the-art transimpedance amplifier (TIA) architectures.
- Comparison of different architectures will be used to decide on a certain topology.
- Designing the schematic in IHP 130nm SiGe BiCMOS technology.
- Designing the layout in IHP 130nm SiGe BiCMOS technology.
- The pre and post-layout results will be compared with one another alongside the theoretical considerations where ever possible.
- The performance will be measured against the state-of-the-art architectures.

Master thesis will be written in English.

Advisor:	Mr. Andy Heinig
1st Reviewer:	Prof. Dr. Gianaurelio Cuniberti
2nd Reviewer:	Assoc. Prof. (PD) Dr. Hans-Georg Braun

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Statement Of Authorship

I, Lavakumar Navilipuri, born on Nov 17th, 1994 in Telangana, India, hereby affirm that I have completed this thesis work on the subject of "Design and Layout of a Transimpedance Amplifier (TIA) at 50 GHz for Optical Receivers in IHP 130nm SiGe BiCMOS Technology" without the unauthorized help of third parties. The thesis work was done in collaboration between Fraunhofer IIS, Institutsteil EAS, Dresden and Technische Universität, Dresden. Thoughts taken directly or indirectly from external sources are marked as such. In selecting and evaluating the material and in preparing the manuscript, I received support from the following persons:

Mr. Andy Heinig, Fraunhofer IIS, Institutsteil EAS.
Assoc.Prof.(PD) Dr.Hans-Georg Braun, Technische Universität Dresden.

Additional persons were not involved in the intellectual preparation of the presented thesis work. I am aware that non-compliance with this declaration can lead to the subsequent withdrawal of the thesis.

Lavakumar Navilipuri.
Dresden, October 31, 2022.

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Abstract

Today's technology allows for a quick and efficient transmission of enormous amounts of data. Optical fibres are currently the most effective way to transmit enormous amounts of data. A photodiode (PD) generates current from the optical fibre's light to receive the data transmitted. However, this current is very small. It is necessary to use an amplifier that, in addition to amplifying the photodiode current, also converts it into a voltage for the optical receiver's subsequent phases. These amplifiers also referred to as transimpedance amplifiers, are an essential component of optical receivers because they must have a high gain to amplify the photodiode current and a large bandwidth to pick up high data rate signals.

This thesis thoroughly analyses these amplifiers, outlining the advantages and disadvantages of various topologies. This thesis uses mathematical equations to describe the operation of the Transimpedance Amplifier (TIA) and to identify the optimal range between the gain, the bandwidth, and the noise (input-referred noise) to produce the amplifier with the desired characteristics. Electrical simulations were used to test all the theoretical assertions and the entire system's behaviour for the four topologies of the common base, common emitter, regulated cascode, and darlington pair.

The minimum transimpedance gain target for the TIA is 60 dBΩ with a minimum bandwidth of 40 GHz. The designed TIA should have an input-referred noise of less than 20 pA/$\sqrt{\text{Hz}}$. After thoroughly examining these four topologies, a layout is designed for darlington pair TIA with resistive feedback. The implemented TIA has achieved a transimpedance gain of 63.74 dBΩ with a broad bandwidth of 60.84 GHz. The designed TIA has achieved a low input-referred noise of 16.20 pA/$\sqrt{\text{Hz}}$. The designed TIA has a chip size of just 0.0064 mm^2 and uses 30.53 mW of DC power.

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Abbreviations

ARPAnet	Advanced Research Projects Agency Network
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BCS, TYP, & WCS	Best-Case Scenario, Typical Scenario, & Worst-case Scenario
CB	Common Base
CE	Common Emitter
CC	Common Collector
CAGR	Compound Annual Growth Rate
CERN	European Council for Nuclear Research
DP	Darlington Pair
DRC	Design Rules Check
GHz & THz	Giga-Hertz & Tera-Hertz
Gbps & Tbps	Gigabit per second & Terabit per second
HBT	Heterojunction Bipolar Transistor
IRN	Input-Referred Noise
LED	Light-Emitting Diodes
LVS	Layout vs Schematic Check
M2M	Machine to Machine
MUX & DMUX	Multiplexer & Demultiplexer
PD	Photo-Diode
PEX	Parasitic Extraction
RGC	Regulated Cascode
RMS	Root Mean Square
SNR	Signal-to-Noise Ratio
TIA	Transimpedance Amplifier
TCP IP	Transmission Control Protocol Internet Protocol
Tx & Rx	Transmitter & Receiver

Symbols

V_{th}	Threshold voltage
nm	Nanometer
dB/km	Decibel per kilometer
V_{p-p}	Peak-to-Peak Voltage
μA	Micro Ampere
dBω	Decibel Ohm
pA/$\sqrt{\text{Hz}}$	pico Ampere per Square-root Hertz
C_{PD}	Photodiode Parasitic Capacitance
I_{PD}	Photodiode Current
fF	femto Farad
I_{in}	Input Current
V_{out}	Output Voltage
Z_{TIA}	Transimpedance Gain
f_c	Corner Frequency
K_F	Rollet Stability factor
S_{11}, S_{22}	Input and Output Reflection Coefficients
S_{12}, S_{21}	Reverse and Forward voltage gains
C_T	Total Capacitance
$V_{n,out}$	Noise Voltage
$I_{n,in}$	Input-referred Noise Current
R_C	Collector Resistance
I_C	Collector Current
g_m	Transconductance
p_n, z_n	Poles and Zeros
R_L	Feedback Resistor
R_E	Emitter Resistance
V_{CE}	Emitter Voltage

Contents

Chapter 1

Introduction

The modern internet is powered by the TCP/IP protocol, which was shifted from ARPAnet (the internet's predecessor) in January 1983, enabling various types of computers on different networks to communicate. The sudden popularity of the World Wide Web and the dot-com bubble in the late 1990s caused a global leap in information access and diffusion, both in the commercial and domestic sectors, resulting in the information age and an economy based on information technology. Enterprises in various domains have begun to explore the possibilities of capitalizing on this new paradigm and can now communicate easily with their employees, customers, and associates, leading to a rise in the number of users and the diversification of connected devices (PCs, tablets, TVs, smartphones). This increase in global internet traffic is explained in the Cisco Annual Internet Report (2018-2023) [1]. Figure 1.1 forecasts a rise of 10% Compound Annual Growth Rate (CAGR) for devices and connections from 2018 to 2023. Every year, plenty of new devices with enhanced capabilities and intelligence are introduced and adopted in the market. A growing number of Machine to Machine (M2M) applications, such as smart meters, video surveillance, healthcare monitoring, transportation, and package tracking, contribute significantly to the growth of devices and connections. This scenario necessitates one thing to provide a satisfactory user experience: higher data transfer rates. The global internet system's data rate must be increased from tens of Gbps to Tbps. This means that bandwidth requirements will increase by more than a factor of 100. Such data rates necessitate using low-loss, high-bandwidth media [2]. Out of all the available communication mediums in the market, optical fibres have the best data transfer performance.

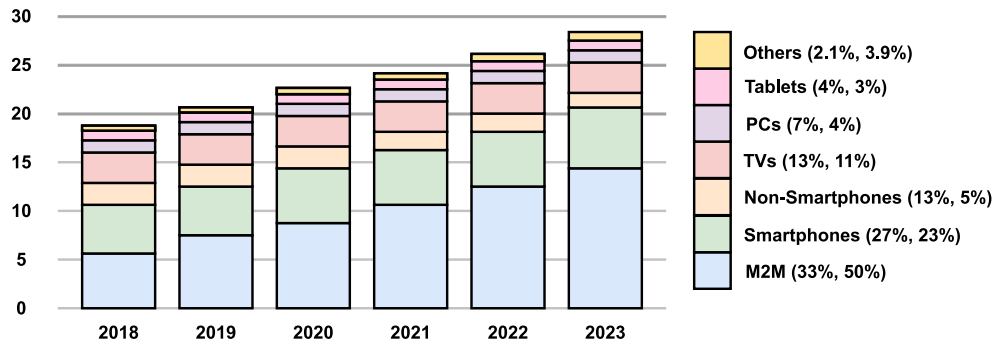

Figure 1.1: Cisco forecast for global device and connection growth (2018-2023) [1].

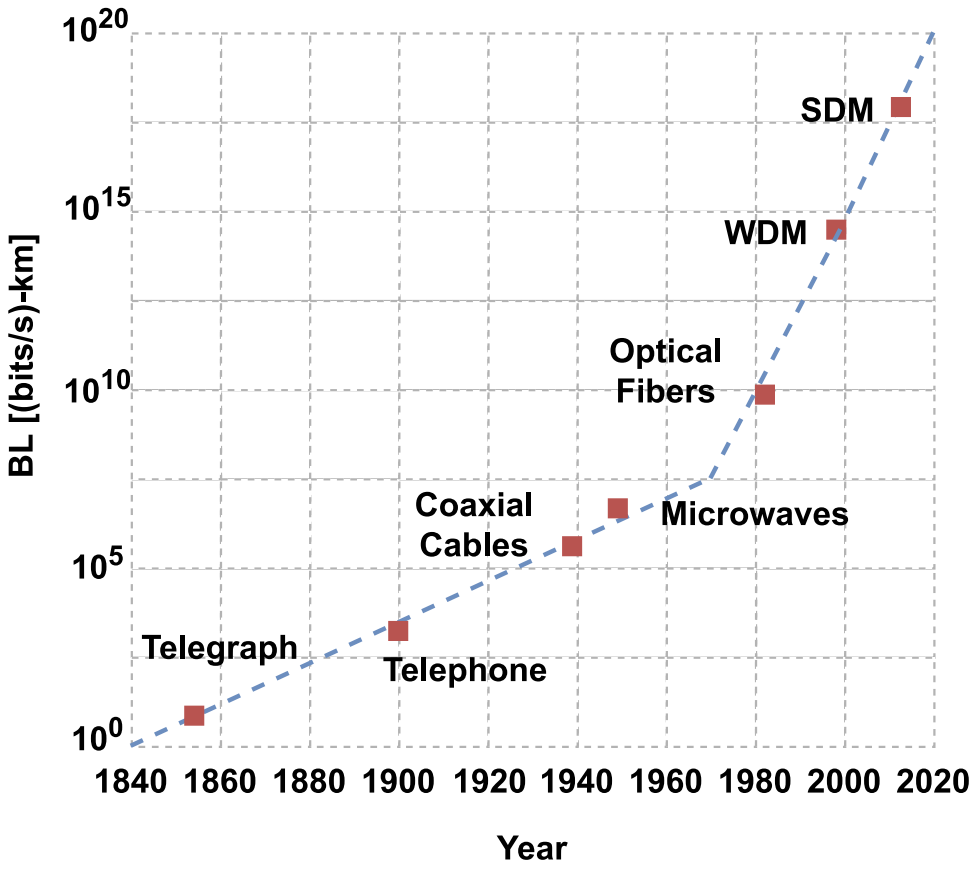

Figure 1.2: Historical increase in the B·L product with new technologies [3].

Optical fibre communication technologies are the driving force behind this expansion. Figure 1.2 depicts how the product of bit rate and signal repeating distance (B.L product) has increased by a factor of 10^{18} as new technologies have emerged [3]. The change in slope that occurred around 1980, when optical fibres were first introduced, is evident. Optical fibre cable is lighter and thinner than electrical wiring, has higher bandwidth, lower loss, and is resistant to electromagnetic interference and crosstalk. With less than 0.2 dB/km attenuation around the emission wavelength of 1550 nm, it allows for data transmission up to terabits per second over thousands of kilometres [4].

1.1 Fibre Optical Communication

With the advent of multimedia technologies mentioned above, the communications sector has increasingly emphasised high-speed data transfer. There are several hurdles to high-speed electronic data communications, including low bandwidth of metallic mediums, cross-talk generated by magnetic induction, and susceptibility to static and Radio Frequency (RF) interference. Data transfer with glass and plastic Fibre optic cables is an alternative to traditional metallic or coaxial cable facilities. Fibre optics provide a high bandwidth medium with none of the limitations associated with electronic data transfer [5]. GTE (General Telephone and Electronics) and AT&T (American Telephone & Telegraph) introduced the first Fibre optic telephone system in 1977. Since then, the rising volume and speed of data transmission

across optical Fibres have transformed how people communicate and conduct business [6]. Optical-Fibre cables now carry more than 80% of the world's long-distance voice and data traffic.

In July 2021, researchers broke the internet transmission speed record [7]. World is One News, WION, reported [8]:

> National Institute of Information and Communications Technology (NICT) researchers from Japan have broken a world record for the fastest internet speed, measuring 319 Terabytes per second for a 3,001-kilometer long-distance data transfer. The previous record was set by University College London researchers, who obtained 178 Terabytes per second. The attained 319 Terabytes per second speed is a high-speed internet connection. According to the researchers, the technology can be used to upgrade existing data transmission models and enable the speeds claimed by 5G, which is not yet accessible everywhere.

The primary goal of an optical communication network is to transmit light pulses from a transmitter to a receiver via an optical Fibre. As illustrated in Figure 1.3, a basic optical communication system consists of three major components: a transmitter block, an optical Fibre, and a receiver block [9].

- The transmitter generates the optical signal by converting the electrical signal to optical information through light pulses. The transmitter comprises an optical emitter and the current drive circuitry that goes with it. The most common optical emitters are light-emitting diodes (LEDs) and laser diodes.
- Optical Fibre delivers optical data over long distances.
- The light pulses received from the optical Fibre are converted back to electrical current pulses by the receiver. The receiver mainly comprises an optical detector and the corresponding amplification circuitry. The receiver employs a photodiode (PD) as an optical detector to convert incoming light pulses to current.

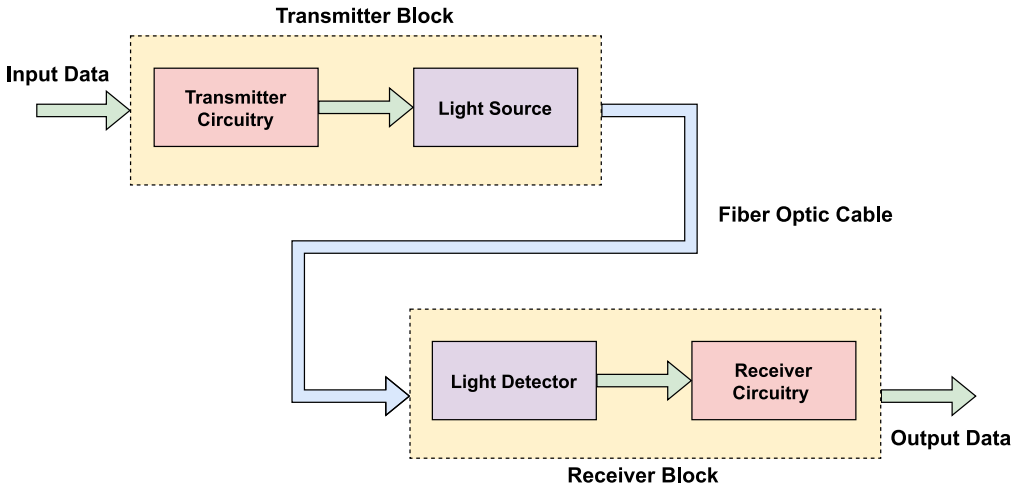

Figure 1.3: Basic blocks of Fibre Optic Communication System

1.2 Optical Transceivers Overview

Like any other communication system, a Fibre-optic transceiver consists of a transmitter, a transport medium, and a receiver. The foundational block diagram of an optical transceiver is shown in Figure 1.3. Because the transmission medium is an optical Fibre rather than a copper wire (used in wired communications), the digital signal should switch from electrical to optical and vice-versa. Optical transmitters (Tx) and receivers (Rx) are required to perform this task. An optical transmitter transforms an electrical analogue or digital signal into an optical signal. Data is serialized in the optical transmitter before being transmitted through the optical channel to achieve high-speed data rates with a small number of channels. A light-emitting diode or a solid-state laser diode can generate the optical signal. Optical transmitters' most common operational wavelengths are 850, 1300, or 1550 nm. One or more glass Fibres act as optical signal waveguides in the Fibre optic cable. Depending on the absorbed light intensity, the optical receiver turns the optical signal back into a replica of the original electrical signal. The optical signal detector is either a PIN-type photodiode or an avalanche-type photodiode. LEDs and PDs are often employed on separate modules due to integration issues with the back-end circuitry of the transmitter and receiver sides. The receiver is the most complex of the three components of an optical communications system to design. Even though an optical receiver comprises several functional blocks, our focus in this study is on the receiver's front-end design, which includes the TIA.

1.2.1 Optical Transmitters

The block diagram of a typical optical transmitter is shown in Figure 1.4. The multiplexer (MUX) on the transmitter side combines the N-bit parallel data from the digital logic component at a lower data rate into a serial data stream operating at a higher data rate. The parallel data is picked using MUX and retimed using a re-timer circuit and a bit-rate clock generated by a frequency synthesizer. This serial data is amplified to the precise swing required to drive an optical modulator with a high enough extinction ratio. The extinction ratio is the ratio of logical "1" optical power to logical "0" optical power that determines the optical link's maximum signal-to-noise ratio (SNR). An envelope similar to electrical serial data is used to modulate the optical carrier. A laser driver or modulator driver uses this high-speed serial data stream to control the associated optoelectronic device (typically a laser diode). The laser driver modulates the current of a laser diode (LD), and the power control circuit adjusts the laser's light intensity [10] [11].

For a better understanding, consider the Optical Carrier 768 (OC-768) transport system. A 16:1 multiplexer (MUX) in an OC-768 optical transport system combines sixteen parallel 2.5 Gb/s electrical signals to a 40 Gb/s serial data, which is retimed by a frequency/clock synthesizer. The data rate of the OC-768 system is 40 Gb/s, while the IEEE 802.3ba Ethernet standard operates at around 40 Gb/s, which combines four parallel 10 Gb/s signals to a 40 Gb/s serial data [12] [13]. The laser diode's light signal stream is attached to optical Fibres for transmission. Before the light signal reaches the electrical receiver, it is usually amplified by an expensive Erbium-Doped Fibre-optical Amplifier (EDFA) to account for transmission loss in long-distance optical transmission systems. The optical wavelength typically em-

ployed for such long-distance transmission is 1550 nm, which has low attenuation and good efficiency for EDFA. However, EDFA is absent in cost-sensitive short-reach optical communication systems, and low-cost 850 nm optoelectronic devices are extensively used.

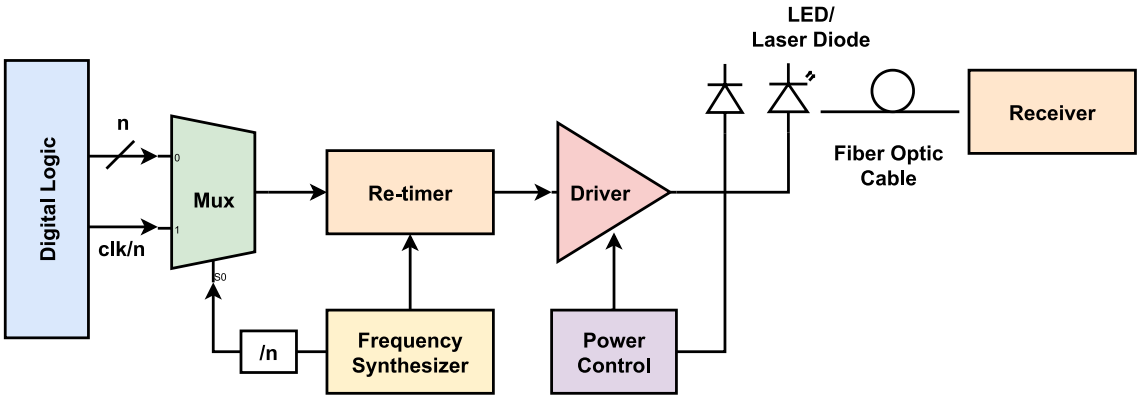

Figure 1.4: Front-end diagram of a typical optical Transmitter

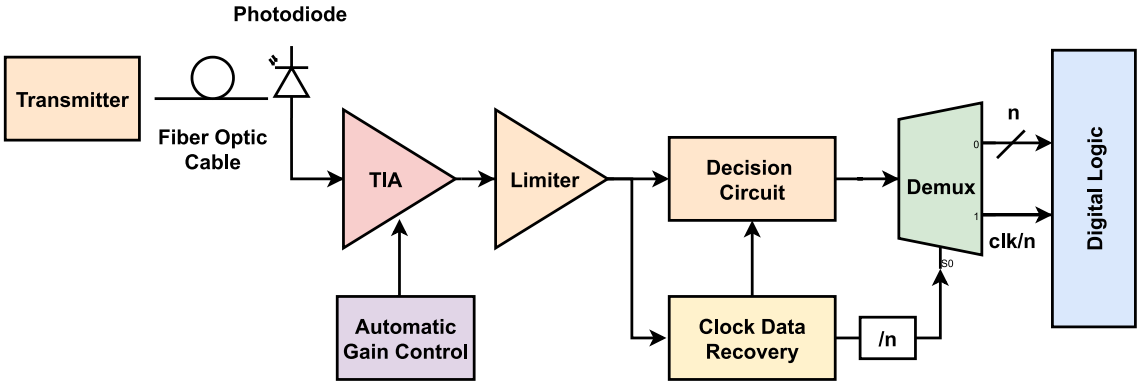

Figure 1.5: Front-end diagram of a typical optical receiver

1.2.2 Optical Receivers

The envelope information received at the optical Fibre's output end should be demodulated back into the original electrical signal and then to digital values by the receiver. Figure 1.5 depicts a typical optical receiver system block diagram. The optical signal attenuates as it travels from one end to the other due to long or low-quality optical Fibre, and a large portion of the optical power is lost. As a result, auxiliary building blocks must be provided before transforming the signal into digital logic to improve performance [14].

In a typical optical receiver, A photodetector or photodiode (PD) converts the incoming optical signal to a small output current proportionate to the input optical power based on the diode responsivity. The ratio of output current produced for a given input power is defined as responsivity. The responsivity of many photodiodes ranges between 0.8 A/W and 1 A/W.

As the first building block after the photodiode, the transimpedance amplifier (TIA) amplifies electrical current with adequate bandwidth, transforming it to volt-

age with as little noise as possible. The transimpedance amplifier should have low-noise and wide-band capabilities to amplify the small current to voltage with a high signal-to-noise ratio (SNR) and with the least amount of intersymbol interference (ISI) [15]. As a result, TIA is, without a doubt, the most significant building block of the optical receiver. This block's design requires numerous noise, bandwidth, gain, and stability trade-offs. The TIA is distinguished by its specification of a low input impedance necessary to absorb current from the photodiode. It should also have a large transimpedance, determined by converting the input current to an output voltage. In most cases, a single TIA stage is insufficient to amplify the input current to detectable logic levels (approximately 500 mVp-p).

Depending on the complexity of the modulation system, the TIA is frequently followed by either a limiting amplifier or a linear amplifier. The voltage signal from the TIA's output is enhanced further by a limiting amplifier (LA) and/or an automatic gain control (AGC) amplifier. The limiting amplifier and automatic gain control amplifier are collectively known as post amplifiers. For the signal to be delivered to the clock and data recovery (CDR) circuit, a limiting amplifier should have a high gain and a large output voltage swing [16]. The TIA and limiting amplifier make up what is generally called the analogue front end of the optical receiver.

A decision circuit removes noise from the received signal after it has been amplified to detectable logic levels. The decision circuit recovers a digital value from the received analogue signal. When the signal swing is large, the decision circuit probabilistically recovers the correct digital value. The decision circuit is timed by a CDR, which samples the serial digital data and recovers a clock signal from the incoming serial data via retiming [17]. The clock controlling the decision flip-flop must have a well-defined phase connection with the received data for the signal to be sampled at the optimal point during the bit period.

In the receiver (Rx), the demultiplexer (DMUX) is required to reconstruct the received serial data stream to the original parallel channels. As a result, a DMUX converts the incoming high-speed serial data stream into an N-bit bus capable of supporting electronic interconnects and digital processing. After recovering the electrical bus, digital signal processing blocks decode the bits, run error checks, and extract the payload data from the framing information [14].

1.3 Goal and Approach of this Thesis

As stated in the above section, TIA is, without a doubt, the most crucial building block of the optical receiver. This block's design necessitates noise, bandwidth, gain, and stability trade-offs. This thesis focuses on developing a transimpedance amplifier for the next generation of optical receivers using several nodes of IHP's SiGe: G2 BiCMOS technology. This thesis seeks to reveal the complications and challenges experienced when constructing differential TIA with high gain, wide bandwidth, and low noise.

The photodiode's peak-to-peak output current is 11.25 μA, as illustrated in Figure 1.6. Because the TIA output voltage signal amplitude required for data recovery is several hundred millivolts, a high transimpedance gain of 60 dBΩ is aimed. Because of the TIA design's stringent noise and bandwidth constraints, the remaining gain must be performed at the post-amplifier. This thesis also includes a thorough

examination of the noise characteristics of TIAs. Because TIA is the first block in retrieving noisy data, the goal is to keep the noise in this block as low as feasible. The goal is to create a TIA with a differential input referred noise less than 20 pA/SqrtHz. Broad bandwidth is another trade-off in TIA implementation. A bandwidth of 40 GHz is desired. Another approach to eliminating common-mode noise and achieving wide bandwidth is using a differential topology.

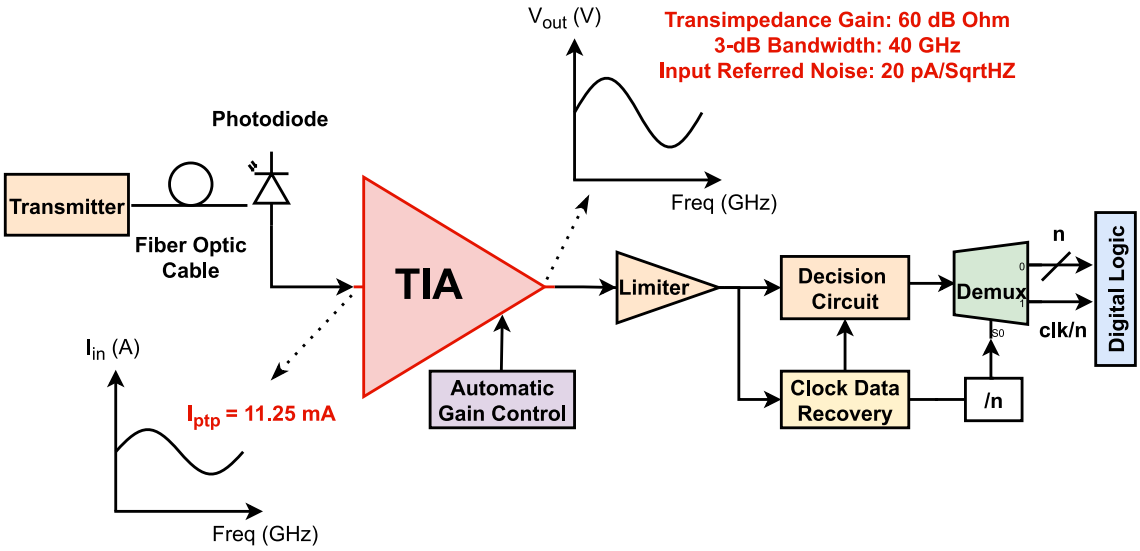

Figure 1.6: Required specifications for TIA design.

Based on this goal, the following are the detailed contributions of this thesis:

- State-of-the-art research will be conducted to assess the performance of various topologies.
- A theoretical examination is to be done of all topologies in terms of transimpedance gain and input-referred noise.
- Schematic design of the best-performing topologies based on the theoretical study.
- After the theoretical and schematic study, develop the layout of one of the best-performing topologies.
- The selected TIA's performance will be compared to the state-of-the-art.

1.4 Thesis Structure

This project investigates the realization of a transimpedance amplifier designed in IHP SiGeG2-BiCMOS technology using cadence virtuoso software. As seen above, this chapter explains TIAs importance and which objectives are pursued with the design of a TIA. The flow chart shown in figure 1.7 gives a brief idea of how each chapter helps select the required topology for designing the TIA.

Chapter 2 discusses the four state-of-the-art topologies possible for TIA design (i.e., common base (CB), common emitter (CE), regulated cascode (RGC), and

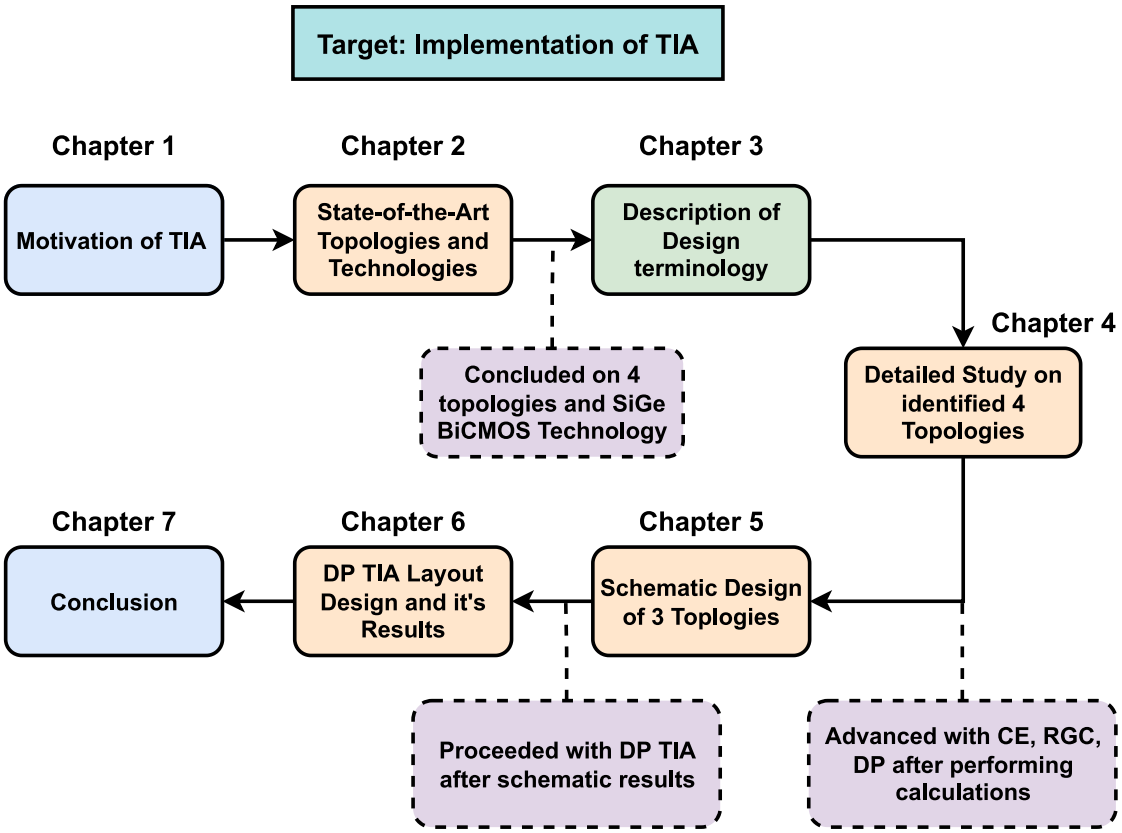

Figure 1.7: Thesis Structure

darlington pair (DP)). This chapter also explains why SiGe-HBT-BiCMOS process technology is advantageous over others on the market. The presented literature review allows putting the contributions of this thesis work into a broader context.

Chapter 3 explains the figure of merits that are considered when designing the TIA. The terminology from this chapter can be encountered throughout the thesis.

Chapter 4 details the basic working of the decided four topologies and their performance compared to each other according to the calculations. It will be clear why common base topology won't be investigated further after reading this chapter.

Chapter 5 describes the schematic design of the TIA in SiGe BiCMOS technology using cadence virtuoso. The schematic design is presented for three topologies (i.e., CE, RGC, DP), followed by their simulation results. Hence after this chapter, why darlington pair topology is selected for layout design can be understood.

Chapter 6 shows the layout of the darlington pair TIA with resistive feedback, followed by its post-layout improvement and outcomes. The findings of the layout are then compared to those of the schematic. The TIA's performance metrics, including transimpedance gain, 3-dB bandwidth, and input-referred noise, are assessed and contrasted for both the schematic and the layout.

Chapter 7 finally gives us the conclusion of this thesis, the comparison of the designed TIA with state-of-the-art topologies, and the future scope of the work.

Chapter 2

Literature Review

This chapter begins with a study of the literature on several state-of-the-art topologies. The list of topologies that can meet the TIA's performance requirements will be finalized using the results of this assessment. This is followed by a description of the state-of-the-art 130 nm SiGe BiCMOS technology that was used to design TIA.

2.1 State-Of-The-Art

A thorough literature review was performed to establish the current state of the field. The review's main objective was to find a preferred topology for the TIA's design. This thesis aims to design a TIA with a transimpedance gain of 60 dBΩ, a bandwidth of 40 GHz, and a differential IRN of 20 pA/$\sqrt{\text{Hz}}$, as stated in section 1.3. Hence, the topologies that are evaluated in this section are compared with each other for the above-targeted specifications. In chapter 4, the design concepts gleaned from the literature review are thoroughly covered.

A common base TIA with low input-referred noise of 14.5 pA/$\sqrt{\text{Hz}}$ and a maximum gain of 71 dBΩ has been proposed by Zhen Zhang [18]. A bandwidth of 31 GHz has been attained using this topology. The proposed TIA was manufactured using SiGe BiCMOS technology at 130 nm. A modified variable-gain amplifier with automatic gain control is used to achieve a significant gain. The circuit now uses more space and power as a result.

A differential common emitter TIA has been implemented by García López [19] in a 130 nm SiGe:C BiCMOS technology with an f_t/f_{max} = 300/500GHz. This common emitter topology has a transimpedance gain of 62.5 dBΩ, a bandwidth of 60 GHz, and an IRN of 5.46 pA/$\sqrt{\text{Hz}}$. A resistive feedback resistor is used to increase the gain and bandwidth. Because of the low input impedance that this resistive feedback resistor achieved, the TIA's performance was enhanced. The thermal noise of this additional resistor causes a decline in the TIA's noise performance.

Joseph S. Weiner [20] used the same common emitter topology and resistive feedback to implement a TIA. Here, a fully differential SiGe TIA suitable for differential phase-shift keying applications has been described. This TIA has an input-referred current noise of less than 30 pA/$\sqrt{\text{Hz}}$, a 50 GHz 3-dB bandwidth, and a transimpedance gain of 49 dBΩ. The additional emitter follower circuit, which serves as a buffer, is then connected to the differential output stage. The bandwidth has improved as a result of this connection. As the bandwidth increased, the gain de-

creased, and the noise increased.

To design the TIA, Kentaro Honda [21] used the common emitter topology with resistive feedback. In this implementation, a level-shift circuit is positioned between the TIA and a post-amplifier stage which lessens the overall system's trade-off between bandwidth and noise. IRN is decreased by 70%. The designed TIA was produced using SiGe BiCMOS technology at 130 nm. The TIA has achieved input-referred noise of 14.8 pA/$\sqrt{\text{Hz}}$, a 3-dB bandwidth of 38.4 GHz, and a transimpedance gain of 72 dBΩ.

To illustrate the TIA, Garca López [22] uses regulated cascode topology in 250 nm SiGe:C BiCMOS technology with f_t/f_{max} = 110/180GHz. The results show an input-referred noise of 13.1 pA/$\sqrt{\text{Hz}}$, a 3-dB bandwidth of 32 GHz, and a transimpedance gain of 52.5 dBΩ. Low input impedance from a common emitter topology and a resistive feedback resistor, as demonstrated in the authors' earlier paper [19], reduces the impact of photodiode capacitance on bandwidth. The additional resistor's noise trade-off was present. Here, a cascode configuration is used to reduce this trade-off and increase bandwidth even without the use of a resistive feedback resistor. As a result, the circuit's noise won't impact; however, the voltage supply is increased to make room for the cascode topology's stacked transistors.

In 130 nm SiGe BiCMOS technology, S. Bashiri Amid [23] implemented a broadband differential TIA. The large parasitic capacitor of the photodiode has been lessened by using a regulated cascode configuration. The TIA has a measured bandwidth of 28 GHz and a 53.6 dBΩ differential transimpedance gain. An Integrated IRN of 36.5 pA/$\sqrt{\text{Hz}}$ was measured. Three stages of buffer circuits follow the designed TIA for better performance. The additional buffer circuits cause the chip's overall power consumption to increase to 110 mW.

Using IBM8HP 130 nm SiGe BiCMOS technology and a 240/200 GHz f_t/f_{max}, Ran Ding [24] has demonstrated a power-efficient, low-noise, and broadband TIA. The paper employs a resistive feedback topology with a darlington pair. The circuit uses only 89 mW of DC power and has a transimpedance gain of 55 dBΩ, an 86 GHz bandwidth, and an input-referred noise of 20.4 pA/$\sqrt{\text{Hz}}$. The designed circuit consists of three cascaded stages: an input transimpedance stage called a shunt-feedback darlington amplifier, a buffering emitter follower, and an output stage called a cascode transadmittance stage.

For the single-ended TIA design, André F. Ponchet [25] used the darlington pair topology with resistive feedback. The TIA has a transimpedance gain of 50.5 dBΩ, a bandwidth of 42 GHz, and an input-referred noise of 12 pA/$\sqrt{\text{Hz}}$. Darlington pair circuits in two stages are used to achieve these TIA performances.

Using cascaded stagger-tuned stages that are equalized for high bandwidth and low gain ripple, Joohwa Kim [26] developed a broadband amplifier. A constructive wave amplifier and a darlington feedback amplifier illustrate the staggered stages. The designed amplifier is implemented in a 120 nm SiGe BiCMOS process and, with the entire circuit, achieves a 3-dB bandwidth of 102 GHz. A transimpedance gain of 47 dBΩ, a 3-dB bandwidth of 53 GHz, and input-referred noise of 14.8 pA/$\sqrt{\text{Hz}}$ are all achieved by the TIA component in the designed amplifier.

We have seen four different topologies for implementing the necessary TIA. They consist of a common base, a common emitter with resistive feedback, a regulated cascode, and a darlington pair with resistive feedback. A concise table 2.1 compares the findings from the state-of-the-art papers mentioned. These implementations

Table 2.1: Comparison of State-of-the-Art TIA Circuits

Reference	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]
Technology	130nm SiGe BiCMOS	130nm SiGe:C BiCMOS	SiGe BiCMOS	130nm SiGe BiCMOS	250nm SiGe BiCMOS	130nm SiGe BiCMOS	130nm SiGe BiCMOS	130nm SiGe BiCMOS	120nm SiGe BiCMOS
Topology	CB	CE RSF	CE RSF	CE RSF	RGC RSF	RGC RSF	DP RSF	2 stage DP RSF	DP RSF
Input-Output	Pseudo-Diff	Diff-Diff	Diff-Diff	SE-SE	Diff-Diff	Diff-Diff	SE-SE	SE-SE	SE-SE
Frequency (GHz)	30	55	40	30	50	30	50	-	40
Transimp. Gain (dBΩ)	71	62.5	49	72	52.5	53.6	55	50.5	47
Bandwidth (GHz)	31	60	50	38.4	32	28	86	42	53
IRN ($pA/\sqrt{Hz}$)	14.5	5.46	30	14.8	13.1	36.5	20.4	12	53.9
Output Matching (dBm)	-20	-10	-12	-	-10	-15	-19	-25	-8
Peaking/Buffers	yes	yes	yes	yes	yes	yes	yes	no	no
DC power cons. (mW)	300	85	200	261	70	110	89	45	73
ft/fmax (GHz)	-	300/500	170/140	-	95/140	160/-	200/240	-	200/-
Chip size (mm^2)	0.54	0.3	0.92	0.2	0.32	0.56	0.28	0.23	0.29

have used extra circuitry, such as peaking or buffering circuits, for increasing gain, bandwidth, and noise immunity. There is a noticeable increase in the amount of space or power consumed due to additional circuits. Therefore, our goal is to choose a topology that can deliver the TIA performance we need without the addition of a second circuit. In chapter 4, these four topologies are covered in more detail. The targeted TIA in this thesis should be implemented in 130 nm SiGe HBT BiCMOS technology; the next section will concentrate on this technology.

2.2 130 nm SiGe HBT BiCMOS Technology

To encode the optical carrier reliably in a transceiver, drivers capable of high-speed broadband operation while generating large output swings are required on the Tx side. On the Rx side, low-noise, high-speed devices with wide bandwidth are preferred. The fibre communication system's massive data transfer potential is virtually unfulfilled because establishing a broad bandwidth is constrained by the speed of front-end circuits. As a result, their design is the most crucial aspect of optical transceiver design. The fundamental goal of this thesis research is to investigate, design, and build a front-end transimpedance amplifier of an optical receiver employing cutting-edge SiGe bipolar technology. This section explains the semiconductor technologies used in optoelectronic applications and why SiGe HBT BiCMOS is the best option among them.

Commercial optical communication products are often implemented in III-V compound semiconductor technologies such as gallium arsenide (GaAs) [27] and indium phosphide (InP)[28], which provide extremely high performance but are not appropriate for cost-sensitive mass-market applications. For lower-cost silicon implementations, two key alternatives remain: CMOS and SiGe. Because of its scaling techniques, CMOS has been employed for many applications over the years. By reducing the gate length, the current gain frequency is continuously increased. These applications operate at frequencies in the tens of gigahertz range [29]. Technology is currently heading into the terahertz (THz) realm, where many new applications demand faster CMOS transistors. Although CMOS is commonly employed for low-frequency applications, SiGe technology has long been regarded as the gold standard for sub-Terahertz and mm-wave applications. CMOS has cost and power dissipation advantages. Still, at a comparable lithography node, it has lower breakdown voltages and worse noise characteristics than SiGe HBTs, which dramatically penalizes circuit performance [30]. As shown in Figure 2.1 [31], the TIA reported in this study is implemented in 130nm IHP SiGe BiCMOS, which provides a good trade-off between high-frequency device performance and manufacturing costs.

Compared to RF CMOS, which achieves a unity gain f_T of around 200GHz in the 65nm node, SiGe HBT BiCMOS reaches the same value in the 250nm node. As a result, the fabrication costs are reduced for the same performance. SiGe BiCMOS offers more than double the performance of CMOS at the same price [32]. The 130nm SiGe HBT BiCMOS technologies used in the design of this TIA have an available back-end line stack of eight metal layers, with five thin and three thick metal stacks. Four thin metal layers and two large metal layers are based on 130nm design criteria, and the final two top metal layers, with thicknesses of 2.8 μm and 0.6 μm, are suited for constructing RF passive components.

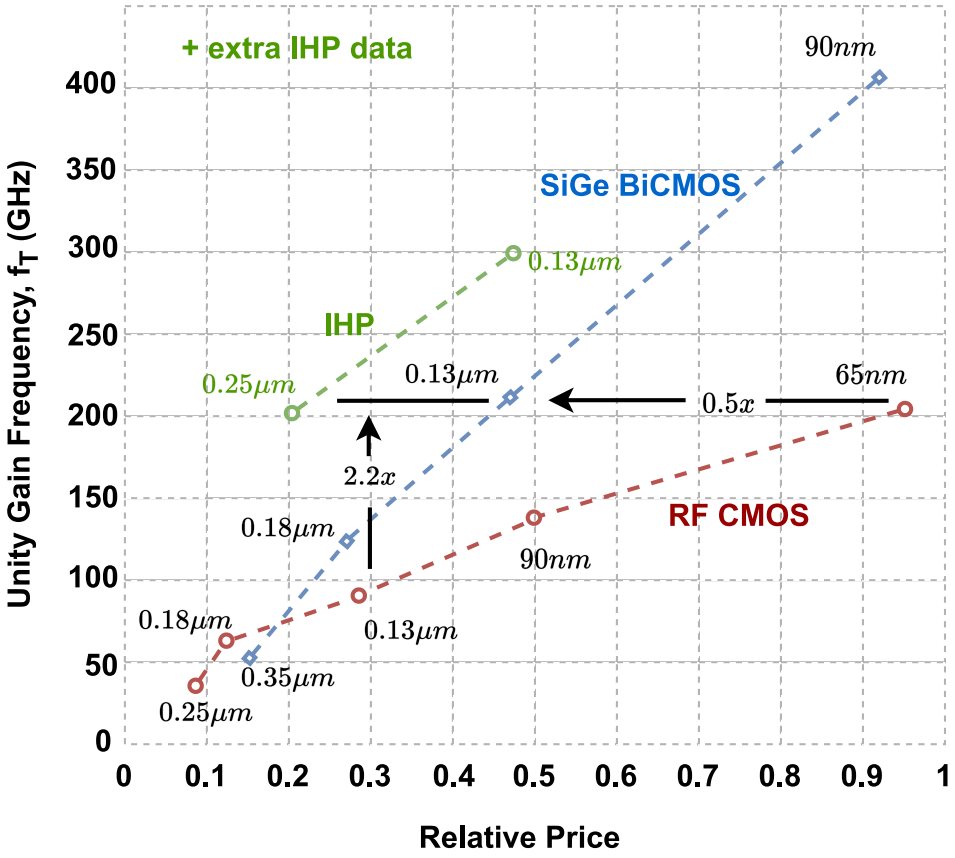

Figure 2.1: Comparison between BiCMOS and CMOS technologies with respect to RF performance vs cost [31].

Operation

A heterojunction bipolar transistor (HBT) is a high-performance silicon technology than that of conventional silicon bipolar and silicon CMOS. HBT is formed by adding Ge composition in the base region of a bipolar junction transistor (BJT). While maintaining the properties of the BJT, incorporating Ge into the base of the device introduced several other benefits by changing the base bandgap of SiGe HBTs [33]. The bandgap is reduced due to compressive strain in the material when Ge is added to the silicon crystal lattice (the Ge atom requires a larger atomic separation than the Si atom). In SiGe HBT technology, the Ge content is inconsistent throughout the base. Instead, it increases as we move deeper into the collector from the emitter, thus reducing the bandgap in the direction of electron flow, as shown in Figure 2.2 bottom. When the electrons are injected from the emitter, they experience a reduced barrier to injection because of the smaller Ge content at this junction. Then the electrons experience an accelerating field from the increasing Ge content towards the collector, as shown in Figure 2.2 top, increasing the transportation speed of the electrons in the device, thus, higher operating frequency. Higher current gain can be achieved by increasing the base doping concentration and reducing the emitter doping concentration. Thus, the base resistance, maximum oscillation frequency, noise figure, base-width modulation effect, and emitter bandgap narrowing effect are greatly improved [34]. Compared with an identically constructed Si BJT, a higher gain, lower RF noise, and low 1/f noise can be achieved with SiGe HBT.

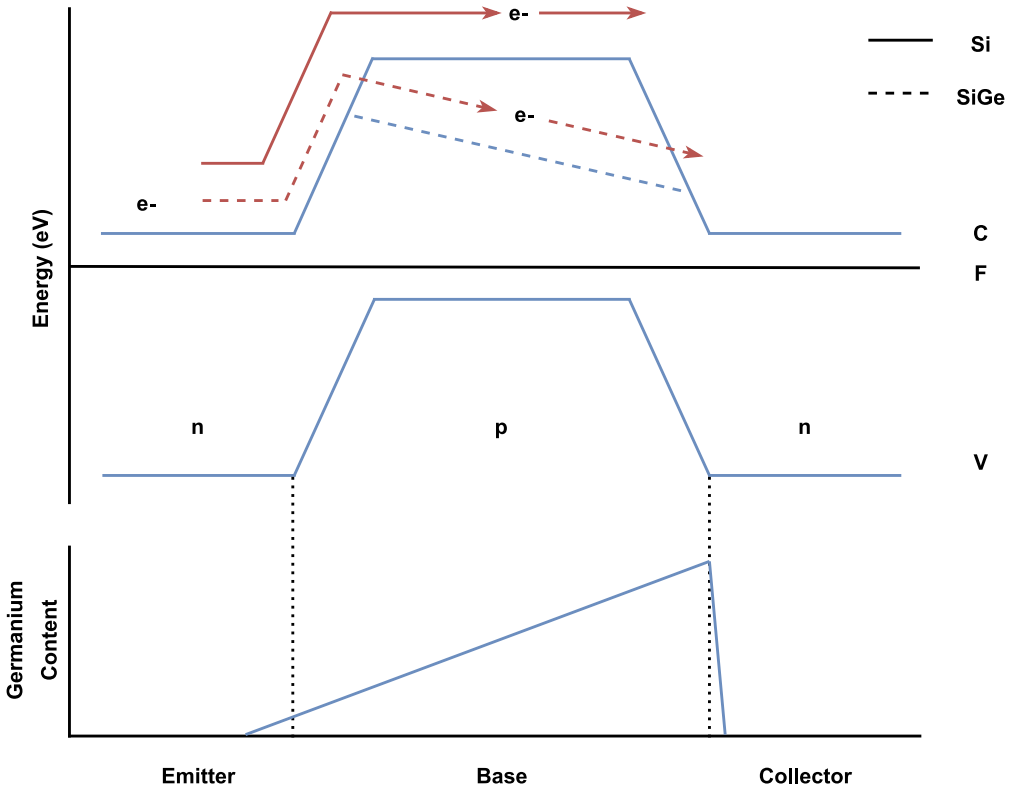

Figure 2.2: Ge concentration (bottom) and band structure (top) of a SiGe heterojunction bipolar transistor.

Comparison of Different SiGe Process Foundries

In the last decades, the transit frequency has continuously increased, with special attention paid to the f_{max}. For example, IHP has developed its 2nd generation 130 nm technology SG13G2 with f_T/f_{max} = 300/450 GHz from its predecessor 130nm technology with f_T/f_{max} = 250/340 GHz. Table 2.2 shows the Peak transit frequencies for different high-speed SiGe HBT technologies.

In this project work, IHP SG13G2 BiCMOS technology is used for designing the TIA. As shown in Table 2.2, it offers a much higher bipolar performance of f_T/f_{max} = 300/450 GHz when compared with other technologies. It has the state-of-the-art SiGe BiCMOS transistors that produce an ultra-fast, low-noise, low-power consumption amplifiers compared to its competitors.

Table 2.2: Peak transit frequencies for different high-speed SiGe HBT technologies.

Company	Process	CMOS Node (nm)	f_T (GHz)	f_{max} (GHz)
IBM [35]	8HP	130	200	270
STM [36]	B9MW	130	230	290
IHP [37]	SG13S	130	250	340
IFX [38]	B11HFC	130	250	370
IHP [39]	SG13G2	130	300	450

Chapter 3

Design Considerations

The TIA, which serves as the optical receiver's electrical front end, is a critical component in optical communication systems. With the PD, it is crucial to determine the optical link budget, such as the system's gain, bandwidth, and losses. Front-end circuits for high-speed applications typically demand high gain, low noise, and broad bandwidth. The TIA design necessitates numerous trade-offs between noise, bandwidth, gain, dynamic range, supply voltage, and power consumption, posing complicated issues, particularly when BiCMOS technology is used. This chapter will give a clear understanding of the design considerations before implementing the TIA. At the start of the chapter, the operation of photodetectors and how the photodiode parasitic capacitance C_{PD} affects the TIA design are explained. TIA's important performance features, like gain, bandwidth, noise, etc., are discussed. The terms defined in this chapter will be used frequently in the coming chapters while designing a TIA.

3.1 Photodetectors

The photodetector at the front end of the optical receiver, is a circuitry which senses incoming light pulses and converts them into transform time-varying electrical signals [40]. Since PD is a square law device, the detected electrical current is proportional to the power of the incident optical signal. When a PD is exposed to an incident light, the photons that impact the junctions cause covalent bonds to break, and generating holes and carriers in depletion region. The electric field in the depletion region allows the loose electrons to migrate to the n side and holes to the p side, resulting in current flow across the junction [41]. The current generated by the PD is voltage independent, but proportionate to the incident light. In most optical detection applications, the response speed of the detector is critical, and is determined by the carrier diffusion time. As a result, Photo-generated minority carriers must diffuse to the junction and be swept to the opposite side quickly.

The overall current generation in a PD is explained below using P-type-Intrinsic-N-type (PIN) diodes are the leading contenders for optical receiver applications [5]. PIN diode comprises of a p-n junction with an intrinsic (undoped or lightly doped) semiconductor layer sandwiched between the p and n-doped materials. Light hits this intrinsic or depletion region, which is thick enough to absorb nearly all photons. The majority of photons are absorbed by electrons in the valence band of the atoms

in the intrinsic material. Photon absorption gives electrons enough energy to jump from the valence band into the conduction band, resulting in electron-hole (E-H) pairs. The presence of a strong electric field in the depletion area is caused by reverse biased p+ and n+ regions. Due to strong reverse polarization, the E-H pairs are separated and gathered at the edges of the depletion region [14]. As a result, photocurrent I_{PD} is detected at the diode terminals.

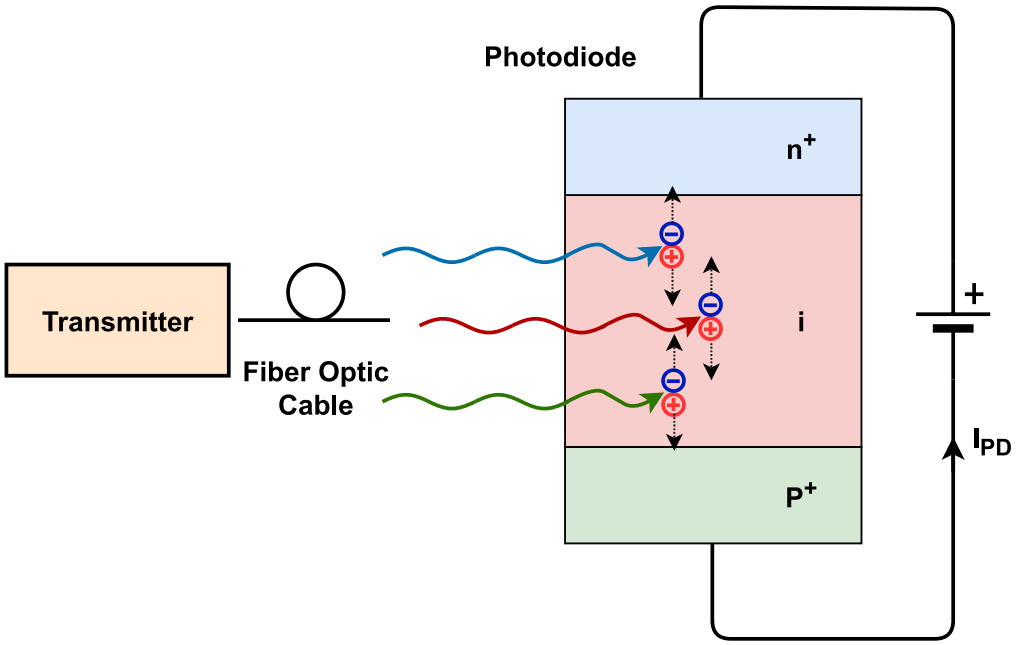

Figure 3.1: PIN Photodiode.

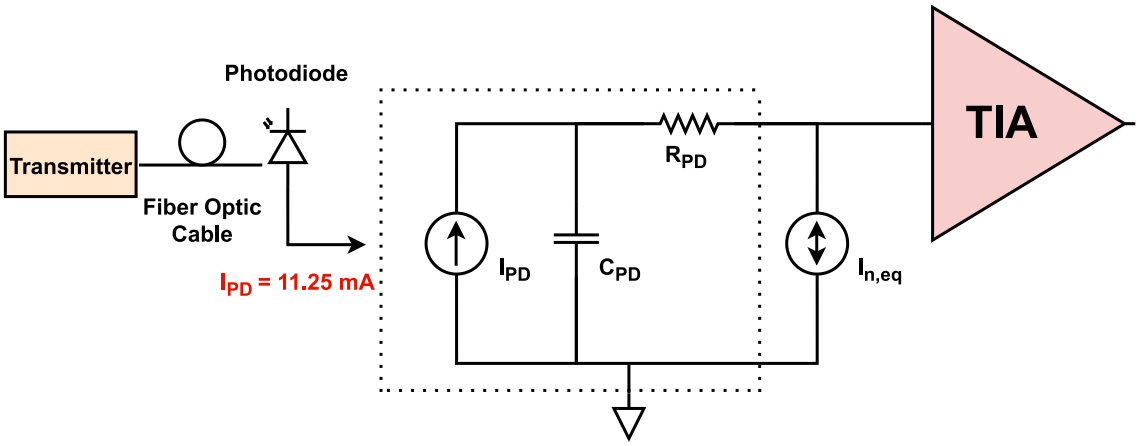

Figure 3.2: Basic receiver front-end model [15] showing the input impedance and noise component $I_{n,eq}$ added to the TIA by PD. Dotted box is a small signal equivalent circuit of a photodiode.

Figure 3.2 depicts a basic photodetector's equivalent small signal circuit, where the current source represents the incident light current, which is 11.25 mA. The main parasitics are the photodiode junction capacitance C_{PD} and the combination of contact intrinsic resistance and bond wire intrinsic resistance R_{PD} [15]. The parasitic capacitance C_{PD} for a 10 Gb/s photodetector is typically between 100 and

200 fF, which cannot be overlooked. The parasitic resistance is typically between 10 and 20 Ohms. For the sake of simplicity, we ignore this resistive component in our analysis [42]. The equivalent input noise current source $I_{n,eq}$ shown in figure 3.2 combined with a noiseless TIA, produces the same output noise as the actual noisy TIA. This equivalent input noise current, also known as the input-referred noise current, is an important figure of merit in TIA design since it directly influences receiver sensitivity. Although the photodetector contributes to overall input noise, for the sake of simplicity, this noise component will be ignored in the analysis of this thesis, as transimpedance amplifier noise dominates.

The physical characteristics of the photodetector, such as the efficiency of converting light energy to proportional current, switching speed, input referred noise, and parasitic capacitance load C_{PD} at the transimpedance amplifier's input node, limit and complicate the TIA circuit design [43]. While an ideal TIA should have zero input impedance, practical systems frequently have impedances of up to 50 Ω. The essential design criteria is the TIA's input impedance, which is primarily influenced by C_{PD}. Implementing a photodiode while designing the TIA is complicated, since the the type of photodetector used depends on the application and is out of scope for this thesis. But for a good TIA design, it is recommended to consider the effects of the C_{PD} while doing the calculations. Nevertheless, the influence of the C_{PD} on TIA performance can be observed in the next section.

3.2 Performance of TIAs

It is required to analyze the performance of the TIAs before deciding on the best topology to use. This section goes through the most important figures of merit for TIA designs. Transimpedance gain, bandwidth, input-referred noise current, and power consumption are necessary when designing a TIA circuit. Because the TIA is a crucial component in an optical receiver, these characteristics limit the overall performance of the receiver system. The goal was to understand how to investigate the basic performance of the various topologies under nearly similar conditions in the following chapters to select the best one for this thesis work.

3.2.1 Transimpedance Gain

The TIA's transimpedance gain is defined as the ratio of its output voltage to its input current. The input current I_{in} is the current from the photodetector. More precisely, it is the photocurrent generated by the intrinsic photodetector [44]. Since the TIA's input is shunted by the PD's parasitic capacitor C_{pd}, the current reaching the TIA is less than the current from the source. If the input current is I_{in} and the output voltage is V_{out} of a TIA. Then, the TIA's transimpedance gain is given by equation 3.1.

$$Z_t = \frac{V_{out}}{I_{in}} \quad \Omega \tag{3.1}$$

For a given input signal I_{in}, the higher the value of Z_t, the more output signal V_{out} is produced. The transimpedance gain is expressed in the units of Ω or dBΩ. The value of dBΩ is calculated by the given equation 3.2. For example, 1 kΩ

corresponds to 60 dBΩ. The following chapters will show the design for a TIA with 1 kΩ or 60 dBΩ transimpedance gain.

$$Z_t(\text{dB}\Omega) = 20\log_{10}(\frac{V_{out}}{I_{in}}) \quad \text{dB}\Omega \tag{3.2}$$

The first benefit of a high-gain TIA is that it produces an output voltage swing with sufficient amplitude to drive the post-amplifier and subsequent stages. However, another factor that could be even more significant is noise. As the TIA is the first stage in the optical receiver, the noise added from the following limiter stages will be suppressed by this high TIA gain. As a result, a lower transimpedance gain cannot be exchanged for a larger post-amplification (for example, to obtain a higher bandwidth) [45]. A trade-off between the gain and bandwidth is well-known, and increasing the gain-bandwidth product without compromising performance metrics like noise and voltage swing is always a design challenge.

The transimpedance gain is a complex quantity with frequency-dependent magnitude $|Z_t(f)|$ and frequency-dependent phase shift $\theta(f)$. The transimpedance gain can be expressed using the magnitude and phase representation given by equation 3.3.

$$Z_t(f) = |Z_t(f)|e^{j\theta(f)} \quad \Omega \tag{3.3}$$

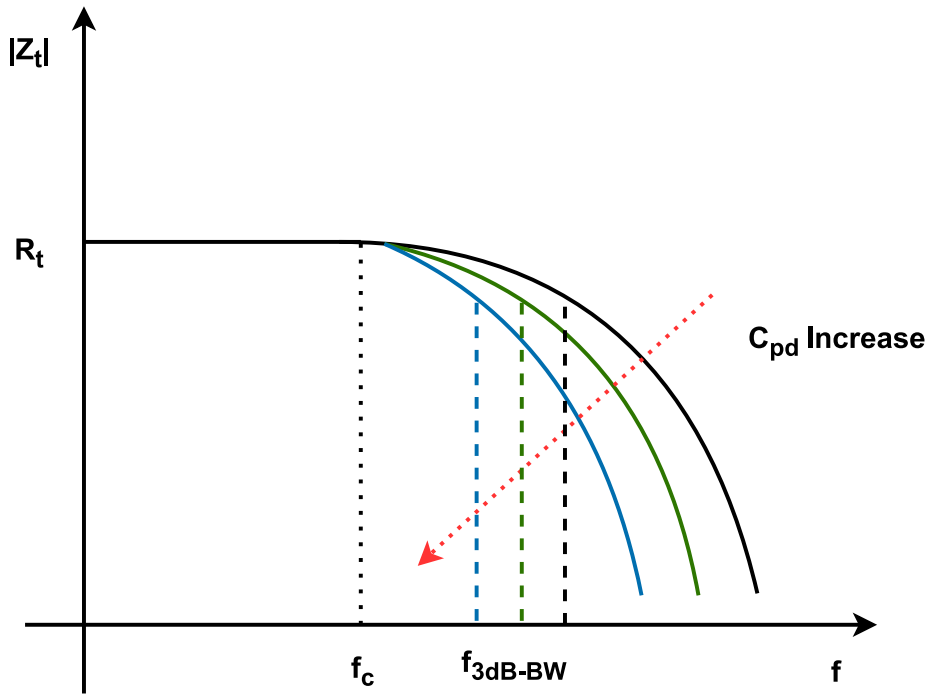

Figure 3.3: Frequency Response of a TIA with changing Photo-Diode Capacitance.

The transimpedance gain at low frequencies is usually flat and represented as the trans-resistance, R_t or the feedback resistor R_f (if any). But at high frequencies, the output voltage swing ΔV_{out} diminishes relative to ΔI_{in}, and the output voltage no longer follows the input current instantaneously. This behaviour is clearly explained in figure 3.3. At low frequencies, all of the photocurrent enters the TIA and there is

no distinction between the intrinsic photocurrent and the current flowing through the TIA's input terminal. At high frequencies, however, photodetector parasitics and packaging parasitics make these two currents different. In particular, the photodetector capacitance, C_{pd}, shunts some of the photocurrent to the ground (how much depends on CD and the TIA's input impedance) [44]. When reporting $Z_t(f)$, the associated C_{pd} must be stated along with it. As illustrated with the blue line in figure 3.3, a larger CD typically reduces the transimpedance gain at high frequencies (i.e., it reduces the bandwidth).

3.2.2 Bandwidth

Bandwidth is the frequency range at which the amplifier provides adequate amplification. Hence, as shown in figure 3.3, the transimpedance amplifier bandwidth ($f_{3dB–BW}$) is defined as the frequency at which the transimpedance gain Z_t is dropped by 3dB below its corner frequency value (f_c). This value is also called the -3dB bandwidth. TIA usually determines the bandwidth of the optical receiver, as its the first and critical component in an optical receiver [15].

In TIA and optical receiver design, there are several bandwidth-limiting factors. Generally, bandwidth is limited by the total capacitance contributed by the photodiode and other parasitic elements existing at the optical front-end [46]. The total capacitance of the PD (including parasitic and pad capacitances), the TIA input impedance, and the feedback resistor (if any) define the frequency performance of the system in terms of an R-C response. Hence, the bandwidth of a general transimpedance amplifier can be given by equation 3.4.

$$BW_{TIA} = \frac{1}{2\pi R_{in}(C_{pd} + C_{TIA})} \quad GHz \tag{3.4}$$

We need to make the bandwidth wide enough to prevent the signal waveform from being distorted by inter-symbol interference (ISI). However, wider bandwidth also translates to more noise picked up, which may corrupt the signal [14]. There must be an optimum bandwidth due to noise and distortion trade-offs.

3.2.3 Noise Sources

Noise is a significant limiting factor in the efficiency of electronic circuits. This section provides an overview of the numerous noise sources. Noise in circuits is caused by various physical events, including the random movement of charge-carrying particles (electrons and holes). Because the flow of charge (current) through a conducting or semiconducting material is not continuous, noise exists. Because electrons are particles, the movement of charge through a material's cross-section is discrete [47]. Electrons are not immobile and move randomly through the material's lattice; electron mobility is not in a straight line, even in an electric field. The amount of charge that passes across a cross-section of a material can be in-homogeneous at any point in time. Noise in circuits is classified according to the process through which it is produced. Flicker noise, Thermal noise, and shot noise are the sources that influence BiCMOS architectures' functioning.

Thermal Noise

Thermal noise is produced when carriers within a conductor are "thermally agitated," resulting in unexpected current and potential across the conductor [48]. So it is the random movement of electrons due to thermal energy, also called Johnson noise or Nyquist noise. The amplitude of the noise voltage across the conductor has a Gaussian distribution, and the PSD of thermal noise is constant across all frequencies. The mean-square current of a resistor is 3.5, and its RMS form is defined as shown in equation 3.6:

$$\overline{I^2_n} = \frac{4kT}{R}\Delta f \quad A^2/Hz \tag{3.5}$$

$$I_n = \sqrt{\frac{4kT}{R}\Delta f} \quad A/\sqrt{Hz} \tag{3.6}$$

Where k is the Boltzmann's constant, T is the temperature in Kelvins, R is the resistance, and Δf is a small bandwidth the noise is calculated over.

Shot Noise

Shot noise is caused by the discontinuous nature of charge transmission at junctions between two materials where an electric field occurs. It is generally caused by individual charges going through a potential barrier [48]. For example, shot noise can be generated in the photodiode in optical systems (which is also known as quantum noise) due to the "random arrival rates of photons" at the detector. The power spectral density of shot noise from a PIN diode is defined as shown in equation 3.7:

$$\overline{I^2_n} = 2qI_{pd} \quad A^2/Hz \tag{3.7}$$

Where q is the charge of electron and I_{pd} is the mean photodiode current, shot noise increases with increasing diode current. Because of its nature, shot noise can form in P-N junctions where electric fields form potential differences across depletion regions.

Flicker Noise

Flicker noise is caused by flaws in the material, where charge carriers might become stuck or slowed down [49]. These imperfections trap charge carriers, causing the current to fluctuate. The spectral density of flicker noise decreases with increasing frequency at a rate of $1/f$. The current passing through the base-emitter zone closest to the surface of BiCMOS transistors will have some flicker noise. The flicker noise's RMS noise current is defined as shown in equation 3.8.

$$\overline{I^2_n} = \frac{2qf_cI_B}{f} \quad A^2/Hz \tag{3.8}$$

Where f_c is the corner frequency at which the influence of thermal noise decreases and other noises dominates. I_B is the current trough the base of the transistor.

3.2.4 Input-Referred Noise (IRN) Current

The input-referred noise current defines the TIA's noise contribution. The noise current that could be applied to the corresponding noiseless TIA to produce an output noise voltage equal to that in the original noisy circuit is referred to as the input-referred noise current [14]. Figure 3.4 illustrates this. Equation 3.9 connects the input-referred noise current to the output noise voltage. Because it is independent of the amplifier's transimpedance gain, the input-referred noise current is used to compare amplifiers fairly. According to Equation 3.9, it is necessary to determine the noise at the output and then refer to the input by dividing the calculated value by the static gain. Input-referred noise current power spectral density is measured in A^2/Hz or pA^2/Hz. The f^2 component at high frequencies and the 1/f component at low frequencies (fibre communication rules do not allow such low frequencies). In addition to thermal noise from the feedback resistor RF, noise sources for the BJT are often shot noises from the collector and base currents, and thermal noise from the intrinsic base resistance has more effect on the TIA's Input-Referred Noise.

$$\overline{I^2_{n,in}} = \frac{\overline{V^2_{n,out}}}{Z_t^2} \quad A^2/Hz \tag{3.9}$$

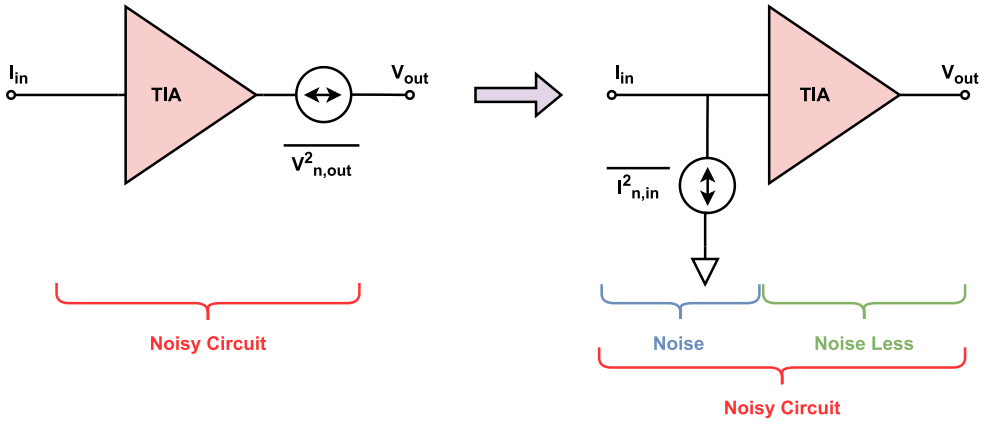

Figure 3.4: Input Referred Noise Current.

3.2.5 Impedance Matching

Changes in the propagating medium's characteristic impedance cause electromagnetic waves to reflect (Z_0). In high-speed systems, these reflections are undesirable because they exacerbate timing jitter, signal distortion, and instability. The ends of the TIA can be roughly matched to solve these issues (input and output matching), calling for impedance matching to be as close as possible to the outside world regarding circuit design specifications (50 Ω impedance). Perfect impedance matching has the drawback of increasing power dissipation in the circuit. Given that the input is connected to the photodiode (a high-impedance lumped element), it is important to note that this requirement only applies to the output of the TIA. The input and output reflection coefficients (S_{11}andS_{22}) must typically be smaller than -10 dB over the operating bandwidth, which means that the reflected wave must be less than 0.1

times as large as the incident wave [50]. Broadband matching over the entire (ideally large) bandwidth requires significant design work because the parasitic elements have a stronger influence at higher frequencies, especially in the output transistors driving the big 50 Ω loads.

3.2.6 Stability Factor

Any amplifier's stability is a crucial factor to consider when designing it. If the amplifier is not stable, the primary function of amplification is violated. The ability of an amplifier to suppress oscillations defines its stability. The Rollet stability factor K_F is the most popular method for calculating stability. Equation 3.10 can be used to calculate it [51].

$$KF = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{21}S_{11}|} \tag{3.10}$$

Where the input and output reflection coefficients are S_{11} and S_{22}, the reverse and forward voltage gains are S_{12} and S_{21}, respectively. The designed TIA will remain stable to all potential impedances on the Smith chart if $K>1$, which indicates that the designed amplifier is unconditionally stable. The amplifier becomes unstable when $K<1$.

Chapter 4

Transimpedance Amplifier Topologies

4.1 Introduction

As mentioned in section 1.2.2, photodiodes generate low current, and the subsequent processing takes place in the voltage domain, so the TIA must convert the photodiode current to voltage. As seen in figure 4.1a, a simple resistor, R_L, can convert the input photodiode current into an output voltage, resulting in a severe trade-off between gain, bandwidth, and noise. This resistor TIA also produces a transimpedance gain roughly equal to -R_L (opposite in phase). The TIAs small-signal resistor model and photodiode parasitics are shown in Figure 4.1b. The photodiode is replaced by an ideal current source I_{PD} and a parasitic capacitance C_{PD}. When the current I_{PD} passes through the resistor R_L, it converts to a voltage V_{out}.

The transimpedance gain of the single-resistor TIA in terms of Ω is written as shown in the equation 4.1 and in terms of dBΩ is shown in the equation 4.2.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{R_L}{1 + j2\pi f R_L C_T} \quad \Omega \tag{4.1}$$

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = 20\log\left(\frac{R_L}{1 + j2\pi f R_L C_T}\right) \quad dB\Omega \tag{4.2}$$

$$|Z_{TIA,DC}| \approx R_L \tag{4.3}$$

where f is frequency and total capacitance $C_T = C_{PD} + C_L$. C_L is the load capacitance of the TIA, which is typically significantly smaller than C_{PD}. The DC transimpedance gain can be written as shown in 4.3. The bandwidth of a single-resistor TIA is given by equation 4.4.

$$BW_{TIA} = \frac{1}{2\pi R_L C_T} \quad Hz \tag{4.4}$$

To calculate the input-referred noise current, it is necessary to consider the noise from R_L, C_L, and C_{PD}. As stated in the section 3.2.4, input-referred noise current PSD $\overline{I^2_{n,in}} = \frac{\overline{V^2_{n,out}}}{Z_t^2}$. The noise voltage PSD $\overline{V^2_{n,out}}$ at the output can be obtained from the equation 4.5.

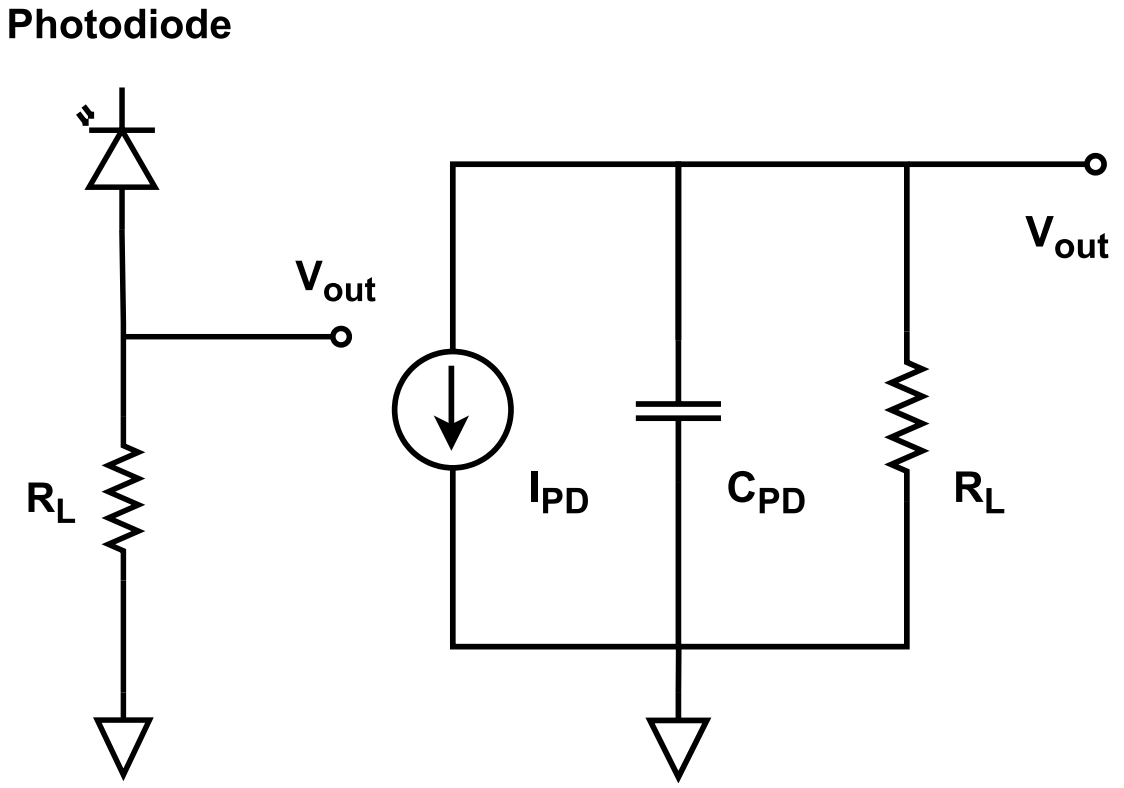

Figure 4.1: (a). Circuit diagram of a single resistor TIA. (b). Equivalent small-signal model.

$$\begin{aligned}\overline{V_{n,out}^2} &= \int_0^\infty \overline{I_{n,R_L}{}^2}|R_{out}|^2\,df \\ &= \int_0^\infty \frac{4kT}{R_L}\frac{R_L^2}{R_L^2C_{PD}^2 4\pi^2 f^2+1}\,df \\ &= \frac{kT}{C_{PD}} \quad \frac{V^2}{Hz}\end{aligned} \tag{4.5}$$

Where, the noise PSD from the resistance is given by $\overline{I_{n,R_L}{}^2} = \frac{4kT}{R_L}$ and equivalent output resistance $R_{out} = R_L||\frac{1}{sC_{PD}}$. Therefore, input-referred noise current PSD $\overline{I^2{}_{n,in}}$ is given by the equation 4.6.

$$\overline{I^2{}_{n,in}} = \frac{kT}{R_L^2 C_{PD}} \quad \frac{A^2}{Hz} \tag{4.6}$$

Equations 4.3, 4.4 and 4.6 represent the DC gain, bandwidth, and input-referred noise of a single resistor TIA. It is conceivable to conclude that raising the value of the R_L resistance will increase gain while lowering input noise. One problem is the trade-off between gain and bandwidth in this single resistor TIA. Equation 4.4 shows that the bandwidth decreases as the resistance value rises. As a result, using a simple resistor setup will always result in a trade-off between gain, input noise,

and bandwidth. Instead, it is crucial to construct more complex structures that allow for this trade-off and maximize design flexibility. So, to optimize three crucial design parameters: gain, bandwidth, and input-referred noise, this chapter analyzes four different topologies.

4.2 Common Base TIA

Due to its extremely low input impedance and high bandwidth, TIA designed with common base (CB) topology has been widely used in wideband optical communication systems since the 1980s [52]. It offers high voltage gain and high output impedance in addition to these benefits, both of which are preferred in TIA design. To reduce the impact of $R_L C_T$ in equation 4.4 and increase the bandwidth of the designed TIA, this common base topology may be a better option. However, because the noise produced by the transistor is added directly to the input, CB input stages typically have higher noise levels than other single-transistor architectures. In figure 4.2, a typical common-base TIA is shown. The transistor is biased at the base with a voltage V_{bias} and has a resistive load R_C.

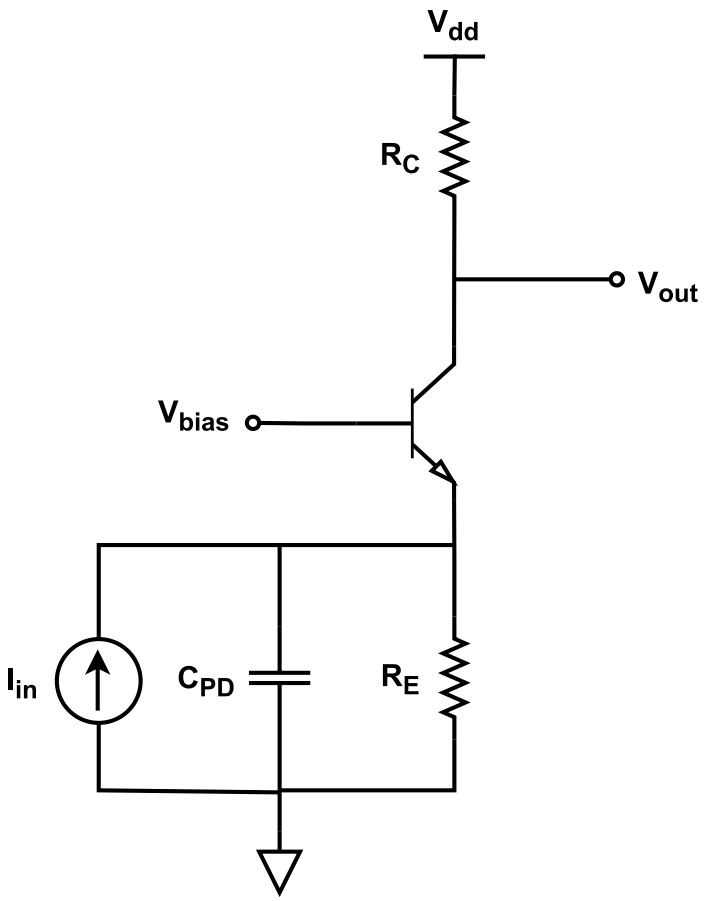

Figure 4.2: Circuit diagram of a basic common base TIA.

The small signal equivalent model of a CB amplifier seen in figure 4.3 is used to determine the high-frequency response of the circuit. C_{in} is the total input capacitance, the sum of photodiode capacitance C_{PD} and internal base-emitter capacitances C_π at the input. C_{out} is the total output capacitance, the sum of load

capacitance C_L and internal collector-base capacitances C_μ at the output. R_E and r_π are emitter and internal base-emitter resistance at the input of the transistor respectively. g_m is the transistor transconductance.

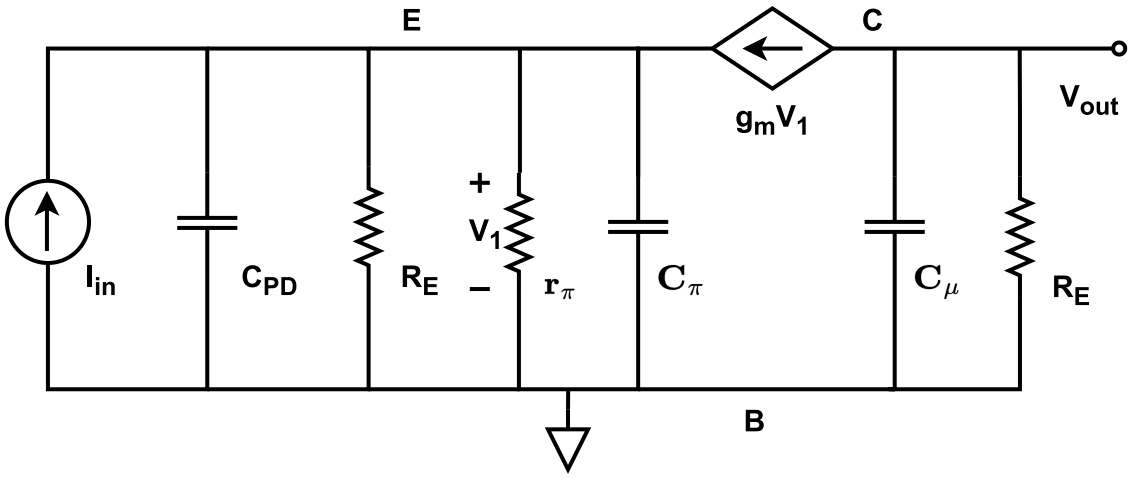

Figure 4.3: Equivalent small signal model of a Common base TIA.

Early effect and base resistance are disregarded to simplify the calculations. The transimpedance gain function of this small signal model of CB TIA is given by equation 4.7 when r_b is very small and transistor current gain β is very large, i.e., $\beta >> 1$. As a result of this equation, the DC transimpedance gain of the CB TIA is roughly equal to R_C, i.e., $|Z_{TIA,DC}| \approx R_C$.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{g_m R_C}{(g_m + sC_{in})(sR_C C_{out} + 1)} \quad \Omega \tag{4.7}$$

The CB TIA has an input impedance of approximately $\frac{1}{g_m}$. The input capacitances C_{in} are isolated from the output by CB TIA. Therefore, the broadband bandwidth produced by the decrease in input impedance allows for more flexibility in gain, bandwidth, and noise trade-offs. Equation 4.8 displays two dominant poles, p_1 at the input and p_2 at the output, which determines the CB TIA's bandwidth.

$$\begin{aligned} p_1 &= \frac{1}{2\pi \frac{1}{g_m} C_{in}} \quad \text{Hz} \\ p_2 &= \frac{1}{2\pi R_C C_{out}} \quad \text{Hz} \end{aligned} \tag{4.8}$$

In the input pole p_1, C_π (Since $C_{in} = C_{PD} + C_\pi$) and $\frac{1}{g_m}$ have an inverse relationship with I_c. Hence, p_1 is dependent of the biasing and will have much effect on bandwidth limitation. At the output pole p_2, R_C coupled with the negligible C_μ and any load capacitance C_L, also form a bandwidth limitation of the circuit. Thus, selecting R_C offers a direct trade-off between transimpedance gain and bandwidth.

Equations 4.7 and 4.8 show the trade-off between the gain and bandwidth of a CB TIA. Let's now look at how gain and bandwidth affect the total input-referred noise current in the circuit. The sources of noise in the circuit are depicted in Figure 4.4. The information mentioned in section 3.2.4 is used to derive IRN. The following are the noise sources that have an impact on a CB TIA's IRN:

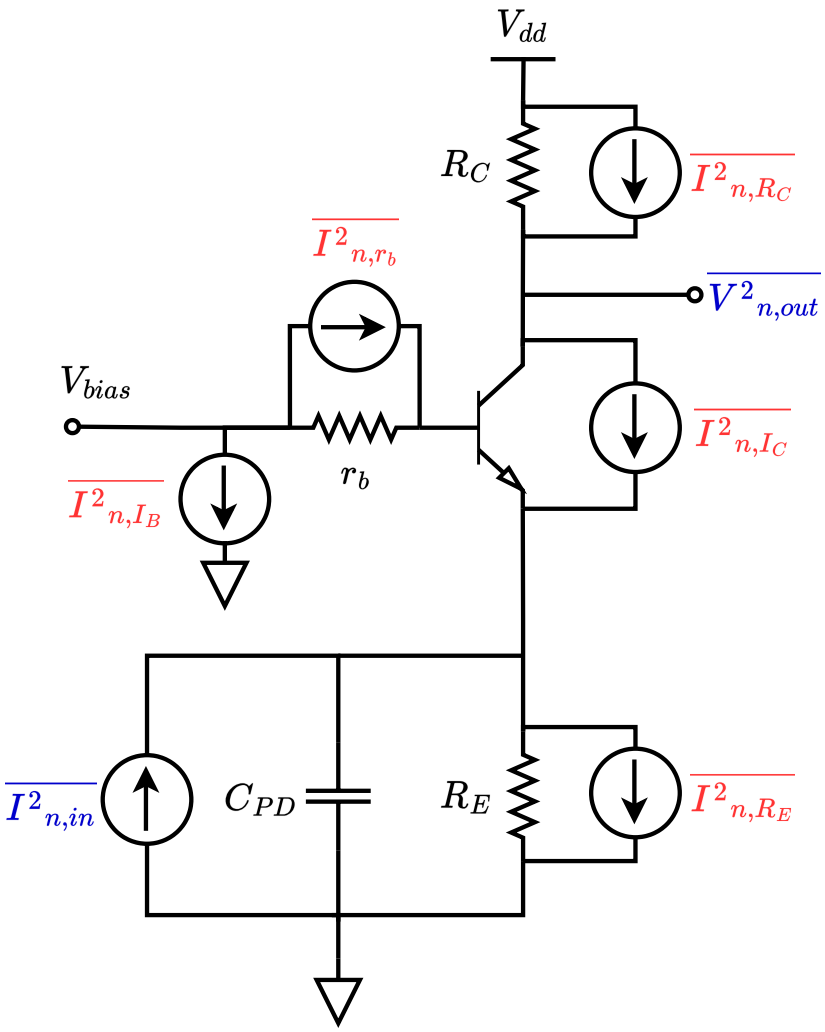

Figure 4.4: CB TIA with individual noise sources (in red).

- Thermal noise from the collector resistor, $\overline{\mathrm{I^2_{n,R_C}}} = \frac{4\mathrm{kT}}{\mathrm{R_C}}$
- Thermal noise from the emitter resistor, $\overline{\mathrm{I^2_{n,R_E}}} = \frac{4\mathrm{kT}}{\mathrm{R_E}}$
- Short noise because of the base current in the transistor, $\overline{\mathrm{I^2_{n,I_B}}} = \frac{2\mathrm{qI_C}}{\beta}$
- Short noise because of the collector current in the transistor, $\overline{\mathrm{I^2_{n,I_C}}} = 2\mathrm{qI_C}\frac{(2\pi \mathrm{C_{in}})^2}{\mathrm{g_m}^2}\mathrm{f}^2$
- Thermal noise from the internal base resistor, $\overline{\mathrm{I^2_{n,r_b}}} = 4\mathrm{kTr_b}(2\pi \mathrm{C_{PD}})^2\mathrm{f}^2$

The total input-referred noise current PSD is the sum of individual noises in the circuit. Hence it is written as shown in equation 4.9. Here, thermal noise from collector $\overline{\mathrm{I^2_{n,R_C}}}$ and emitter resistors $\overline{\mathrm{I^2_{n,R_E}}}$ and short noise of the base current $\overline{\mathrm{I^2_{n,I_B}}}$ have more impact at lower frequencies. As the frequency increases, IRN increases due the addition of short noise from collector current $\overline{\mathrm{I^2_{n,I_C}}}$ and thermal noise from the internal base resistor $\overline{\mathrm{I^2_{n,r_b}}}$.

$$\overline{I^2_{n,TIA}}(f^2) = \frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_C}{\beta} + 2qI_C\frac{(2\pi C_{in})^2}{{g_m}^2}f^2 + 4kTr_b(2\pi C_{PD})^2 f^2 \quad \frac{A^2}{Hz} \quad (4.9)$$

In conclusion, R_C must be increased for a given photodiode and technology to improve gain in equation 4.7. This will result in a greater voltage drop across R_C, reducing the available voltage headroom. According to equation 4.8, increasing R_C will decrease the p_2 pole frequency, which will affect the bandwidth. As shown in equation 4.9, attempting to reduce R_C will result in lower transimpedance gain and increased IRN due to the thermal noise of R_C. $\overline{I^2_{n,I_C}}$ and $\overline{I^2_{n,r_b}}$ depend on frequency. To enhance the overall noise performance, it is crucial to reduce these noise sources. Larger transistors can be used for this because they will have lower base resistance. However, junction capacitances will be higher in large transistors [14]. As a result, the CB TIA architecture adds extra noise to the TIA.

4.3 Common Emitter with Negative Resistive Feedback TIA

The shunt-feedback TIA circuit topology shown in figure 4.5 is used most frequently for TIAs in optical fibre applications. If the Miller effect is mitigated, it offers high current, voltage gain, and adequate bandwidth. Still, it needs sophisticated bias networks and emitter degeneration to maintain stable operation over temperature. When designing OP-amps, where an infinite input impedance is desired, CE's relatively high input impedance can be very advantageous. However, in TIA design, where a low input impedance is optimal, this is typically addressed with shunt-shunt feedback to lower the input impedance seen by the photodiode while at the same time decreasing the noise. As mentioned, another downside is the Miller effect, which can degrade the bandwidth of the CE stage.

The stringent trade-offs in common-base TIA circuits make achieving low noise and low power operation difficult. As mentioned in the above section 4.2, the noise current PSD of the resistors R_C and R_E are directly referred to the input, leading to high noise. To overcome these issues, a CE amplifier with a negative resistive feedback R_F is preferable, which provides a large bandwidth by synthesizing a small input impedance while maintaining a large resistor value in the feedback path to improve noise behaviour. The small signal equivalent model of a CE amplifier with a negative resistive feedback TIA, seen in figure 4.6, is used to calculate the high-frequency response of the circuit.

C_{in} is the total capacitance while finding input impedance, which includes photodiode capacitance C_{PD}, internal base-emitter capacitance C_π, and internal collector-base capacitance C_μ. Total capacitance C_{out} is the sum of capacitances while finding output impedance, which includes load capacitance C_L and internal collector-base capacitance C_μ. R_F, r_π, and r_b are feedback resistance from output to input, internal base-emitter resistance, and internal base resistance at the transistor's input. g_m is the transistor transconductance.

Under the condition that transistor current gain β is very large, i.e., $\beta >> 1$ and r_b is very small, the transimpedance gain function of this small signal model of the CE TIA with resistive feedback is given by the equation 4.10. The derivation

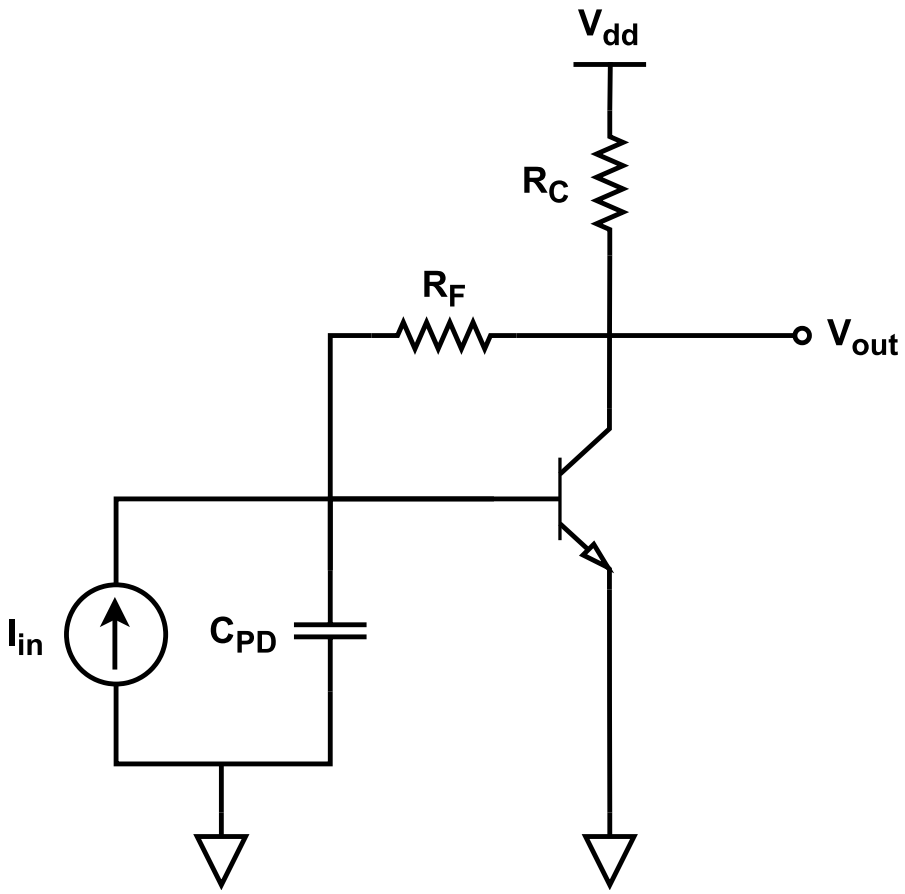

Figure 4.5: Circuit diagram of a basic common emitter TIA.

for the DC transimpedance gain $Z_{TIA_{DC}}$ of the common emitter TIA is given in the appendix A.1. Hence, from this equation, the DC transimpedance gain of the CE TIA with resistive feedback is approximately equal to $(R_C||R_F)$, i.e., $|Z_{TIA,DC}| \approx (R_C||R_F)$.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{g_m(R_C||R_F)}{(1 + s(R_C||R_F)C_{out})} \quad \Omega \tag{4.10}$$

The input impedance of the CE TIA is about $\frac{R_F}{1+sR_FC_{in}}$. The output impedance of the CE TIA is about $\frac{(R_C||R_F)}{1+s(R_C||R_F)C_{out}}$. CE TIA isolates the input capacitances C_{in} from the output using a feedback resistor R_F. Therefore, decrease in input impedance, resulting in broadband bandwidth, giving more flexibility for gain, bandwidth and noise trade-offs. The bandwidth of the CE TIA is determined by two dominant poles, one at the input and the other at the output. These dominant poles p_1 at the input and pole p_2 at the output are shown in the equation 4.8. The derivation for finding the input and output poles of the common emitter TIA is given in the appendix A.1.

$$\begin{aligned} p_1 &= \frac{1}{2\pi R_F C_{in}} \quad \text{Hz} \\ p_2 &= \frac{1}{2\pi (R_C||R_F) C_{out}} \quad \text{Hz} \end{aligned} \tag{4.11}$$

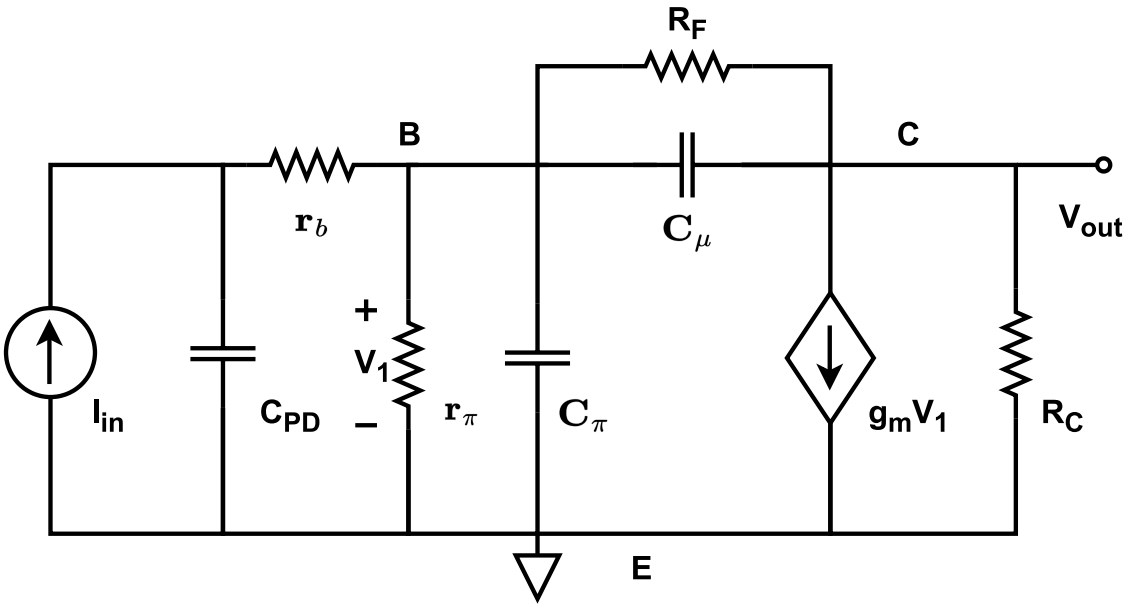

Figure 4.6: Equivalent small signal model of a Common emitter TIA.

In the input pole p_1, R_F has an inverse relationship with the pole frequency. At the output pole, $R_C||R_F$ have an inverse relationship with the pole frequency. If R_F is large and R_C is small, then pole p_1 will form at a lower frequency and pole p_2 form at a higher frequency improving the bandwidth. But this, in turn, reduces the TIA gain. Thus, selecting R_C and R_F offers a direct trade-off between transimpedance gain and bandwidth.

The trade-off between the gain and bandwidth of a CE TIA with resistive feedback can be seen from equations 4.10 and 4.11. Now let's investigate the total input-referred noise current in the circuit and its trade-off with gain and bandwidth. Figure 4.7 shows the noise sources present in the circuit. IRN is derived according to the information mentioned in the section 3.2.4. The list of noise sources affecting the IRN of a CE TIA with resistive feedback are:

- Thermal noise from the collector resistor, $\overline{I^2_{n,R_C}} = \frac{4kT}{R_C}$
- Thermal noise from the feedback resistor, $\overline{I^2_{n,R_E}} = \frac{4kT}{R_E}$
- Short noise because of the base current in the transistor, $\overline{I^2_{n,I_B}} = \frac{2qI_C}{\beta}$
- Short noise because of the collector current in the transistor, $\overline{I^2_{n,I_C}} = 2qI_C\frac{(2\pi C_{in})^2}{{g_m}^2}f^2$
- Thermal noise from the internal base resistor, $\overline{I^2_{n,r_b}} = 4kTr_b(2\pi C_{PD})^2f^2$

The effect of all these noise sources can be described by a single equivalent noise current source $\overline{I^2_{n,in}}$ at the input of the TIA. Hence it is written as shown in the equation 4.12. Here, thermal noise from collector $\overline{I^2_{n,R_C}}$ and feedback resistors $\overline{I^2_{n,R_E}}$ contributes directly to the input. Short noise of the base current $\overline{I^2_{n,I_B}}$ adds

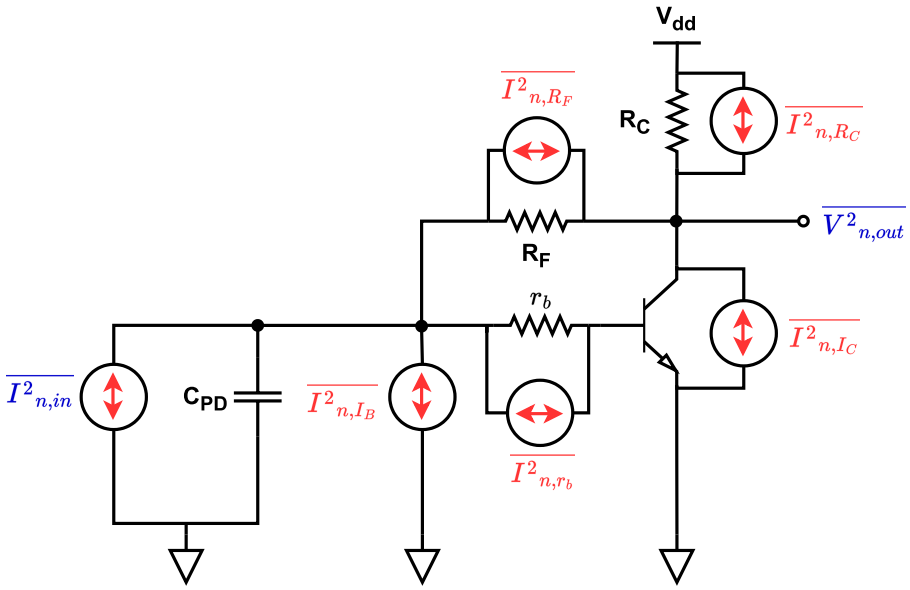

Figure 4.7: CE TIA with individual noise sources (in red).

directly to the input. Short noise from collector current $\overline{I^2_{n,I_C}}$ and thermal noise from the internal base resistor $\overline{I^2_{n,r_b}}$ are referred to the input.

$$\overline{I^2_{n,TIA}}(f^2) = \frac{4kT}{R_C} + \frac{4kT}{R_F} + \frac{2qI_C}{\beta} + 2qI_C\frac{(2\pi C_{in})^2}{g_m{}^2}f^2 + 4kTr_b(2\pi C_{PD})^2f^2 \quad \frac{A^2}{Hz} \tag{4.12}$$

To increase gain in equation 4.10 for a given photodiode and technology, both $R_C||R_F$ must be increased. Voltage headroom will decrease as R_C is increased because the voltage drop across R_C will be greater. Since R_C depends on TIA gain, it should be smaller. According to equation 4.11, reducing R_C causes the pole frequency of pole p_2 to increase, and increasing the value of R_F causes the pole frequency of pole p_1 to decrease. It is increasing the TIA circuit's bandwidth as a result. As shown in equation 4.12, attempting to reduce R_C will increase IRN due to R_C's thermal noise. But because R_F generates thermal noise, increasing R_F will lower IRN. Hence Selecting a lower value of R_C and a higher value of R_F will give a better trade-off between transimpedance gain, bandwidth and IRN.

4.4 Regulated Cascode TIA

As seen earlier, the common-base topology imposes severe trade-offs on the main performance parameters, namely bandwidth, noise, and gain. To relax these tight trade-offs, a two-stage shunt-series feedback amplifier shown in figure 4.8, also called "regulated-cascode (RGC)", is commonly utilized. This RGC TIA can be viewed in two different ways. They are:

- A common-base (Q_2) transistor with a local feedback loop consisting of Q_1 and R_{C_1}.

- A closed-loop current amplifier consisting of a two-stage open-loop amplifier (i.e., a common-emitter stage Q_1 followed by another emitter-degenerated common-emitter stage Q_2) surrounded by a shunt-series resistive feedback R_E.

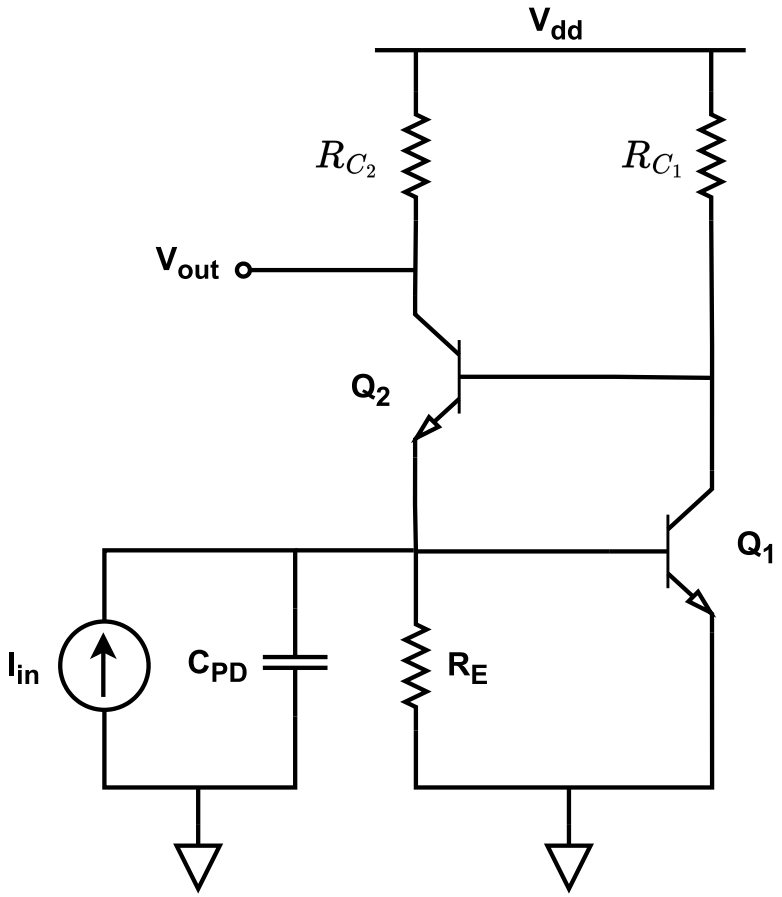

Figure 4.8: Circuit diagram of a basic regulated cascode TIA.

The small signal equivalent model of an RGC TIA seen in figure 4.9 is used to calculate the high-frequency response of the circuit. C_{in} is the total capacitance while finding input impedance, which includes photodiode capacitance C_{PD} and internal base-emitter capacitance C_{π_1} of Q_1. Total capacitance C_{out} is the sum of capacitances while finding output impedance, which includes load capacitance C_L, internal collector-base capacitance C_{μ_1}, C_{μ_2} of transistors Q_1, Q_2, and internal base-emitter capacitance C_{π_2} of Q_2. R_{C_1}, R_{C_2}, and R_E are collector resistors of Q_1, Q_2 and emitter resistor of Q_1. r_{π_1}, r_{π_1} are internal base-emitter resistances of Q_1, Q_2 and g_{m_1}, g_{m_2} are the transconductance of transistors Q_1, Q_2.

Early effect and base resistance are disregarded to simplify the calculations. Under the condition that transistor current gain β_1, β_2 are very large, i.e., β_1, $\beta_2 >> 1$ and r_{b_1}, r_{b_2} are very small, the transimpedance gain function of this small signal model of the regulated cascode TIA is given by the equation 4.13. The derivation for the DC transimpedance gain $Z_{TIA_{DC}}$ of the regulated cascode TIA is given in the appendix A.2. Hence, from this equation, the DC gain of the regulated cascode TIA is approximately equal to R_{C_2}, i.e., $|Z_{TIA,DC}| \approx R_{C_2}$.

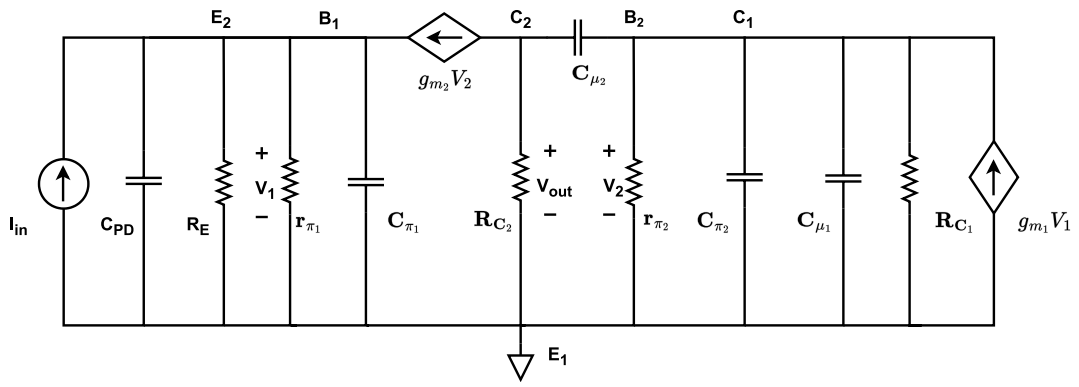

Figure 4.9: Equivalent small signal model of a regulated cascode TIA.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{R_{C_2}(1 + sR_{C_1}C_{out})}{(1 - sR_{C_1}R_{C_2}C_{\mu_2})} \quad \Omega \tag{4.13}$$

Finding the number of poles and zeros in the circuit by analyzing the input and output impedances is crucial for predicting the bandwidth of the cascode circuit. Since each transistor's base is connected to another transistor's emitter, finding the impedances will be tricky. The input impedance Z_{in}, input pole p_1 and input zero z_1 is shown 4.14. The output impedance Z_{out}, pole p_2, and zero z_2 of the regulated cascode TIA are shown in equation 4.15. The derivation for finding the input and output poles and zeros of the regulated cascode TIA is given in the appendix A.2.

$$\begin{aligned} Z_{in} = \frac{V_{in}}{I_{in}} = (R_{C_2} + R_E)\frac{1 + s(R_{C_2}||R_E)C_{in}}{1 + sR_EC_{in}} \quad & \Omega \\ p_1 = \frac{1}{2\pi R_EC_{in}} \quad & \text{Hz} \\ z_1 = \frac{1}{2\pi(R_{C_2}||R_E)C_{in}} \quad & \text{Hz} \end{aligned} \tag{4.14}$$

$$\begin{aligned} Z_{out} = \frac{V_{out}}{I_{out}} = \frac{1 + sR_{C_1}C_{out}}{1 + s(R_{C_1}C_{out} + R_{C_2}C_{\pi_2})} \quad & \Omega \\ p_2 = \frac{1}{2\pi(R_{C_1}C_{out} + R_{C_2}C_{\pi_2})} \quad & \text{Hz} \\ z_2 = \frac{1}{2\pi R_{C_1}C_{out}} \quad & \text{Hz} \end{aligned} \tag{4.15}$$

In the input pole p_1 and zero z_1, R_{C_2} and R_E have an inverse relationship with the input pole and zero frequency. At the output pole, R_{C_1} and R_{C_2} have an inverse relationship with the output pole and zero frequency. If R_{C_2} is large and R_E is small, then poles p_1 and zero z_1 will form at the frequency, cancelling each other and improving the bandwidth. In the case of increasing R_{C_2}, the voltage drop across it will be higher, which degrades voltage headroom. Selecting a low R_{C_1} will improve the bandwidth by increasing the output pole and zero frequency.

Equations 4.13, 4.14 and 4.15 show how a regulated cascode TIA trades off gain for bandwidth. Let's now examine the total input-referred noise current in the

circuit and how gain and bandwidth are impacted by it. The circuit's noise sources are depicted in figure 4.10. The information in the section 3.2.4 is used to derive IRN. The following are the noise sources that can affect the IRN of a regulated cascode TIA:

- Thermal noise from the collector resistor R_{C_1}, $\overline{I^2_{n,R_{C_1}}} = \frac{4kT}{R_{C_1}}$
- Thermal noise from the collector resistor R_{C_2}, $\overline{I^2_{n,R_{C_2}}} = \frac{4kT}{R_{C_2}}$
- Thermal noise from the degenerative emitter resistor R_E, $\overline{I^2_{n,R_E}} = \frac{4kT}{R_E}$
- Short noise because of the collector current I_{C_1} in the transistor Q_1, $\overline{I^2_{n,I_{C_1}}} = 2qI_{C_1}\frac{(2\pi C_{in})^2}{{g_{m_1}}^2}f^2$
- Short noise because of the collector current I_{C_2} in the transistor Q_2, $\overline{I^2_{n,I_{C_2}}} = 2qI_{C_2}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2$

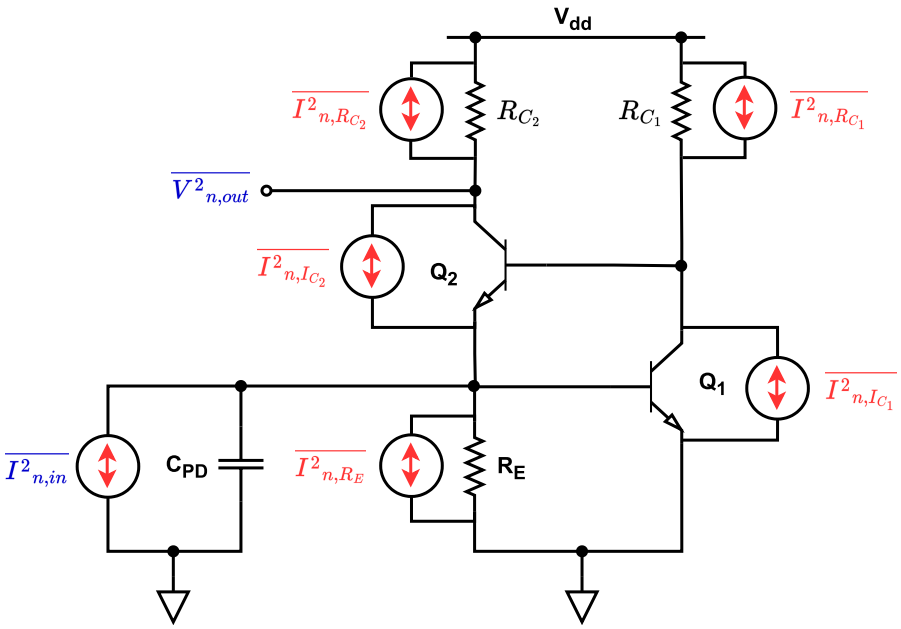

Figure 4.10: RGC TIA with individual noise sources (in red).

The effect of all these noise sources can be described by a single equivalent noise current source $\overline{I^2_{n,in}}$ at the input of the TIA. Hence it is written as shown in equation 4.16. Here, thermal noise from collector resistances $\overline{I^2_{n,R_{C_1}}}$ and $\overline{I^2_{n,R_{C_2}}}$, and degenerative emitter resistor $\overline{I^2_{n,R_E}}$ contributes directly to the input. Short noise from collector currents of transistors Q_1andQ_2, $\overline{I^2_{n,I_{C_1}}}$ and $\overline{I^2_{n,I_{C_2}}}$ are referred to the input. Thermal noises from collector resistors R_{C_1}, R_{C_2} and degenerative emitter resistor R_E have more impact at lower frequencies. As the frequency increases, IRN increases due to the addition of short noise from collector currents I_{C_1} and I_{C_2}.

$$\overline{I^2{}_{n,TIA}}(f^2) = \frac{4kT}{R_{C_1}} + \frac{4kT}{R_{C_2}} + \frac{4kT}{R_E} + 2qI_{C_1}\frac{(2\pi C_{in})^2}{{g_{m_1}}^2}f^2 + 2qI_{C_2}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2 \quad \frac{A^2}{Hz} \tag{4.16}$$

In conclusion, for a given photodiode and technology, to improve gain in equation 4.13, R_{C_2} both must be increased. In the case of increasing R_{C_2}, the voltage drop across it will be higher, which degrades voltage headroom. From equation 4.14 and 4.15, larger R_{C_2} and lower R_{C_1} will cancel the input pole and zero and reduces the output pole which might lead to an improvement in bandwidth. But due to the increase in output zero z_2 frequency, the gain graph will be hard to predict. Increasing R_{C_2} will increase the IRN due to the thermal noise of R_{C_2} as shown in equation 4.12. But decreasing the value of R_{C_1} will increase the IRN due to the thermal noise of R_{C_1}. Hence achieving a trade-off between transimpedance gain, bandwidth and IRN of the regulated cascode TIA will be complicated.

4.5 Darlington pair with Negative Resistive Feedback TIA

As discussed in section 4.3, feedback transimpedance amplifiers are a popular approach to avoid the dynamic range problem because an R_F feedback resistor does not have to carry a bias current. The common-emitter topology discussed in that section imposes severe trade-offs on the main performance parameters, namely bandwidth, noise, and gain. To relax these tight trade-offs, a darlington pair can be implemented. A darlington pair consists of two bipolar transistors connected so that the current amplified by the first transistor is amplified again by the second transistor. The configuration of the darlington transistor gives a much higher current gain than a single transistor taken individually. A darlington transistor pair comprises a couple of bipolar transistors that are coupled in order to deliver a very high-current gain from a low-base current. The input impedance of this topology is high, which is not desired for a good TIA design. This drawback can be mitigated by using a negative feedback resistor. As the input impedance reduces, The bandwidth of the TIA will be improved due to the increase in the input pole magnitude. The feedback structure also reduces output resistance, yielding better drive capability [53].

A basic schematic of a darlington pair TIA with negative resistive feedback can be seen in figure 4.11. The emitter of the input transistor Q_1 is connected to the base terminal of the output transistor Q_2. Here, the incoming current signal is amplified by Q_1 with a current gain factor of β_1 and the emitter current of the Q_1 is obtained. This emitter current from Q_1 is fed to the base of Q_2, amplified by its current gain factor β_2. This darlington pair TIA topology acts as a single CE TIA topology shown in section 4.3, but with high current gain. The effective current gain of the whole circuit is approximately the product of the gains of the two transistors Q_1 and Q_2. Therefore the effective current gain can be written as $\beta_{eff} \approx \beta_1\beta_2$. Hence, the transconductance of both transistor Q_1 and Q_2 will be equal, i.e., $g_{m_1} = g_{m_2} = g_m$. A collector resistance R_C is used to regulate the amplification and provide better control of the amplified current signal.

In figure 4.11, the transistor Q_1 acts as a common collector with a degenerative resistor R_E and transistor Q_2 acts as a common emitter with a feedback resistor

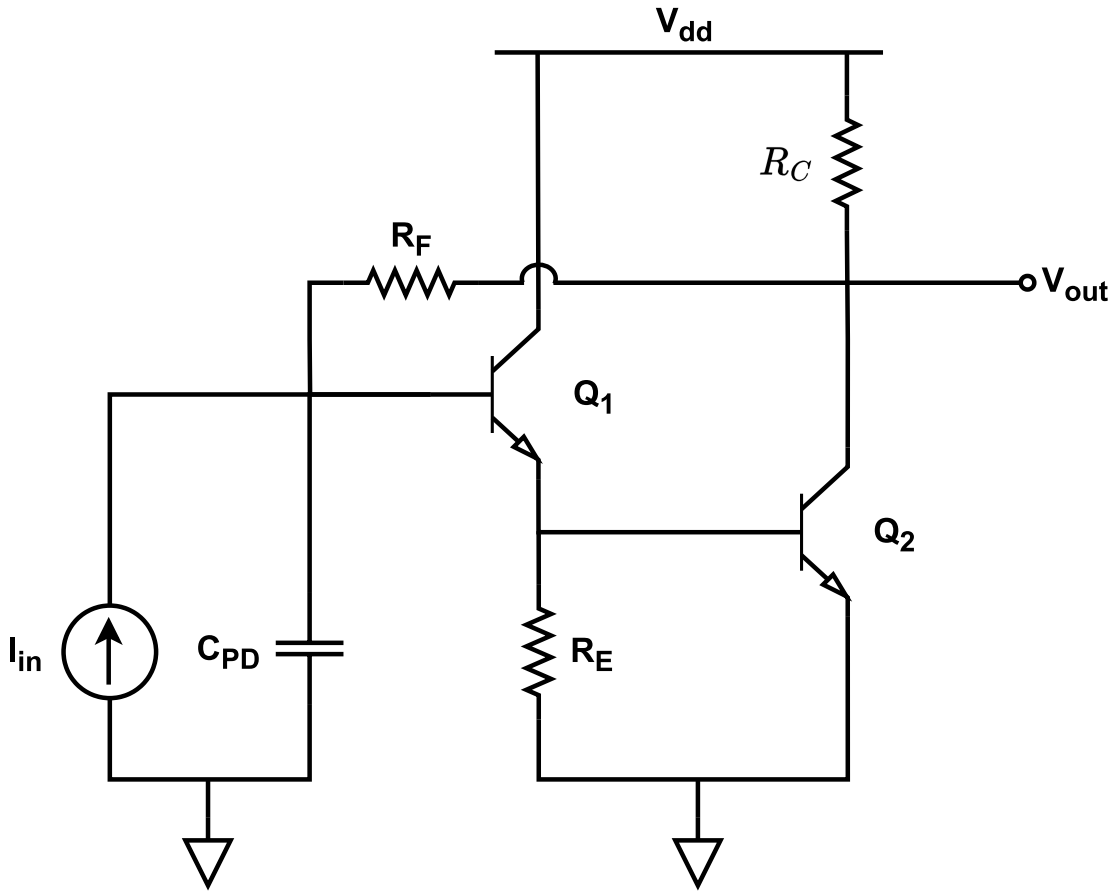

Figure 4.11: Circuit diagram of a basic Darlington TIA with Negative Resistive Feedback.

R_F. For finding the DC transimpedance gain $Z_{TIA_{DC}}$ of the whole darlington pair, it can be easily realised by finding the DC transimpedance gain of common collector Q_1 ($Z_{TIA_{DC}} = V_{out_1}/I_{in}$) and DC transimpedance gain of common emitter Q_2 ($Z_{TIA_{DC}} = V_{out}/I_{in_1}$) separately and multiplying them. The derivation for the DC transimpedance gain $Z_{TIA_{DC}}$ of the darlington pair TIA is given in the appendix A.3. Hence, the DC transimpedance gain of the darlington pair TIA is approximately given by the equation 4.17.

$$Z_{TIA_{DC}} = \frac{V_{out}}{I_{in}} \approx \beta_1 R_E g_{m_2}(R_C||R_F) \quad \Omega \tag{4.17}$$

Here $\beta_1 R_E$ is the DC gain of common source transistor Q_1 and $g_{m_2}(R_C||R_F)$ is the DC gain of common emitter transistor Q_2. Any amplifier's bandwidth depends on the circuit's input and output pole. For finding the bandwidth of the darlington pair TIA, it can be easily realised by considering the input pole from the common collector Q_1 and output pole from the common emitter Q_2. So, these dominant poles at input p_1 and pole p_2 at the output are shown in the equation 4.18. The derivation for finding the input and output poles of the darlington pair TIA is given in the appendix A.3.

$$\begin{aligned} p_1 &= \frac{1}{2\pi\beta_1 R_E C_{in}} \quad \text{Hz} \\ p_2 &= \frac{1}{2\pi(R_C||R_F)C_{out}} \quad \text{Hz} \end{aligned} \tag{4.18}$$

In the input pole p_1, β_1 has a direct relationship with the collector current I_1. So to reduce the pole frequency, I_1 or R_E should be increased to increase the bandwidth. The output pole $R_C||R_F$ have an inverse relationship with the pole frequency. If R_F is large and R_C is small, then pole p_2 forms at a higher frequency improving the bandwidth and reducing the TIA gain. Thus, selecting I_1, R_E, R_C, and R_F offers a direct trade-off between transimpedance gain and bandwidth.

The trade-off between the gain and bandwidth of a darlington pair TIA with Negative Resistive Feedback can be seen from equations 4.17 and 4.18. Now let's investigate the total input-referred noise current in the circuit and its trade-off with gain and bandwidth. Figure 4.12 shows the noise sources present in the circuit. IRN is derived according to the information mentioned in the section 3.2.4. Since both the transistors Q_1andQ_2 in the darlington pair form as a single transistor $Q_e$ff, the noise sources due to the individual transistors will be transformed into effective noise sources. The list of noise sources affecting the IRN of a CE TIA with resistive feedback are:

- Thermal noise from the feedback resistor R_F, $\overline{I^2_{n,R_F}} = \frac{4kT}{R_F}$
- Thermal noise from the collector resistor R_C, $\overline{I^2_{n,R_C}} = \frac{4kT}{R_C}$
- Thermal noise from the degenerative emitter resistor R_E, $\overline{I^2_{n,R_E}} = \frac{4kT}{R_E}$
- Effective short noise because of the base current in the transistors Q_1andQ_2, $\overline{I^2_{n,I_{B_{eff}}}} = \frac{2qI_{C_{eff}}}{\beta_1\beta_2}$
- Effective short noise because of the collector current in the transistors Q_1andQ_2, $\overline{I^2_{n,I_{C_{eff}}}} = 2qI_{C_{eff}}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2$

The effect of all these noise sources can be described by a single equivalent noise current source $\overline{I^2_{n,in}}$ at the input of the TIA. Hence it is written as shown in the equation 4.19. Here, thermal noise from the feedback resistor $\overline{I^2_{n,R_F}}$, collector resistances $\overline{I^2_{n,R_{C_1}}}$ and $\overline{I^2_{n,R_{C_2}}}$, and degenerative emitter resistor $\overline{I^2_{n,R_E}}$ contributes directly to the input. These noises have more impact at lower frequencies. Effective short noise from the base and collector currents $\overline{I^2_{n,I_{B_{eff}}}}$ and $\overline{I^2_{n,I_{C_{eff}}}}$ are referred to the input. As the frequency increases, IRN increases due to the addition of short noise from base and collector currents $I_{B_{eff}}$ and $I_{C_{eff}}$, respectively.

$$\overline{I^2_{n,TIA}}(f^2) = \frac{4kT}{R_F} + \frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_{C_{eff}}}{\beta_1\beta_2} + 2qI_{C_{eff}}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2 \quad \frac{A^2}{Hz} \tag{4.19}$$

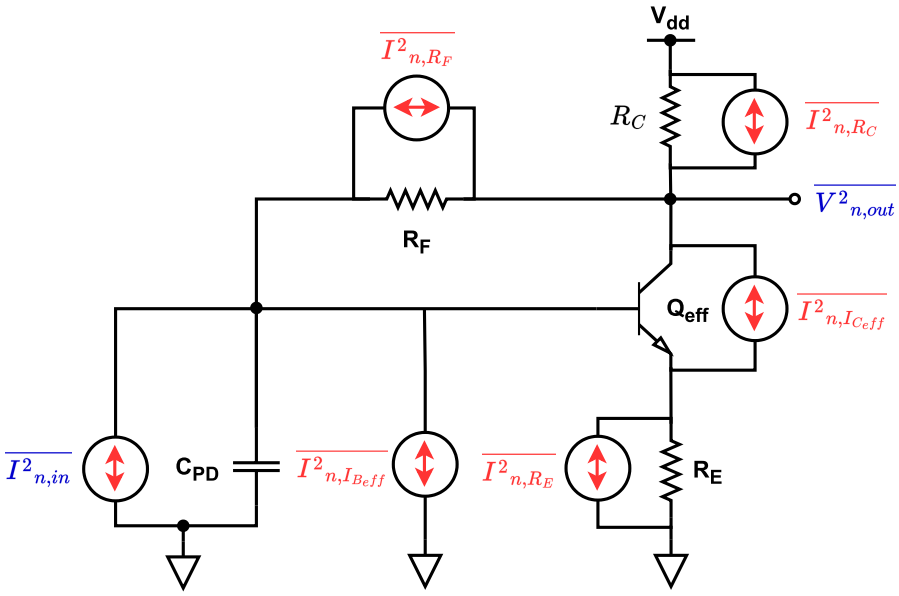

Figure 4.12: Darlington TIA with individual noise sources (in red).

In conclusion, for a given photodiode and technology, to improve gain in equation 4.17, multiple options like increasing I_{C_1}, I_{C_1}, R_E, $(R_C||R_F)$ are possible. From equation 4.18, increasing R_E will decrease the pole frequency of the p_1 and decreasing the value of $(R_C||R_F)$ will increase the pole frequency of the pole p_2. This can be done by taking low R_C and high R_F. Hence, increasing the bandwidth $(R_C||R_F)$ can be reduced but will affect the gain. But other parameters can improve transimpedance gain, which leads to a flexible design. While trying to increase R_E and R_F, IRN will reduce as shown in the equation 4.19. But reducing the value of R_C will increase the IRN due to the thermal noise of R_C. This increase in IRN due to R_C can be traded off with the decrease in IRN by R_E and R_F.

4.6 Conclusion

A summarized table 4.1 compares performance parameters for different TIA topologies discussed above. For achieving the targeted transimpedance gain (60 dBΩ), darlington pair topology offers more flexible options (varying β_1, R_E, g_{m_2}, and $(R_C||R_F)$) when compared to other topologies. In CB, CE, and RGC, the transimpedance gain can only be improved by varying one component. This gives an edge to DP TIA while improving transimpedance gain.

For achieving the required broadband bandwidth (40 GHz) in CB, I_C should be increased, and R_C should be reduced. But increasing I_C requires an increase of R_C to maintain the transistor's operating point. Hence CB topology cannot provide a nice trade-off between gain and bandwidth. The bandwidth improves by reducing the input pole frequency while maintaining the gain by selecting huge values of R_F in CE and R_E in RGC topologies. But these two topologies' output poles will be a trade-off between gain and bandwidth. In DP topology, both the poles are a trade-off for gain, but the dependence of poles and gain are on five different variables. Hence selecting these values can give optimal results.

According to the explanation in section 3.2.3, the input-referred noise PSD of

Table 4.1: Comparison of performance parameters for different TIA topologies.

	TIA DC Gain (Ω)	**Poles & Zeros** (Hz)	**IRN** (A^2/Hz)
CB	R_C	$p_1 = \frac{1}{2\pi\frac{1}{g_m}C_{in}}$, $p_2 = \frac{1}{2\pi R_C C_{out}}$	$\frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_C}{\beta} + 2qI_C\frac{(2\pi C_{in})^2}{{g_m}^2}f^2 + 4kTr_b(2\pi C_{PD})^2f^2$
CE RSF	$(R_C\|\|R_F)$	$p_1 = \frac{1}{2\pi R_F C_{in}}$, $p_2 = \frac{1}{2\pi(R_C\|\|R_F)C_{out}}$	$\frac{4kT}{R_C} + \frac{4kT}{R_F} + \frac{2qI_C}{\beta} + 2qI_C\frac{(2\pi C_{in})^2}{{g_m}^2}f^2 + 4kTr_b(2\pi C_{PD})^2f^2$
RGC	R_{C_2}	$p_1 = \frac{1}{2\pi R_E C_{in}}$, $z_1 = \frac{1}{2\pi(R_{C_2}\|\|R_E)C_{in}}$, $p_2 = \frac{1}{2\pi(R_{C_1}C_{out}+R_{C_2}C_{\pi_2})}$, $z_2 = \frac{1}{2\pi R_{C_1}C_{out}}$	$\frac{4kT}{R_{C_1}} + \frac{4kT}{R_{C_2}} + \frac{4kT}{R_E} + 2qI_{C_1}\frac{(2\pi C_{in})^2}{{g_{m_1}}^2}f^2 + 2qI_{C_2}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2$
DP RSF	$\beta_1 R_E$ $g_{m_2}(R_C\|\|R_F)$	$p_1 = \frac{1}{2\pi\beta_1 R_E C_{in}}$, $p_2 = \frac{1}{2\pi(R_C\|\|R_F)C_{out}}$	$\frac{4kT}{R_F} + \frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_{C_{eff}}}{\beta_1\beta_2} + 2qI_{C_{eff}}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2$

a TIA can be divided into three distinct noises. They are: 1. flicker noise (1/f), whose frequency dependence is inverse; 2. White or thermal noise is frequency-independent; 3. shot noise (f^2), whose magnitude is inversely correlated with the frequency square. Because BiCMOS transistors are less vulnerable, flicker noise will impact at a lower frequency, which is not considered in the IRN calculation. There are two-shot and three white noise terms in CB, CE, and RGC TIAs. In contrast, DP TIA has only one f^2 and four white noise terms. This clearly states that darling pair TIA will have lesser noise at higher frequencies when compared to CB, CE, and RGC TIAs. But the white noise coefficients in DP TIA can increase the overall noise.

Therefore, since CB topology offers less flexibility for a designer, it can be disregarded for further study. Broadband with a trade-off between noise and transimpedance gain is possible with CE and RGC topologies. High gain can be achieved with DP topology, but choosing the proper resistors and currents for the circuit is essential for getting the best results. The schematic designs for the CE, RGC, and DP topologies are finished in the following chapter. The outcomes of the schematic design process will serve as criteria for choosing the final topology for the layout design.

Chapter 5

Transimpedance Amplifier Schematic Design

Different topologies for TIA implementation were explained in the previous chapter. For each topology, the transimpedance gain, bandwidth, and IRN equations are displayed, and their performance is compared using the calculations. As a result of their severe restrictions and lack of flexibility to enhance TIA performance, resistor TIA and common base TIA topologies are withdrawn for the following step. Important factors to consider before beginning the schematic design are explained at the beginning of this chapter. The following topologies are schematically designed in the cadence tool, and their performance is compared.

- Common Emitter with Resistive Feedback
- Regulated Cascode
- Darlington Pair with Resistive Feedback

Differential Signaling

The differential circuits discussed in this thesis have several advantages over their single-ended counterparts. Differential signals are produced when two balanced signal pairs with opposite polarity and identical amplitude are transmitted. Any external disturbance will equally impact both signal paths. Equally coupled signals are muted as a common-mode disturbance as the information is encoded in the difference of the transferred signals. Due to this, differential circuits offer superior rejection of parasitically coupled signals and improved immunity to supply and substrate noise. They also have low crosstalk and instability issues, are immune to supply and ground inductance and allow for easier mounting methods and more durable designs. Because there is a natural reduction in even-order harmonics, there is less distortion. Additionally, they require only half the voltage swing across the load resistors compared to single-ended stages, which results in steeper pulse edges and higher achievable data rates with improved eye diagrams [54].

To achieve differentiality, two key circuit design considerations must be made: both signal paths must be as equal as possible, and the circuit may only amplify the differential signal, i.e., the common mode must be suppressed as much as is practicable. Because of this, each stage of an amplifier circuit must consist of two

identical transistors, one in each signal path. Those transistors must have a common reference point that is the same as the common mode of the input signal. When differential pairs and derived cells satisfy these conditions, both transistors have the floating base node as their reference. The differential pair has infinite common-mode rejection if the tail current source is ideal. Given that the circuits used in this thesis will use differential input signalling, the current obtained from the photodiode (11.25 μA) to the TIA, as mentioned in the section 1.3 will be split into four distinct phases. A current of 2.8125 μA will be applied to each phase of the signal.

DC Operating Point

Before beginning the schematic design, it is crucial to talk about the transistor's behaviour and choose the DC operating point current that will allow it to operate in the active region. The DC operating point, also referred to as the quiescent or Q point is when transistor has no input current. The I-V characteristic graph can be used to determine the Q point of any transistor. When there is no input signal, an active region can be found by adjusting the collector current I_C and collector-emitter voltage V_{CE} values. The transistor functions as an amplifier in this area when it is active (the input signal is amplified at the output). A load line should be drawn to determine the operating point. The maximum collector current in the circuit is obtained at the point on the Y-axis (saturation point), and the maximum CE voltage is considered at the point on the X-axis (the cutoff point). The DC operating point should be chosen, so the input signal is amplified perfectly to the output without clipping. Therefore, I_C and V_{CE} for the circuit implementations illustrated in this thesis should be in the range of 3–4 mA and 1-2 V, respectively.

Current Mirrors for DC Bias

Given the above analysis of the DC operating point, I_C should be 3 to 4 mA range. Biasing is the process of supplying DC voltage that aids in the circuit's operation. A transistor is biased so that the CB junction is reverse biased, and the EB junction is forward biased, keeping the transistor in the active region where it can function as an amplifier. An ideal current source can supply the transistor's bias current, but ideal current sources don't exist. Since a current mirror circuit will supply a constant current to the circuit, it can be used in place of an ideal current source.

An analogue circuit known as the current mirror detects the reference current and generates a copy or several copies with identical properties. A diode-connected transistor is used in current mirrors to make the reference current stable, as the source of the reference current is the replicated current. The replicated current may be equal to the reference current ($I_{copy} = I_{ref}$), a multiple of the reference current ($I_{copy} = N * I_{ref}$ or $I_{copy} = (1/N) * I_{ref}$), or a fraction of the reference current. The current mirror circuit is depicted in Figure 5.1 with a reference current I_{ref} flowing to the collector of the BJT Q_1 connected to the diode. The bias current I_{copy} that must be provided to the core transistors of TIA is equal to the collector current in transistor Q_2. V_{BE_2} can alter I_{copy} because $I_C \approx I_S exp(V_{BE}/V_T)$ can be changed. I_{copy} can be controlled by V_{BE_1}, which I_{ref} can control because $V_{BE_1} = V_{BE_2}$. Equation 5.1 demonstrates the copying of the reference current provided to Q_1 as an output at Q_2.

$$
\begin{aligned}
I_{copy} &\approx I_{S_2} \exp\left(\frac{V_{BE_2}}{V_T}\right) \\
I_{ref} &\approx I_{S_1} \exp\left(\frac{V_{BE_1}}{V_T}\right) \\
I_{copy} &= \frac{I_{S_2}}{I_{S_1}} I_{ref}
\end{aligned}
\tag{5.1}
$$

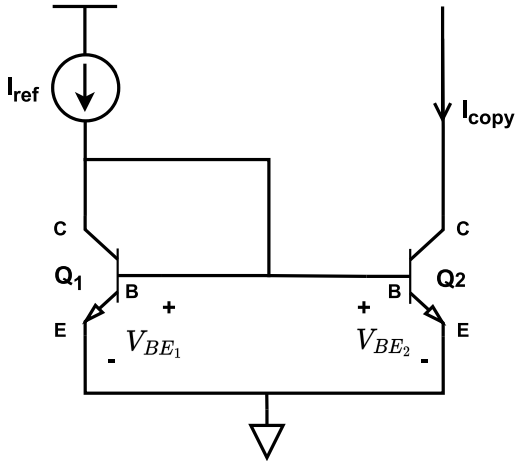

Figure 5.1: Current mirror circuit for DC bias.

For simplicity, early effect and base resistance are ignored in equation 5.1. Here I_S and V_T are the reverse saturation current and thermal voltage of a transistor respectively. So when the reverse saturation current I_{S_1} and I_{S_2} of both transistors Q_1 and Q_2 are the same, then $I_{copy} = I_{ref}$.

5.1 Common Emitter with Negative Resistive Feedback TIA

This section introduces the schematic design for the common emitter TIA with negative resistive feedback. This topology was explained in detail in the section 4.3. For the selection of R_C and R_F in the common emitter TIA, a trade-off between gain, bandwidth and noise should be considered. To achieve the required specifications shown in the section 1.3, the values of R_C and R_F are considered as 900 Ω and 1100 Ω, respectively. From the equation 4.10, the transimpedance gain achieved after substituting these values is 53.89 dBΩ. The calculated poles from equation 4.11 are at 11.84 and 120 GHz, achieving a bandwidth of 110 GHz. For finding the noise, C_{in} = 12.21 fF is considered along with the R_C and R_F values in the equation 4.12. The calculated IRN achieved after CE topology is 47 pA/$\sqrt{\text{Hz}}$. Although these values are just predictions for the initial start, the common emitter TIAs noise exceeds the target.

A final schematic after tuning the values of resistors, biasing current to achieved optimal results is shown in the figure 5.2. The designed CE TIA with negative resistive Feedback has a differential input and differential output using the transistors

Q_1 and Q_2. Current mirror circuit consisting transistors Q_3, Q_4, and Q_5 are used for DC biasing. Table 5.1 shows the final values of the resistors and DC operating points of the circuit.

In the figure 5.2, a final schematic created by adjusting the resistor values and biasing current to achieve the best results is displayed. The transistors Q_1 and Q_2 are used to create a differential input and output for the CE TIA with negative resistive Feedback that was designed. A current mirror circuit made up of transistors Q_3, Q_4, and Q_5 is used for DC biasing. The resistors' final values and the circuit's DC operating points are displayed in table 5.1.

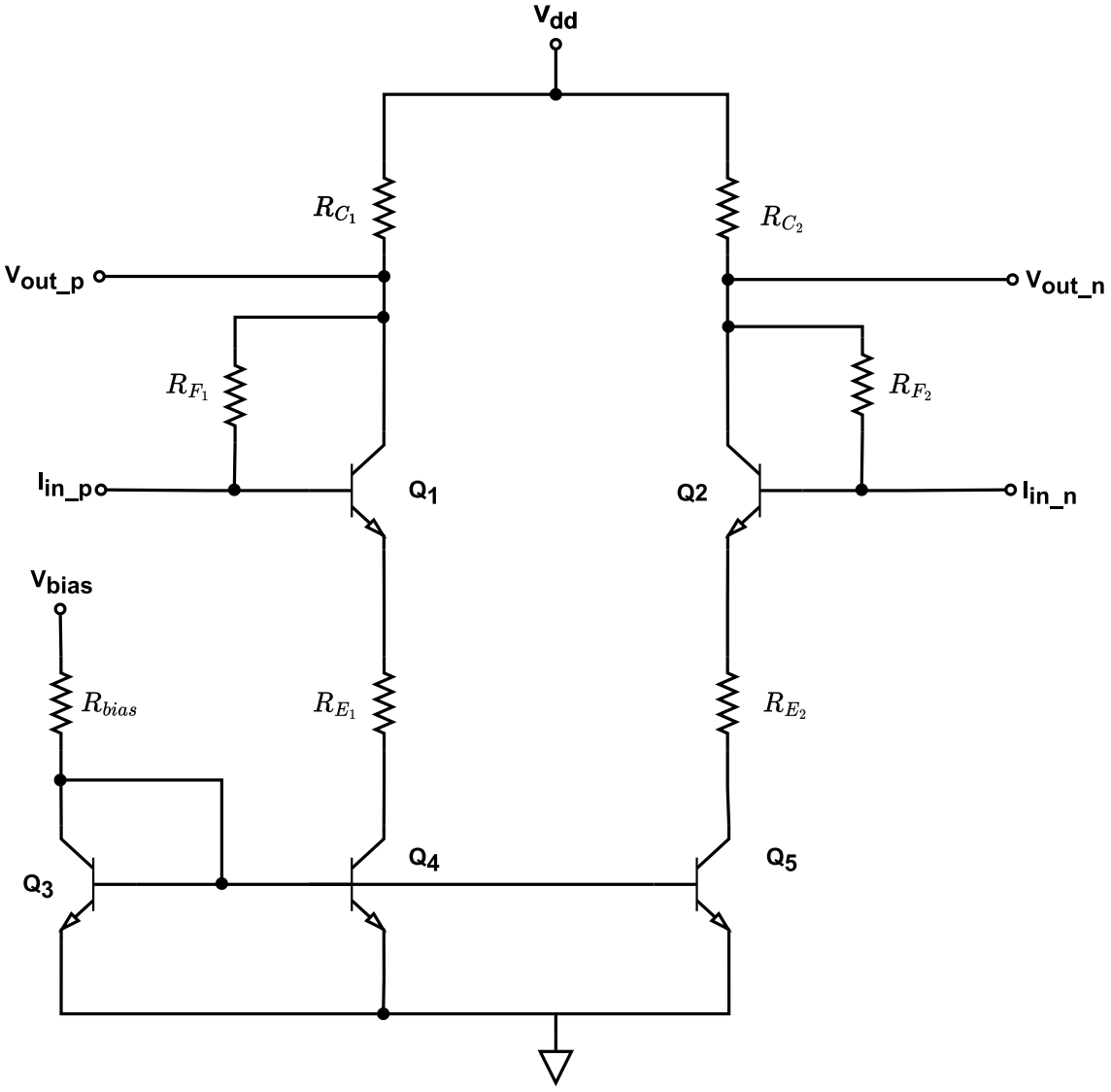

Figure 5.2: Schematic diagram of a Common Emitter with Negative Resistive Feedback TIA

Results

A DC transimpedance gain of 53.62 dBΩ is obtained from calculations shown in 4.10 with the final values of the resistors. A plot of the transimpedance gain vs frequency is shown in figure 5.3. At the operating frequency of 50 GHz, the CE TIA

Table 5.1: Final values of components in CE TIA with negative resistive Feedback.

Name	Value
$R_{C_1} = R_{C_2}$ (Ω)	800
$R_{F_1} = R_{F_2}$ (Ω)	1200
$R_{E_1} = R_{E_1}$ (Ω)	700
R_{bias} (Ω)	340
V_{bias} (V)	2
V_{cc} (V)	4
$I_{C_1} = I_{C_2}$ (mA)	3.285

has achieved 51.17 dBΩ of transimpedance gain. Still, a 9 dBΩ transimpedance gain is required to achieve the target. A broad 3dB bandwidth of 250.5 GHz is obtained from this CE TIA, starting from 10 GHz to 266.5 GHz. There is a huge headroom for the bandwidth when compared to the required target. By reducing the bandwidth, the transimpedance gain of the CE TIA can be improved.

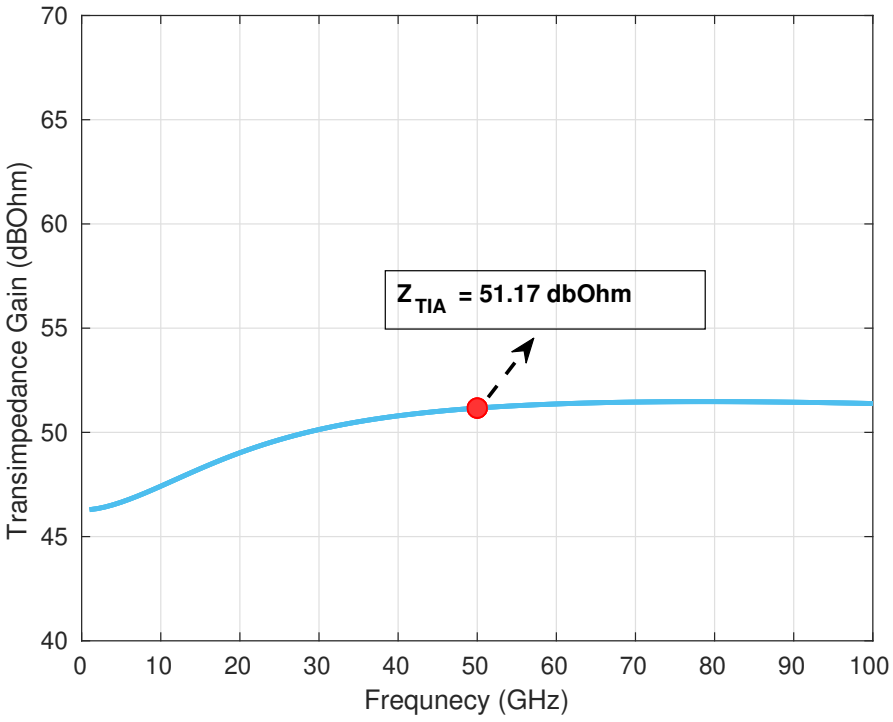

Figure 5.3: Transimpedance gain and bandwidth results of the CE TIA.

The graph shown in figure 5.4 compares the IRN obtained after the schematic design and IRN calculated from equation 4.12. At the centre frequency of 50 GHz, the IRN obtained from the schematic design is 18.2 pA/$\sqrt{\text{Hz}}$ and that obtained from the derived equation is 16.4 pA/$\sqrt{\text{Hz}}$. At the lower frequencies, additional flicker noise is added to the circuit, which is not considered in the equation 4.12. The

flicker noise is given by $\frac{2qf_c(I_B+I_C)}{F}$, where f_c is the frequency where the magnitudes of the white and flicker noises of a device are equal.

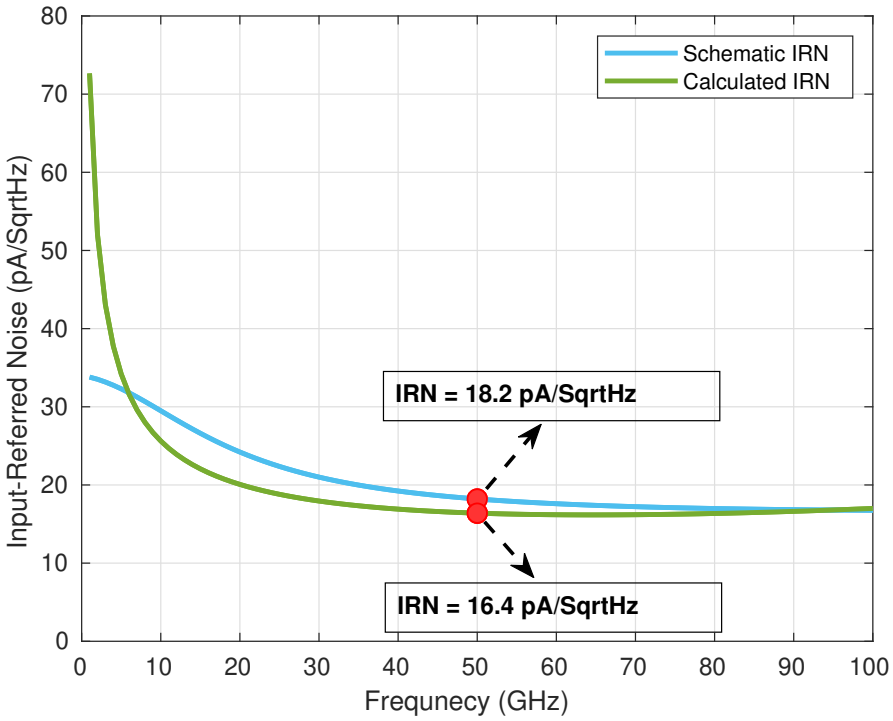

Figure 5.4: Input-Referred Noise of CE TIA.

Transimpedance gain, bandwidth, and IRN are obtained as expected from the calculations shown in the section 4.3. Even though the gain did not match the target, it can be improved by reducing the bandwidth, which has huge headroom. But the IRN obtained for CE TIA has an additional flicker noise added to the circuit at lower frequencies which cannot be avoided. Hence further proceeding does not need to be done to improve the transimpedance gain.

5.2 Regulated Cascode TIA

The schematic for the regulated cascode TIA is introduced in this section. The section 4.4 provided a detailed explanation of this topology. Trade-offs between gain, bandwidth, and noise should be considered when choosing R_{C_2}. The value of R_{C_2} is considered to be 1000 Ω to meet the specifications shown in the section referred to as 1.3. The transimpedance gain obtained after substituting the R_{C_2} in the equation 4.13 is 60 dBΩ. To determine the noise, the values of C_{in} = 17.77 fF, R_{C_1} = 800Ω, and R_E = 500Ω are taken into account in the equation 4.16. 18.5 pA/$\sqrt{\text{Hz}}$ is the calculated IRN obtained after CE topology. Equations 4.14, 4.15 yielded calculated poles and zeros at 12, 26, and 204 GHz, resulting in a bandwidth of 178 GHz. With these initial values, the regulated cascode TIA is meeting the objectives. But these figures are just predictions; they do not represent the final outcome.

After tuning the values of resistors, a final schematic, biasing current to achieve

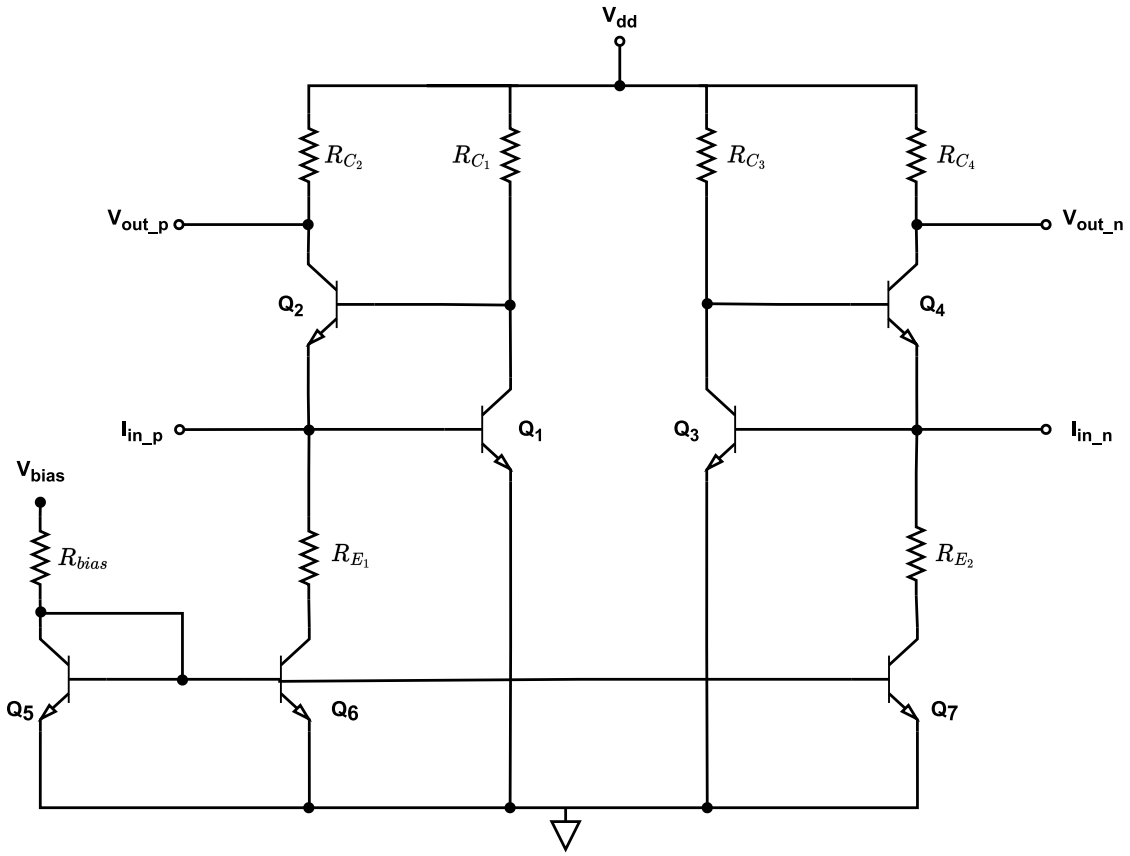

Figure 5.5: Schematic diagram of a Regulated Cascode TIA

optimal results, is shown in figure 5.5. The designed regulated cascode TIA has a differential input using the transistors pair Q_1, Q_2, and differential output using the transistors Q_3, Q_4. Current mirror circuits consisting of transistors Q_5, Q_6, and Q_7 are used for DC biasing. Table 5.2 shows the final values of the circuit's resistors and DC operating points.

Table 5.2: Final values of components in RGC TIA.

Name	**Value**
$R_{C_1} = R_{C_3}$ (Ω)	600
$R_{C_2} = R_{C_4}$ (Ω)	400
$R_{E_1} = R_{E_2}$ (Ω)	700
R_{bias} (Ω)	1000
V_{bias} (V)	3.5
V_{cc} (V)	3
$I_{C_1} = I_{C_3}$ (mA)	2.135
$I_{C_2} = I_{C_4}$ (mA)	1.131

Results

With the resistors' final values, the calculations shown in 4.13 yield a DC transimpedance gain of 52.04 dBΩ. Figure 5.6 displays a plot of the transimpedance gain. The regulated cascode TIA has 50.83 dBΩ transimpedance gain at the 50 GHz centre frequency. However, a 9 dBΩ transimpedance gain is needed to hit the target. This controlled cascode TIA provides a wide 3dB bandwidth ranging from 0 GHz to 94.66 GHz. When compared to the desired target, the bandwidth has a huge headroom. The transimpedance gain of the CE TIA can be increased by reducing the bandwidth.

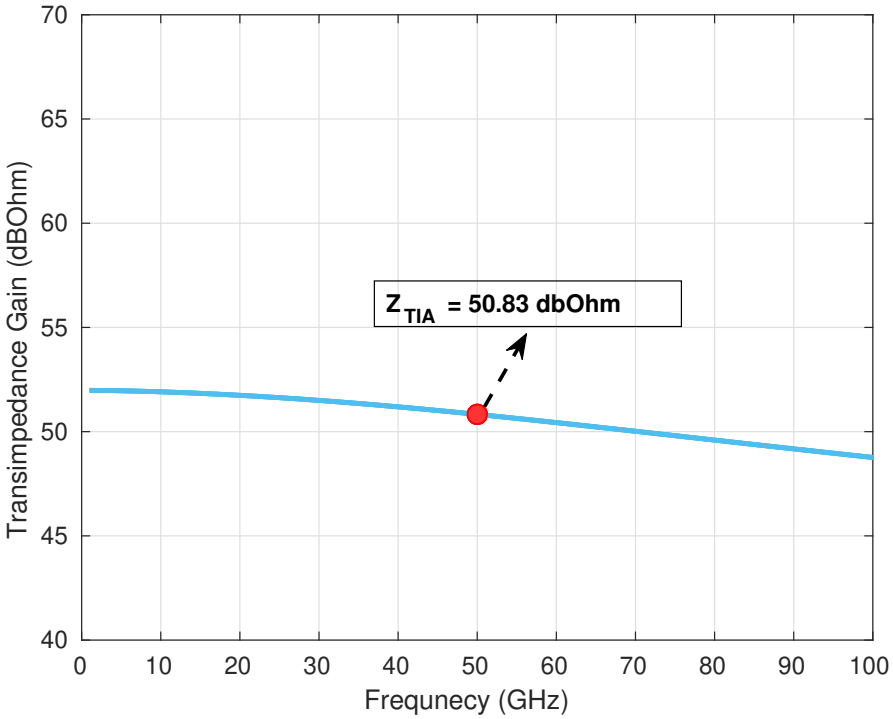

Figure 5.6: Transimpedance gain and bandwidth results of the Regulated Cascode TIA.

The IRN obtained after the schematic design and the IRN calculated from equation 5.7 are compared in the graph in figure 4.16. The IRN obtained from the schematic design is 19.52 pA/$\sqrt{\text{Hz}}$ at the centre frequency of 50 GHz, while the IRN derived from the equation is 20.81 pA/$\sqrt{\text{Hz}}$. This regulated cascode TIA does not exhibit a flicker noise effect, adversely affecting the CB TIA's noise performance.

From the calculations displayed in the section 4.4 transimpedance gain, bandwidth, and IRN are obtained as anticipated. Even though the gain did not meet the target, there is still room for improvement by lowering the bandwidth. However, there is a trade-off with the input-referred noise. IRN increases, which has no headroom to lose, as the gain is increased by adjusting the resistances and the DC biasing point. Therefore, additional steps are not required to increase the transimpedance gain.

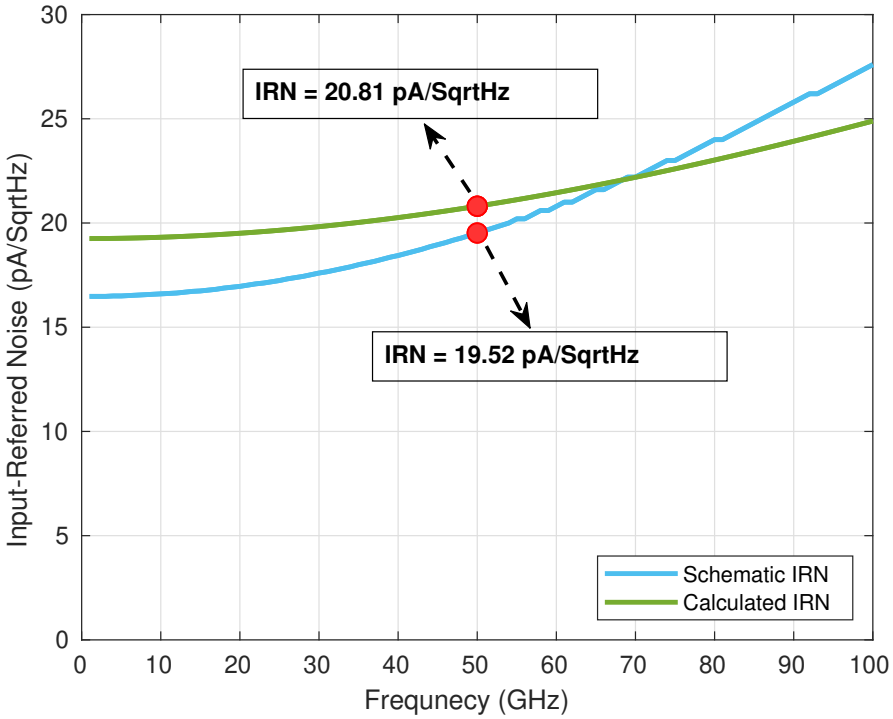

Figure 5.7: Input-Referred Noise of Regulated Cascode TIA.

5.3 Darlington Pair with Negative Resistive Feedback TIA

The schematic design for the Darlington pair TIA with negative resistive feedback is introduced in this section. This topology was thoroughly discussed in the section titled 4.5. With a high current gain, the two transistors in a darlington pair operate as a single transistor. It has a base, emitter, and collector terminals as its three terminals. These are equivalent to a standard individual transistor's terminals. To activate this transistor, there must be 0.7V across the darlington pair's series-connected BE terminals. Therefore, 1.4V is required for it to turn on. Darlington transistor pairs use low-power primary transistors but typically require high-power secondary transistors.

For the selection of R_{C_1}, R_{C_2}, R_{E_1}, and R_{F_1} values in the darlington pair TIA, a trade-off between gain, bandwidth and noise should be considered. To achieve the required specifications shown in the section 1.3, the values of R_{C_1}, R_{C_2}, R_{E_1}, and R_{F_1} are considered as 30 Ω, 30 Ω, 100 Ω and 500 Ω respectively. From the equation 4.17, the transimpedance gain achieved after substituting these values is 71.3 dBΩ. The calculated poles from equation 4.18 are at 4.7 and 57 GHz, achieving a bandwidth of 52.3 GHz. For finding the noise, C_{in} = 12.21 fF is considered in the equation 4.19, and the calculated IRN achieved is 28.5 pA/$\sqrt{\text{Hz}}$. The darlington pair TIAs noise exceeds the target, but with these initial values, gain and bandwidth are achievable. These numbers represent starting values only; they do not represent final outcomes.

Figure 5.8 depicts a final schematic that uses biasing current to achieve the best results after adjusting the resistor values. The designed regulated cascode TIA has

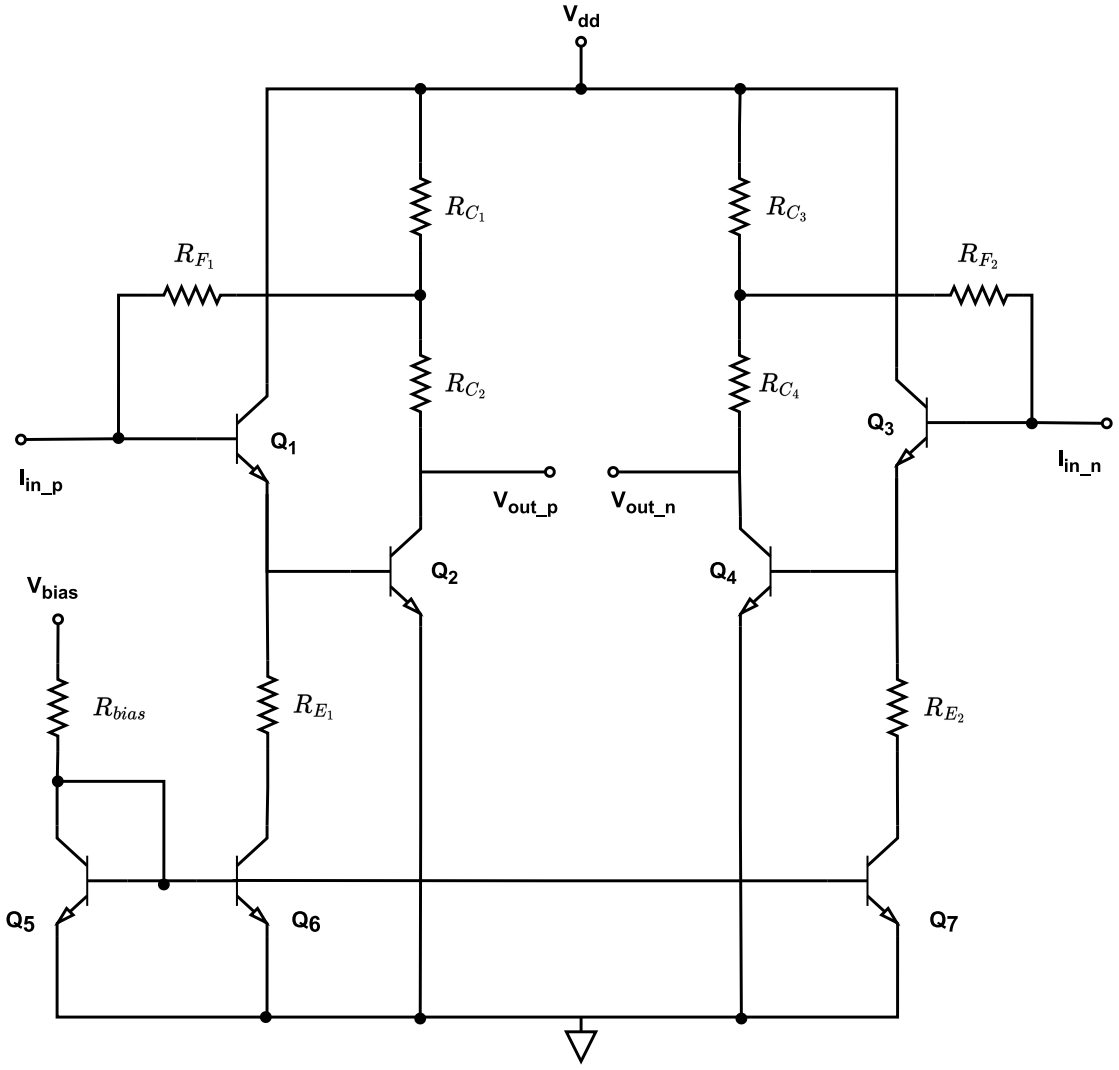

Figure 5.8: Schematic diagram of a Darlington pair with Negative Resistive Feedback TIA

Table 5.3: Final values of components in DP TIA with negative resistive Feedback.

Name	**Value**
$R_{C_1} = R_{C_3}$ (Ω)	60
$R_{C_2} = R_{C_4}$ (Ω)	80
$R_{F_1} = R_{F_2}$ (Ω)	730
$R_{E_1} = R_{E_2}$ (Ω)	250
R_{bias} (Ω)	340
$V_{bias} = V_{cc}$ (V)	2
I_{C_1} (mA)	3
I_{C_2} (mA)	3.28

a differential input using the transistors Q_1 and Q_2 and differential output using the transistors Q_3 and Q_4. Current mirror circuits consisting of transistors Q_5, Q_6, and Q_7 are used for DC biasing. Table 5.3 shows the final values of the circuit's resistors and DC operating points.

Results

A DC transimpedance gain of 69.21 dBΩ is obtained from calculations shown in 4.17 with the final values of the resistors. A plot of the transimpedance gain is shown in figure 5.9. At the centre frequency 50 GHz, the darlington pair TIA has achieved 64.38 dBΩ of transimpedance gain. A broad 3dB-bandwidth of 66.29 GHz is obtained from this darlington pair TIA starting from 0 GHz to 66.29 GHz. Both the gain and noise specifications are achieved from this design.

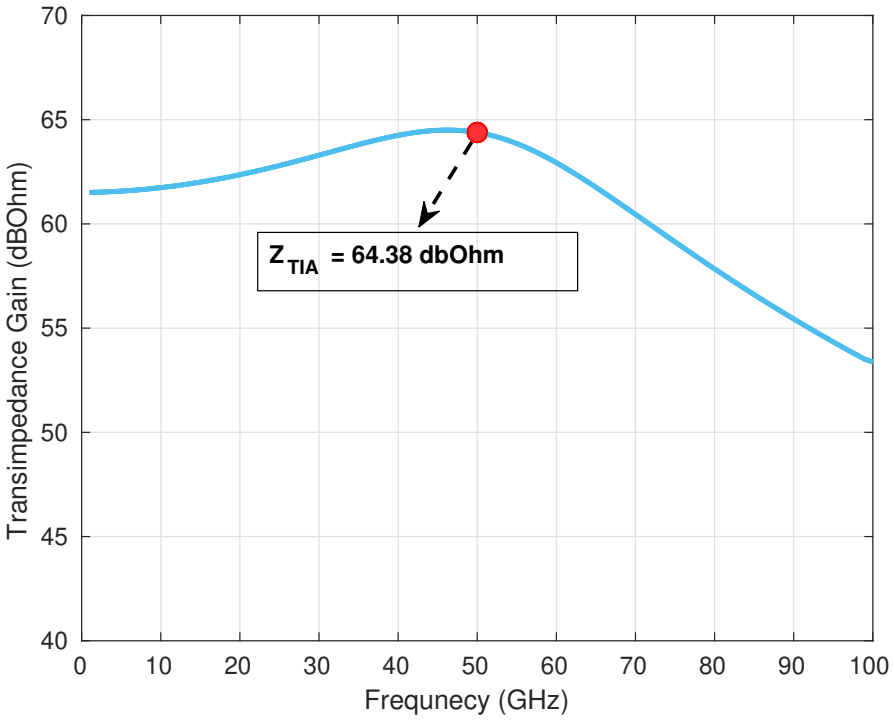

Figure 5.9: Transimpedance gain and bandwidth results of the Darlington Pair TIA.

The graph shown in figure 5.10 compares the IRN obtained after the schematic design and IRN calculated from equation 4.19. At the centre frequency of 50 GHz, the IRN obtained from the schematic design is 15.49 pA/$\sqrt{\text{Hz}}$ and that obtained from the derived equation is 21.66 pA/$\sqrt{\text{Hz}}$. The flicker noise effect that affected the CB TIA's noise performance is not seen in this darlington pair TIA.

Transimpedance gain, bandwidth, and IRN are obtained as expected from the calculations shown in the section 4.4. All three targets of this TIA design: Gain, bandwidth, and noise are achieved with sufficient headroom for further variations by this darlington pair TIA.

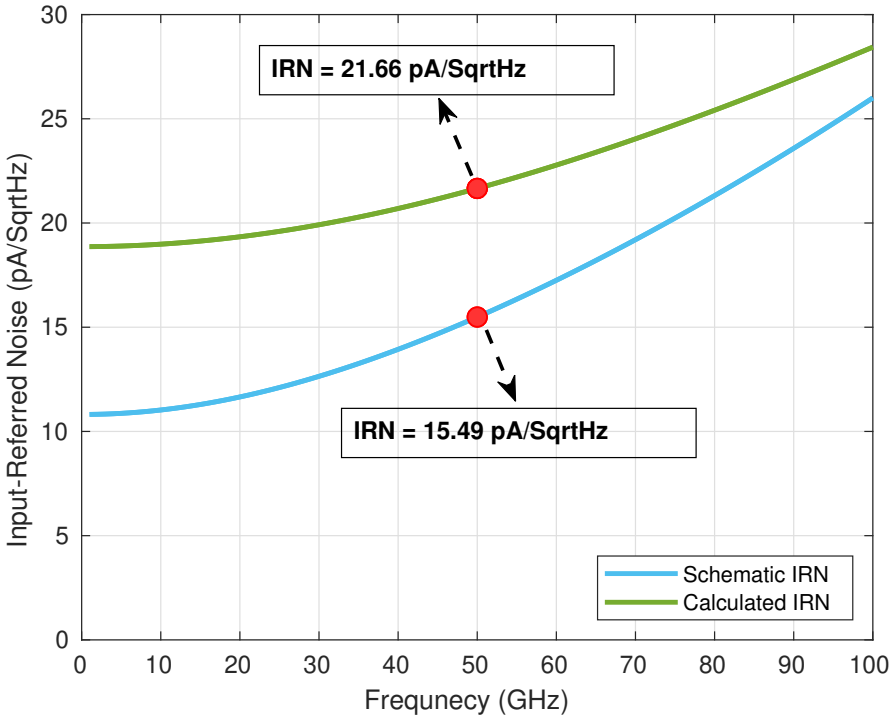

Figure 5.10: Input-Referred Noise of Darlington Pair TIA.

5.4 Conclusion

In conclusion, Table 5.4 compares the outcomes of various schematic designs to the demanded specifications. Here, we can see that only the darlington pair has produced the desired outcomes for every criterion. Large bandwidth in CE and RGC topologies can be sacrificed to increase gain, but the noise increases. It is challenging to choose between increasing gain and IRN because the IRN for these two topologies is already very close to its limit. Darlington pair TIAs have met all of the specifications, so CE and RGC TIAs need no further improvement. As a result, the schematic results and the layout for the darlington pair TIA with resistive feedback are compared in the following chapter.

Table 5.4: Comparison of results obtained from different schematic designs

	Target	**CE RSF**	**RGC**	**DP RSF**
Transimpedance Gain (dBΩ)	60	51.17	50.83	64.38
Bandwidth (GHz)	40	250.5	94.66	66.29
Input-Referred Noise ($pA/\sqrt{Hz}$)	20	18.2	19.52	15.49
Output Matching, S_{22} (dB)		-2.01	-2.16	-7.87
Stability Factor, KF	>1	3.05	6.48	2.18
Power Consumption (mW)		22.17	28.73	31.53

Chapter 6

Transimpedance Amplifier Layout Design

Once the proposed TIA has been designed, and its results are validated in all the processed corners, it is necessary to implement the layout. So after the layout implementation, the next step is to validate all the results again using the TIA's post-layout simulations. Hence, this chapter explores the layout implementation for the proposed darlington pair TIA with negative resistive Feedback. Then, post-layout simulations are illustrated. Finally, this chapter is concluded with a brief discussion on the extracted parasitics and bandwidth enhancement. Hence, the main goal of this chapter can be divided into:

- An optimum floor-planning and placement should be done to occupy the minimum area possible.
- A good routing should be done for minimizing the parasitics.
- Implementing the TIA's layout in order to make the circuit as symmetrical as possible in order to get an identical results to the of a schematic.
- Post layout improvements, if necessary.

Floor-planning

Floor planning, placement, and routing are the fundamental steps in creating a layout. Floor planning provides a rough estimate of placement strategies to achieve minimum circuit area. Followed by placing the various components in the best possible positions based on the design goal. The pin positions for the darlington pair TIA are presented in figure 6.1. The layout can be divided into three main parts, 1. input and output DC blocks, 2. darlington pair core block, and 3. DC biasing circuit. While doing the floor planning, the primary consideration is to keep a minimal path for the AC signal to travel from input to output pins. AC signal travels from input pins I_{in_p} and I_{in_n} to output pins V_{out_p} and V_{out_n} trough darlington pair TIA's p and n core respectively. So this path should be as minimal as possible in the layout for reducing parasitics to improve the results. Hence, the quality of the layout is decided here as issues like noise and parasitics of interconnects are considered. The last step is to route these blocks with a proper selection of available metals and vias.

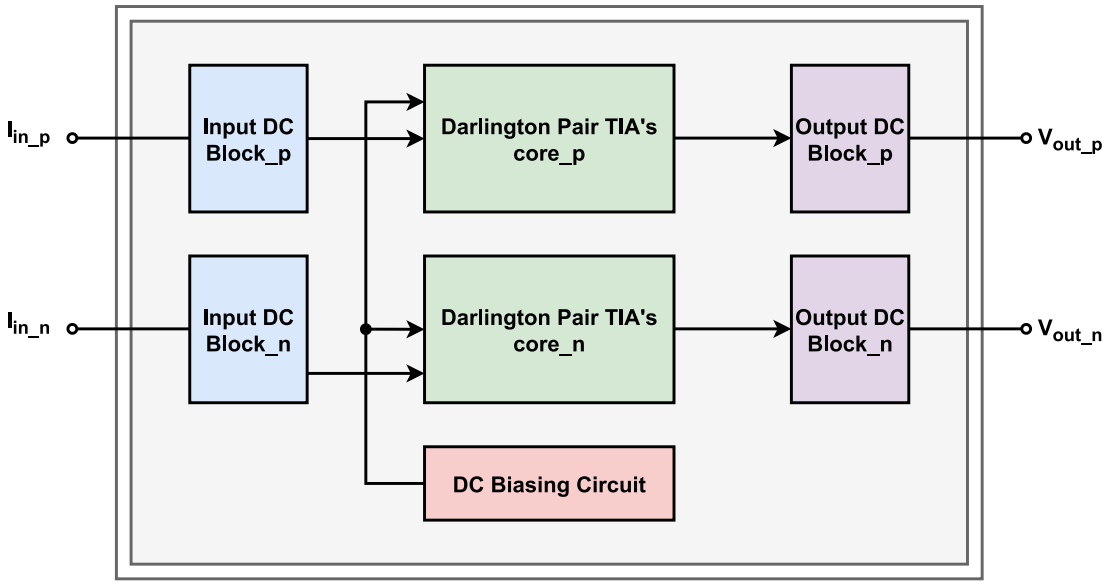

Figure 6.1: Floor planning diagram for the darlington pair TIAs layout.

Routing

The performances of an analogue circuit are critically dependent on parasitics. Stray resistances, due to the finite resistivity of the materials used for interconnections, cause undesired voltage drops and affect current values. Stray capacitances may introduce signal crosstalk and together with resistances, modify the frequency behaviour of the circuit. Furthermore, differential structures require matching the parasitics associated with topologically symmetric nets [55]. As floor planning decides the position of different blocks in the layout, routing is used to connect those blocks with metal wires according to their working. In the layout, components like transistors, resistors, and capacitors have inbuilt pins connected using metal wires. The main targets to keep in mind while routing are:

- Lower parasitics by reducing the area utilization.
- Create connections such that all terminals assigned to the same net are connected (no open terminals).
- No terminals assigned to different nets should be connected (no short terminals).
- Follow all design rules by the technology.
- Avoid cross-talk problems by placing two adjacent wires with adequate distance between them.

A total of 8 metal wire layers are available in the IHP 0.13 μm SiGe BiCMOS technology for using as interconnects. The list of metals and their thickness is shown in the table 6.1. Each metal layer add some additional parasitic resistance into the circuit which will degrade the performance of the TIA. The parasitic resistance of a metal layer can be calculated by using $R_{parasitic} = \frac{\rho L}{A}\Omega$. Where, ρ is electrical conductivity of the metal, L is the length of the metal layer, and A is the area of the

metal layer. In order to reduce the parasitic resistance, three different approaches can be implemented. Firstly, by reducing the length of the interconnected metal between two pin. This can be achieved by placing the same net components very near while routing. Secondly, by using the higher metal layers (TTC1, TTC2, TTA1, TTA2) which has more thickness when compared with the lower layers. Since, the area of the metal layer can be increased by increasing the thickness. Finally, Using metal layers made of aluminium (TTA1, TTA2) rather than using the metal layers with copper. Since aluminium has low electrical conductivity ρ than copper. As a conclusion, ThinAl (TTA1) and ThickAl (TTA2) metal layers will be used for the AC signal path. Metal 4 will be used for the DC signaling path. ThickCu 1 and ThickCu 2 will be used for interconnects with larger lengths. Finally, Metal 1 to 4 are used for shorter interconnect lengths.

Table 6.1: Thickness of different metal layers available for routing.

Metal Layer Name	**Code**	**Thickness** (nm)
Metal 1, 2, 3 and 4	TM1, TM2, TM3, and TM4	Less
ThickCu 1 and 2	TTC1 and TTC2	More
ThinAl	TTA1	Less
ThickAl	TTA2	More

6.1 Initial Layout

The designed darlington pair TIA was fabricated in an IHP 0.13 μm SiGe BiCMOS process (IHP SG13G2). Figure 6.2 shows the layout of the proposed design. Similar to the floor planning shown in figure 6.1, the entire block of the TIA is represented in the middle of the figure. The 4 DC block capacitors are placed on the left and right sides of the TIA core circuit. At the bottom, DC biasing circuit is placed. The layout occupies 0.00628 mm^2 (99.94×62.85 μm^2) area in which each core occupies 0.000419 mm^2 (22.45×18.68 μm^2) area. The area occupied by each DC block is 0.000289 mm^2 (17×17 μm^2). The DC biasing circuit takes 0.000433 mm^2 (31.96×13.56 μm^2) in the layout. The rest area is either occupied by the routing metals or wasted.

6.1.1 Extraction Process

Various tools are available in the Cadence Virtuoso environment to check the correctness of the layout. The process of checking the layout's proper functionality is termed layout extraction. It is comprised of two main steps. Design Rules Check (DRC) and Layout vs Schematic Check (LVS). Design Rule Checking (DRC) verifies whether a specific design meets the constraints imposed by the process technology to be used for its manufacturing. It is an essential part of the physical design flow and ensures the design will not result in a chip failure. Only when a layout is free of DRC errors is it approved to proceed to the next steps. Each process technology will have its own set of rules. The number of DRC rules and the complexity of rules increases as the manufacturing technology shrinks at advanced nodes. Some of the DRC rules which appeared and cleared off during the layout are:

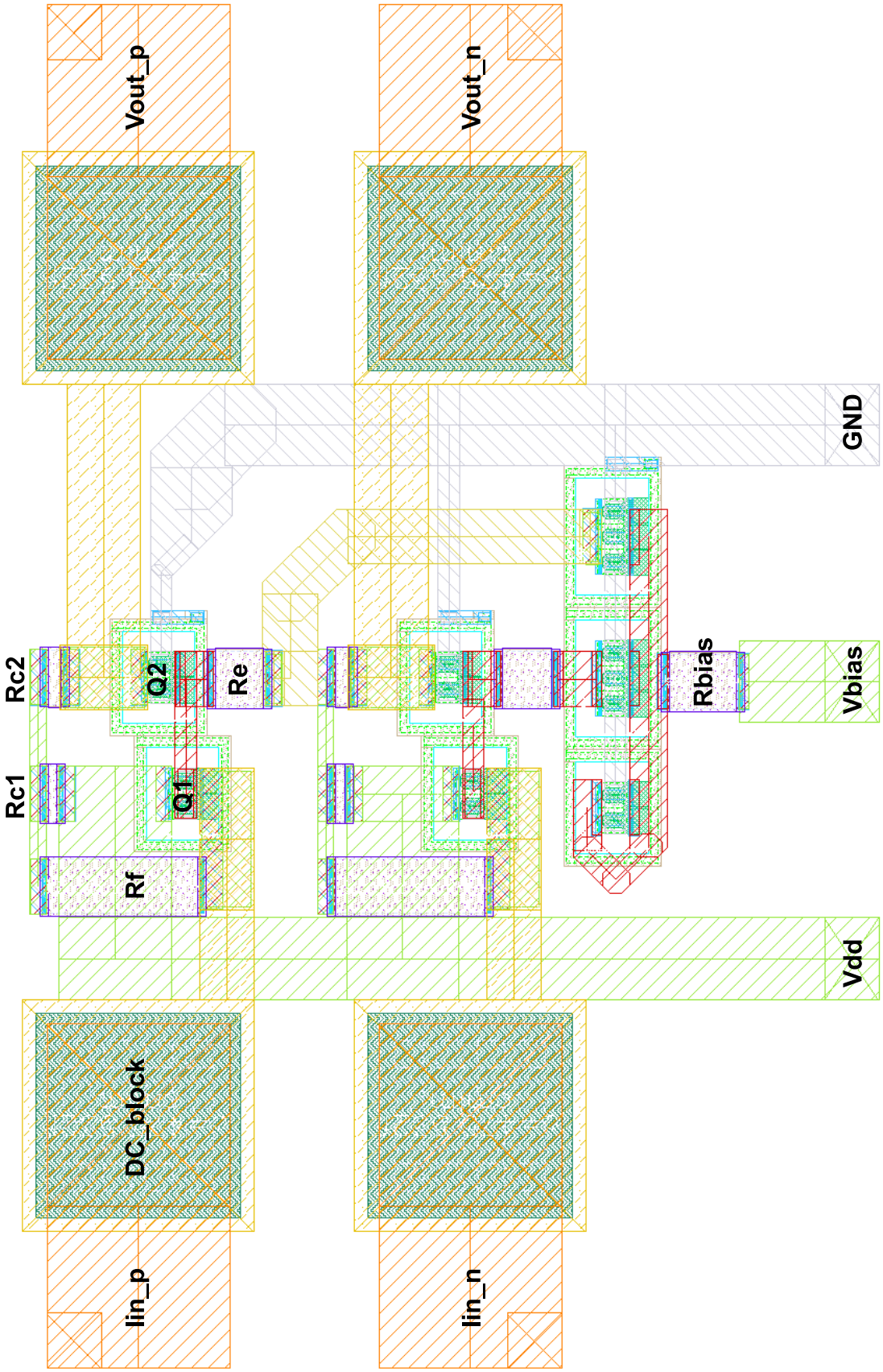

Figure 6.2: Initial layout of the designed darlington pair TIA with resistive feedback.

- Minimum width
- Minimum spacing
- Minimum area enclosure
- pSD Overlapping
- Shape and angle of the metal

The next step is to check the layout against the schematic it is designed for. This is done using the Layout vs Schematic Check (LVS) tool. While DRC ensures that all the design rules have been obeyed, LVS helps us check the layout's authenticity. At the same time, doing LVS checks, all the layers, terminals, pins, underlying wiring, and vias are connected between them and extracted and defined. Typical errors encountered during LVS checks are: short circuits, open, mismatched components and parameters, and missing components. Changes are made until the clean report is generated from LVS. A clean DRC and LVS ensure that the layout has adhered to all the design constraints set by technology and that all netlists and components are matched between schematic and layout. A DRC and LVS check is performed on the layout shown in figure 6.2, and a clean result is obtained. The layout, however, has several parasitic resistance and capacitance that need to be examined and rectified. This is done in post-layout simulations.

6.1.2 Post-Layout Simulation Results

DRC and LVS simulations are vital, but the overall efficiency is checked only after post-layout simulations (PEX analysis). PEX simulations check the accuracy and quality of outputs by extracting the parasitic resistances and capacitances. Then the extracted view is added to pre-layout test benches to estimate vital design parameters like transimpedance gain, bandwidth, and input-referred noise values. Although pre-layout simulations help us develop and verify design constraints, post-layout simulations help us reveal their validity of them before fabrication.

From the post-layout simulation, the initial TIA layout shown in figure 6.2 has a maximum transimpedance gain of 62.81 dBΩ and a corresponding 3-dB bandwidth of 57.96 GHz. The simulated graph for the transimpedance gain response of the initial layout is shown in Figure 6.3. The graph compares the frequency response of the designed TIA pre and post-layout. As discussed in the section 5.3, the transimpedance gain achieved from the schematic design was 64.38 dBΩ and its corresponding 3-dB bandwidth of 66.29 GHz. There is a loss of around 1.6 dBΩ transimpedance gain after the post layout and a decrease of around 9 GHz 3-dB bandwidth. This decrease in performance is due to the addition of parasitic resistances and capacitances into the circuit. As shown in figure 6.3, at lower frequencies, the frequency response of the TIA is similar, but a 4 dBΩ drop can be seen at higher frequencies (after 60 GHz). This gain drop leads to a drop in overall 3-dB bandwidth. The main reason for this loss is the miller effect, explained in the next section. The final layout after the necessary changes to compensate for the miller effect is shown in the coming section.

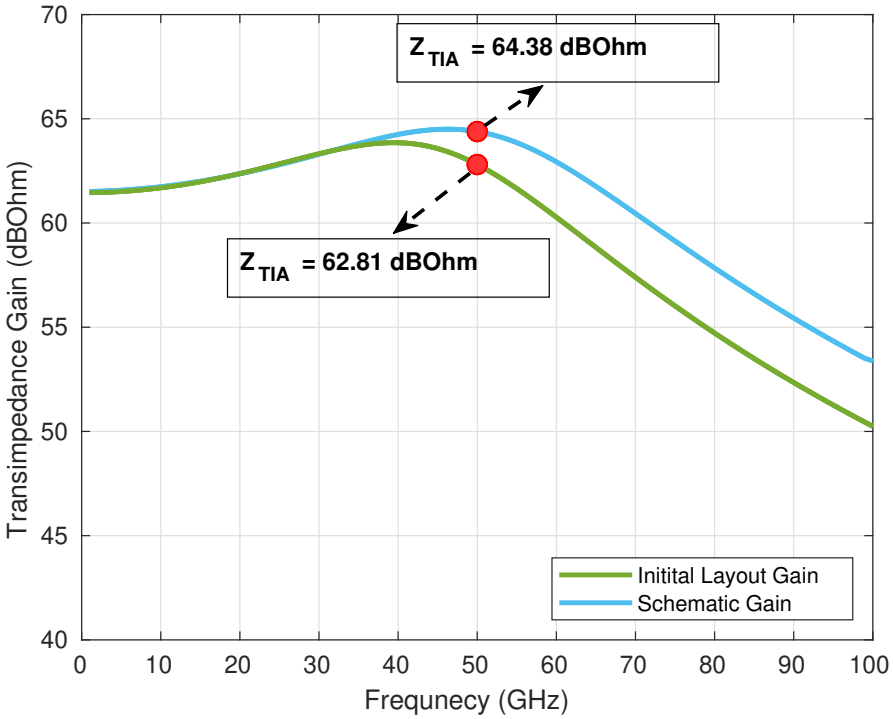

Figure 6.3: Transimpedance gain and bandwidth results of the schematic vs initial layout.

6.1.3 Miller Effect

The parasitic capacitance between the TIA's output and input terminals causes the Miller capacitance to form. The presence of the miller capacitor causes the high-frequency pole's value to drop because it is inversely proportional to the total capacitance ($P_2 = \frac{1}{2\pi RC}$) resulting in a 3-dB bandwidth reduction. The parasitic base-collector capacitance is multiplied by the transistor gain by the miller effect, creating an input impedance with a sizable capacitive component. At low frequencies, the input impedance is essentially just its small signal input resistance (r_π), but at higher frequencies, any capacitance detected at the input reduces the input impedance. A resistive feedback darlington pair topology is used to implement the designed TIA. The parasitic capacitance in the feedback resistor will be added to the amount of capacitance in the high-frequency pole following the parasitic extraction (PEX), reducing the TIA's bandwidth.

6.2 Final Layout

As mentioned in the above section, the miller effect is due to the parasitic capacitance of the feedback resistor that appears internally between the input-output nodes. To reduces this miller capacitance, the size of the feedback resistor in figure 6.3 has been reduced. Resistor length and width are defined according to the required resistance it should produce and the maximum current it can handle. So for a required resistance $R_F = 730\Omega$, the current handling capacity should be reduced to reduce the size. Since the current flows through the feedback resistor, R_F is low,

and it is acceptable to reduce the maximum current flowing through it. Figure 6.4 shows the final layout of the proposed design. The layout occupies 0.0064 mm^2 (99.94×64.04 μm^2) area in which each core occupies 0.00043 mm^2 (21.75×19.83 μm^2) area. The area occupied by each DC block is 0.000289 mm^2 (17×17 μm^2). The DC biasing circuit takes 0.000433 mm^2 (31.96×13.56 μm^2) in the layout. The rest area is either occupied by the routing metals or wasted. Table 6.2 shows the total chip size and comparison between the amount of size consumed by individual components in the chip. Here, the transistors' size is small compared to the DC block's area consumption. As expected, Routing and wastage are consuming most of the chip area (more than 50%). There is room for reducing the total chip area by reducing the wastage.

Table 6.2: Comparison of area consumed by different components on the chip.

Component	**Area Consumed** (mm^2)
4 DC Blocks	0.001156
2 TIA Cores	0.00086
DC biasing circuit	0.000433
Routing and wastage	0.00395
Total Chip Size	0.0064

6.2.1 Post-Layout Simulation Results

Transimpedance Gain and Bandwidth

Before simulating the post-layout results, the final layout was done through DRC and LVS checks. So in this section, the final results are explained and compared with the schematic and initial layout results. Figure 6.5 shows the TIA's transimpedance gain and its corresponding 3-dB bandwidth. We can say that the transimpedance gain achieved at the centre frequency, i.e., 50 GHz is 63.74 dBΩ. There is an improvement of around 1 dBΩ in gain at centre frequency compared with the initial layout. In terms of 3-dB bandwidth, an improvement of around 3 GHz is seen in the final layout after the miller compensation. The final layout has achieved a bandwidth of 60.84 GHz. Compared with schematic results, the gain is reduced by less than 1 dB, and the bandwidth is reduced by 5 GHz.

Input-Referred Noise

The input-referred current noise of the final layout is shown in figure 6.6. It is about $16.20\frac{\text{pA}}{\sqrt{\text{Hz}}}$ at the centre frequency of 50 GHz. This noise is a differential-ended input-referred noise. Hence the single-ended input-referred noise will be $8.10\frac{\text{pA}}{\sqrt{\text{Hz}}}$. It is seen that less than $1\frac{\text{pA}}{\sqrt{\text{Hz}}}$ noise is increased from the schematic. The IRN is performing better than expected from the calculations.

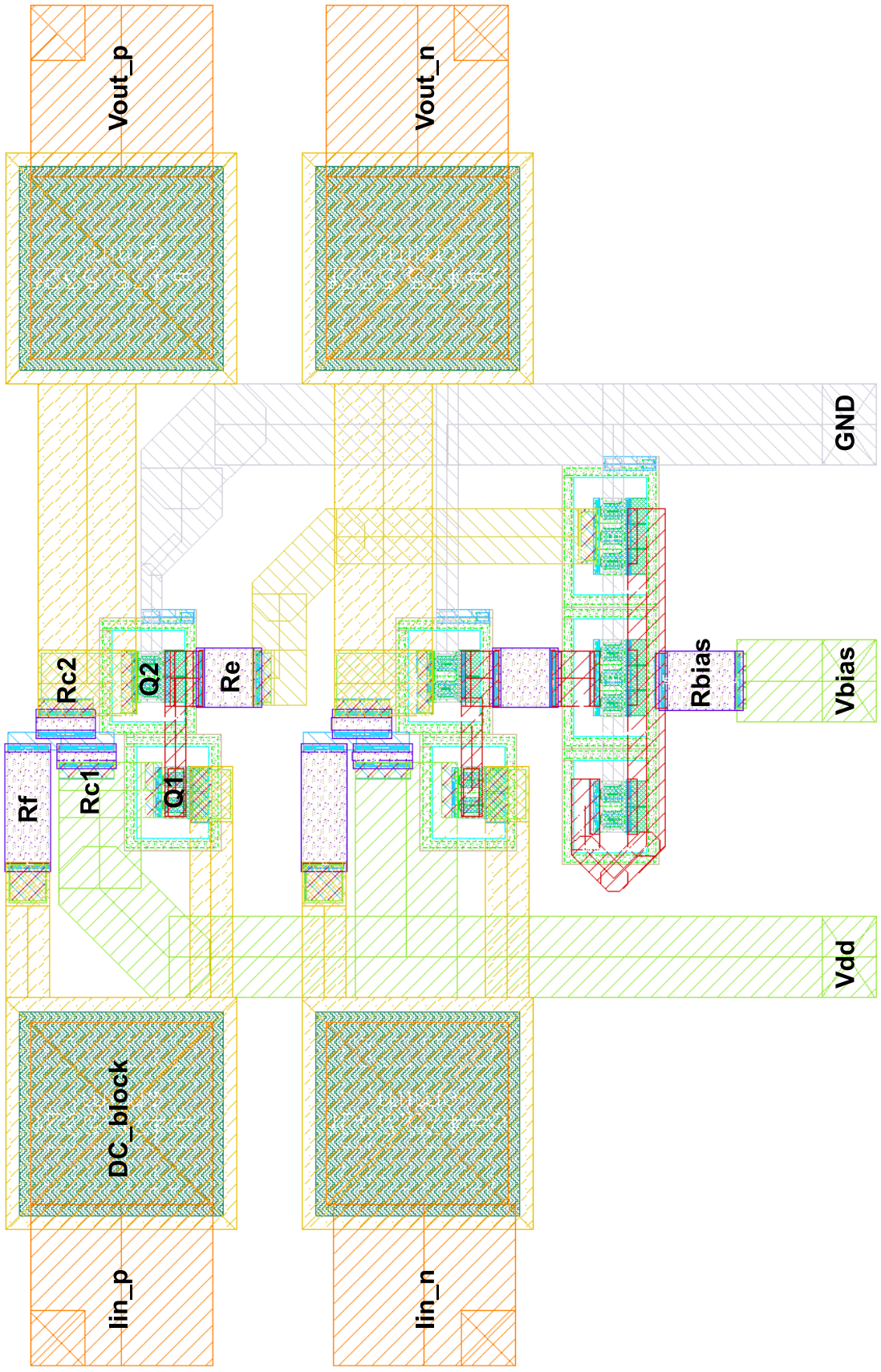

Figure 6.4: Final layout of the designed darlington pair TIA with resistive feedback.

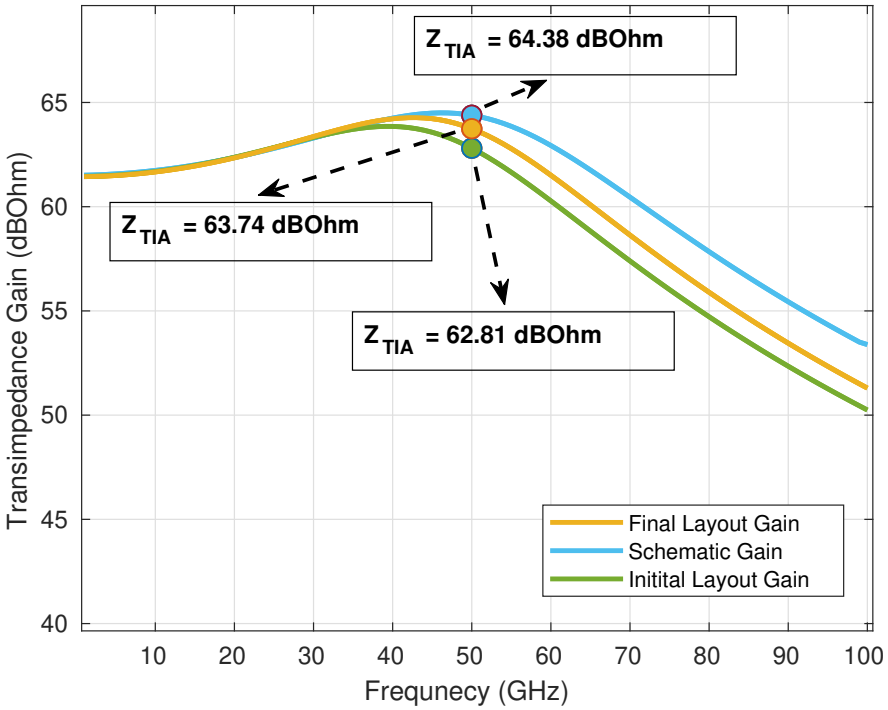

Figure 6.5: Transimpedance gain and bandwidth results of the initial layout vs final layout.

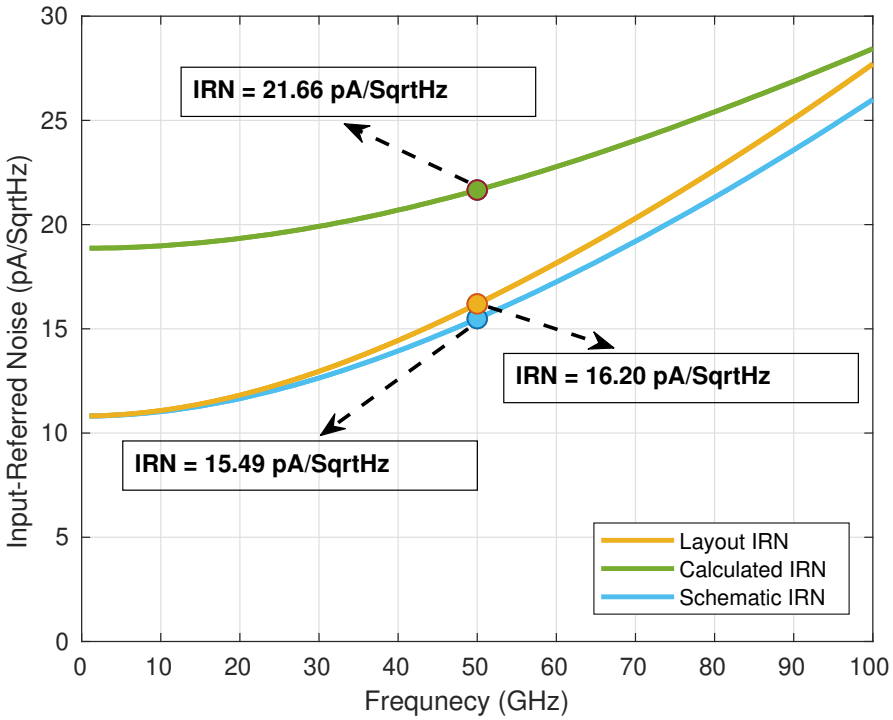

Figure 6.6: Input-referred noise results of the final layout.

Output Impedance Matching

Output impedance matching of the designed TIA after the layout is shown in figure 6.7. The output reflection coefficient S22 is not perfectly matched to 50 Ω, and

its value is –7.23 dB at 50 GHz. As mentioned in the section 3.2.5, obtaining the reflection coefficient value lower than –10 dB over the operating bandwidth is ideal. On the contrary, this will increase power consumption and reduce the gain bandwidth product. It is also possible to add an external matching circuit (off-chip matching) to achieve perfect matching. But it is hard to improve the TIA performances by external circuits. Hence the obtained –7.23 dB of S_{22} is a trade off between an excellent output matching, gain, bandwidth, and power consumption.

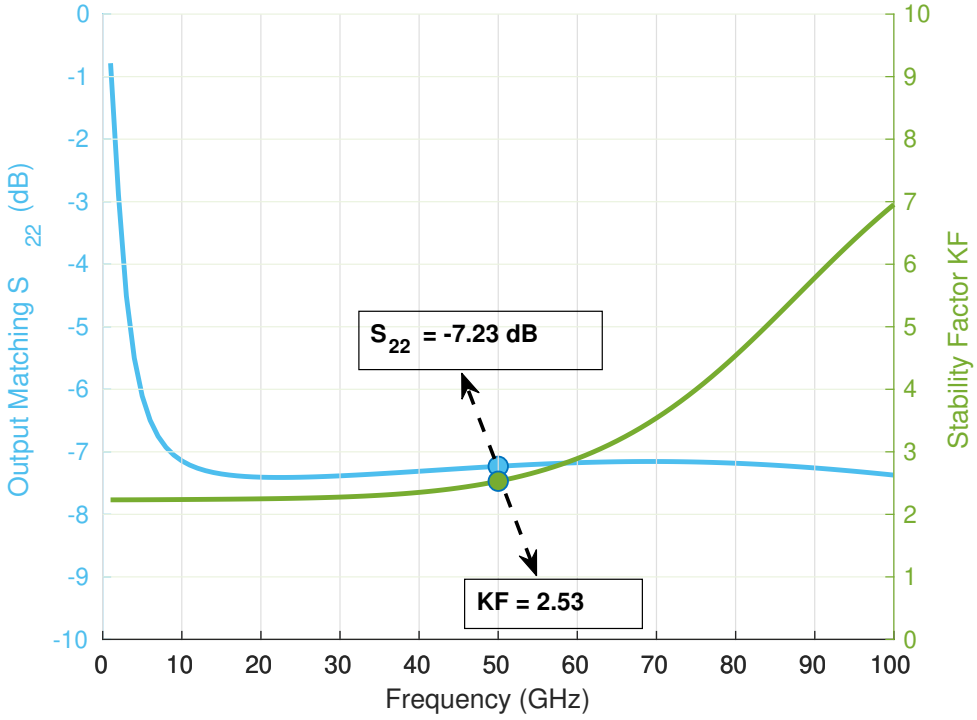

Figure 6.7: Output impedance (S_{22}) and stability factor (KF) of the final TIAs layout.

Stability Factor

Figure 6.7 also shows the designed TIA's stability factor (KF) after layout. As explained in the section 3.2.6, a circuit is said to be stable when its stability factor is greater than one through out the operating frequency range. From figure 6.7, we can see that the stability factor is greater than 2.2 for all the frequency ranges. At the operating frequency of 50 GHz, the obtained stability factor is 2.53.

Corner Analysis

Process variation is one of the most significant constraints on an integrated circuit (IC) design. Process variation occurs in transistor properties during IC fabrication, such as L, W, and thickness. Because the variation (ΔL or ΔW) becomes a larger percentage of the full length or width of the device with smaller feature sizes, process variation becomes significant, especially at smaller process nodes. Another cause of process variation, particularly in analogue circuits, is device mismatch; as

a result, the output performance of all circuits changes. The "Process Corner Simulation" can somewhat predict or measure these changes. The overall yield for that group of devices decreases if this variance causes a specific circuit's simulated output performance (BW, gain, etc.) to fall below or above the specification.

For the simulation, the process corners used in this work are BCS (best-case scenario), TYP (typical scenario), and WCS (worst-case scenario). The investigation starts with checking all the achieved performance parameters of the designed TIA. For this sake, a process corner is set up, shown in figure 6.8. European Council for Nuclear Research (CERN) defines these process corner specifications. Here the three corners are simulated for the transistors, resistors, and capacitors used in the circuit under three different temperatures (–40°, 27° and 100°). So in total, 81 corner analysis is done for three components (transistors, resistors, and capacitors) for three process variations (BCS, TYP; and WCS) under three temperatures (–40°, 27° and 100°). The summary of the results of the corner simulation is shown in table 6.3. This compares the minimum and maximum achieved results for multiple TIA performance parameters. The focus of discussion will be on the corners that have not achieved the TIAs required performance specifications (60 dBΩ transimpedance gain, 40 GHz bandwidth, 20 pA/$\sqrt{\text{Hz}}$ IRN, KF>1, S_{22} and power consumption as low as possible).

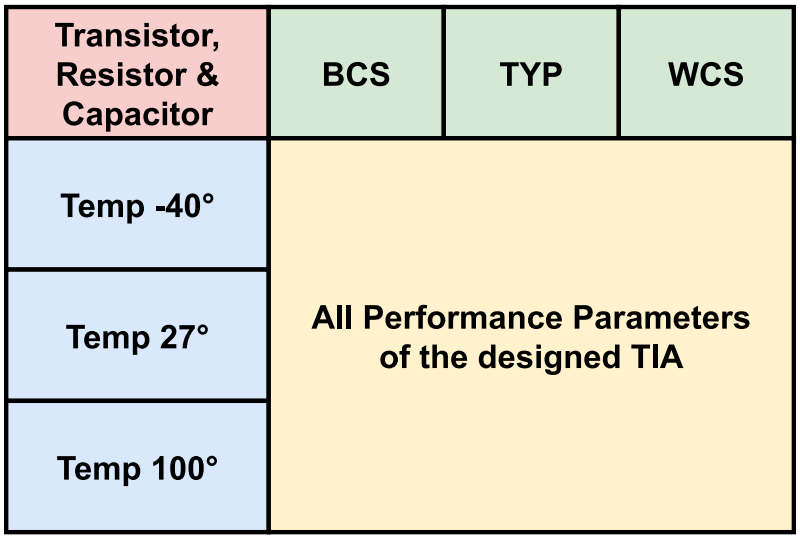

Figure 6.8: Process corner setup for designed TIA.

It is seen from table 6.3, except bandwidth and IRN, the maximum and minimum values of all the performance parameters match the specification in all the corners. The target for transimpedance gain was not met in 9 corners by less than 0.6 dBΩ. All these corner scenarios are when the transistor is in WCS. In the transistor WCS, the thickness of the transistor terminals (B, E, C) changes, and the current flowing through these will change, resulting in a change in the amplification factor (β). The bandwidth requirement was not achieved in six corners. A 10% decrease in bandwidth (35.95 GHz) from the target can be seen at only three corners, and at the other three corners, the bandwidth was 39.4 GHz. All six corners where the bandwidth was reduced were the corners when the temperature was high (100°). When the temperature increases, the value of the resistors and capacitors in the circuit increases. This change in the RC value will affect the bandwidth (BW $\propto$

Table 6.3: Maximum and minimum values of all performances parameters.

Parameters	**Minimum**	**Maximum**
Transimpedance Gain (dBΩ)	59.42	67.47
Bandwidth (GHz)	35.95	79.82
Input-Referred Noise (pA/$\sqrt{\text{Hz}}$)	13.25	24.12
Output Matching, S_{22} (dB)	-8.483	-6.266
Stability Factor, KF	2.064	3.336
Power Consumption (mW)	23.11	40.65

1/RC). Maximum Input-referred noise was 24.12 pA/$\sqrt{\text{Hz}}$, which was 4 pA/$\sqrt{\text{Hz}}$, more than the specification limit. A total of 18 corners at high temperature (100°) exceeded the noise limit of the TIA design. As temperature increases, the movements of electrons in the circuit increase. Hence an increase in the thermal noise of the circuit. Since thermal noise is the biggest contributor to any TIA circuit, The total IRN has increased with the increase in temperature. Parameters like S_{22}, KF, and power consumption have good results in all the corners.

6.3 Results Comparison

In conclusion, table 6.4 compares results obtained from calculations, schematic design and layout design with the required specifications for darlington pair TIA. Here is a slight variation in the results after the layout compared to the schematic results. As expected, darlington pair TIA has offered an excellent trade-off between transimpedance gain, bandwidth and IRN. Along with these specifications, the designed TIA has achieved low power consumption and stable trough throughout the frequency range.

Table 6.4: Comparison of results obtained from calculations, schematic design and layout design

	Target	**Calculations**	**Schematic**	**Layout**
Transimpedance Gain (dBΩ)	60	69.21	64.38	63.74
Bandwidth (GHz)	40	52.3	66.29	60.84
Input-Referred Noise (pA/$\sqrt{\text{Hz}}$)	20	21.66	15.49	16.20
Output Matching, S_{22} (dB)			-7.87	-7.23
Stability Factor, KF	>1		2.18	2.53
Power Consumption (mW)			31.53	30.53

Chapter 7

Conclusion

In systems for high data rate communication, optical receivers are crucial. These receivers can handle multiple Gb/s of data. Wideband transimpedance amplifiers are required in the optical receivers' signal path to achieve such a high data rates. The transimpedance amplifier, one of the critical components of the receiver front, is used to amplify the small current that the photodiode sends. The bandwidth of transimpedance amplifiers should be high to meet the high data rate of fibre optic communication systems. Finding the ideal topology that can satisfy the design requirements while making good trade-offs is crucial. To achieve a good trade-off between transimpedance gain, bandwidth, and IRN, this thesis proposes a differential 180 nm SiGe BiCMOS transimpedance amplifier design based on a darlington pair topology with resistive feedback.

Many of the design challenges and a qualitative study of the various trade-offs involved in the design process have been discussed. The performance of various TIA topologies are studied and calculated in the first section of the thesis. Four topologies in total (CB, CE, RGC, and DP) are investigated. The performance of the schematic designs for the CE, RGC, and DP topologies is calculated and verified in the thesis' second section. Each topology in this thesis underwent a thorough analysis followed by simulations to confirm it. After the necessary comparisons have been made, the darlington pair topology is chosen as the ideal one for designing the TIA. As a result, the layout for this resistive darlington pair topology is implemented in cadence. The designed TIA has a transimpedance gain of 63.7 dBΩ with a wide bandwidth of 60.84 GHz after the layout implementation. A low input-referred noise of 16.20 pA/$\sqrt{\text{Hz}}$ has been attained. The designed TIA has a chip size of just 0.0064 mm^2 and uses 30.53 mW of DC power. The designed darlington pair has met all of the necessary performance criteria. Thus, this thesis was finished exceeding all design objectives.

Table 7.1 summarizes simulation performance of the realized TIA circuit and makes comparison to the some existing designs. The transimpedance gain of the proposed TIA in this thesis is lower than that of references [18] and [21]. Still, the TIA described in these papers operates at a lower frequency, necessitating less effort to achieve gain. Aside from these two papers, this thesis has a very high gain TIA. The designed TIA outperformed all other designs, except for [24], in terms of 3-dB bandwidth. Darlington pair was also used in this paper to implement the TIA. The gain in this paper is less than the TIA from this thesis, as can be seen. According to the requirements, there is a clear trade-off.

There are many papers whose IRN is lower than what the TIA have accom-

Table 7.1: Comparison of State-of-the-Art TIA Circuits with this work.

Reference	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	This Work
Technology	130nm SiGe BiCMOS	130nm SiGe:C BiCMOS	SiGe BiCMOS	130nm SiGe BiCMOS	250nm SiGe BiCMOS	130nm SiGe BiCMOS	130nm SiGe BiCMOS	130nm SiGe BiCMOS	120nm SiGe BiCMOS	130nm SiGe BiCMOS
Topology	CB	CE RSF	CE RSF	CE RSF	RGC RSF	RGC RSF	DP RSF	2 stage DP RSF	DP RSF	DP RSF
Input-Output	Pseudo-Diff	Diff-Diff	Diff-Diff	SE-SE	Diff-Diff	Diff-Diff	SE-SE	SE-SE	SE-SE	Diff-Diff
Frequency (GHz)	30	55	40	30	50	30	50	-	40	50
Transimp. Gain (dBΩ)	71	62.5	49	72	52.5	53.6	55	50.5	47	64.38
Bandwidth (GHz)	31	60	50	38.4	32	28	86	42	53	66.29
IRN (pA/$\sqrt{\text{Hz}}$)	14.5	5.46	30	14.8	13.1	36.5	20.4	12	53.9	15.49
Output Matching (dBm)	-20	-10	-12	-	-10	-15	-19	-25	-8	-7.87
Peaking/Buffers	yes	yes	yes	yes	yes	yes	yes	no	no	no
DC power cons. (mW)	300	85	200	261	70	110	89	45	73	31.53
ft/fmax (GHz)	-	300/500	170/140	-	95/140	160/-	200/240	-	200/-	300/450
Chip size (mm^2)	0.54	0.3	0.92	0.2	0.32	0.56	0.28	0.23	0.29	0.0064

plished in this thesis. This might make for a nice improvement in the future. The main benefit of the TIA used in this thesis is that it achieves performance without any additional circuitry, in contrast to most papers that have done so. Compared to other works, the designed TIA uses minimal power and chip space. Since the results presented here were only simulated once and the others were measured, these numbers might increase after the tape out.

7.1 Future Scope

This thesis considered one of the most useful methods for choosing the topology of a transimpedance amplifier. Mathematical analysis and extensive simulation were used to carry out a thorough analysis of transimpedance amplifier topologies. A complete understanding of these processes can aid researchers in moving towards better TIA designs in different aspects. Here are a few potential future developments that could be considered for better outcomes.

- Although it was considered in the mathematical analysis, simulations conveniently ignored photodiode capacitance. It is necessary to conduct additional research to determine this photodiode capacitance's impact while designing. It might be possible to lower C_{in}, thereby raising the system's overall bandwidth. There will, however, always be a trade-off associated with gain.
- Some techniques in the TIA design have lowered the miller capacitance's impact after the layout. But it can still be enhanced by including a feedback capacitor. The parasitic capacitor that forms between the input-output nodes will reduce its value due to adding a feedback capacitor.
- There are several methods for increasing the bandwidth, such as capacitive degeneration and inductive peaking. Since the TIA created for this thesis has met its bandwidth goal, these techniques are yet to be researched and put into practice.
- Measurements for the taped-out TIA must also be performed. It is crucial to analyze the causes of any performance degradation after tape-out and make improvements.

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Appendix A

Mathematical Analysis

A.1 Common Emitter TIA With Resistive Feedback

Input Impedance

For finding the input pole P_1, input impedance ($Z_{in} = \frac{V_{in}}{I_{in}}$) should be calculated. lets consider the small signal model circuit of the common emitter TIA with resistive feedback shown in the figure 4.6. While finding the input impedance, I_{out} is zero, and r_b is negligible. Then the equivalent small signal signal circuit will become as shown in the figure A.1. Hence from this, the input impedance of the device yields as shown in the equation A.1. Therefore, the input pole of the common emitter TIA with resistive feedback is given from equation A.2.

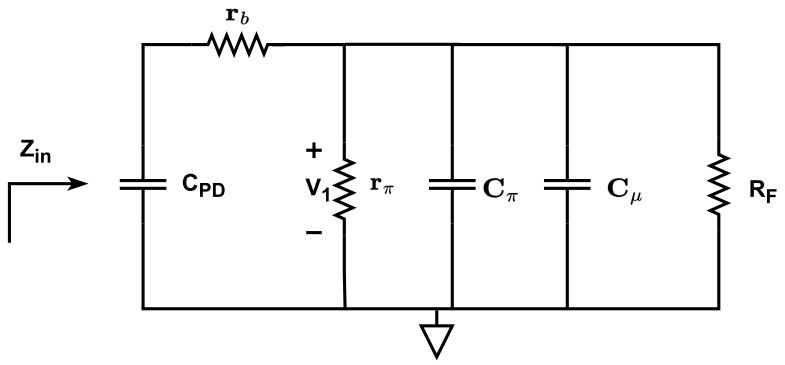

Figure A.1: Equivalent small signal model of a common emitter TIA while finding input impedance.

$$\begin{aligned} Z_{in} &= \frac{V_{in}}{I_{in}}, \text{ when } I_{out} = 0. \\ &= (r_\pi \,||\, R_F) \,||\, \frac{1}{j \cdot \omega \cdot (C_\pi + C_\mu + C_{PD})}, \\ &= R_F \,||\, \frac{1}{(j \cdot \omega \cdot C_{in})}, \text{ where } r_\pi >> R_F \text{ and } C_{in} = C_\pi + C_\mu + C_{PD}, \\ &= \frac{R_F}{1 + (j \cdot \omega \cdot R_F \cdot C_{in})} \quad \Omega \end{aligned} \tag{A.1}$$

$$P_1 = \frac{1}{2 \cdot \pi \cdot R_F \cdot C_{in}} \quad \text{Hz} \tag{A.2}$$

Output Impedance

For finding the output pole P_2, output impedance ($Z_{out} = \frac{V_{out}}{I_{out}}$) should be calculated. lets consider the small signal model circuit of the common emitter TIA with resistive feedback shown in the figure 4.6. While finding the output impedance, V_{in} is zero, and r_b is negligible. Then the equivalent small signal signal circuit will become as shown in the figure A.2. Hence from this, the output impedance of the device yields as shown in the equation A.3. Therefore, the output pole of the common emitter TIA with resistive feedback is given from equation A.4.

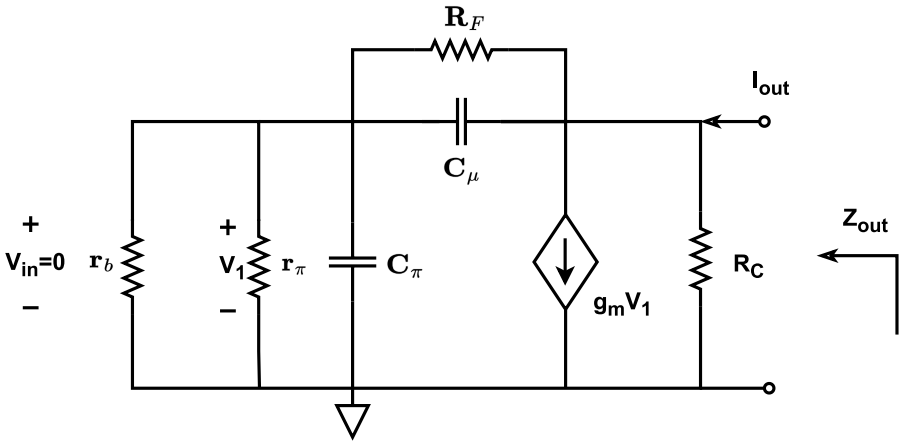

Figure A.2: Equivalent small signal model of a common emitter TIA while finding output impedance.

$$\begin{aligned} Z_{out} &= \frac{V_{out}}{I_{out}}, \text{ when } V_{in} = 0. \\ &= \frac{1}{\left(\frac{1}{R_C} + \frac{1}{Z_F}\right)} = \frac{R_C}{1 + \frac{R_C}{Z_F}}, \\ &= \frac{R_C}{1 + R_C \cdot \left(\frac{1 + (j \cdot \omega \cdot R_F \cdot C_\mu)}{R_F}\right)}, \\ &\text{where } Z_F = R_F \parallel \frac{1}{(j \cdot \omega \cdot C_\mu)} = \frac{R_F}{1 + (j \cdot \omega \cdot R_F \cdot C_\mu)}, \\ &= \frac{R_C \parallel R_F}{1 + (j \cdot \omega \cdot (R_C \parallel R_F) \cdot C_\mu)} \quad \Omega \end{aligned} \tag{A.3}$$

$$P_2 = \frac{1}{2 \cdot \pi \cdot (R_C \parallel R_F) \cdot C_\mu} \quad \text{Hz} \tag{A.4}$$

Transimpedance Gain

The DC transimpedance gain $Z_{TIA} = \frac{V_{out}}{I_{in}}$ of the common emitter TIA with resistive feedback yields as shown in the equation A.5.

$$\begin{aligned} Z_{TIA} = \frac{V_{out}}{I_{in}} &= g_m \cdot Z_{out}, \\ &= g_m \cdot \frac{R_C \parallel R_F}{1 + (j \cdot \omega \cdot (R_C \parallel R_F) \cdot C_\mu)} \quad \Omega \end{aligned} \tag{A.5}$$

Hence the DC gain $\approx (R_C \parallel R_F)\ \Omega$.

A.2 Regulated Cascode TIA

Input Impedance

For finding the input pole and zero, P_1 and Z_1, input impedance ($Z_{in} = \frac{V_{in}}{I_{in}}$) should be calculated. lets consider the small signal model circuit of the regulated cascode TIA shown in the figure 4.9. While finding the input impedance, I_{out} is zero, and r_b is negligible. For simplify, lets consider equivalent series and parallel combinations Z_1 and Z_2 as shown in equation A.6. Then the equivalent small signal signal circuit will become as shown in the figure A.3. By superposition theorem, assume $V_2 = 0$ and $V_{in} = V_1$. Hence from this, the input impedance of the device yields as shown in the equation A.8. Therefore, the input pole and zero of the regulated cascode TIA is given from equation A.9.

$$\begin{aligned} Z_1 &= \frac{1}{j \cdot \omega \cdot (C_{PD} + C_{\pi_1})} \parallel R_E \parallel r_{\pi_1}, \\ Z_2 &= \frac{1}{j \cdot \omega \cdot (C_{\mu_1} + C_{\pi_2})} \parallel R_{C_1} \parallel r_{\pi_2}, \end{aligned} \tag{A.6}$$

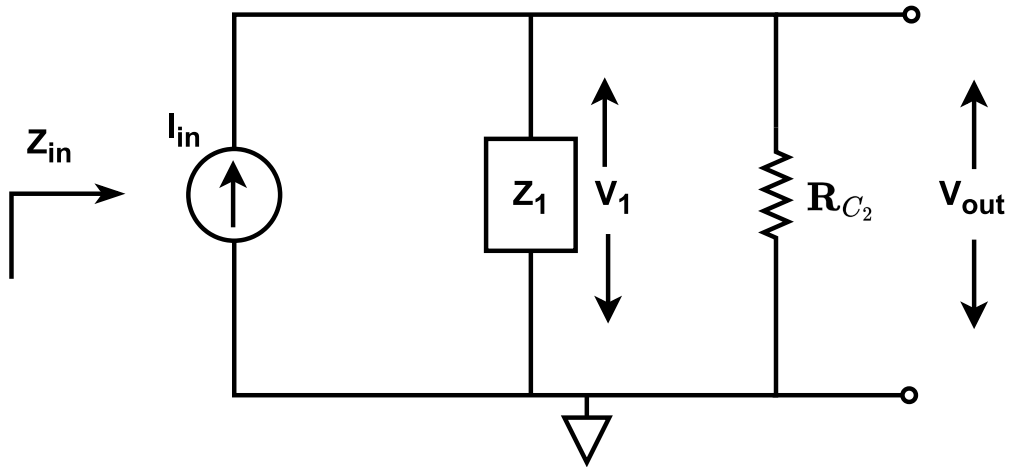

Figure A.3: Equivalent small signal model of a regulated cascode TIA while finding input impedance.

$$\begin{aligned} Z_{in} &= \frac{V_{in}}{I_{in}},\ \text{when } I_{out} = 0, \\ &= Z_1 + R_{C_2}, \\ &= \left(\frac{1}{j \cdot \omega \cdot (C_{PD} + C_{\pi_1})} \mid\mid R_E \mid\mid r_{\pi_1} \right) + R_{C_2}. \end{aligned} \tag{A.7}$$

Since the input impedance of the transistor is high, $r_{\pi_1} >> R_E \implies R_E \mid\mid r_{\pi_1} \approx R_E$ and consider $C_{PD} + C_{\pi_1} = C_{in}$. Therefore from A.7,

$$\begin{aligned} Z_{in} = \frac{V_{in}}{I_{in}} &= \left(\frac{1}{j \cdot \omega \cdot C_{in}} \mid\mid R_E \right) + R_{C_2}, \\ &= (R_{C_2} + R_E) \cdot \frac{1 + \left(j \cdot \omega \cdot (R_{C_2} \mid\mid R_E) \cdot C_{in} \right)}{1 + (j \cdot \omega \cdot R_E \cdot C_{in})} \quad \Omega \end{aligned} \tag{A.8}$$

$$\begin{aligned} Pole_1 = P_1 &= \frac{1}{2\pi \cdot R_E \cdot C_{in}} \quad \text{Hz} \\ Zero_1 = Z_1 &= \frac{1}{2\pi \cdot (R_{C_2} \mid\mid R_E) \cdot C_{in}} \quad \text{Hz} \end{aligned} \tag{A.9}$$

Output Impedance

For finding the output pole and zero, P_2 and Z_2, output impedance ($Z_{out} = \frac{V_{out}}{I_{out}}$) should be calculated. lets consider the small signal model circuit of the regulated cascode TIA shown in the figure 4.9. While finding the output impedance, V_{in} is zero, and r_b is negligible. For simplify, lets consider equivalent series and parallel combination Z_3 as shown in equation A.10. Then the equivalent small signal signal circuit will become as shown in the figure A.4. By superposition theorem, assume $V_1 = 0$. Hence from this, the output impedance of the device yields as shown in the equation A.14. Therefore, the output pole and zero of the regulated cascode TIA is given from equation A.15.

$$Z_3 = R_{C_2} \mid\mid \left(Z_2 + \frac{1}{j \cdot \omega \cdot C_{\mu_2}} \right). \tag{A.10}$$

Since the output voltage is given by:

$$V_{out} = g_{m_2} \cdot V_2 \cdot Z_3. \tag{A.11}$$

$$\begin{aligned} Z_{out} &= \frac{V_{out}}{I_{out}},\ \text{when } V_1 = 0, \\ &= Z_3 = R_{C_2} \mid\mid \left(\frac{1 + (j \cdot \omega \cdot Z_2 \cdot C_{\mu_2})}{j \cdot \omega \cdot C_{\mu_2}} \right). \end{aligned} \tag{A.12}$$

From (A.6), $r_{\pi_2} >> R_{C_1} \implies R_{C_1} \mid\mid r_{\pi_2} \approx R_{C_1}$ and consider $C_{\mu_1} + C_{\pi_2} = C_{int}$. Therefore

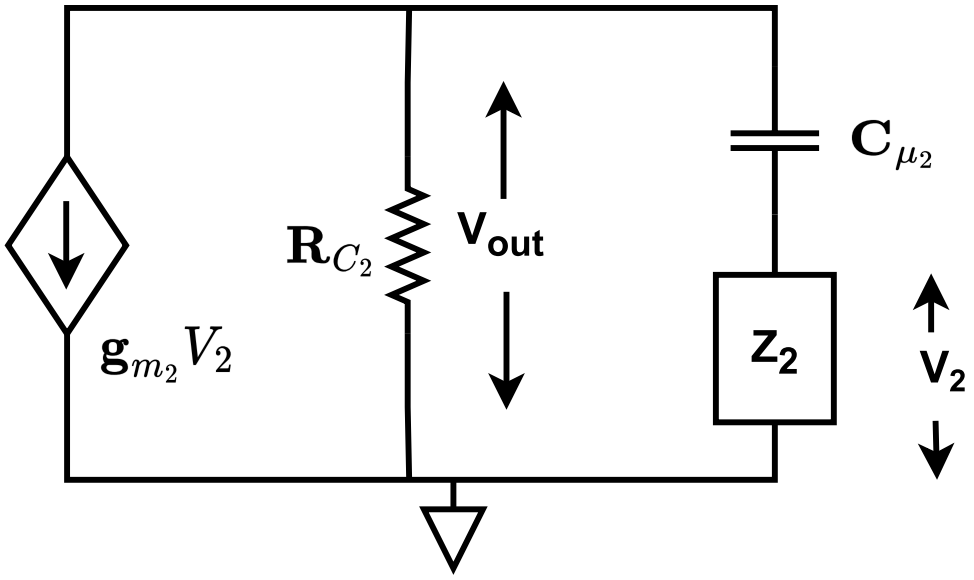

Figure A.4: Equivalent small signal model of a regulated cascode TIA while finding output impedance.

$$\begin{aligned} Z_2 &= \frac{1}{j \cdot \omega \cdot C_{int}} \parallel R_{C_1}, \\ &= \frac{R_{C_1}}{1 + (j \cdot \omega \cdot R_{C_1} \cdot C_{int})}, \end{aligned} \tag{A.13}$$

From (A.12) and (A.13),

$$\begin{aligned} Z_{out} &= \frac{1 + (j \cdot \omega \cdot Z_2 \cdot R_{C_2} \cdot C_{\mu_2})}{1 + (j \cdot \omega \cdot R_{C_2} \cdot C_{\mu_2}) + (j \cdot \omega \cdot Z_2 \cdot C_{\mu_2})} \\ &= \frac{1 + sR_{C_1}C_{out}}{1 + s(R_{C_1}C_{out} + R_{C_2}C_{\pi_2})} \quad \Omega \end{aligned} \tag{A.14}$$

where $C_{out} = C_{\mu_2} + C_{\mu_1} + C_{\pi_2}$. Therefore, the output pole and zero are:

$$\begin{aligned} Pole_2 = P_1 &= \frac{1}{2\pi \cdot (R_{C_1} \cdot C_{out} + R_{C_2} \cdot C_{\pi_2})} \quad \text{Hz}, \\ Zero_2 = Z_1 &= \frac{1}{2\pi \cdot R_{C_1} \cdot C_{out}} \quad \text{Hz}. \end{aligned} \tag{A.15}$$

Transimpedance Gain

The DC transimpedance gain $Z_{TIA} = \frac{V_{out}}{I_{in}}$ of the regulated cascode TIA yields as shown in the equation A.17.

$$V_{out} = I_C \cdot \frac{1}{(j \cdot \omega \cdot C_{\mu_2})} + (I_C - (g_{m_1} \cdot V_1)) \cdot Z_2. \tag{A.16}$$

$$\frac{V_{out}}{I_{in}} = \frac{\frac{1}{(j \cdot \omega \cdot C_{\mu_2})} + Z_2}{1 - Z_2 + \frac{\frac{1}{(j \cdot \omega \cdot C_{\mu_2})} + Z_2}{R_{C_2}}} = \frac{R_{C_2} \cdot (1 + (j \cdot \omega \cdot R_{C_1} \cdot C_X))}{-j \cdot \omega \cdot R_{C_1} \cdot R_{C_2} \cdot C_{\mu_2}} \quad \Omega \tag{A.17}$$

where $C_X = C_{int} + C_{\mu_2}$. Hence the DC gain $\approx R_{C_2}$ Ω.

A.3 Darlington Pair TIA With Resistive Feedback

As discussed in the section 4.5, the darlington pair can be simplified into to two different blocks as shown in the figure A.5. This will make the calculation to find the poles and DC gain easy. The first stage is a simple common collector amplifier, the required calculation are in [56]. The second stage is a common emitter with resistive feedback and the calculations for this is already explained in section A.1. The transimpedance gain of darlington pair can be written as a product of the transimpedance gain of the common collector and voltage gain of common emitter with resistive feedback as shown in equation A.18.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{V_1}{I_{in}} \cdot \frac{V_{out}}{V_1} \tag{A.18}$$

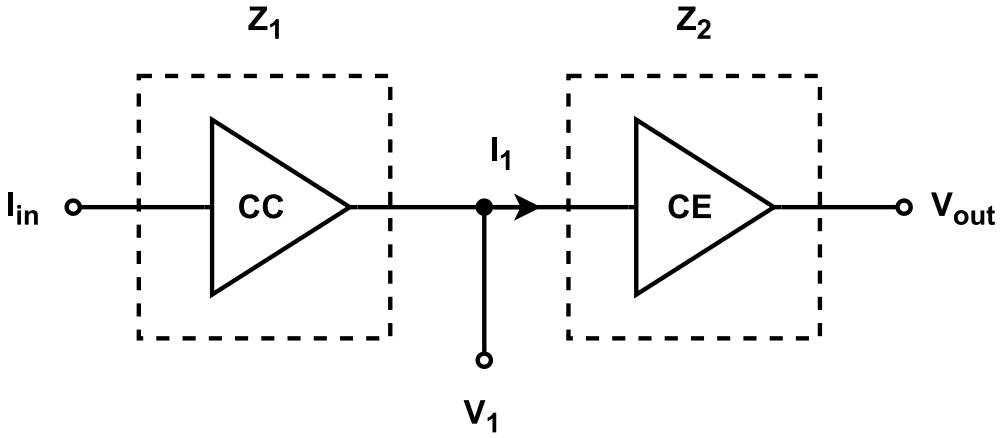

Figure A.5: Equivalent model of a darlington pair TIA into common collector and common emitter.

The transimpedance gain of the common collector is a product of voltage gain and input resistance. It can be approximated to $\beta_1 R_E$. The voltage gain of the common emitter with resistive feedback is given by $g_m(R_C||R_F)$. Hence the transimpedance gain of the darlington pair is given by the equation A.19.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} \approx \beta_1 \cdot R_E \cdot g_m \cdot (R_C||R_F) \quad \Omega \tag{A.19}$$

The input pole for the darlington pair TIA will be same as input pole of the common collector TIA and output pole will be the same as output pole of the common emitter with feedback resistor TIA. Hence the input and output poles are shown in the equation A.20.

$$\begin{aligned} P_1 &= \frac{1}{2 \cdot \pi \cdot \beta_1 \cdot R_E \cdot C_{in}} \quad \text{Hz} \\ P_2 &= \frac{1}{2 \cdot \pi \cdot (R_C || R_F) \cdot C_{out}} \quad \text{Hz} \end{aligned} \tag{A.20}$$