

INLINE PECVD DEPOSITION OF A-SI LAYERS FOR HETEROJUNCTION SOLAR CELLS ON AN INDUSTRIAL SCALE

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ABSTRACT: In this work the recent results concerning inline deposition of amorphous silicon obtained with a PECVD tool from Meyer Burger Germany (MBG) are presented. The depositions are done with an adapted MAiA tool which for this matter contains radio frequency linear plasma sources for the intrinsic as well as the doped amorphous silicon layers. In order to investigate the properties of these layers/layer stacks, especially concerning passivation quality and selectivity, we prepared various sample structures to determine minority carrier lifetime/implied open-circuit voltage, band bending and electrical properties. Minority carrier lifetimes of up to 7 ms and average implied open-circuit voltages of above 730 mV are verified for intrinsic amorphous silicon. We could proof a sufficient band bending for both n- and p-doped and demonstrate an n-doped inline process which leads to external open-circuit voltages above 700 mV and pseudo fill factor values above 80 %. It is also shown for the layer stack consisting of intrinsic and n-doped amorphous silicon that we can reach a sufficient net doping to obtain required selectivity of the contact for the extraction of excess charge carriers.

Keywords: silicon heterojunction, amorphous silicon, inline PECVD, passivation, selective contacts

1 INTRODUCTION/MOTIVATION

Silicon Heterojunction (SHJ) solar cells represent a key technology to approach very high conversion efficiencies close to the theoretical limit of silicon solar cells. The main advantages of SHJ solar cells are a lean production chain with low temperature processes and carrier selective hetero-structures for excellent passivation. Both-side contacted SHJ solar cells featuring amorphous thin-film layer stacks enable high conversion efficiencies up to 25.1 % [1]. To achieve such high efficiencies different features as the front grid electrode, the transparent conductive oxide (TCO), the quality of the hydrogenated amorphous silicon (a-Si:H) layers and the c-Si surface structure must be carefully optimized. Aiming to reduce the cost of ownership (COO) an increased throughput is required which can be realized within an inline PECVD deposition process. Hydrogenated amorphous silicon (a-Si:H) which is used as passivation and selective layer for silicon heterojunction (SHJ) solar cells has to fulfill two important basic requirements:

- excellent passivation of the c-Si absorber
- high selectivity with respect to the charge carriers to obtain the best possible electrical contact.

In this work results concerning passivation quality and selectivity regarding photo-generated excess charge carriers of the layer stack consisting of intrinsic and doped a-Si:H obtained with an adapted MAiA inline PECVD tool from Meyer Burger Germany (MBG) are presented.

2 PASSIVATION QUALITY

First step is the development/optimization of an intrinsic a-Si:H layer for passivation. For this purpose first experiments were carried out to screen the whole deposition parameter space (process pressure, process temperature, plasma power and gas flows (SiH_4 , H_2)). Having determined the temperature as a key parameter for excellent passivation, we conducted an experiment

with a variation of only the process temperature aiming to determine the optimal process range (chapter 2.1). Next we examined the homogeneity over one wafer, over the whole deposition tray and also over time (chapter 2.2). To obtain the passivation properties of the a-Si:H(i) layers lifetime samples (textured n-type Cz c-Si, 180 μm , 3.5 $\Omega\cdot\text{cm}$ with 12 nm a-Si:H(i) on both sides) were prepared and analyzed by Quasi Steady-State Photoconductance measurements (QSSPC) in order to determine the minority carrier lifetime (τ_{eff}) and implied V_{OC} (iV_{OC}) [2]. We reached very good passivation quality with $iV_{\text{OC}} > 730$ mV (see Fig. 4).

2.1 Process Temperature

Fig. 1 and 2 depict the lifetime τ_{eff} and iV_{OC} values achieved for different process temperatures of the inline PECVD process and after annealing for 15 min at 180°C. The process temperature was varied in the range between 200°C and 300°C.

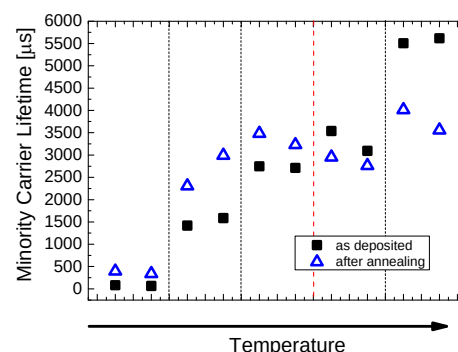


Figure 1: Minority carrier lifetime τ_{eff} in μs as a function of the process temperature; as deposited and after annealing (15min, 180°C).

One can observe an overall rise of both parameters τ_{eff} / iV_{OC} with increasing process temperature. For the lower process temperature range there is a rise of τ_{eff} / iV_{OC} after annealing, whereas to the higher range there is

a decrease of $\tau_{\text{eff}}/iV_{\text{OC}}$ after annealing. We assume that for higher temperatures an in-situ annealing and also partly epitaxial growth of the layers might occur, which lowers the lifetime after annealing and hence does not lead to improvement by annealing.

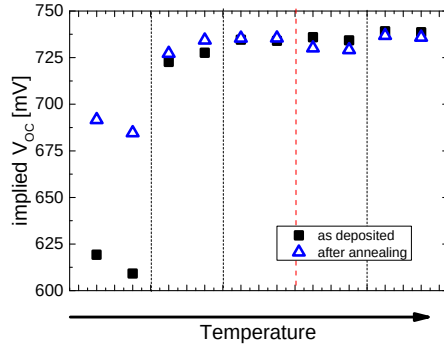


Figure 2: Implied V_{OC} in mV as a function of the process temperature; as deposited and after annealing (15min, 180°C).

2.2 Process Homogeneity

In the next step the homogeneity of the passivation concerning wafer area, position on deposition tray (consisting of 5 columns and 4 rows) and also over time was analyzed. Fig 3. shows a photoluminescence (PL) image of one wafer deposited with 12nm a-Si:H(i) on both sides measured immediately after deposition. The defects at the edge or in the middle of the wafer can be traced back to tweezers and wafer markings.

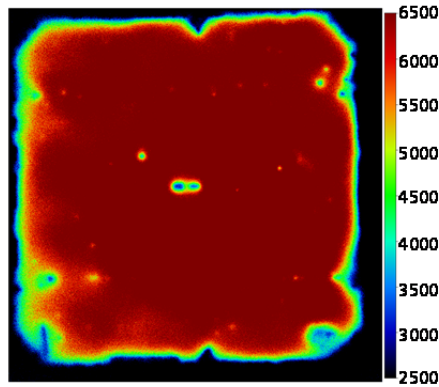


Figure 3: PL image of the minority carrier lifetime τ_{eff} in μs after deposition with 12nm a-Si:H(i) layer on both sides; scale from 2500 to 6500 μs .

Fig. 4 depicts the result for the iV_{OC} as a function of the wafer position on the deposition tray. It can be seen that with an optimized process iV_{OC} values over 730 mV were obtained for all positions whereby a slight degradation in transport direction (from top to bottom) can be observed. In Fig. 5 the lifetime τ_{eff} is shown as a function of time. One can see a fluctuation of the τ_{eff} , but an overall level of above 3 ms (corresponding to an $iV_{\text{OC}} > 730$ mV). The a-Si:H(i) process supplies excellent stability concerning passivation even after chamber cleaning by an etching process and although to the fact that other processes carried out within the same deposition chamber.

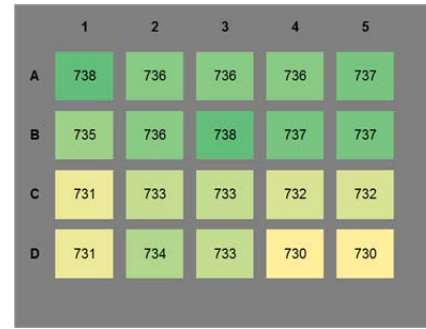


Figure 4: Scheme of the inline deposition tray (5 columns, 4 rows) with iV_{OC} values in mV measured by QSSPC as a function of the tray position.

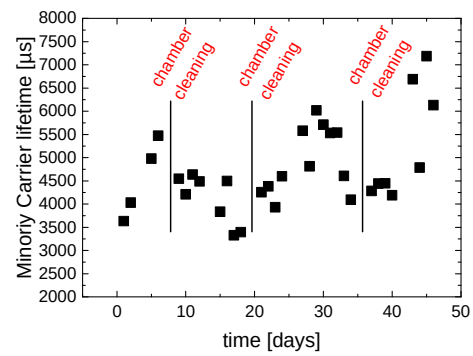


Figure 5: Minority carrier lifetime τ_{eff} in μs as a function of the time to outline the reproducibility and/or stability of the a-Si:H(i) process; black lines show chamber cleaning by an etching process.

3 ELECTRICAL PROPERTIES (SELECTIVITY)

The doped a-Si:H layers have to provide a sufficient net doping to induce a strong band bending and therefore a high built-in potential within the absorber. This causes the formation of the high/low junction and the selective charge carrier extraction from the absorber to the external contacts. For investigation of the electrical properties two different sample structures were prepared (Fig. 6)

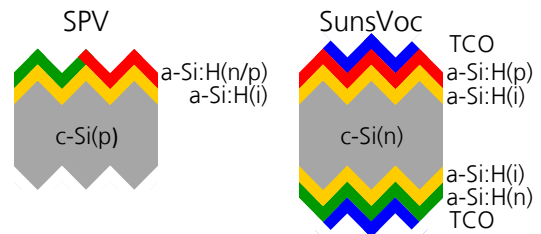


Figure 6: Sample structures for the different measurements concerning the electrical properties; samples with only a-Si:H(i) and the layer under investigation (either a-Si:H(n) or a-Si:H(p), left) for SPV measurements and samples with layer stacks of intrinsic and n-doped layer and ITO on top for SunsVoc measurements (right) to investigate the a-Si(i/n) layer stack.

For the investigations concerning band bending of a-Si:H(n) we used textured FZ c-Si, p-type, 250 μm ,

0.5 $\Omega\cdot\text{cm}$ whereas for the band bending of a-Si:H(n) and for the SunsVoc samples textured FZ c-Si, n-type, 200 μm , 1.0 $\Omega\cdot\text{cm}$ were utilized. For both experiments the buffer layer (intrinsic a-Si:H) was 12 nm on textured surfaces and was deposited with the MAiA tool. The doped a-Si:H layers have a thickness of 10 nm and the ITO layers were 70 nm thick. Doping is realized by adding B_2H_6 (a-Si:H(p)) respectively PH_3 (a-Si:H(n)) to the deposition process.

3.1 Band Bending (SPV)

Fig. 7 shows the band bending $V_{\text{bb, dark}}$ which is induced by the doped a-Si:H layer into the c-Si absorber. It can be seen that in the case of n-doped a-Si:H layers a saturation of the band bending for a gas phase doping above 1000 ppm is reached whereas for the p-doped a-Si:H is a slight rise (below 2000 ppm) to be observed. Above that value no clear trend for both doping types reveals.

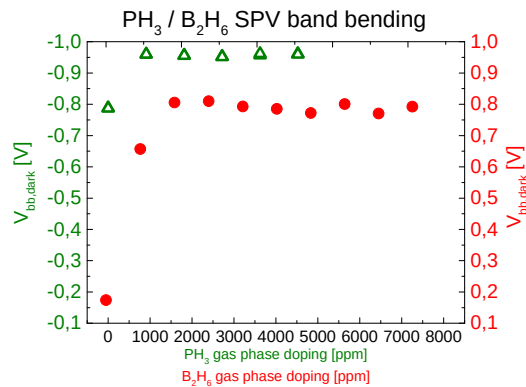


Figure 7: Band Bending $V_{\text{bb, dark}}$ in V as a function of the gas phase doping in ppm for either p-doped a-Si:H (B_2H_6) or n-doped a-Si:H (PH_3) layers with 12nm intrinsic buffer layer between c-Si and doped a-Si:H.

3.2 Electrical parameters (SunsVoc)

SunsVoc samples are a simple and quick way to further analyze and evaluate various electrical properties (e.g. of the doped a-Si:H layers) on preliminary test structures without having to prepare complete solar cells. The first experiment deals with the investigation of the n-doped a-Si:H (PH_3) layer more specifically the layer stack consisting of intrinsic and n-doped a-Si:H. The layer stack and also the intrinsic buffer layer on the other side of the wafer were deposited with the MAiA tool. All other layers (p-doped a-Si:H, ITO) come from a reference PECVD tool.

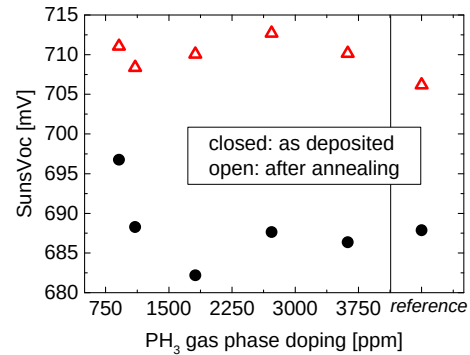


Figure 8: External V_{OC} in mV as a function of the PH_3 gas phase doping; values as deposited (closed circles) and after annealing (open triangles).

Fig. 8 depicts the values of V_{OC} as a function of the PH_3 doping gas flow. After annealing values above 700 mV were reached. Just like for the SPV investigation, there is no clear trend. The slight increase for the regime of low gas phase doping (starting from 1000 ppm to 2700 ppm) could be due to the fact that more doping material leads to an improved extraction of the photo-generated excess charge carriers whereas the decrease with higher gas phase doping (above 2700 ppm) could be explained by incorporation of more doping material within the doped layers which creates more defects and therefore increased recombination.

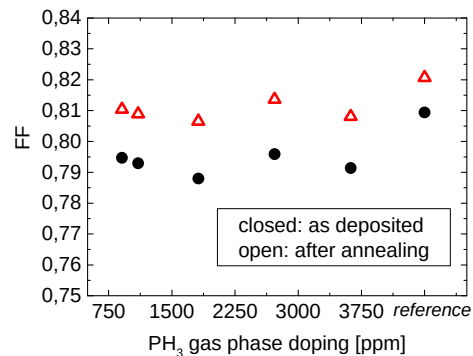


Figure 9: Pseudo fill factor as a function of the PH_3 gas phase doping; values as deposited (closed circles) and after annealing (open triangles).

In Fig. 9 one can see the Pseudo fill factor (pFF) as a function of the PH_3 gas flow. For all variations we get values around 0.8. There is a slight increase of pFF with PH_3 which could be due to improved selectivity of the doped layer and therefore more efficient extraction of photo-generated excess charge carrier. For more information on the net doping SHJ test structures are analyzed by means of Suns- V_{OC} measurements for high illumination intensities [6] (Fig. 10,11).

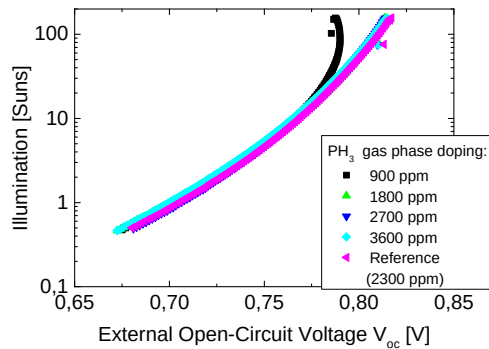


Figure 10: Illumination (Suns) as a function of the external V_{OC} for the n-doped a-Si:H (PH_3) layers. Insufficient selectivity is characterized by a kinking of the curve towards lower V_{OC} values.

Under these conditions the contact is “pushed” towards flat band and thus high-injection conditions with increasing illumination intensity which is reflected in a characteristic “back bending” as shown in Fig. 10 for the lowest doping (black curve). To get a qualitative interpretation the slope of this external V_{OC} at 100 suns (ideality factor $n_{100\text{suns}}$) is analyzed. Fig. 11 shows this slope as a function of the PH_3 gas phase doping. Towards higher doping $n_{100\text{suns}}$ increases and especially for the highest doping approaches the value of the reference. That indicates a sufficient selectivity and therewith associated the absence of a pronounced ITO / a-Si:H(n) Schottky contact.

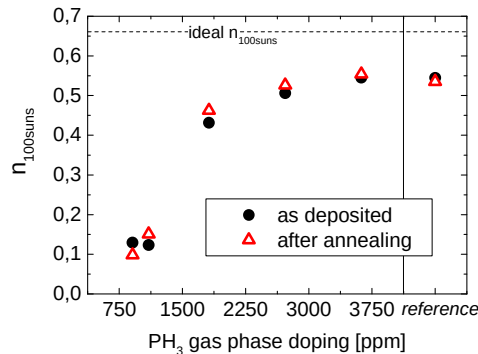


Figure 11: Ideality factor $n_{100\text{suns}}$ as a function of the PH_3 gas phase doping; as deposited (closed circles) and after annealing (open triangles).

4 SUMMARY/CONCLUSION

Within development/optimization of inline deposition of a-Si:H(i) as passivation layer for SHJ the temperature turned out to be a key parameter for excellent passivation quality. We could show lifetimes τ_{eff} of up to 7 ms and on average iV_{OC} values above 730 mV. An excellent homogeneity over the wafer area and a very good homogeneity over the whole deposition tray and for the process over time was verified (especially also after chamber cleaning by a plasma etching). Concerning inline deposition of doped a-Si:H SPV measurements revealed a sufficient band bending for both n- and p-doped a-Si:H. Further experiments regarding a-Si:H(n) led to V_{OC} values above 700 mV after annealing

and pFF above 80 %. Suns V_{OC} measurements with high illumination intensities showed the necessity of the highest gas phase doping to reach a sufficient net doping to obtain the required selectivity respectively absence of a pronounced ITO / a-Si:H(n) Schottky contact.

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