Low-Power Modular Multi-Sensor Node with ZeSCIP Analog Frontend

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***Abstract*—The *Zero-Power Signal Conditioning IP* (ZeSCIP) aims to operate in an autonomous environmental sensor node with energy harvester-extended life time. In this application, the sensor analog frontend has to process environmental signals of different nature, while it is confronted with power and space limitations and low operating voltages. In a flexible modular setup, the ZeSCIP analog frontend is attached to commercial sensors, which represent a specific air quality sensing scenario. This multi-sensor module is stacked to an ARM Cortex M4-based STM32 Nucleo™ board, creating an operational test setup of a modular sensor node, controlled via USB link. In measurement, the module consumes only 35.5 µW during processing of light, CO gas and temperature sensor signals, which makes it suitable to be autonomously powered by energy harvesters.**

***Index Terms*—analog frontend, ultra-low power, harvester-powered autonomous sensor node, NUCLEO, ARM Cortex M4**

I. Introduction

With the advent of the Internet of Things (IoT), the usage of sensor networks for various applications has seen an explosive growth. As a starting point on the road to autonomous, harvester-powered (zero power) sensor nodes, the integrated ZeSCIP zero power analog frontend (AFE) was designed to readout typical environmental sensors with microwatt power consumption [1]. It aims at the dynamic IoT market, where short market times and low production costs are an important factor. The sensor data, digitized and pre-processed by ZeSCIP, is available for further processing and transmitting by a microcontroller, which was not taken into account in [1]. In this paper, ZeSCIP is brought into a realistic application scenario by attaching it in a test setup to a microntroller and to commercial sensors. This modular device stack demonstrates the capabilities of the ZeSCIP in an IoT environment. The resulting modular multi-sensor node is shown in Figure 1.

A brief overview of the ZeSCIP zero power AFE is given in Section II. In Section III, the modular printed-circuit board concept is presented. Section IV shows measurement approaches and results. Based on that, conclusions and prospects of the system are presented in Section V.

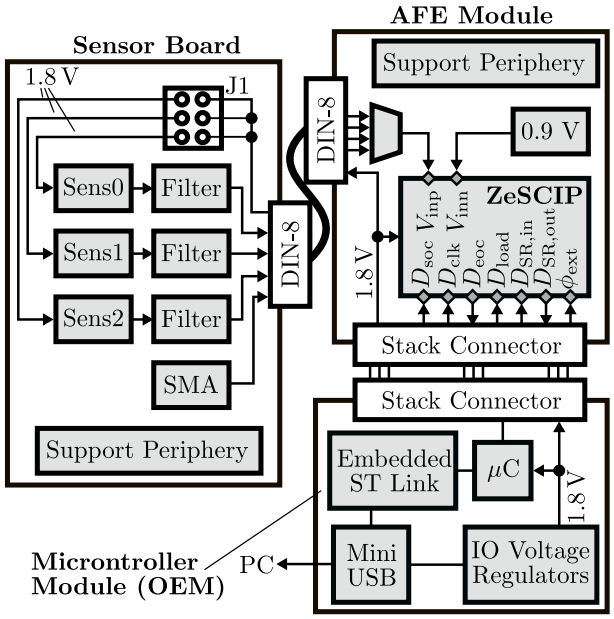

Fig. 1. Block diagram of modular multi-sensor node for environmental sensing

II. Zero Power Analog Frontend

A detailed block diagram of the ZeSCIP single-channel AFE is depicted in Figure 2. A switched-capacitor programmable gain amplifier (SC PGSA) serves as low-noise preamplifier with integrated sample-and-hold stage. It supplies one amplified sample of the sensor output voltage to the top-plates of a capacitive successive approximation analog to digital converter (SAR ADC). The buffer stage, which is typically inserted between SC PGSA and SAR ADC, is omitted in this topology.

The ZeSCIP AFE employs four programmable gain levels, rail-to-rail differential input range and a programmable resolution of 6 to 13 bit. Experimental results presented in page 4 show a maximum precision of 10.1 bit at a sample rate of 0.5 to 10 kS/s. Power consumption results of 1.96 µW (without SC PGSA) and 9.7 µW (including SC PGSA) are obtained. Table I shows key design specification and validated

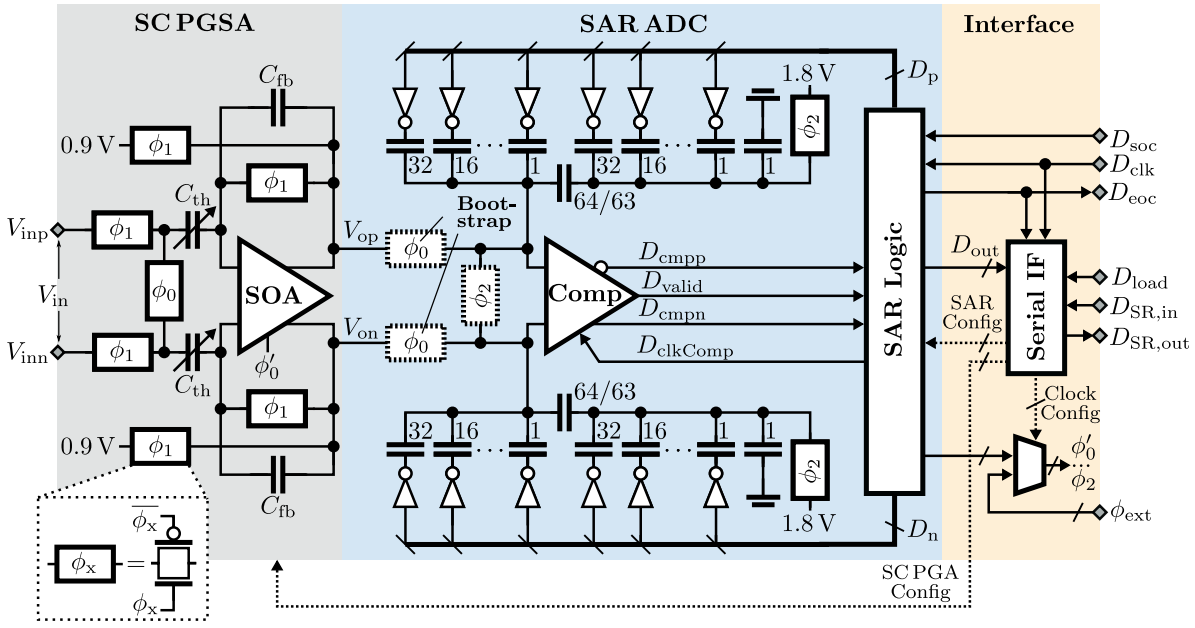

Fig. 2. Blockdiagram of ZeSCIP AFE

performances, compared to state-of-the-art AFEs.

A. SC Programmable Gain Switched Amplifier

The left side of Figure 2 shows the SC PGSA (grey-boxed), which combines the power-savings of switched opamp (SOA) technique with the area and accuracy benefits of switched capacitor (SC) circuits. The SC PGSA consists of a SOA and a SC network. The feedback capacitor C_{fb} and the variable track-and-hold capacitor C_{th} enable simultaneous sampling and gain adjustment. The waveforms of one conversion cycle are presented in Figure 3. In phase ϕ_1, C_{th} tracks the differential sensor output voltage V_{sens}, while the SOA is powered down and C_{fb} is shorted. Phase ϕ_0', which starts slightly (one half clock cycle) before ϕ_0, powers up the SOA. The feedback path of the SOA remains shorted by ϕ_1, and the voltage gain is defined by $C_{\mathrm{th}}/C_{\mathrm{fb}}$.

The power savings of a measurement cycle are result of the channel timing management approach. The clock generation of $\{\phi_1, \phi_0', \phi_0\}$ is derived from the ADC operation phase. The SC PGSA is enabled only one half clock cycle before the ADC sample phase (ϕ_0), while it is powered down during bit conversion phase (ϕ_1), avoiding any DC current components adding to the total power consumption. The active time $t_{\mathrm{on},i}$ of the power-demanding circuitry is minimized in relation to one conversion cycle t_{p}. The average dynamic power dissipation $P_{\mathrm{dyn},i}$ is therefore scaled with duty-cycled fashion:

$$P_{\mathrm{av,total}} = \sum_i \frac{t_{\mathrm{on},i}}{t_{\mathrm{p}}} \cdot P_{\mathrm{dyn,i}} + P_{\mathrm{dc,leak}} \qquad (1)$$

Where $P_{\mathrm{av,total}}$ is the total average power consumption and $P_{\mathrm{dc,leak}}$ are unavoidable leakage currents. In experiments, the ZeSCIP AFE can reduce the power consumption at a sample rate of 10 kS/s from 92.5 µW to 9.7 µW by a factor of 89%.

TABLE I
SPECIFICATIONS AND PERFORMANCES OF ZESCIP AFE AND COMPARISION TO STATE-OF-THE-ART AFES

	ZeSCIP [1], 2020	**[2] 2018**	**[3], 2017**	**[4], 2017**	**[5], 2016**
Supply (V)	1.8	0.6	1.2	0.3	1.8
Tech. (nm)	180	40	65	65	180
Sensor Type	IoT	Bio	Bio	Bio	N/A
Area (mm^2)	0.16	1	0.13	0.22	1.74
Sample rate (kS/s)	0.5-10	20-400	0.4	1.0	15.6
Resolution (bit)	6-13	13	10	8	8-12
ENOB (bit)	10.1	9.7	9.6	7	11.3
$\mathrm{FoM_{ADC}}$ (fJ/st.)	178.5	14.4	322.0	15.6	34.8
Gain (dB)	-6-12	20-30	N/A	40	40-60
Max. Bandwidth (kHz)	31.0	128	N/A	0.43	0.25
Power (µW)	1.96* / 9.7	0.24* / 3.8	0.1*	3.8e-3	9.5

* excluding preamplifier

B. Successive Approximation Register ADC

The capacitive SAR ADC within the blue box in Figure 2. During ϕ_0, the amplified sensor output voltages are sampled via bootstrapped switches on the top-plates of split-capacitor networks. As soon as the ϕ_1 phase starts, the clock signal D_{clkComp} triggers a comparision of the clocked comparator. The length of the D_{clkComp} pulse is self-defined by the

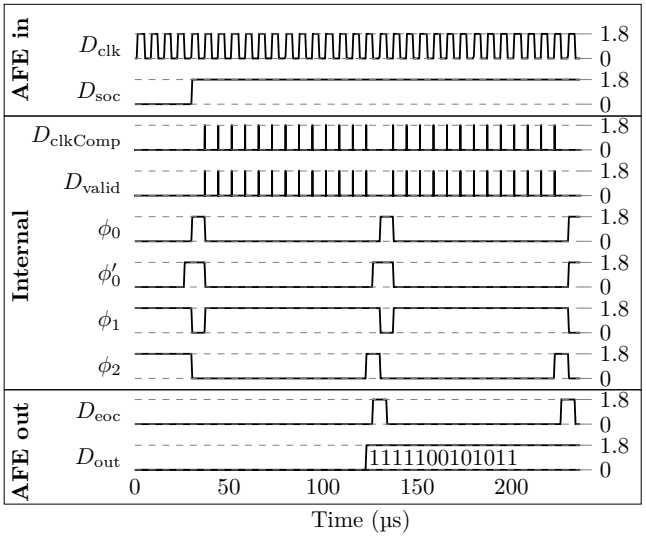

Fig. 3. Simulated waveforms of ZeSCIP's internal and interface signals within one single conversion cycle

loop formed of the comparator, a loop delay generating the D_{valid} signal, and the digital part. With a rising edge of D_{valid}, new values for the vectors D_{sp} and D_{sn} are generated. In that manner, the settling time of the capacitor network is maximized, ensuring accuracy and easing the design of the switch components. The generation of D_{sp} and D_{sn} follows the switching scheme suggested in [6], which employs high energy efficiency without additional reference buffers. However, the proposed scheme of this work is inverse. Charging of capacitors happens only in the first decision step and during reset, while during the rest of the cycle, capacitors are discharged. In that way, a better-performing NMOS comparator can be used and the generation of supply voltage drop is reduced.

C. Serial Interface and Clock Multiplexer

The connection between ZeSCIP and peripherals is achieved with a custom low-power serial interface based on SPI (orange box in Figure 2). Configuration data and parallel ADC output data are serialized, transmitted and saved in on-chip shift registers. The ASIC can be set in several debug modes. A clock multiplexer switches between ADC-controlled timing and external clock source ϕ_{ext}.

III. Modular Multi-Sensor Node

A photograph of the modular node is shown in Figure 4. It is implemented in three parts – the Microcontroller Module, the AFE Module and the Sensor Board, which are explained in the following sections. Important specifications and dimensions of the stack are listed in Table II.

A. Microntroller Module

The Microcontroller Module is a commercial STM32 NUCLEO™ board from STMicroelectronics,

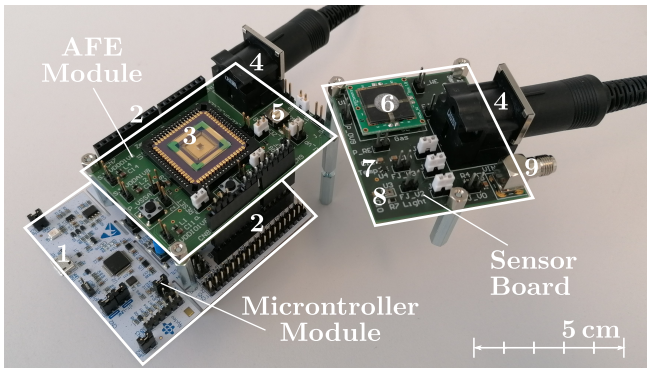

Fig. 4. Photograph of modular multi-sensor node stack with STM32 Nucleo™ Board

featuring a low voltage CMOS ARM Cortex M4 microcontroller [7]. This specific microcontroller is chosen due to its low power and low voltage operation, which makes it compatible with the 1.8 V operating voltage of the AFE's digital unit. The NUCLEO board provides a link to PC via Mini USB (1) and Arduino style headers (2), which form the basis of the modular approach presented here. It enables other commercially available modules, for example sensor or communication hardware, to be immediately connected to our stack for additional functionality. The stack is supplied either by the NUCLEO™ IO voltage of 1.8 V, or an external energy harvester module. The microcontroller carries setup code which configures the AFE's on power-up. A sensor signal is selected through a multiplexer, converted by the ZeSCIP to its digital representation, and transmitted via serial interface. The PC reads out the data through UART interface.

B. AFE Module

The AFE Module follows the structure and header style of the NUCLEO™ board in order to form the stack. A socket is used to mount the ZeSCIP AFE (3). Little peripheral hardware such as push buttons and jumpers serve for debugging and configuration purposes. A common mode bias of 0.9 V is generated on-board, which enables a single ended signal to

TABLE II
Modular multi-sensor node specifications and current measurement results

Supported Sensors	Ambient Light Intensity	ISL29102 (Renesas)
	Ambient Temperature	MAX6607 (TI)
	CO Gas Concentration	3SP_CO_1000 (Spec)
Power Consumption (mW)	Sleep Mode (Total)	2.2
	Active (Total)	17.1
	AFE Module	35.5e-3
	ZeSCIP AFE (incl. preamp)	9.7e-3
Physical dimensions (mm^2)	Micro-C Module	70.0 x 53.0
	AFE Module	53.0 x 74.5
	Sensor Board	47.0 x 53.5

be measured. The AFE Module carries an eight pin round connector (4) with a grounded shield. An eight core wire carries the power supplies of the Sensor Board, as well as the multiple sensor signals. A multiplexer component (5) selects one out of the sensor signals to be applied to the AFE's input V_{inp}.

C. Sensor Board

The wire-connected, smaller Sensor Board can be placed in a remote location, where the entire stack cannot be accommodated. It is designed for environmental sensing applications and contains three sensors (6,7,8) listed in Table II. Each sensor is selectively supplied via jumpers J1, in order to power-down complete sensor channels if unwanted. This functionality will be later integrated in the ZeSCIP. An additional SMA connector (9) is placed to provide an arbitrary signal input for testing purposes. Discrete support circuitry, provided by the manufacturers, is added to operate the sensors correctly.

IV. Measurement Results

The laboratory characterization of the stand-alone ZeSCIP device proved the general functionality and simulated behavior. Electrical performances of the SAR ADC like Effective Number of Bits (ENOB) and ADC Figure of Merit ($\mathrm{FoM_{ADC}} = P_{\mathrm{av,ADC}}$ / 2^{ENOB} / Sample Rate) were extracted and results are presented in Table III.

A validation of the modular setup was done in a second step. The SMA input of the Sensor Board is connected to a source which feeds a full sweep of single-ended input voltages from 0 to 1.8 V to ZeSCIP. This sweep is done in steps of 100 mV and the process is automated through a python interface to the measurement devices. The power supply of the AFE Module is provided through several source measuring unit channels, in order to measure the power consumption of analog and digital part of ZeSCIP and the module's I/O circuitry and periperals separately.

Plots of the conversion characteristics in Figure 5 for different gain settings, and measurement result of the power consumption parts are presented in Table II. The overall response is strongly linear. The power consumption of the AFE Module, excluding the Microntroller Module, is shown in Figure 5 and averages to 35.5 µW. Out of that, the ZeSCIP AFE (including preamplifier) needs 9.7 µW, while the remainder is consumed by peripherals. The complete modular sensor

TABLE III
Measurement results of stand-alone ZeSCIP SAR ADC (excl. preamplifier)

Parameter	Worst Sample	Best Sample
ENOB @ 1 kHz (bit)	8.0	10.1
$P_{\mathrm{av,ADC}}$ (µW)	1.98	1.96
$\mathrm{FoM_{ADC}}$ (fJ/st.)	773.44	178.5

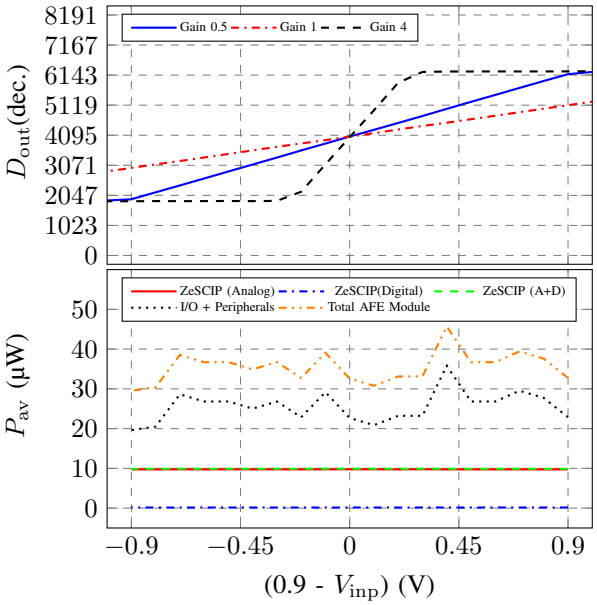

Fig. 5. Characteristics of AFE Module vs. Gain Settings, single-ended voltage input via SMA

node's consumes 17.1 mW in active (transmission) mode, and 2.2 mW in sleep mode, drawn from a 1.8 V source. These values results from the on-board periphery of the commercial Microcontroller Module, which are laid out for much higher computational power, and which are not powered-down during sleep mode. In order to reduce the node's active and sleep power towards microwatt resp. nanowatt level, a future setup of a highly integrated sensor node is already in design phase [8]. Custom-designed Microcontroller, software, transmitter, wake-up, energy harvesting and power management blocks are integrated in a printed-circuit board with small form factor. Each component is power-optimized in order to achieve zero-power consumption with the combined setup. The laid-out evaluation of ZeSCIP fits into that context and results are expected in the year 2021.

V. Conclusion

The presented modular multi-sensor node with ZeSCIP demonstrates new opportunities for the development of autonomous sensor nodes. The flexible test setup of Sensor Board and AFE Module is easily configured to fit desired application scenarios and different sensor types, while the backbone STM microcontroller is interchangeable with other, application specific hardware. In experiments, the power consumption of the AFE Module was measured to be lower than 35.5 µW in average, with three commercial sensors attached. The setup can be further extended with energy harvesters to achieve lifetime extension towards true zero power operation. In that way, the broad functionality and zero power capability of ZeSCIP is demonstrated.

ACKNOWLEDGMENT

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