IIP Generators to Ease Analog IC Design

Benjamin Prautsch, Uwe Eichler, Torsten Reich
Fraunhofer IIS/EAS, Institute for Integrated Circuits,
Engineering of Adaptive Systems, Dresden, Germany
{Benjamin.Prautsch, Uwe.Eichler, Torsten.Reich}@eas.iis.fraunhofer.de

***Abstract*—Semiconductor technology has shown significant progress over the last decades. Digital EDA (electronic design automation) allowed that this progress could be converted to high-performance digital ICs. Analog components are part of Systems-on-Chip (SoC) too, but analog EDA lags far behind. Therefore, a lot of effort was spent to automate analog IC design. Mayor results are constraint-based layout-aware optimization tools using predefined layout templates or pure automation as well as analog generators containing expert knowledge. While optimization is a holistic top-down approach, generators allow parameterized and fast bottom-up generation of critical schematic and layout parts, pre-planned by experienced designers. With IIP Generators, we follow three use cases to ease analog design: 1) design on higher hierarchy levels, 2) development of hierarchical high-level IIPs, and 3) automated design porting due to highly technology-independent blocks down to 22nm.**

Keywords—Analog Design Automation, Analog Generators, IIP, Reuse, 22 nm FD-SOI

I. Introduction

Academic work on analog design automation reaches from layout-aware top-down flows over template-based approaches to bottom-up generators. We believe that generators will become a crucial part in future analog automation flows. Also, generators may significantly enhance productivity in conventional design flows.

II. Generator-Based Analog Design

Using generators, the following three fundamental partly automated design approaches can be pursued (see Fig. 1).

A. Base-Level Design Entry

In the standard design flow, every single transistor is placed into (hierarchical) schematics. With generators, basic building blocks, such as differential pairs or current mirrors (but also more complex blocks), can be encapsulated. Therefore, design effort is reduced to placement and routing of more complex building blocks.

B. Hierarchical High-Level Generator Development

Since IIPs handle hierarchies seamlessly and exactly the same way as designers do using hierarchical library cells, any kind of hierarchical circuit can be implemented as an IIP. It was shown in the past that, depending on the particular circuit, implementation effort of IIPs can pay out quickly [1].

C. Generator-Based Design Porting

The underlying abstract IIP description language [2] can handle various technologies, currently ranging from 180 nm down to 22 nm. This approach is constantly improved to reach ever higher degrees of technology independence. Currently, mapping of devices, device parameters with constraints, layers and vias, static and dependent design rules, derived layers as well as access of further process data is supported by IIP.

IIPs can be (re)executed for multiple technologies and specifications based on user-defined parameter sets. As IIPs are used during design entry (II.A.), the resulting cell can be copied to other processes followed by one single re-execution of the contained IIPs. Alternatively, hierarchical IIPs (II.B.) can be developed (with tool support). As the result, all required data (schematic, symbol, and layout) is available in the new technology—within minutes (II.C.).

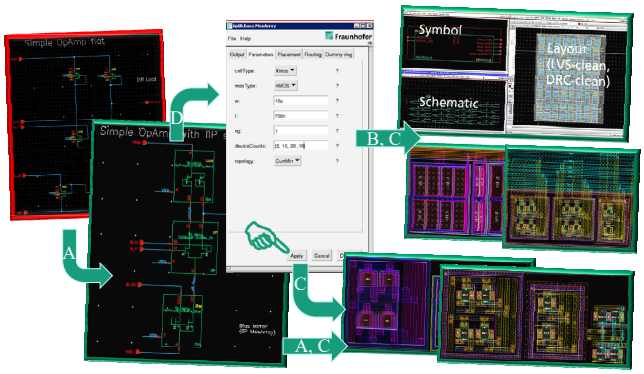

Fig. 1 Use cases of IIP-based analog IC design: A) base-level design entry, B) hierarchical IIP development, and C) design porting by IIP re-execution for other technologies or specifications. Moreover, IIP code templates can be generated from existing schematics (D) which eases both B and C.

III. Conclusion and Outlook

Generators such as our IIPs are capable of increasing design efficiency while automation ensures a high level of design safety. IIPs accelerate design entry and allow the development of complex analog soft IPs down to 22 nm. Furthermore, a high degree of technology independence is supported based on the generic IIP description language.

Next steps will concern both further discussion of technology independence and the interface between top-down automation and bottom-up generators.

Acknowledgements

This work was partly supported by the European Union and the Free State of Saxony within the projects THINGS2DO (Ref. No. 16ES0240) and PRIME (Ref. No. 16ESE0110S).

References

[1] B. Prautsch, S. Rao, U. Eichler, A. Puppala and T. Reich, "A DAC stage analog circuit generator for UDSM and FD-SOI technologies," *University Booth of Design, Automation and Test in Europe Conference & Exhibition, DATE 2016,* 14–18 March 2016.

[2] B. Prautsch, U. Eichler, T. Reich, A. Puppala and J. Lienig, "Abstract technology handling for generator-based analog circuit design," *VDE/VDI-Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik -GMM-:,* pp. 56–61, 21–22 September 2015.