W-Band LNA MMICs Based on a Noise-Optimized 50-nm Gate-Length Metamorphic HEMT Technology

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***Abstract* — In this paper, the design, analysis, and room-temperature performance of two W-band LNA MMICs fabricated in two different technology variations are presented. The investigation demonstrates the noise improvement of the given 50-nm gate-length InGaAs mHEMT technology with reduced necessary drain currents. Therefore, a single-ended and balanced W-band LNA MMIC were designed, fabricated, and characterized. The amplifiers exhibit state-of-the-art noise temperatures with an average value for the single-ended LNA of 159 K (1.9 dB) with lowest values of 132 K (1.6 dB). Due to the technology investigation it was possible to reduce the noise temperature by about 15 K compared to the reference technology in combination with superior MMIC yield.**

***Keywords* — Balanced amplifiers, high-electron-mobility transistors (HEMTs), low-noise amplifiers (LNAs), millimeter-wave integrated circuits (MMICs), E-band, W-band.**

I. Introduction

Low-noise amplifiers (LNAs) are crucial building blocks that are used in a multitude of systems, such as radio astronomy, wireless communication, passive imaging and radiometric systems, or earth observation. Over decades, radio astronomy had, most likely, the most ambitious noise requirements. However, since a few years quantum computing is an increasing topic and thus, limits of today's low-noise technologies have to be pushed even further. While state-of-the-art quantum computing systems utilize LNAs in the low gigahertz range, there is an increasing interest for low-noise technologies at higher frequencies that can answer to these needs. An advantage of high-electron-mobility transistor (HEMT) technologies which are based on an InGaAs channel is not only that state-of-the-art noise performance can be achieve but also that such a process can address room temperature and cryogenic applications with the same technology. Since the drain noise current spectral density is proportional to the drain current [1], in general, a low-noise technology should enable small drain currents while still achieving a high transconductance (g_m).

State-of-the-art LNA millimeter-wave integrated circuits (MMICs) in W-band (75 to 110 GHz) yield noise temperatures (T_n) of about 130 K (NF = 1.6 dB) for some part of the band [2–4]. In [2, 4], this was achieved with an $In_{0.8}Ga_{0.2}As$ channel. Over the entire band an average noise temperature of 159 K (NF = 1.9 dB) was published [4].

Based on a 50-nm gate-length InGaAs mHEMT process, two technology variations are investigated, fabricated, and analyzed by means of dc and RF measurement data. First, the technology variations are introduced. Next, a single-ended and a balanced LNA MMIC design are presented. The measured data of these circuits are the basis for the given analysis.

II. Technology Description

This work is based on a 50-nm gate-length InAlAs/InGaAs mHEMT technology. For a lattice matched growth of the HEMT layers on 100-mm semi-insulating GaAs wafers, a metamorphic buffer is used. The 2-D electron gas is confined in a composite $In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ channel. The T-gates are defined by electron beam lithography. The gates are encapsulated in benzocyclobutene (BCB) and a 250-nm-thick SiN layer which also acts as dielectric layer of the on-wafer metal–insulator–metal capacitors. The process features two metallization layers; the top layer in air bridge technology. After the front side process, a full back side process follows. This includes wafer thinning to 50-µm-thickness, through substrate via holes, and back side metallization. Apart from the standard process (named Technology B), a noise-optimized variation (Technology A) is presented and investigated. A major difference is that Technology A utilizes only the $In_{0.8}Ga_{0.2}As$ main channel and no composite channel.

III. Low-Noise Amplifier MMICs

The single-ended LNA MMIC is based on a four-stage common-source topology with inductive source degeneration in all stages for an improved simultaneous noise and power input matching. Each transistor has a total gate width of $4 \times 12\,\mu\mathrm{m}$. For an improved bandwidth, the stubs at gate and drain as well as the source transmission lines use a high characteristic impedance. The layout of the circuits is realized in a grounded coplanar waveguide with a ground plane separation of 50 µm. For stability reasons, the stages two to four contain 10-Ω resistors in the RF drain path. The design concept is introduced in [4]. The balanced LNA MMIC is based on the single-ended version with slight adjustments. Simulations show unconditional stability of the balanced LNA even if the resistors in the drain path are removed. Hence, no resistor in the RF drain path are used. For the balanced topology, a Lange Coupler is used. A comparison of the 3D-EM simulation and the fabricated test structures is depicted in Fig. 1 and a good agreement between prediction and measurements can be observed. To simplify the S-parameter measurements, the two test structure were fabricated, both with an on-wafer terminated isolation port. The amplitude balance is better than ±0.5 dB from 65 to 120 GHz and the

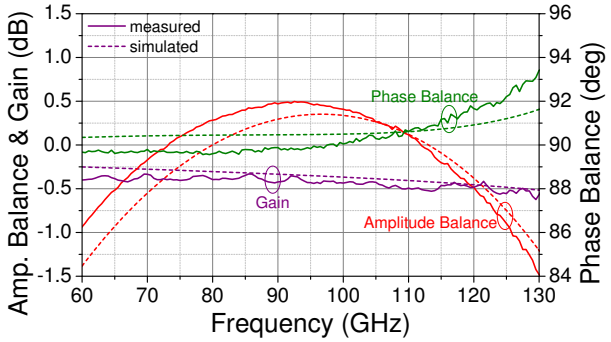
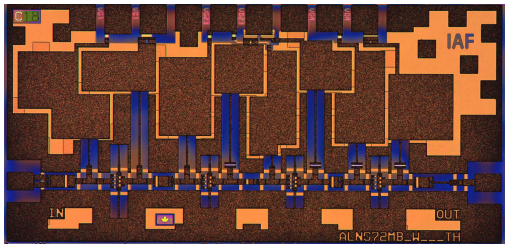
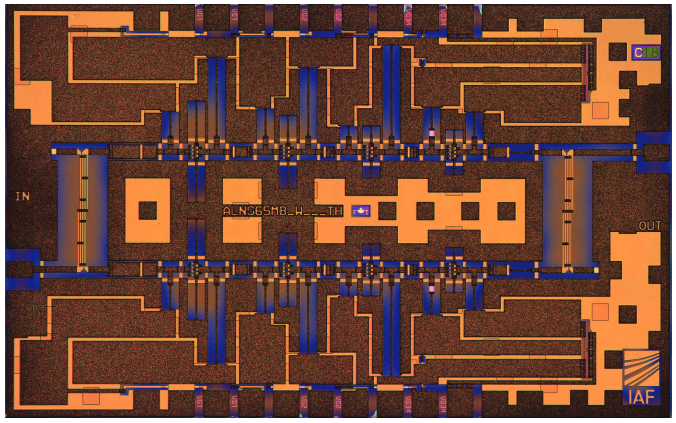


Fig. 1. On-wafer amplitude balance, phase balance, and gain of the utilized Lange Coupler. The measurements and 3D-EM simulations are shown as solid and dashed lines, respectively.



(a) Single-ended LNA.



(b) Balanced LNA.

Fig. 2. Chip photographs of the fabricated LNA MMICs. The dimensions of (a) the single-ended and (b) the balanced LNA are $(1.5 \times 0.75)\,\mathrm{mm}^2$ and $(2 \times 1.25)\,\mathrm{mm}^2$, respectively.

phase balance is within an error of 1° over most of the band. The loss is between 0.3 and 0.5 dB. Photographs of the fabricated MMICs are shown in Fig. 2.

IV. Measurement Results and Discussion

A. Dc Measurements

In Fig. 3, the dc g_m of $2 \times 60\,\mu\mathrm{m}$ transistors that are fabricated in Technology A (left) and B (right) is shown. The drain voltage (V_d) and current (I_d) at the device level are varied from 0.1 to 1 V and 50 to 500 mA/mm, respectively. For both technology versions, the maximum g_m is about 2100 mS/mm. However, while Technology B requires a drain current of more than 500 mA/mm, achieves Technology A peak g_m for less than 400 mA/mm. Furthermore

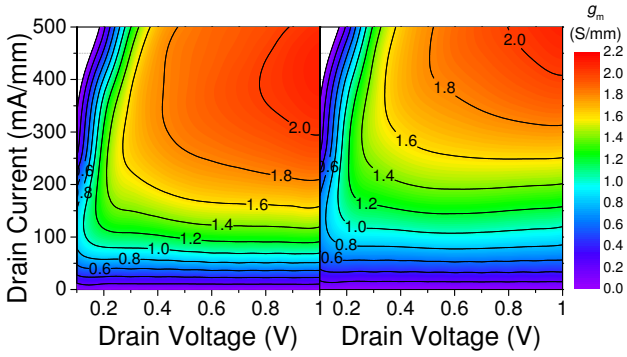
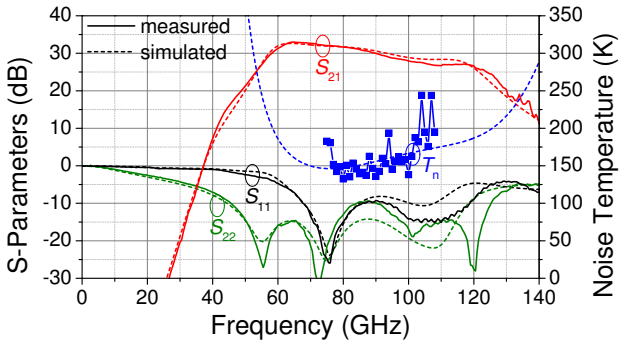
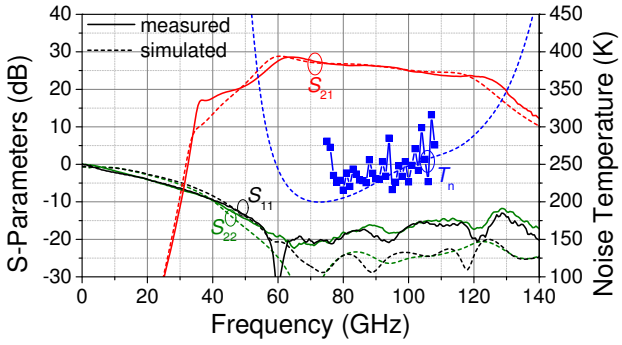


Fig. 3. Contour plots of the measured dc transconductance of (left) Technology A and (right) Technology B. Drain voltage and current of a $2 \times 60\,\mu\mathrm{m}$ transistor are varied from 0.1 to 1 V and 50 to 500 mA/mm, respectively.



(a) Single-ended LNA.



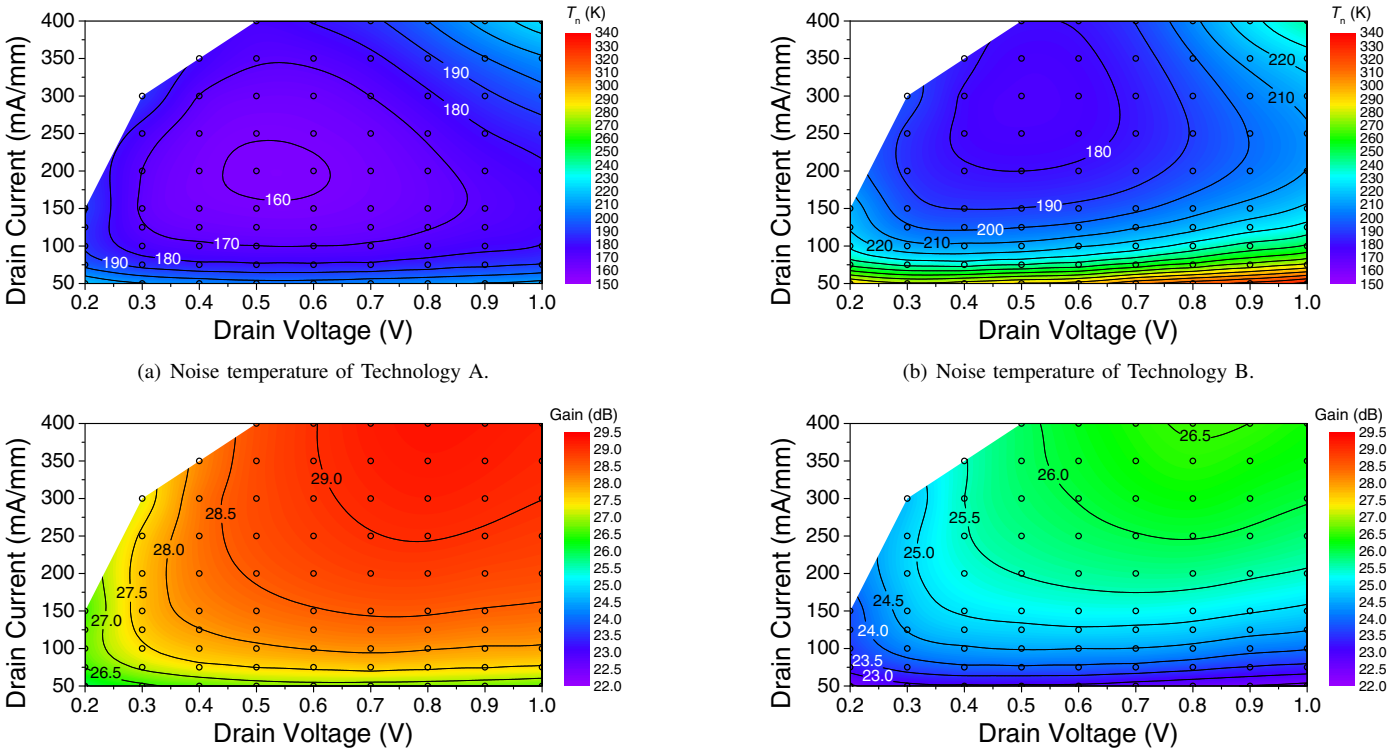
(b) Balanced LNA.

Fig. 4. Measured and simulated (dashed lines) on-wafer S-parameters and noise temperature versus operating frequency of (a) the single-ended and (b) balanced LNA MMIC fabricated in Technology A. Both LNAs are bias for optimum noise with a drain voltage at transistor level of 0.6 V and a drain current of 200 mA/mm.

for noise-optimal drain currents (75 to 200 mA/mm), the transconductance of Technology A is about 300 mS/mm higher than for Technology B; e.g. at a bias of V_d = 0.6 V and I_d = 200 mA/mm, g_m reaches for Technology A and B 1.71 and 1.44 mS/mm, respectively. Thus, already the given dc data indicate that Technology A offers advantages at common low-noise bias conditions. Both technologies feature typical drain-gate breakdown voltages of >3 V (@ $I_\mathrm{g} = 1\,\mathrm{mA/mm}$).

B. RF Measurements

The on-wafer S-parameters of the fabricated circuits are measured using an Anritsu VectorStar (0 to 145 GHz). The



(a) Noise temperature of Technology A.

(b) Noise temperature of Technology B.

(c) Gain of Technology A.

(d) Gain of Technology B.

Fig. 5. Contour plots of the on-wafer measured T_n and gain versus V_d and I_d of the first stage of the single-ended LNA. The bias of the other stages is kept constant. Gain and T_n are measured for the given supporting points (black circles) and are averaged over the entire frequency range from 75 to 108 GHz.

on-wafer noise measurement setup is based on an ELVA-1 WM-2540 waveguide noise diode and operates from 75 to 108 GHz. The down-converter after the device under test utilizes a commercially-available fundamental mixer module. The actual noise measurements are performed with a Keysight noise figure analyzer at an intermediate frequency of 99 MHz.

In Fig. 4, the S-parameters and noise temperature of the single-ended and balanced LNA MMICs fabricated in Technology A are depicted. Both circuits are biased for optimum noise performance with a drain voltage and current of 0.6 V and 200 mA/mm, respectively. The single-ended LNA yields a small-signal gain of more than 25 dB over a frequency range from 60 to 124 GHz. At 65 GHz, a peak gain of 33 dB is achieved. The input and output return loss is better than 10 dB over most part of the band. The noise temperature exhibits an average value of 159 K ($NF = 1.9$ dB) with values between 132 and 243 K (1.6 to 2.6 dB). The measured performance of the balanced LNA is shown in Fig. 4(b). The achieved gain is better than 23 dB over a frequency range from 60 to 124 GHz and peaks a value of 28.5 dB at 65 GHz. The input and output return loss is between 14.5 and 22 dB. The noise temperature is between 215 and 316 K (2.4 to 3.2 dB) and exhibits an average value of 242 K ($NF = 2.6$ dB). The simulations are illustrated as dashed line in Fig. 4 and for both circuits a very good agreement with the experiment can be observed.

For a comprehensive comparison of the two investigated mHEMT technologies, two experiments were performed. First, the noise temperature and gain of the single-ended LNA were measured and compared for a multitude of bias points. Second, the noise and gain of the single-ended LNA MMIC were measured on three wafers for each technology version. Thus, 111 MMICs were tested for each technology version. Furthermore, the balanced amplifier version was as well measured for Technology A on three wafers.

The measured results for investigating the bias dependence of the technologies are illustrated in Fig. 5. For this experiment, the bias only of the first stage was varied between V_d = 0.2 to 1 V and I_d = 50 to 400 mA/mm. Low drain voltages and high drain currents were excluded in order to prevent the gate diode to get conductive. The bias of the latter stages is fixed at V_d = 0.6 V and I_d = 200 mA/mm for Technology A and V_d = 0.6 V and I_d = 250 mA/mm for Technology B. For each supporting point, a noise and gain measurement were performed and averaged. The gain contours of both technologies are comparable with a slightly higher gradient for currents below 100 mA/mm for Technology B. However, a more obvious difference between Technology A and B is a gain difference of about 3 dB. The benefit of Technology A is even more distinct when considering the noise contour. First of all, Technology A has a noise advantage of 15 K at the noise-optimal bias point which is at a drain current of 200 mA/mm, whereas Technology B requires a drain current of 300 mA/mm for optimum noise performance. Furthermore, the contour of Technology A is much more flat.

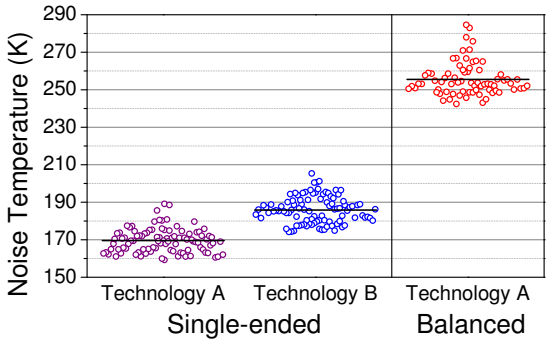


Fig. 6. Measured average noise temperature (75–108 GHz) for the single-ended LNA MMIC processed in Technology A and B and the balanced LNA MMIC processed in Technology A. Each technology and amplifier version were measured on three different wafers. This includes 111 test MMICs per circuit type and technology. Circuits that utilize Technology A are biased as stated above (V_d = 0.6 V and I_d = 200 mA/mm), whereas the single-ended MMIC with Technology B is biased with an I_d of 250 mA/mm.

While Technology A achieves a noise temperature of 180 K (2.1 dB), which is only an increase of about 20 K, over a large bias range, a comparable area for Technology B is much smaller. In addition, the noise temperature degrades stronger for drain currents below 100 mA/mm.

The second experiment includes the measured noise temperature and gain of 111 tested MMICs from three wafers of Technology A and B for the single-ended LNA and of Technology A for the balanced LNA. In Fig. 6, the corresponding scatter diagram is illustrated. 65 % of the tested balanced MMIC are working with an average noise temperature of 255 K (2.7 dB). The overall yield of the single-ended LNAs is for both technologies 89 % with mean values for Technology A and B of 169 and 186 K (2 and 2.15 dB), respectively. This demonstrates a distinct benefit of the noise performance of Technology A.

C. Discussion

Even though there is only one difference between the two technology variations, the difference in RF performance, especially noise, is quite strong. Our explanation for the different behavior of the technologies is given in the following part. For the on state of Technology B, the electrons in the composite channel concentrate mainly in the $In_{0.8}Ga_{0.2}As$ channel. When pinching off the channel, the electron concentration is more and more shifted towards the sub-channel where the indium content is only 53 %. This results in a shift of the threshold voltage towards more negative gate voltages and the g_m curve is widened. Effectively, the pinch-off behavior of Technology B is degraded due to the possibility of the electrons to be pushed into the sub-channel. In addition, the electron mobility in the $In_{0.53}Ga_{0.47}As$ channel is reduced which unfavorably impacts the noise performance. It is the idea of Technology A to prevent this behavior by fully removing the $In_{0.53}Ga_{0.47}As$ sub-channel and exclusively utilizing an $In_{0.8}Ga_{0.2}As$ channel. We believe that the presented dc and RF data can confirm this hypothesis.

Table 1. State-of-the-Art W-Band LNA MMICs

Ref.	Technology	Topology	Freq. (GHz)	P_{dc} (mW)	Gain (dB)	T_n (K)
[5]	50-nm mHEMT	single-ended	65–101	38.4	20–27	139–226 (66–104 GHz)
[4]	50-nm mHEMT	single-ended	49–117	34.6	20–27	180 (149–238) (75–110 GHz)
[2]	50-nm mHEMT	single-ended	30–100	45	20–26	159 (129–202) (71–86 GHz)
[3]	35-nm InP HEMT	single-ended	75–90	6.9	22.5–29	129–226
		balanced	75–100	29.7	20–28	214–289
[4]	35-nm mHEMT	single-ended	52–126	40.8	23–28	159 (129–191) (75–110 GHz)
This work	50-nm mHEMT "A"	single-ended	60–124	30.3	25–33	159 (132–243) (75–108 GHz)
This work	50-nm mHEMT "B"	single-ended	60–120	35.3	23–28.5	174 (151–265) (75–108 GHz)
This work	50-nm mHEMT "A"	balanced	60–124	50.2	23–28.5	242 (215–316) (75–108 GHz)

V. Conclusion

In this paper, two 50-nm gate-length mHEMT technology variations have been investigated and compared. Based on single-ended and balanced LNA MMIC designs, the advantages and disadvantages of a pure $In_{0.8}Ga_{0.2}As$ and a composite $In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ channel are analyzed at room temperature. As a result of this work, state-of-the-art performance (average T_n = 159 K; NF = 1.9 dB) has been achieved (as illustrated by Table 1) demonstrating that an optimized 50-nm gate-length mHEMT process can achieve results which were previously only realized, over a comparable bandwidth, by 35-nm gate-length transistors. Furthermore, high yield is demonstrated which makes the noise-improved technology a promising candidate for room-temperature and cryogenic applications, such as wireless communication, imaging systems, radio astronomy, or quantum computing.

Acknowledgment

The authors would like to thank the colleagues in the IAF epitaxy and technology departments for their excellent contributions during epitaxial growth and wafer processing. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 730562.

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