Originally published in: 2022 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC) | ©2022 IEEE | DOI: 10.1109/INMMIC54248.2022.9762221

Harmonic-Injection Doherty Power Amplifiers with a High Small-Signal Gain

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***Abstract*—This paper presents a novel Doherty power amplifier (DPA) in which a second harmonic (2*f*0) current is injected into the drain of the auxiliary device. Hence, the name harmonic-injection Doherty power amplifier (HI-DPA). The performance parameters of the HI-DPA are analytically derived and show that the injection of a 2*f*0 current into the drain of the auxiliary device reduces the maximum current required from the auxiliary PA. Consequently, the portion of input power allocated to the auxiliary PA reduces, resulting in a significant improvement in small-signal gain (SSG) and power-added efficiency (*PAE*) compared to the conventional DPA. The analytical results are validated through the design and simulation of two GaN HEMTs single-stage HI-DPAs exhibiting a SSG of 9.5 and 13.6 dB at 3.6 GHz while maintaining a high *PAE* at peak and 6 dB back-off power.**

Keywords—Doherty power amplifier, harmonic-injection, high-efficiency, high-gain

I. Introduction

The Doherty power amplifier (DPA), introduced in [1] and further analyzed in [2]-[3], has found widespread usage due to its ability to amplify signals with a high peak-to-average power ratio (PAPR) while maintaining a high-efficiency operation. However, the Class-C biased auxiliary power amplifier (PA) adopted in the DPA in [2]-[3] has a lower fundamental-frequency (f_0) drain current relative to the Class-B biased main PA. Hence, the auxiliary PA requires a higher portion of input power to generate the f_0 current required to modulate the impedance seen by the main device. However, the auxiliary PA is off during the small-signal operation of the DPA. Thus, allocating a large portion of input power to the auxiliary PA severely impedes the small-signal gain (SSG) and subsequently the power-added efficiency (*PAE*) of the DPA. The generalized DPA analysis reported in [4] shows that the SSG increases by maximizing the portion of input power allocated to the main PA while in [5], it was shown that adopting a Class-AB bias condition on the main PA increases the SSG of the DPA. The harmonic injection technique was used in the DPAs in [6]-[8], where the $2f_0$ components of the main and auxiliary devices are injected into each other's drains through a harmonic injection network. The HI-DPA in [6] exhibits an extended back-off range at the expense of reduced circuit bandwidth while those in [7]-[8] employ a modified harmonic-injection network to address the circuit bandwidth limitations and linearity of [6].

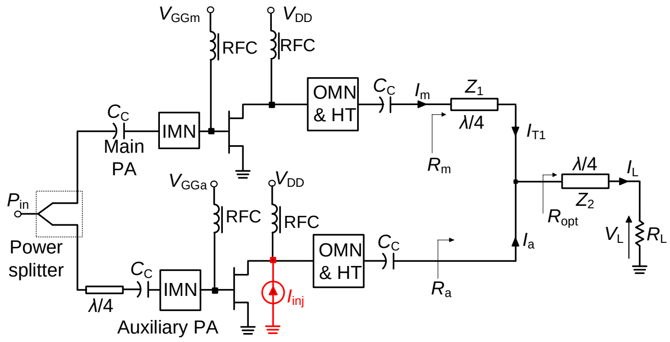

Fig. 1. Proposed harmonic–injection Doherty power amplifier.

In this paper, we investigate the effect of a second harmonic injection ($2f_0$) on the DPA. This investigation is conducted through the analysis of a harmonic-injection Doherty power amplifier (HI-DPA) depicted in Fig. 1, wherein a $2f_0$ current is injected into the drain of the auxiliary device. Unlike, the DPAs in [6]-[8], the HI-DPA herein presented employs an external PA to inject the $2f_0$ current only in the auxiliary cell. It will be shown that the proposed HI-DPA requires an auxiliary device with a lower maximum current compared to the conventional DPA. Hence, the size of the auxiliary device with respect to that of the main device decreases leading to less input power P_{in} required by the auxiliary PA. Consequently, the portion of P_{in} delivered to the main PA increases resulting in a higher SSG and *PAE*. Increasing the SSG of the DPA is of interest as it relaxes the requirement on the driver PA, subsequently improving the overall efficiency of the transmitter system.

II. Idealized Circuit Operation And Analysis

The proposed HI-DPA shown in Fig. 1 consists of an input power splitter, a Class-B biased main PA operating at f_0, a Class-C biased auxiliary PA operating at f_0, an output power combiner, and a Class-C biased injection PA (IPA) operating at $2f_0$. The IPA is represented by an ideal current source for sake of simplicity. The purpose of the IPA is to inject a $2f_0$ current into the drain of the auxiliary device. The Class-C bias condition on the IPA implies that the $2f_0$ current injection occurs at the break-point. Hence, in the low power region, the working principle of the proposed HI-DPA is similar to the DPA reported in [5].

To simplify, the analysis of the HI-DPA shown in Fig. 1, the following assumptions are introduced:

1. The transistor is modeled as an ideal voltage-controlled

current source.

2. The same drain bias voltage is used on the main and auxiliary PA.
3. The phase-offset between the main and auxiliary PA is $\pi/2$
4. The IPA and auxiliary PA only interact at $2f_0$.

The current flowing through the drain of the main device is given in [5, eq. (1)] while current flowing through the drain of auxiliary device is given by

$$i_{da}(\theta) = \frac{v_i I_A}{1-\cos\left(\frac{\theta_A}{2}\right)}\left(\cos(\theta) - \cos\left(\frac{\theta_x}{2}\right)\right) + v_i I_{inj}\cos(2\theta) \tag{1}$$

which is valid for $-\theta_x/2 \leq \theta \leq \theta_x/2$ and where $0 \leq v_i \leq 1$ is the normalized input signal. I_A is the maximum current of the auxiliary device, θ_A is the auxiliary device current conduction angle at the maximum input signal, i.e., $v_i = 1$, and I_{inj} is the amplitude of the $2f_0$ injected current. It can be shown that the maximum current of the auxiliary device is related to that of the main device, I_M by (2) while the input power splitting factor of the auxiliary PA is given in (3).

$$\frac{I_A}{I_M} = \frac{\sin^2\left(\frac{\theta_A}{4}\right)\left(\theta_M - \sin\left(\theta_M\right)\right)}{4\sin^2\left(\frac{\theta_M}{4}\right)} - \frac{4I_{inj}\sin^3\left(\frac{\theta_A}{4}\right)\cos\left(\frac{\theta_A}{4}\right)\left(\cos\left(\theta_A\right)+2\right)}{3I_M} \tag{2}$$

$$\psi_A = \frac{1}{\left[\frac{I_M g_{mA}{}^2(\zeta-1)(v_{bk}-1)}{I_A g_{mM}{}^2}\right]^2 \frac{R_{inA}}{R_{inM}} + 1} \tag{3}$$

with θ_M in (2) being the main device current conduction angle at $v_i = 1$, while ζ is defined as the ratio between the selected dc bias point, and the maximum current of the main device I_M. The parameter v_{bk} is the input signal level at which the auxiliary PA turns-on. The parameters g_{mM} and g_{mA} are the trans-conductance of the main and auxiliary devices while R_{inM} and R_{inA} are the input resistances of the main and auxiliary devices. The normalized maximum current of the auxiliary device I_A/I_M and the input power splitting factors ψ_M and ψ_A are plotted in Fig. 2(a) versus the normalized $2f_0$ injected current I_{inj}/I_M.

Fig. 2(a) shows that $I_A = 1.27$, $\psi_M = 0.13$, and $\psi_A = 0.87$ for $I_{inj} = 0$. Thus, the HI-DPA exhibits the characteristics of the DPA. As I_{inj} increases, I_A and ψ_A decrease while ψ_M increases. A symmetrical HI-DPA, i.e., $I_A = I_M$, is obtained at $I_{inj} = 0.4$ with $\psi_M = 0.2$ and $\psi_A = 0.8$. At $I_{inj} = 1.1$, the size of the auxiliary device is half that of the main device, i.e., $I_A = I_M/2$ and the input power is equally shared between the main and the auxiliary PA, i.e., $\psi_M = \psi_A$. Fig. 2(a) also provides an insight into the relative size of the IPA device, a relatively small IPA device ($I_{inj} = 0.4$) is required for a symmetrical HI-DPA while a relatively large device ($I_{inj} = 1.1$) is required for an even input power splitting.

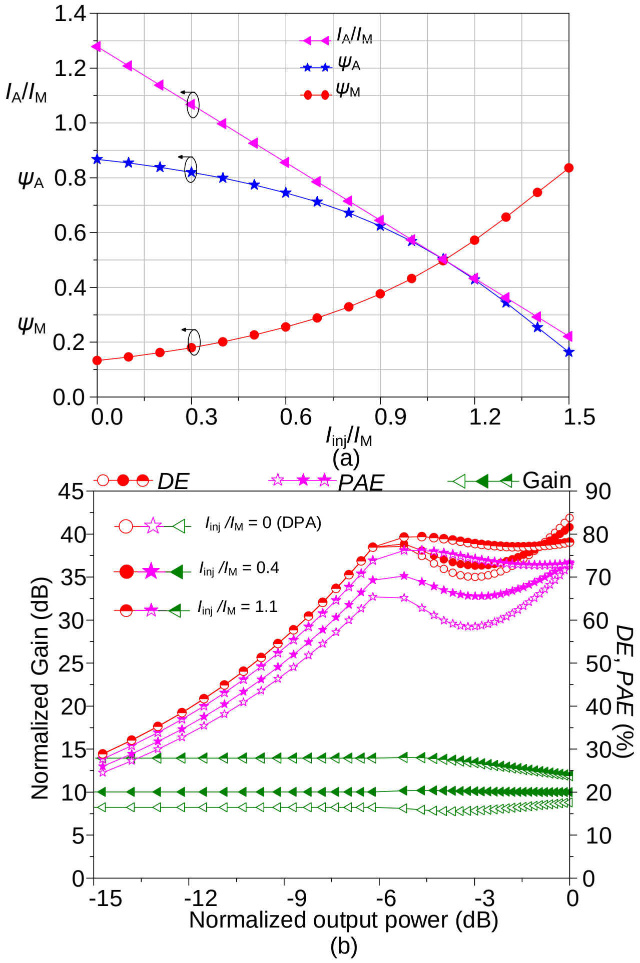

Fig. 2. Theoretical performance parameters of the proposed HI-DPA: (a) normalized maximum current of the auxiliary device and input power-splitting factor of the main and auxiliary device, (b) normalized gain, *DE,* and *PAE.*

The performance of the HI-DPA is plotted in Fig. 2(b) versus the normalized output power. Three distinctive values of I_{inj} are considered for a back-off range of 6 dB. The gain is normalized to a Class-A gain of 20 dB and the drain efficiency (*DE*) of the IPA is assumed to be 60%. As expected, Fig. 2(b) shows that for $I_{inj} = 0$, the HI-DPA exhibits the performance of the conventional DPA with a SSG of 8.3 dB. A significant performance improvement is observed as I_{inj} increases. It worth noting that for $I_{inj} = 0.4$ (symmetrical HI-DPA), a linear gain of 10 dB is achieved. The achieved linear gain has a direct effect on improving the linearity of the HI-DPA. As I_{inj} further increases to 1.1, the SSG increases to 13.9 dB, and the gain compression at peak power increases to 2 dB. The significant improvement in SSG translates into an increased *PAE*.

It worth mentioning that the HI-DPA outperforms the conventional DPA in term of SSG. Nonetheless, the IPA operates at $2f_0$ thus, the efficient operation thereof is strongly influenced by the size of the active device used in the design. Generally, for an efficient PA design, a smaller device size is adopted as the frequency of operation increases. Hence, the symmetrical HI-DPA ($I_{inj} = 0.4$) would be suitable for the lower millimeter wave frequencies applications given that the size of the IPA device is much smaller than those of the main and auxiliary PA. On the other hand even input power split HI-DPA (I_{inj} = 1.1) would be suitable for sub 6 GHz applications given that the size of the IPA device is almost the same as that of the main device.

III. Design And Simulations

To validate the theoretical results presented in Section II, a single stage symmetrical and an even input power split HI-DPA were designed and simulated in ADS at 3.6 GHz using large signal models of the Fraunhofer IAF 500 nm GaN HEMT technology (GaN50). Load pull simulations were performed on the devices to extract the optimum load-line resistance (R_{LL}) with the corresponding device output capacitance (C_{out}). The Doherty combiner in [9] was adopted as output matching network and power combiner while the device C_{out} was absorbed by a short-circuited transmission line through which the dc supply voltage is supplied to the devices. The isolation circuit in [10] was incorporated between the auxiliary PA and the injection port, which represent an IPA with an assumed *DE* of 60%.

Fig. 3 shows the simulated performance of the designed HI-DPAs compared to the performance of a conventional DPA designed using the same active device under the same operating conditions in terms of frequency of operation and dc bias. The two HI-DPAs exhibit a SSG of 9.5 and 13.6 dB at 3.6 GHz, which is 1.9 and 6 dB higher than that of the DPA. The design parameters and performance of the HI-DPAs are summarized in Table I.

IV. Conclusion

The analysis of a novel harmonic-injection Doherty power amplifier (HI-DPA) has been presented. The proposed PA maintains a high-efficiency operation over a 6 dB back-off range with a relatively small auxiliary device. The injected second harmonic current reduces the size of the auxiliary device resulting in an improved small-signal gain and power-added efficiency. The relatively high small-signal gain relaxes the requirements for a driver PA hence improving the overall transmitter's efficiency.

Acknowledgment

This project has received funding from the European Union's Horizon 2020 research and innovation program under the Marie Sklodowska-Curie grant agreement No. 860023.

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TABLE I
Design Parameters and Performance Summary Of HI-DPAs

Parameters	Conventional DPA	Symmetrical HI-DPA	Even input power split HI-DPA
Size of main device (mm)	25.6	25.6	25.6
Size of Aux. device (mm)	32.6	25.6	12.8
P_{in} split main PA (%)	13	20	50
P_{in} split Aux. PA (%)	87	80	50
P_{inj} (dBm)	n/a	45	47
P_{out} (dBm)	56.4	57.2	57.1
SSG (dB)	7.6	9.5	13.6
PAE at peak power	55	62	62
PAE at 6 dB back-off	43	50	58

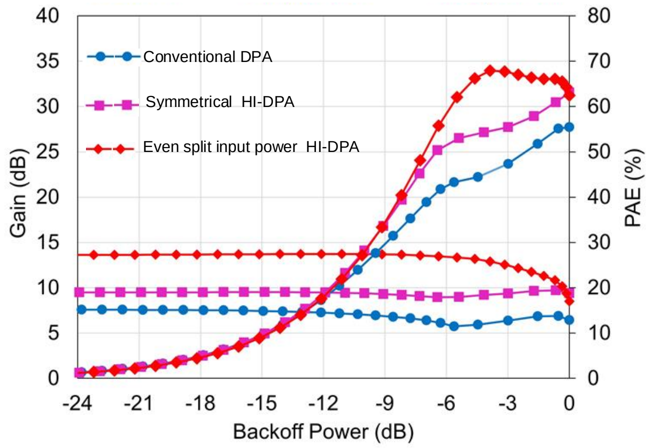

Fig. 3. Simulated performance versus normalized output power at 3.6 GHz.

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