Device Design and Process Integration of SiC Trench MOSFETs

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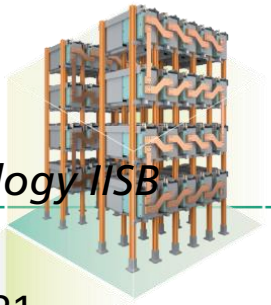

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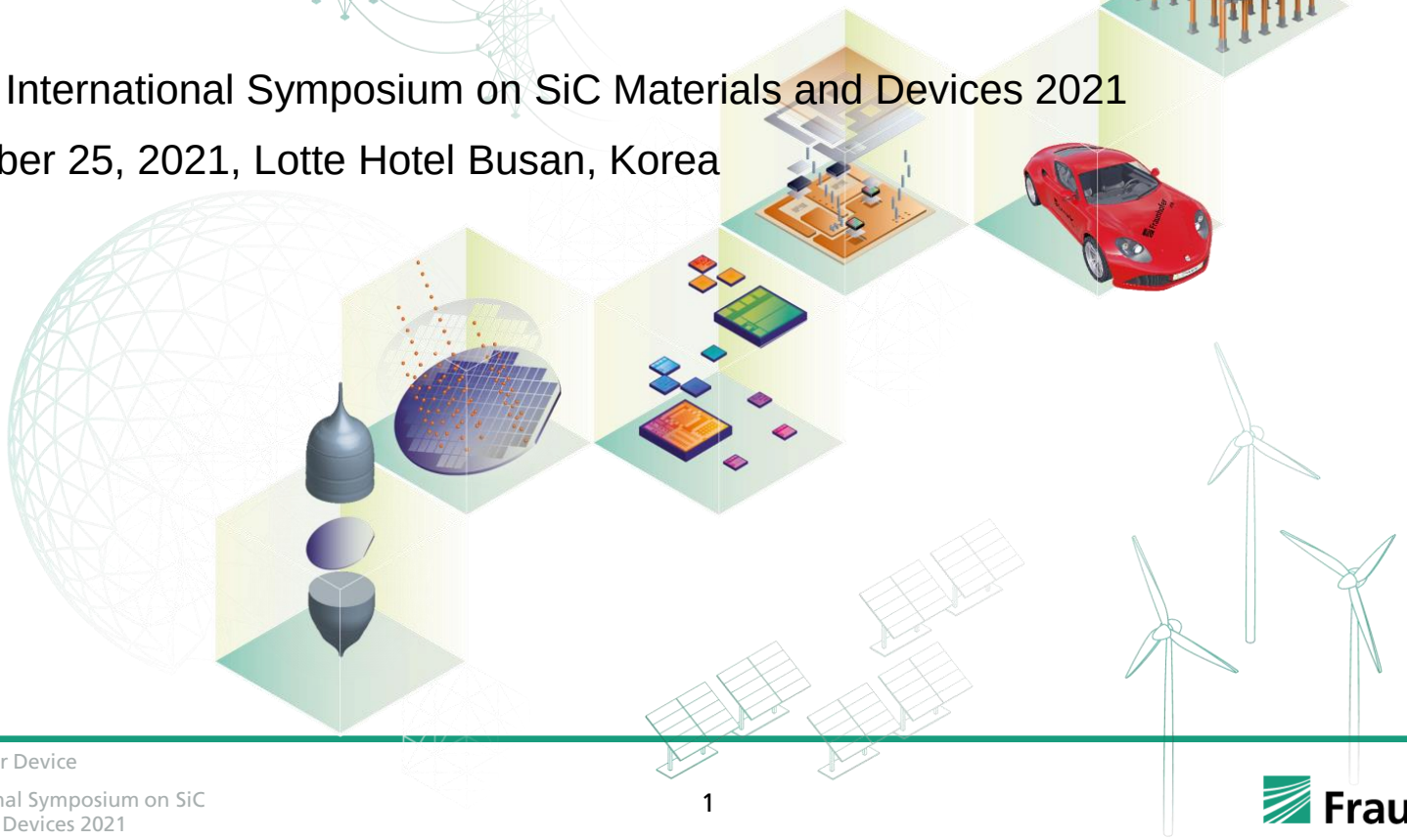

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- Motivation
  - Additional shielded TrenchMOS design
  - Exploiting benefits of trench-first process
- Design optimization of Double-TrenchMOS
  - Initial design proposal
  - Process flow modeled by using process simulation
  - Static electrical characteristics by using device simulation
- Process Integration
  - Edge termination verified simulation
  - Gate oxide reliability and interface quality
- Conclusion

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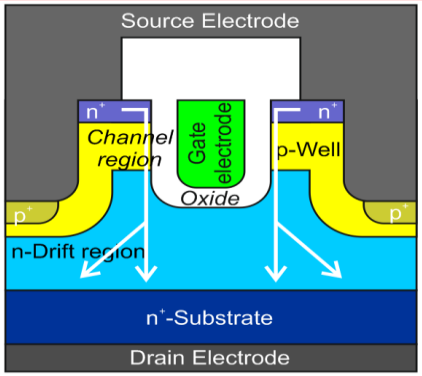
State of the Art
Additional shielded TrenchMOS Design

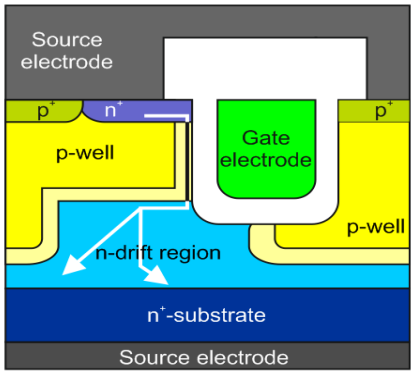
Trench structure compared to planar structure

- ☺ Higher cell density w/o JFET region
- ☺ Higher mobility due to vertical channel
  - → Reduction of resistance
  - → Saving chip area and chip cost
- ☹ Needed stable technology for trench etching
- ☹ Gate oxide reliability has to be improved
  - → Additional shielding required



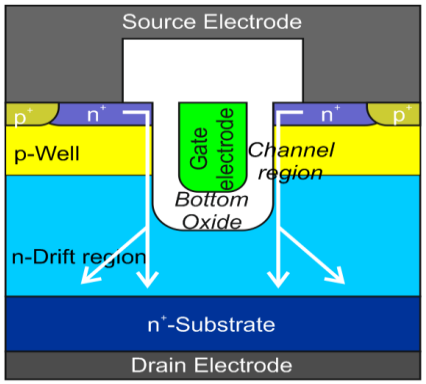
Double-UMOS

- Proposed by Rohm
- Deep p-well by double-trench
- BV = 1746 V demonstrated
- $\rho_{DS,on}$ = 2.8 mΩcm²



Single channel-UMOS

- Proposed by Infineon
- Deep p-well by single channel
- BV = 1366 V demonstrated
- $\rho_{DS,on}$ = 3.2 mΩcm²



Thick bottom oxide-UMOS

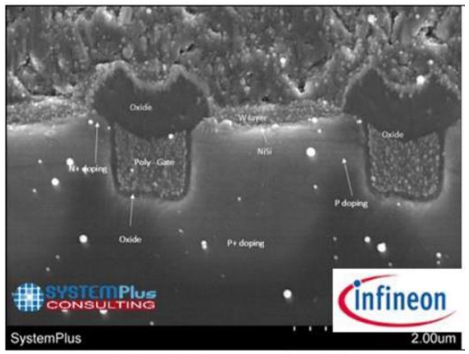
- Proposed by Bosch
- Thick bottom oxide
- 1.5 mΩcm² at 600 V
- 2.7 mΩcm² at 1200 V

Exploting Benefits of Trench-First Process

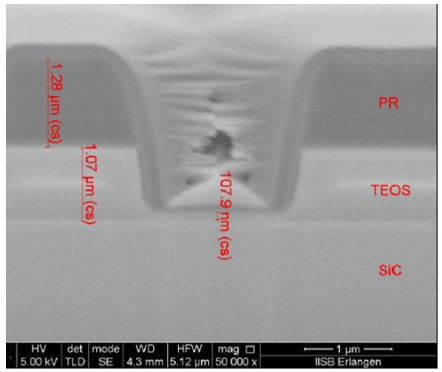
Stable technology of critical fabrication step

"Implantation-First" process

- A maximal alignment accuracy is allowed
- Difficulty to control the etching behavior
  - → Undesirable RIE-rate for ion-implanted silicon carbide
  - → Optimal etching process needed for every implantation parameters
- Obstacle by passivating layer and persistent Si + O layers



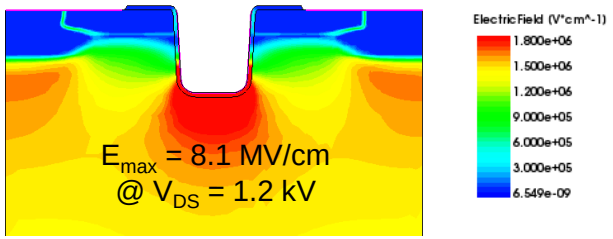
Infineon Mosfet cross section : SEM view



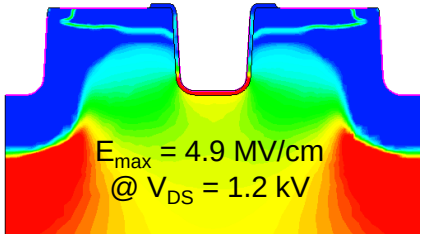
"Trench-First" process

- Stable SiC-trench etching
- High temperature annealing
  - → Reshaping trench formation to minimize dielectric breakdown field concentration
  - → H_2-etching is favorable for surface conditioning [1].
- Implantation mask is required?
  - → Self-aligned process proposed!

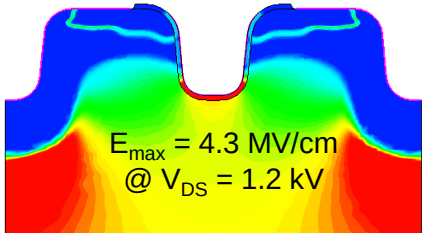
Conventional UMOS



Double-UMOS



Reshaped Double-UMOS



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Device Design Optimization

Design proposal

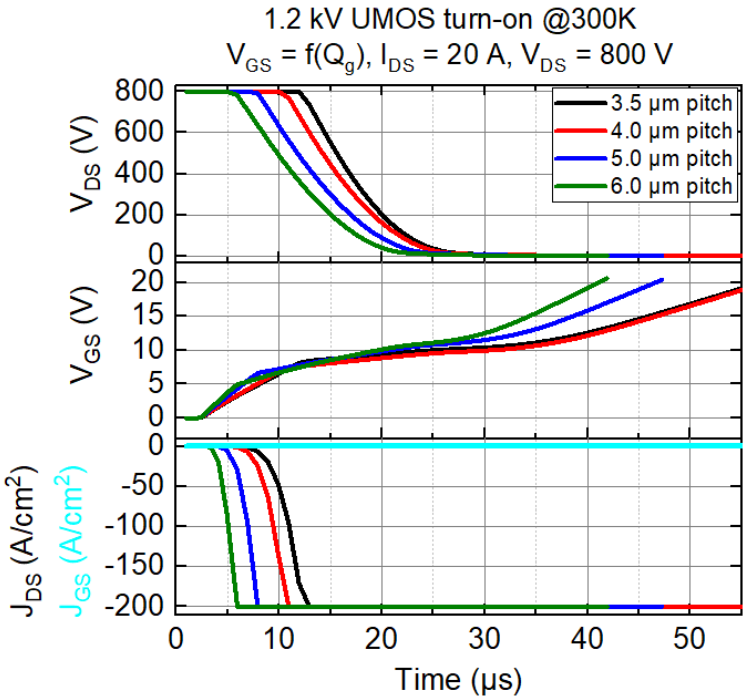
Technology variation

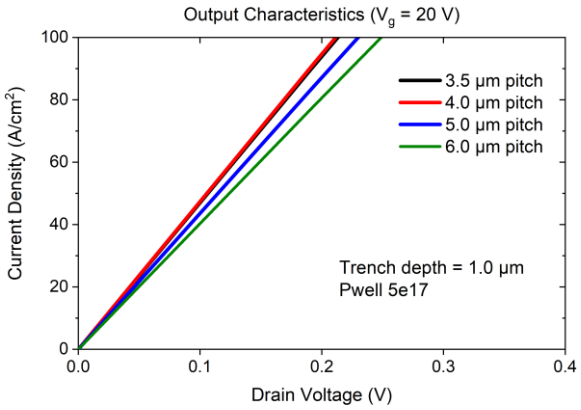
- Performance vs. Manufacturability
- Performance vs. Shielding for gate oxide
- Pitch: … / 3.5 µm / 4.0 µm / 5.0 µm / …

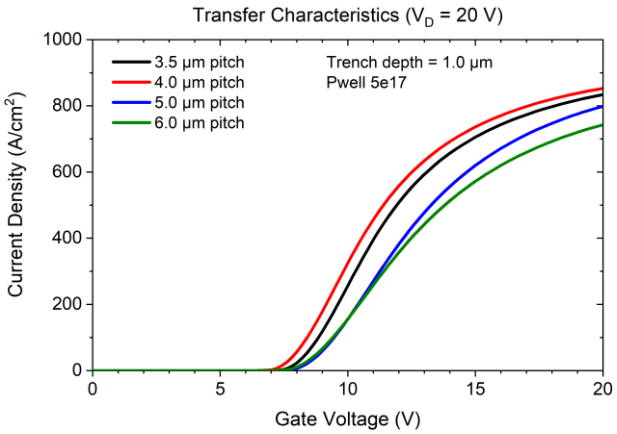
TCAD simulation

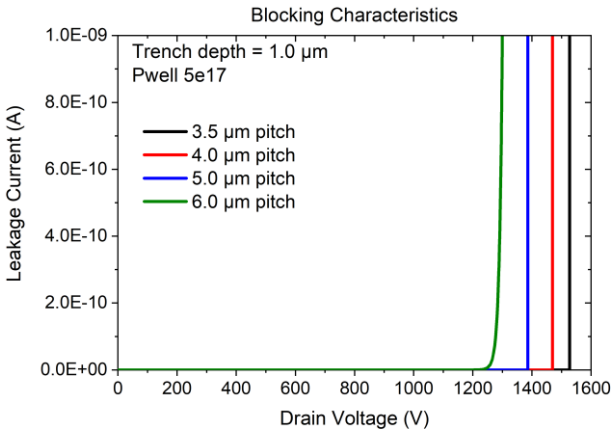
- Charge compensation
- D_{it} from planar devices
- Smaller cell pitch

→ Lower $R_{DS,on}$, higher BV









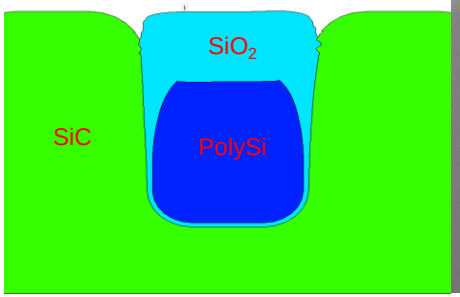
Device Design Optimization

Process flow of fabricated devices based on modeling by using process simulatioin

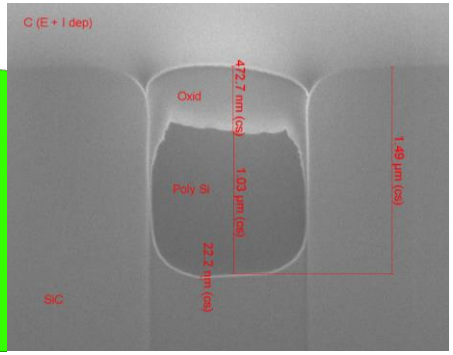
Self-aligned n⁺-source and p-well implantation

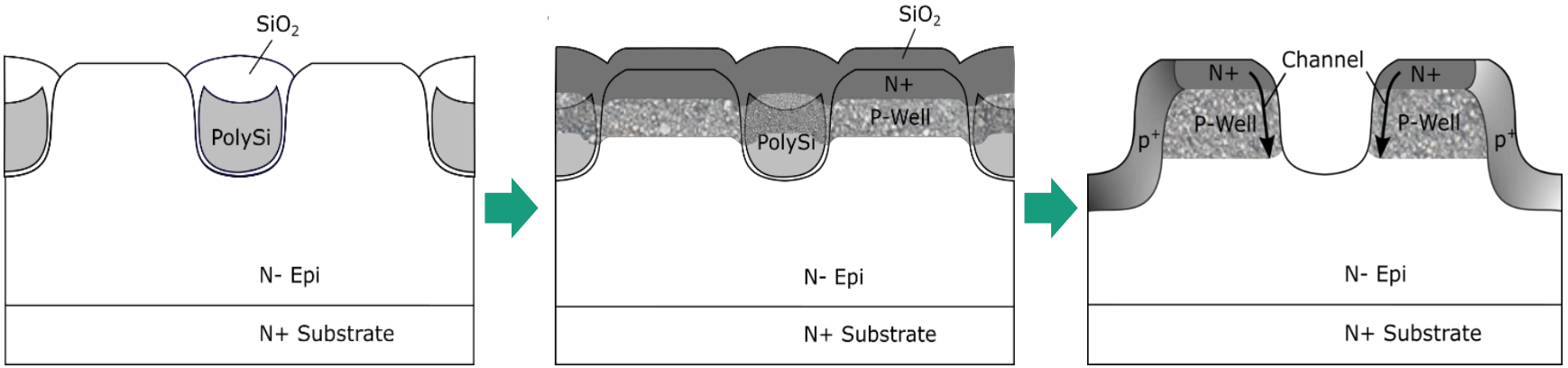
- Deposited and planarized Poly
- Low temperature oxidizing Poly
- Independent on the resolution of lithography system
- Channel length can be controlled by determination of oxide thickness
- Formation of oxide-cap can be surely predicted by calibrated process simulation

Process simulation



Fabricated sample



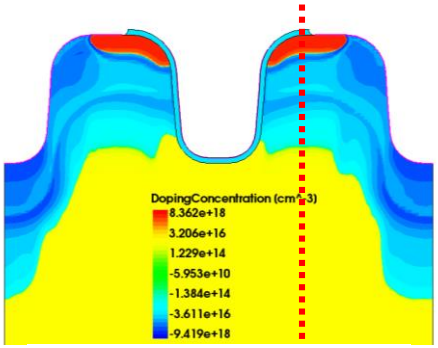


Device Design Optimization

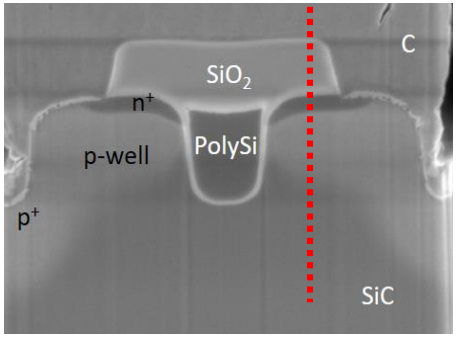
Process flow of fabricated devices based on modeling by using process simulatioin

Ion-Implantation from MC process simulation calibrated by

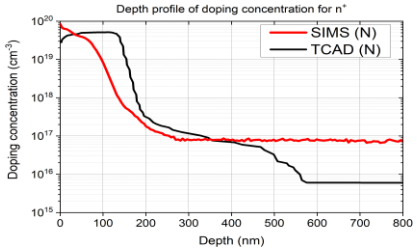
- SEM dopant contrast quantitatively
- SIMS measurement qualitatively

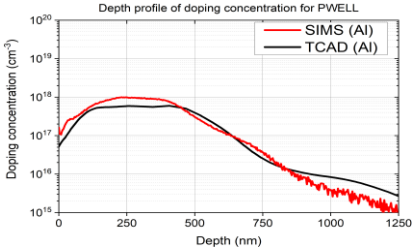


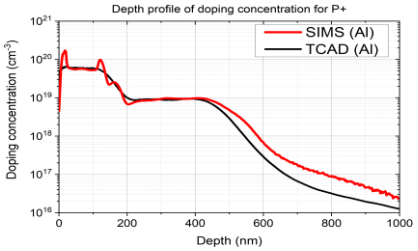
TCAD process model



Fabricated TrenchMOS

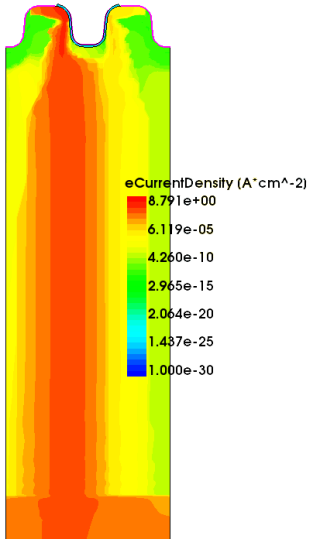


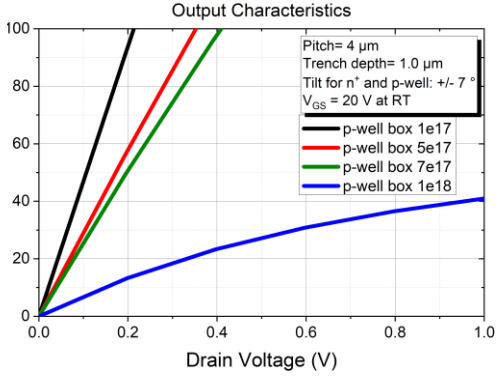




p-well implantation optimization

- Appropriate p-well parameter should be verified due to a trade-off
- Too lower doses prone to reach-through breakdown effect
- Too higher doses cause higher resistance and threshold voltage





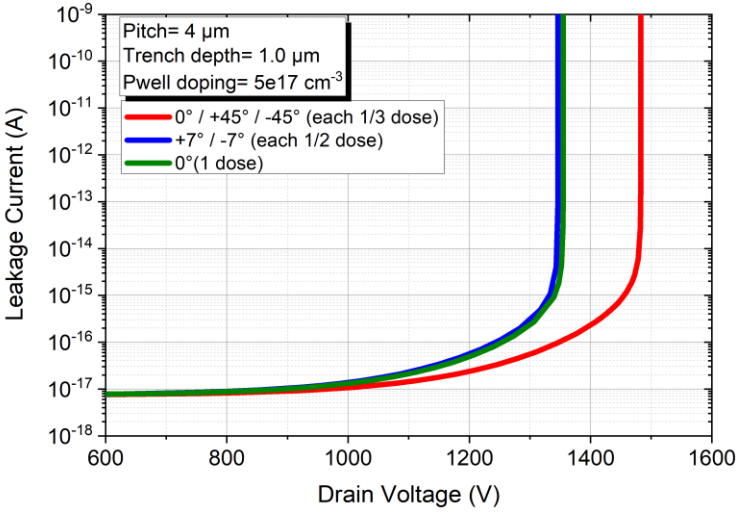
Device Design Optimization

Process flow of fabricated devices based on modeling by using process simulatioin

p+-shielding implantation

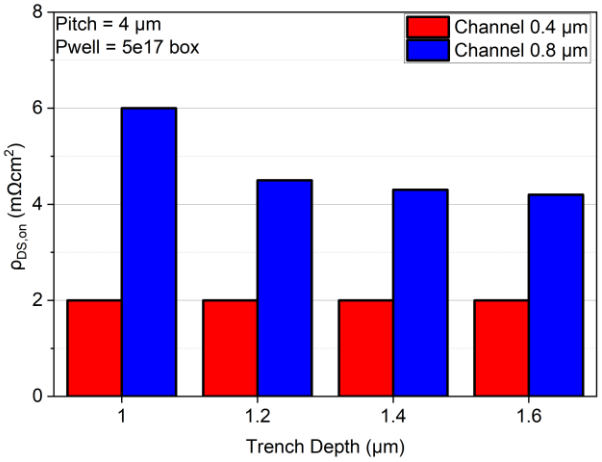
- Tilted implantation proposed
- Trench width : depth = 1: 1

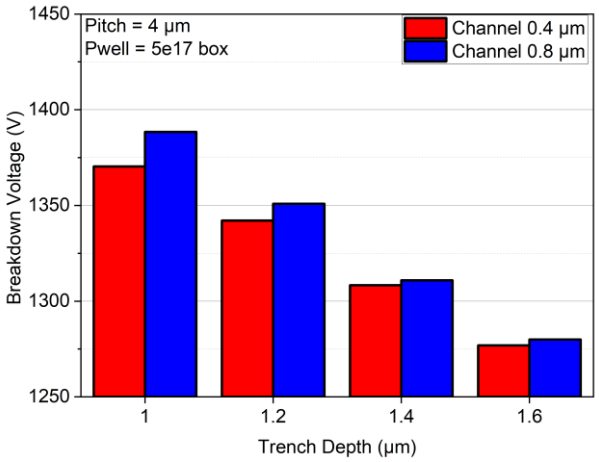
  → +45° / -45° / 0° for symmetrical doping profile
- Too high energy or doses are to be cautiously used due to deteriorating $R_{DS,on}$ from increasing the effectiveness of JFET region between p-body



Trench depth

- Deeper trench is not absolutely beneficial for BV with limited max. implant energy
- Optimized channel length for trench depth accordingly



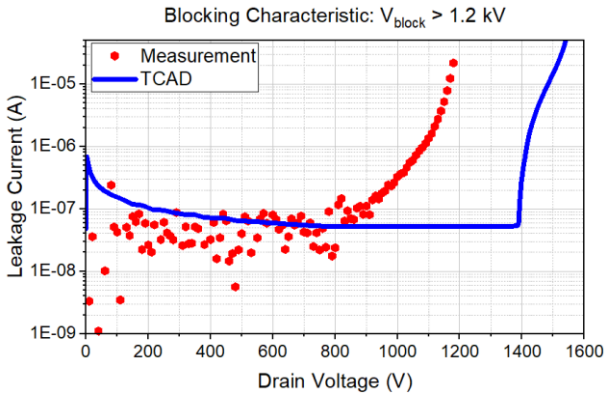


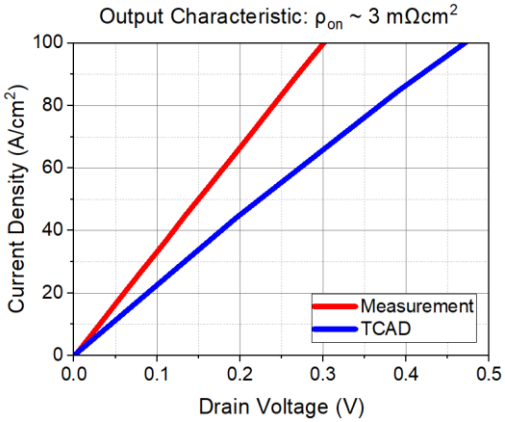
Device Design Optimization

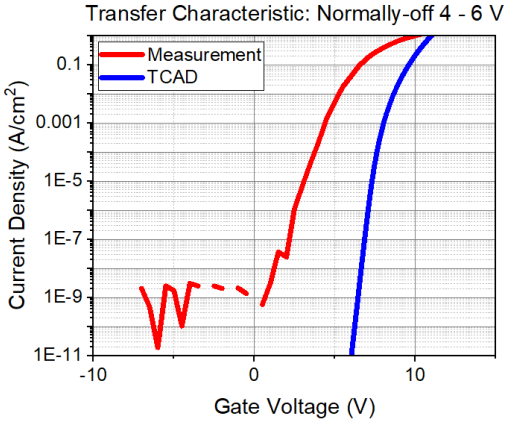
Static electrical characteristic

Achieved ~1.2 kV and > 50A devices → Room for improvement

- Blocking capability
  - Short channel effect: Possibility for higher blocking voltage (~1.6 kV) with optimized p-well implantation parameters
  - Tilted p^+-shielding implantation
- Output- and transfer characteristic
  - Design optimization: Short circuit causing increased leakage current
  - Misalignment field oxide and shallow n^+-source regioin should undergo improvment
  - Gate oxide optimization for higher mobility, dielectric breakdown field strength and improved threshold voltage shift







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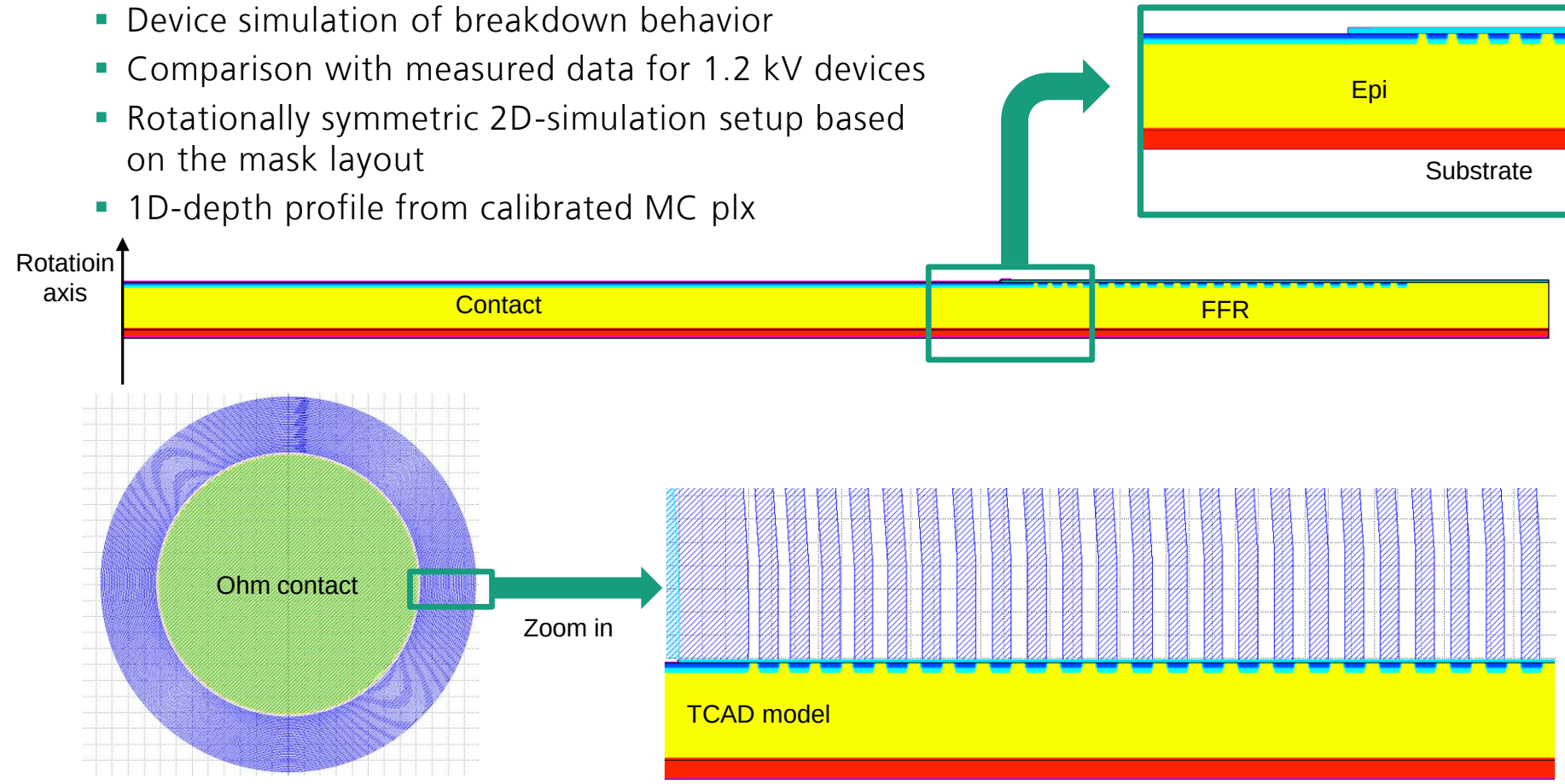
Process Integration

Edge Termination verified by TCAD simulation

Floating Field Ring

- Device simulation of breakdown behavior
- Comparison with measured data for 1.2 kV devices
- Rotationally symmetric 2D-simulation setup based on the mask layout
- 1D-depth profile from calibrated MC plx

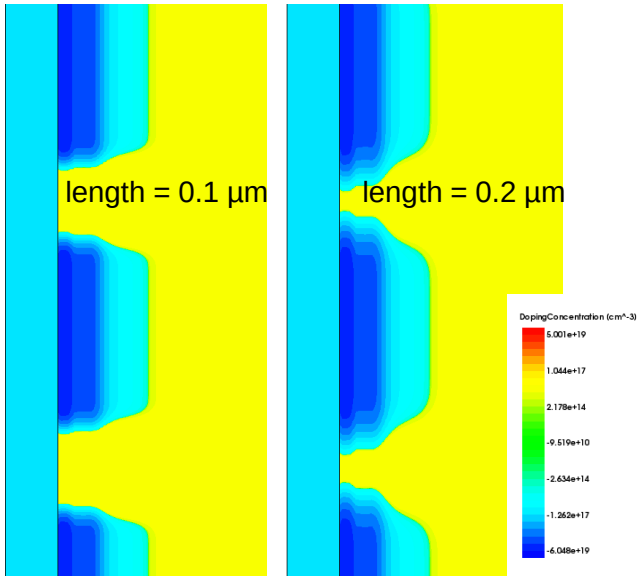


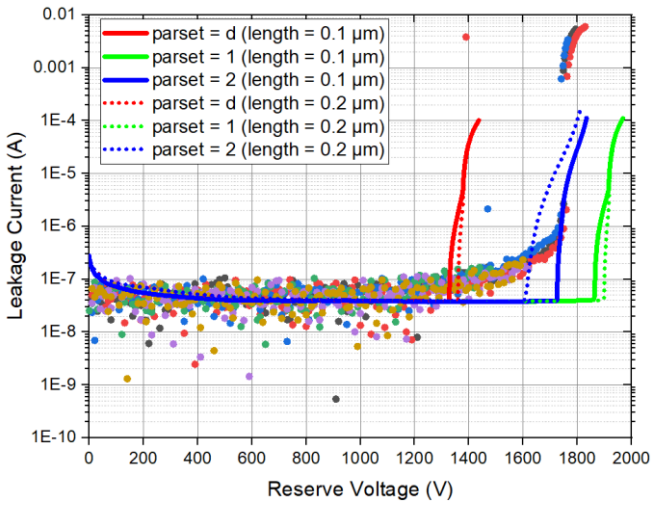
Process Integration

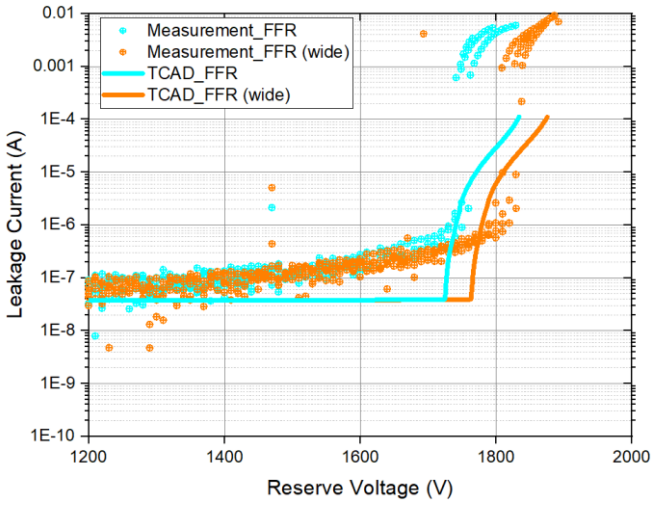
Edge Termination verified by TCAD simulation

Floating Field Ring

- Breakdown behavior depending on lateral scattering (parameter “length“)
- Avalanche model dependency:
  - d (default): Van Overstareten
  - parset = 1: Application Library
  - parset = 2: Material DB
- Optimal ring distance for increasing blocking capability
- Model calibration for JTE, Trench-FFR and SJ-FFR for HV (> 3.3kV) devices







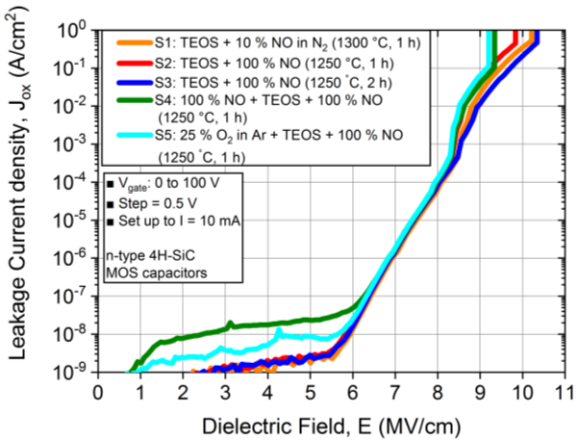
Process Integration

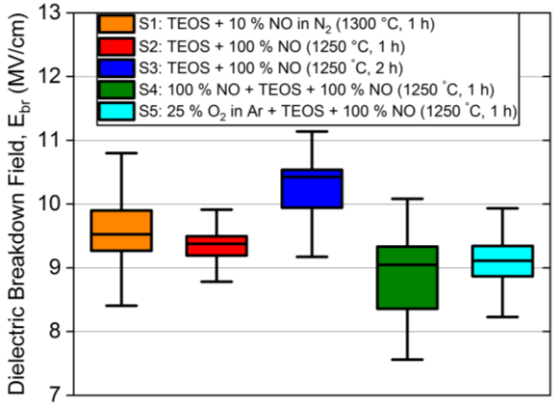
Gate Oxide Reliability and Interface State Density

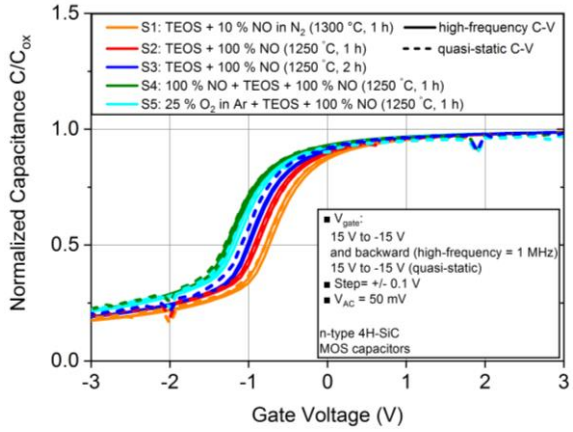
Minwho Lim et al., ICSCRM 2019

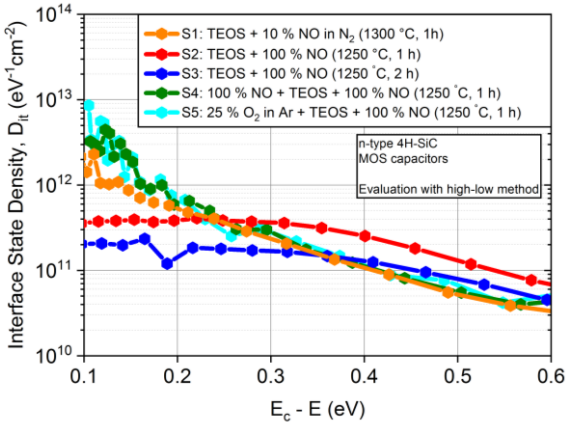
TEOS as precursor

- Planar MOS capacitors
- TEOS gate oxide suited for Trench Gate devices
  - Conformal trench oxide with high gate oxide integrity
- Post-deposition-annealing in NO in different ambient
- Pre-deposition oxidation in NO or O_2 deleterious for dielectric strength and surface quality
- High temperature H_2-etching is favorable for surface conditioning [2]
  - Connected with trench reshaping









Conclusion

- Trench-First process facilitates feasible devices enabling
  - Self-aligned process controlled by oxidation parameters
  - Various customized ion implantation with stable trench formation
  - Room for design improvement depending on foundry (narrow cell, deeper trench etc.)
- Process integration
  - TCAD modeling matching actual design could verify the further advanced edge termination for high voltage devices
  - Gate oxide can be further optimized based on deposited homogene oxide type

Thank you for your attention!

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