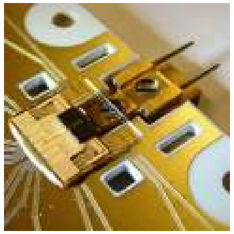
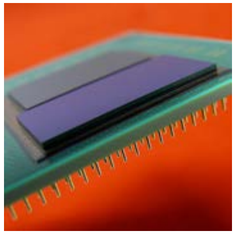
Forschung für die Elektroniksysteme von morgen

R. Aschenbrenner









Outline

Trends in Advanced Packaging

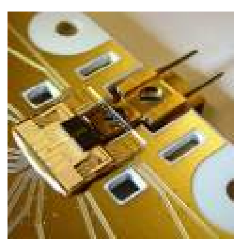
Was ist Panel Level Packaging

Embedding für Fan Out

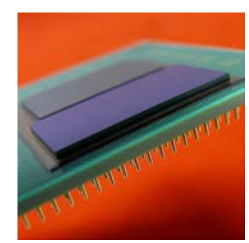
Embedding für LP

Beispiele

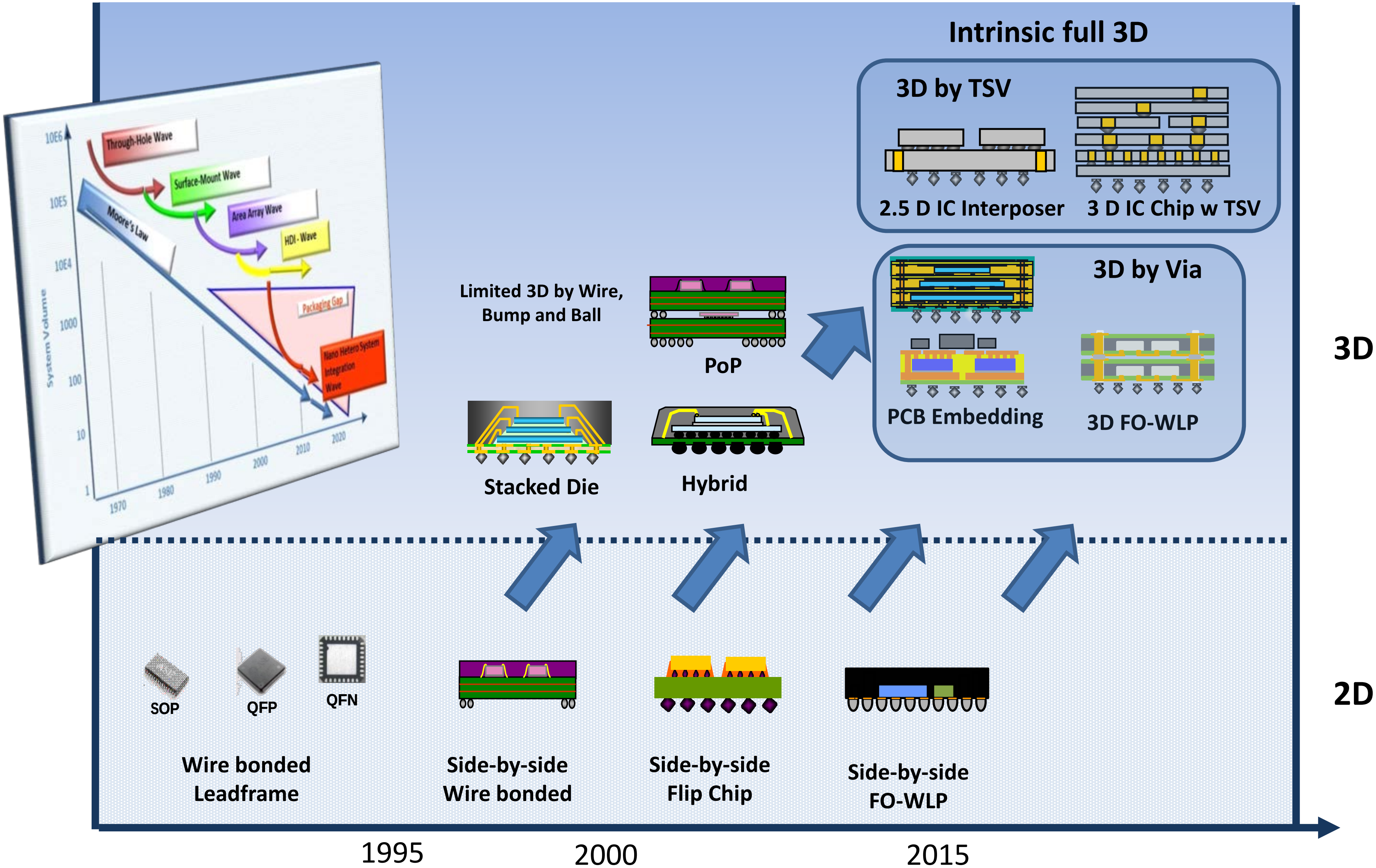








Trend on ICs and Packages 2D -> 3D

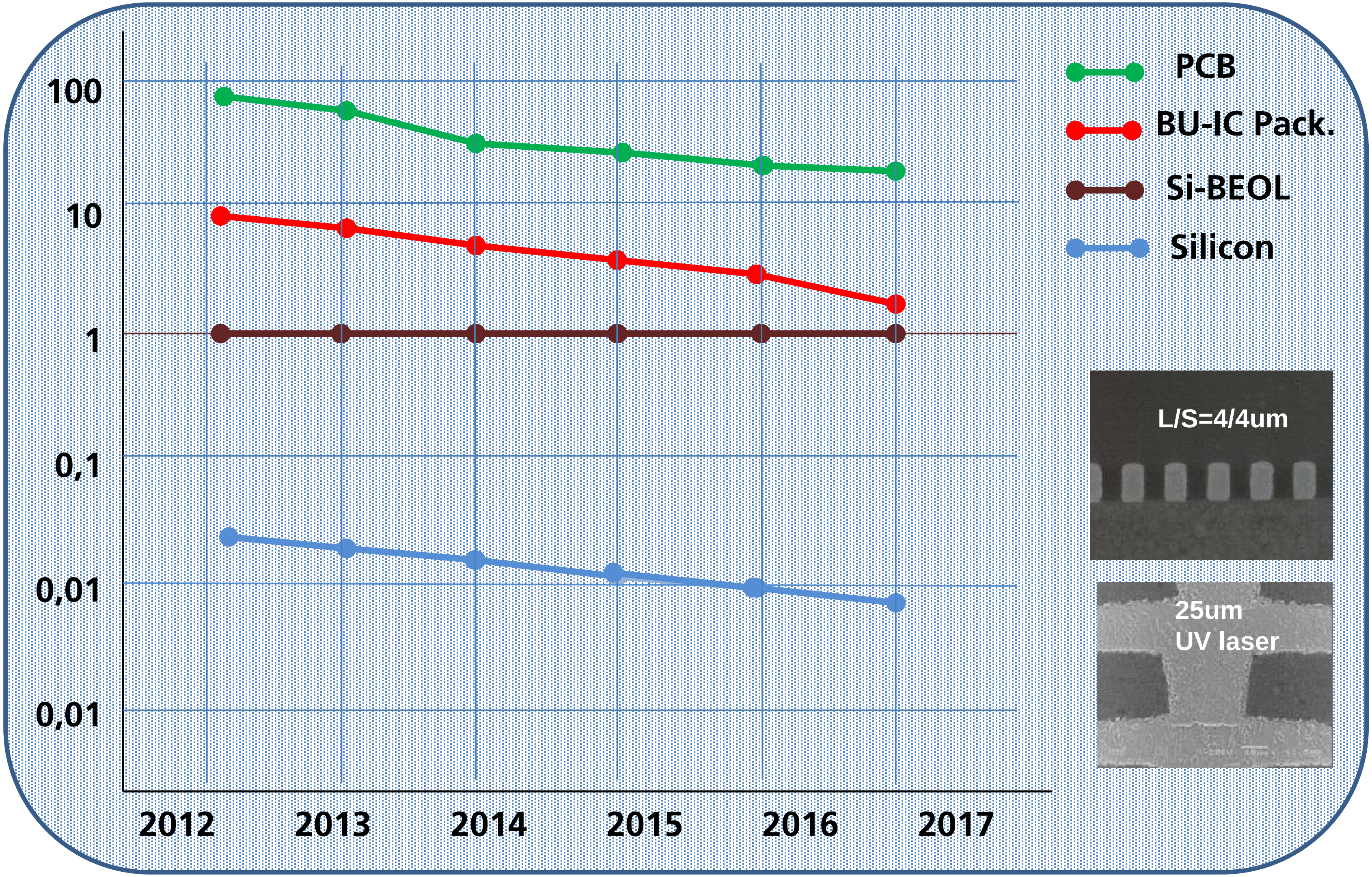


Rolf Aschenbrenner

Source: ASE and IZM

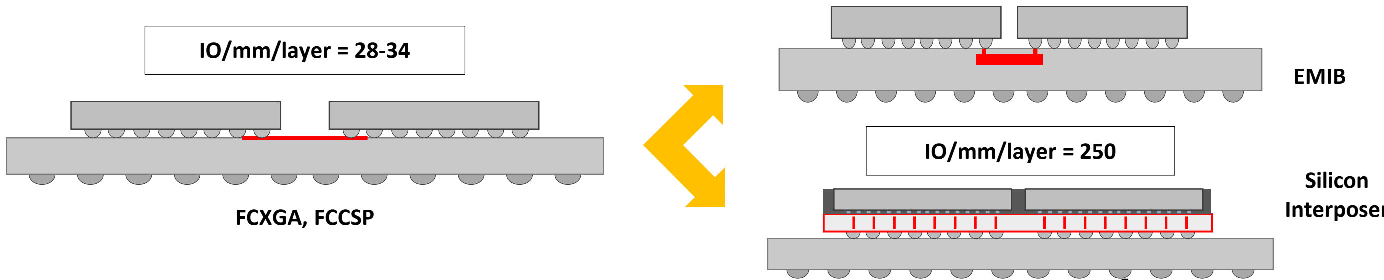
Fraunhofer IZM

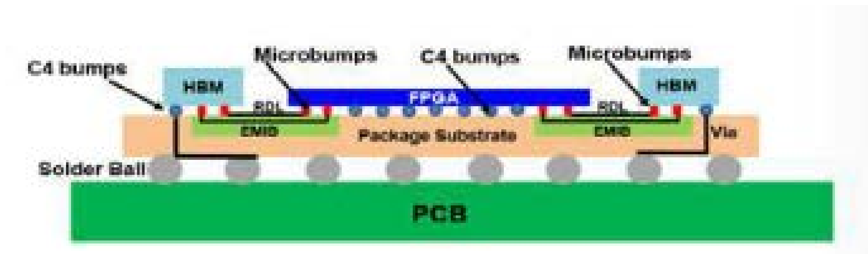
Interconnect Resolution Trend

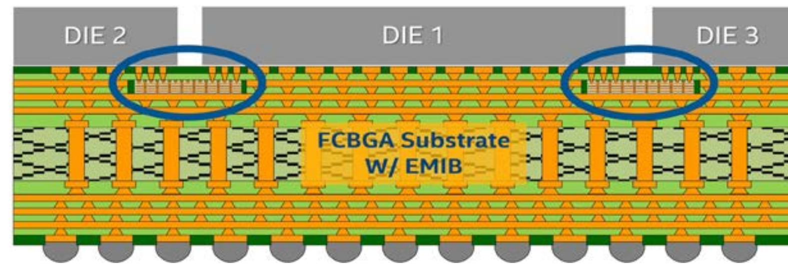


- Organic interconnect density is rapidly approaching Si-BEOL

Intel’s Silicon Bridge



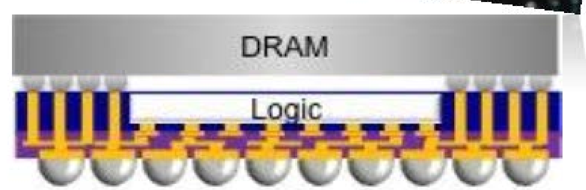




- **Embedded Multi-die Interconnect Bridge (EMIB) available to Intel’s 14nm foundry customers**
- **A small silicon bridge chip is embedded into the package (no TSVs)**
- **Micro bumps on chips and communication between chips through interposers**
- **Package substrate is provided by substrate supplier (no info on substrate price)**
- Considered less expensive because only small area for high-density silicon and no TSVs

Source: Intel.

IPHONE 7 ADOPTS FAN-OUT WAFER LEVEL PACKAGING INSTEAD OF PCB



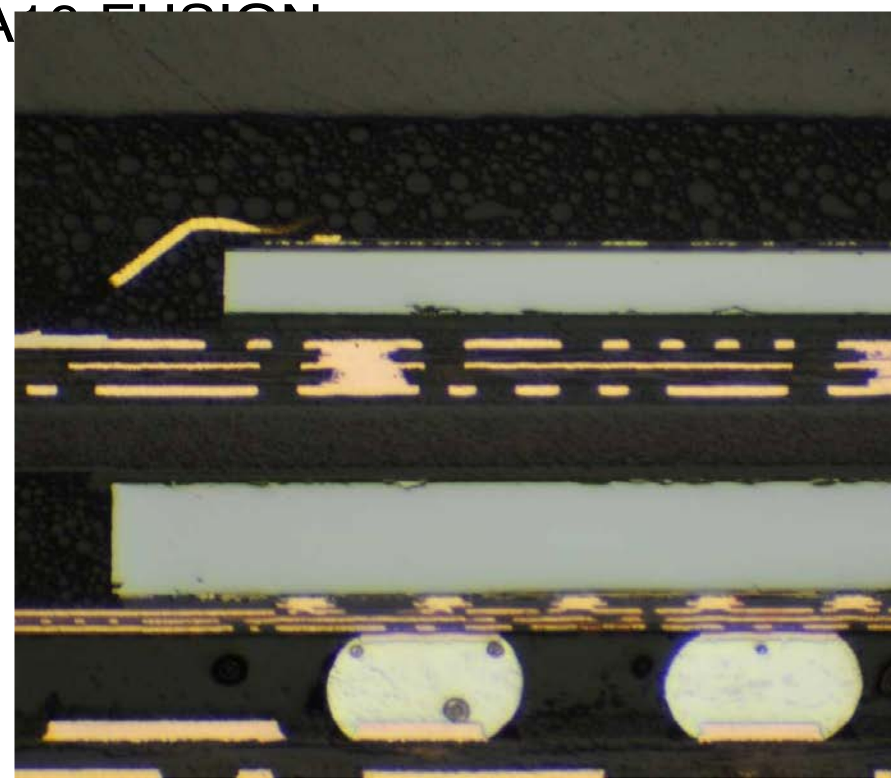
Deshalb ist InFO-WLP so wichtig
Die Technologie zur Chip-Anbringung, die TSMC nutzt, wird InFO-WLP genannt (eigentlich „Integrated Fan-Out Wafer-Level Packing". Sie unterscheidet sich von der herkömmlichen Methode, bei der CPU oder SoC via Lötperlen auf PCB angebracht werden.

iPhone 7 Processor – Memory Integration

Source: Prismark Partners

916.6/193bp

APPLE A



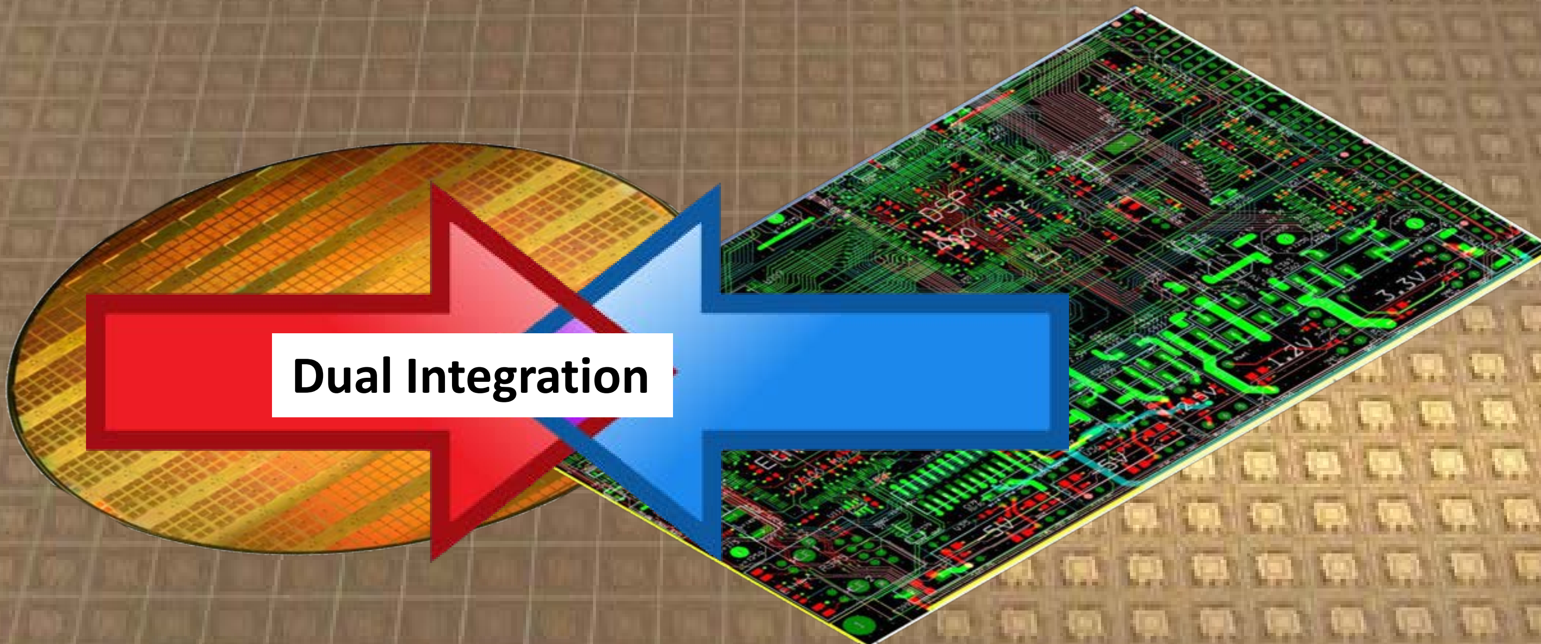
- 14.4 x 15.5mm InFO PoP Package
  - ~1300 balls at 0.4mm pitch
  - 825µm package height
- Memory package with 5 die (4 shown)
  - Die Thickness:105µm
  - 170µm EMC thickness over die
  - 3L substrate; 100µm thick
  - 386 balls at 0.3mm pitch
  - Underfill between packages
- Processor : 11.6 x ~10.8mm
  - 165µm thick; 12µm "top coat"
  - 50µm thick 3 Layer RDL

Photos source: Prismark/Binghamton University

FAN-OUT ACTIVITY MARKET FORECAST WITH APPLE ENTRY

Scenario 2: Apple example will show the way to competitors

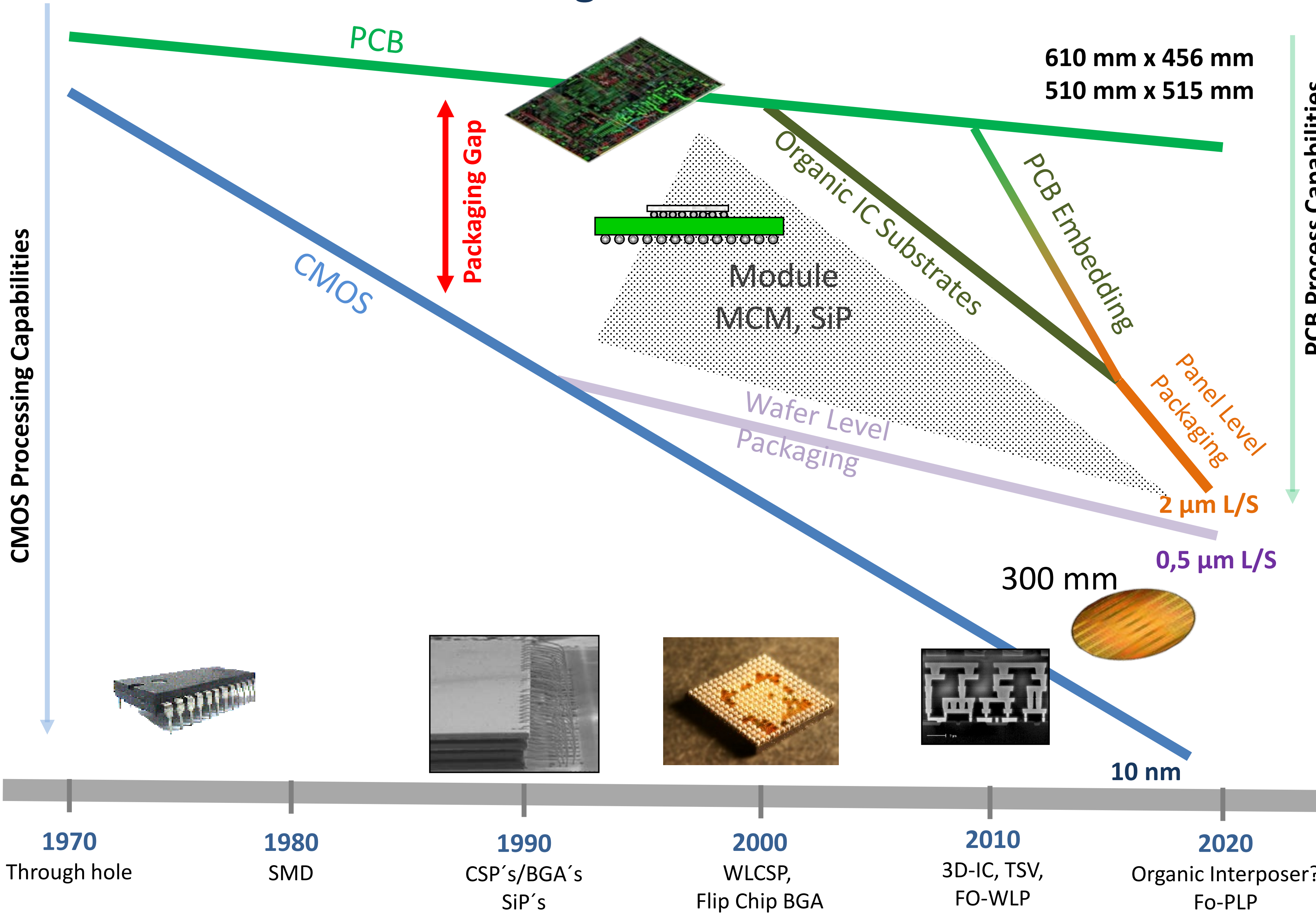
Panel Level is: The intelligent combination of Wafer Level Processing, FO WLP and PCB Embedding



"Fusion"
of semi WLP / LCD / PCB / Solar / flexible electronic infrastructures

- Finer lines and spaces in combination with semiconductor equipment and organic substrates
- Embedding of bare dies into organic substrates
- Glass, PCB, Filled Epoxy

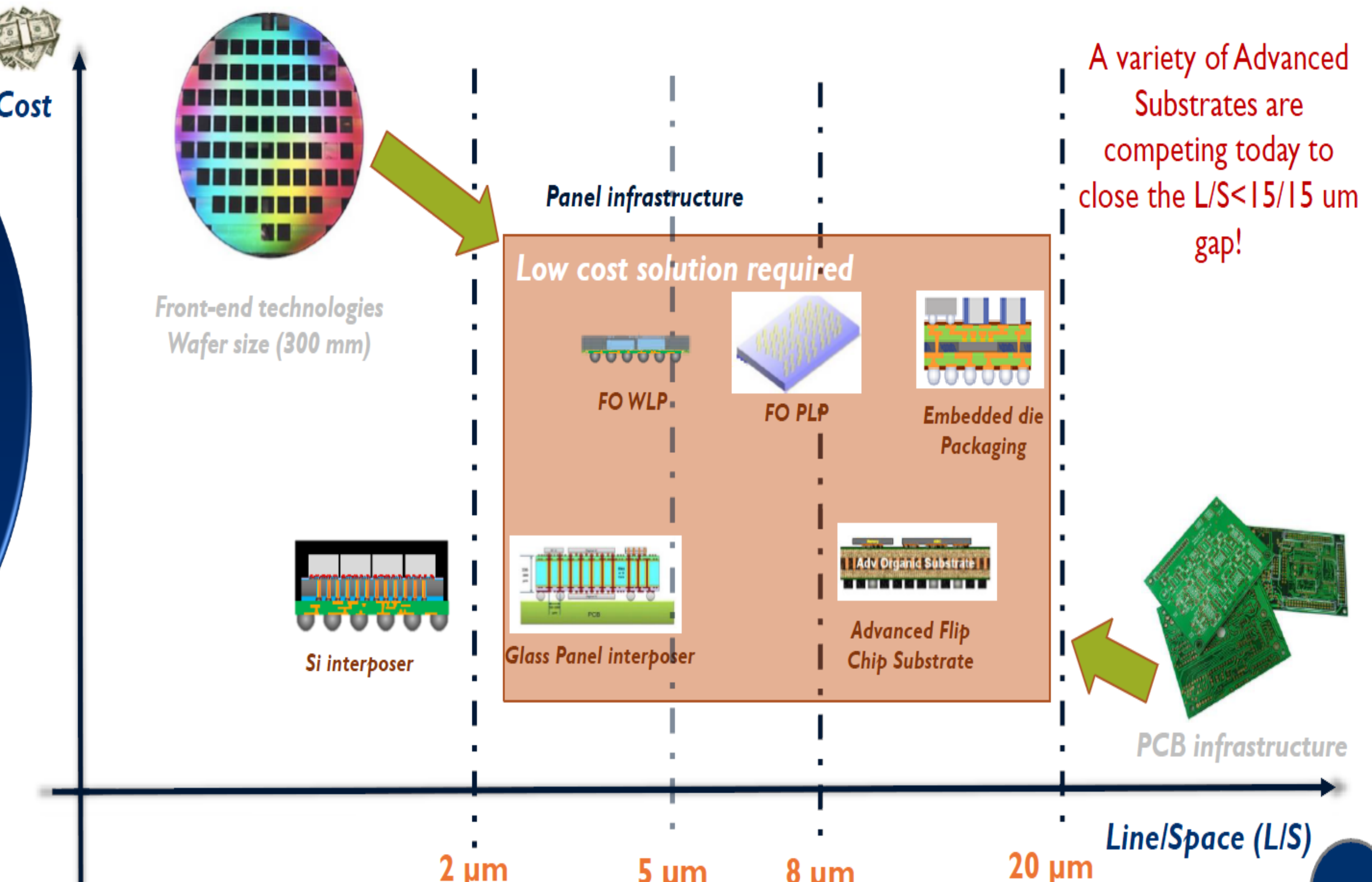
Zusammenfassung: Interconnect Resolution Trend



TECHNICAL GAPS BETWEEN THE WAFER AND PCB INFRASTRUCTURES

Filled by the panel infrastructure

Between the front-end and PCB areas, a gap exists in terms of cost structure, technical features and infrastructures



Merging of Wafer Level and PCB Technologies

Fan-Out WLP and Embedded Die Technologies

Mainstream - black
Exceptions - red
Examples - blue

Embedded Packaging Technologies

Die Embedding in Organic Laminate *"Embedded Die"*

Fan-In Type

Chip-First

- NA

Fan-Out Type

Chip-First

- **ECP** (ATS)
- **SESUB** (TDK)
- **I²Board** (Schweizer)
- **I²Pack**, **µ²Pack** (Schweizer)
- **WFOP** (J-Devices)
- **BLADE** (Infineon)
- **BossB2it**, **B2itPWB** (Dai Nippon)
- **ChipsetT/ChipletT** (FlipChip/ TSHT, Fujikura)
- **aEASI** (ASE)
- **EOMIN** (Taiyo Yuden)
- **Clover embedded device** (Unimicron)
- **MCeP** (Shinko)
- **EMIB/Si-Bridge** (Intel)
- **EWLP** (Imbera)

Chip-Last

- **EMAP** (GTPRC)

Die Embedding in Epoxy Moldcompound *"Fan-Out WLP/PLP"*

Fan-In Type

Chip-First

- **WLCSP+** (NANIUM)
- **eWLCSP** (STATS)

Fan-Out Type

Chip-First

- **eWLB**, **aWLP**, **WLFO** (Infineon, JCET STATS ChipPAC, ASE, NANIUM)
- **RCP** (Freescale/NXP, Nepes)
- **M-Series** (DECA)
- **InFO** (TSMC)
- **WLFO** (Amkor)
- ADL/SinoChip
- **FOWLP** (SPIL)
- **NTI** (SPIL)
- **WFP** (Samsung)

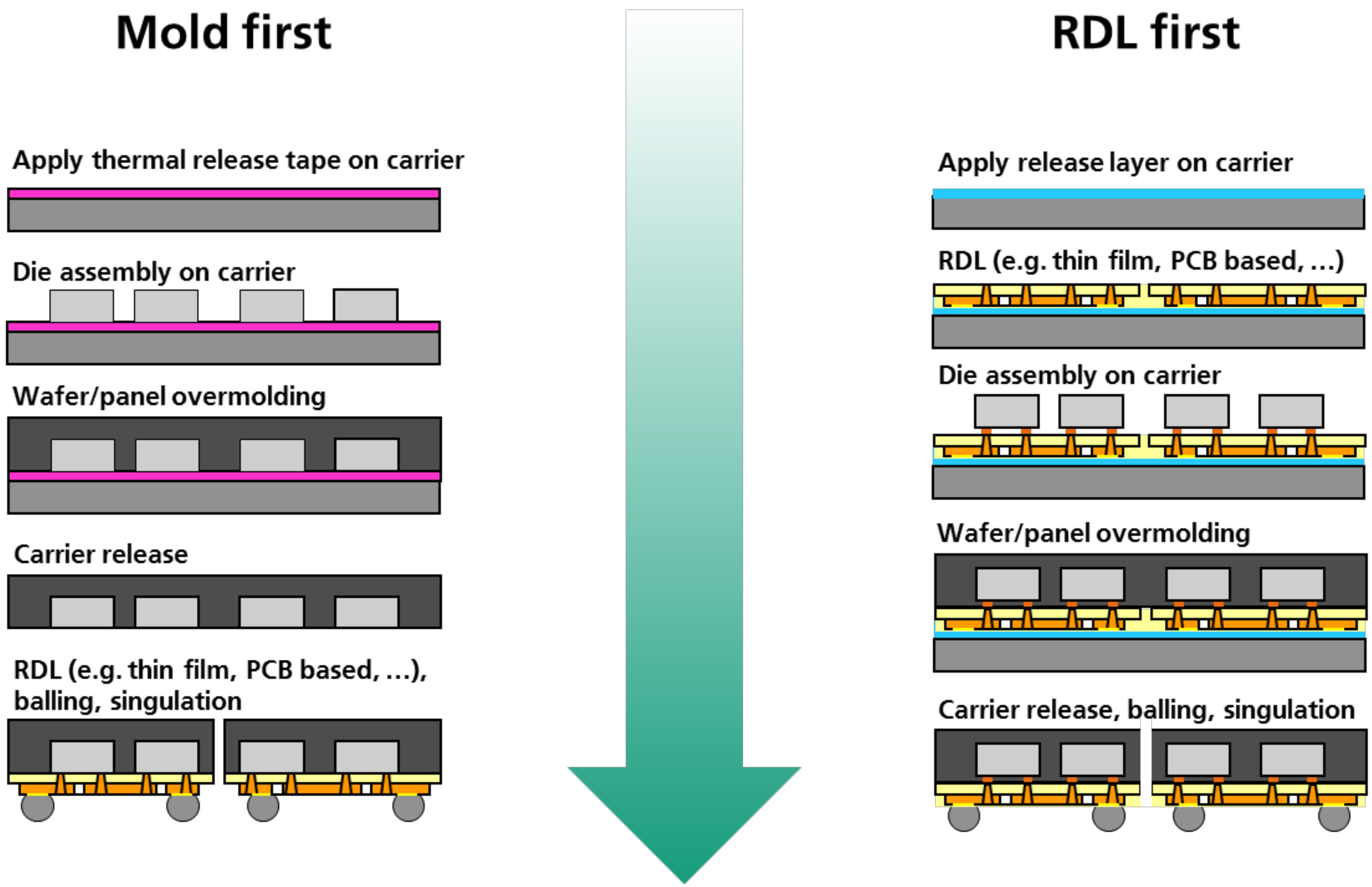
Chip-Last

Solutions that can be categorized as Advanced Flip Chip technologies:

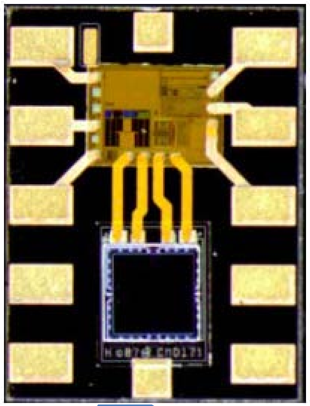
- **FOCLP** (ASE)
- **SWIFT** (Amkor)
- **SLIM** (Amkor)
- **RDL-First FOWLP** (IME)
- **HDL** (QPL)
- **FC-MISBGA** (SPIL)
- **EMIB/Si-Bridge** (Intel)

Source: Steffen Kroehnert, NANIUM

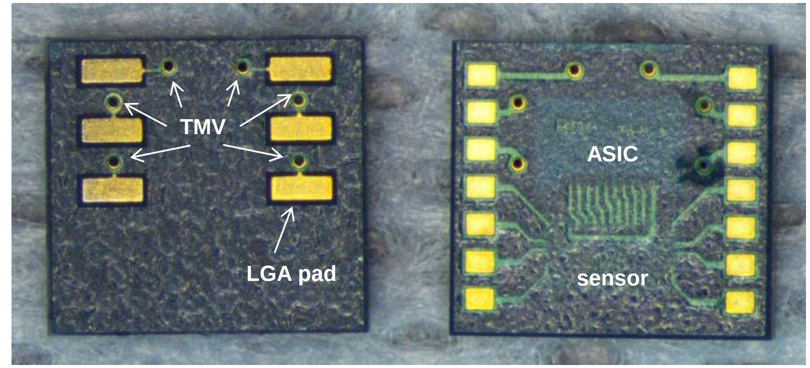
FOWLP/FOPLP Process Flow Steps



Example: FO-Packaging of a Multi-Sensor System

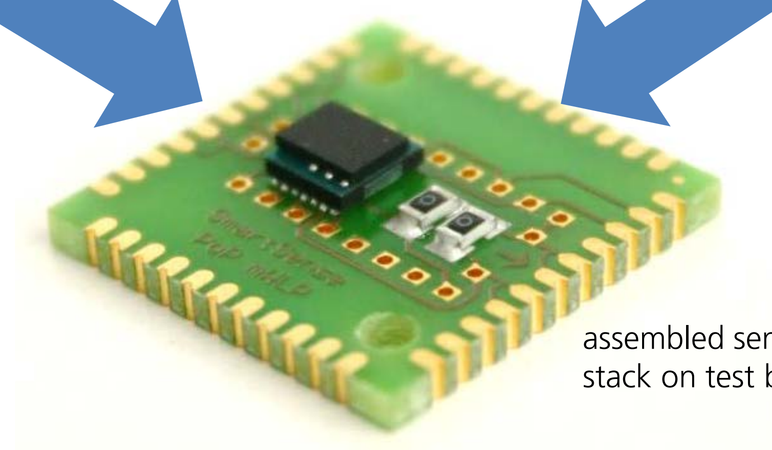


pressure sensor/ASIC package with thin film RDL



Acceleration sensor/ASIC package with PCB based RDL
and Through Mold Vias (TMV) for package stacking

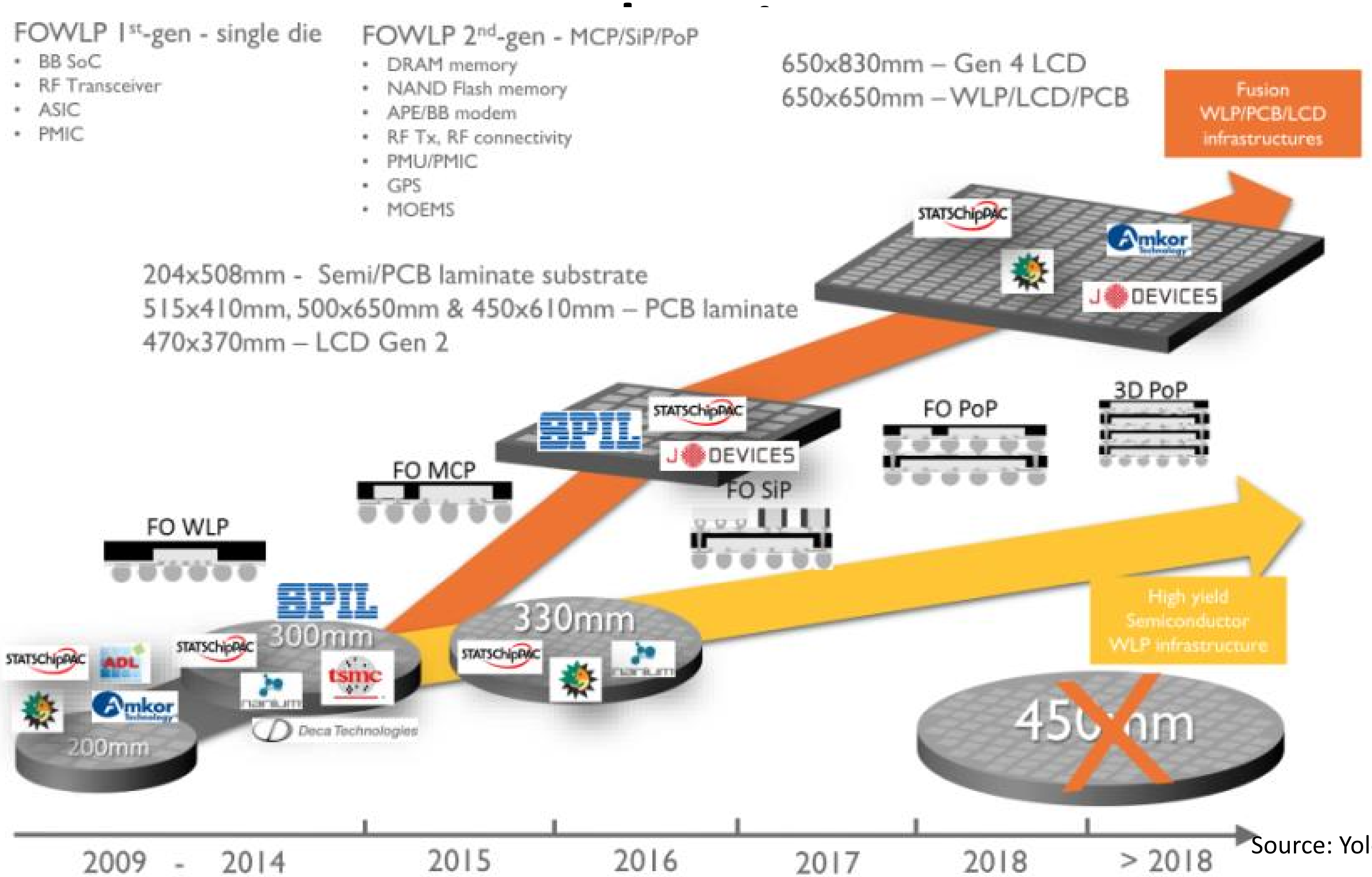
BOSCH



assembled sensor
stack on test board

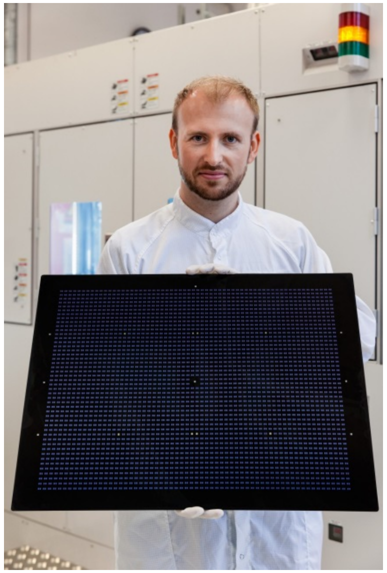
- **Functional tests show sensor performance in specs**

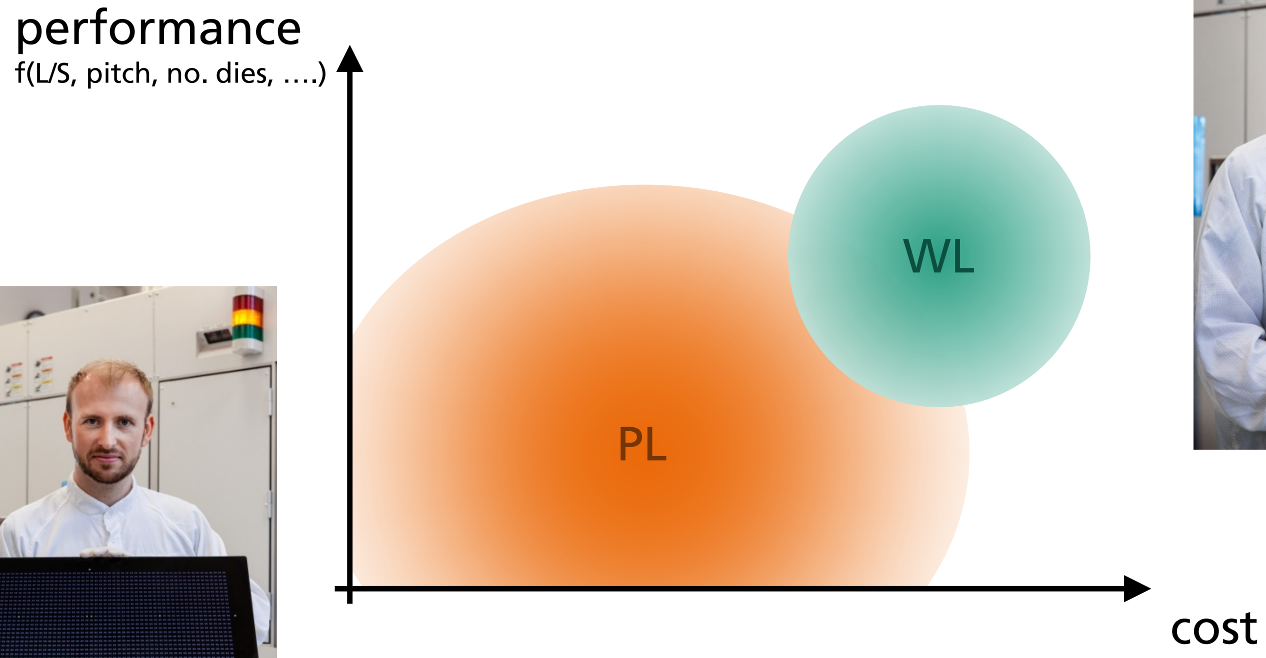
Roadmap Fan-Out Panel Level



Source: Yole

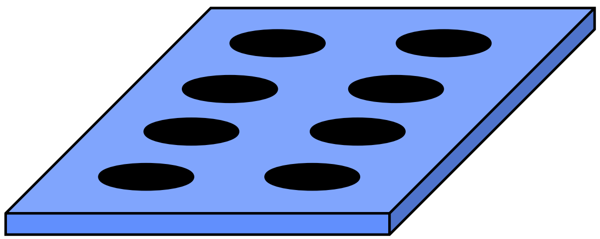
PLPC – Current Status





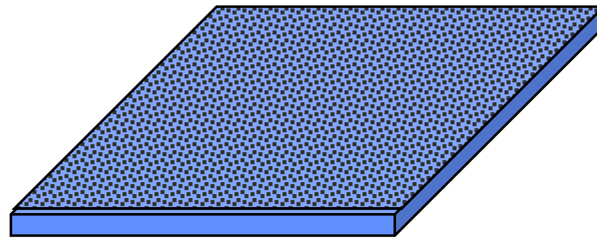
Molding Compounds for Large Area Encapsulation

Liquid Compression Molding Compounds



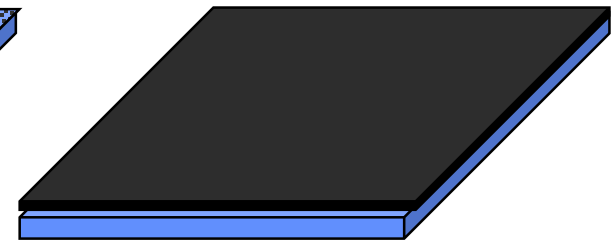
- Standard material for wafer level embedding
- **Paste-like material** is dispensed in the cavity and flows during tool closing and compression of the tooling
- *Limited potential for large area due to complex dispense patterns needed and longer flow length***?**
- **€€**

Granular Compression Molding Compounds



- Standard material for MAP compression molding
- **Granular materia**l is distributed nearly homogeneously all over the cavity and melts and the droplets have to fuse during closing and compression of the tooling
- **No limitations for large area application**
- **€**

Sheet Lamination Molding Compounds

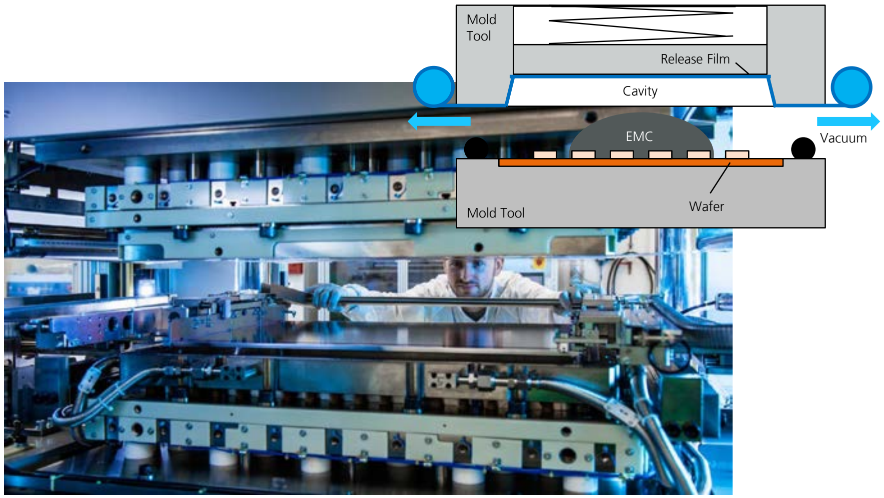


- Standard material for wafer level embedding
- **Material sheets** are melting and only flow around dies for encapsulation
- Sheets in defined thicknesses/volume
- **No limitations for large area application**
- **€€€**

Fraunhofer IZM

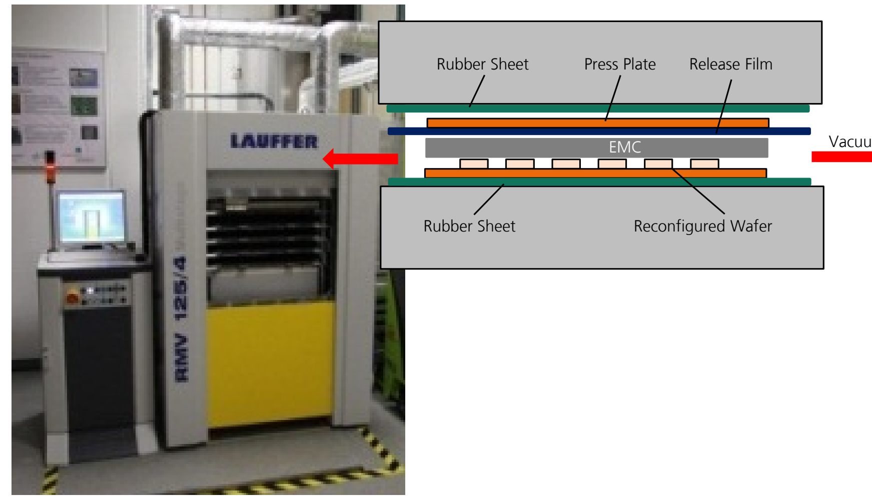
Panel Mold Embedding Technologies

Compression Molding



- Standard process for MAP molding and WL mold embedding
- Use of liquid or granular compounds
- Tooling adapted to wafer size needed
- Thickness control by material weight
- Molding at constant temperature
- Typically an electro-mechanical press
- Current max. mold area: O/☐ 300 mm

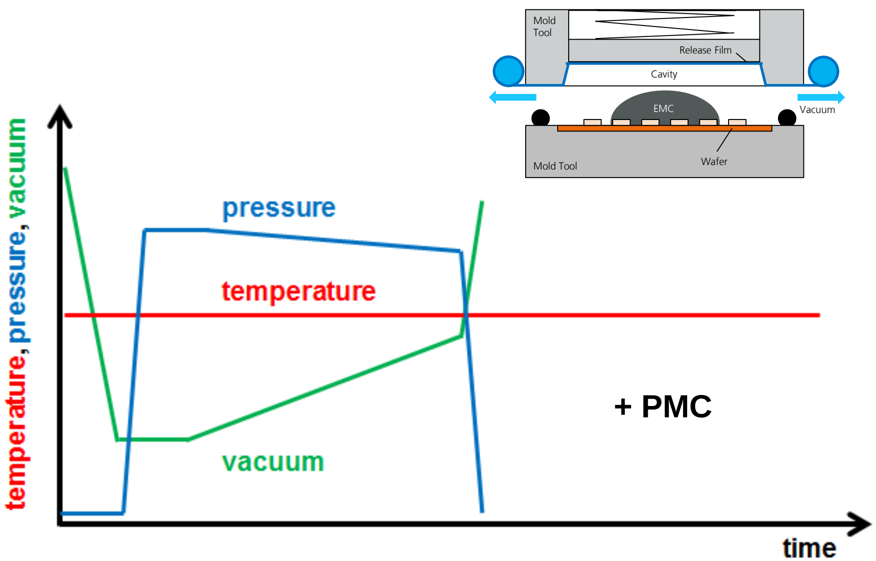
Lamination



- Standard process in PCB manufacturing
- Use of sheets is standard, use of granular or liquid compounds is feasible
- No expensive tooling needed
- Thickness control needed
- Lamination with temperature profile (heating/cooling)
- Typically a hydraulic press
- Current max. sheet size: 610x457 mm²

Compression Mold vs. Lamination - Press Profile

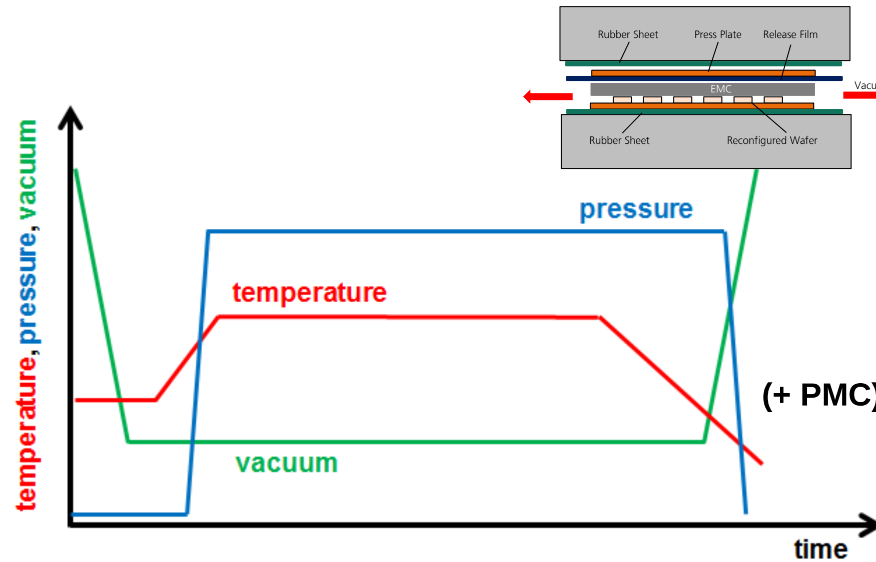
Compression Molding



2 – 15 min

- Short cycle time
- Constant temperature -> no heating or cooling ramps
- No full compression pressure over longer time
- PMC and mold release extra process steps

Lamination



30 – 60 min

- Long cycle time, but multi-stack lamination is standard
- Heating or cooling ramps
- Full compression pressure over longer time
- PMC and mold release can be included

Panel Packaging Process Step Tasks To Solve

Equipment

- Tape laminator
  - ➢ Available automatic equipment?
- Pick and Place
  - ➢ Accuracy on panel size?
- Material application
  - ➢ Dispensing, sprinkle, …
- Molding
  - ➢ Uniformity, thickness control, …
- Debonder
  - ➢ Available automatic equipment?
- Lithography
  - ➢ Stepper, laser ablation, LDI
- Sputtering, plating
  - ➢ Thickness variation, lines & spaces
- Thinning & Dicing
  - ➢ Available automatic equipment?

carrier preparation → **assembly** → **compression molding** → **debonding** → **redistri-bution** → **handling, thinning & singulation**

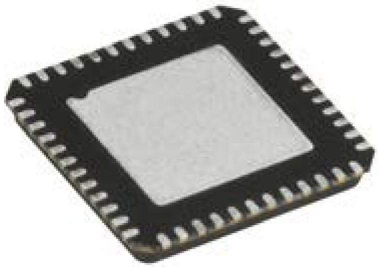
Material

- Carrier
  - ➢ steel, glass,..?
- Thermo release tape
  - ➢ Alternatives?
- EMC
  - ➢ liquid, granular, sheet?
- Dielectric polymers
  - ➢ liquid or film?
  - ➢ photosensitive or not?
- Sputter targets
- Plating
- Handling carrier
  - ➢ Tape or other material
  - ➢ Temporary adhesives

➢ **Still a lot of open issues and questions**

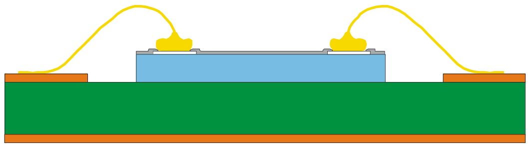
Rolf Aschenbrenner

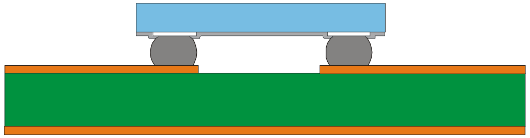
Embedding Technology - First Level Interconnection

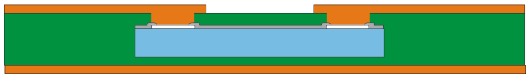


First level chip interconnection technologies inside a package:

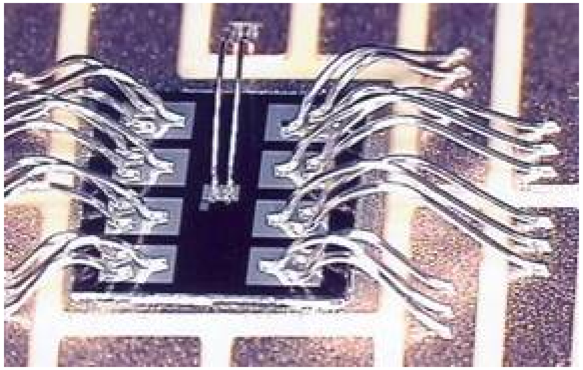
chip & wire | **flip chip** | **chip embedding**

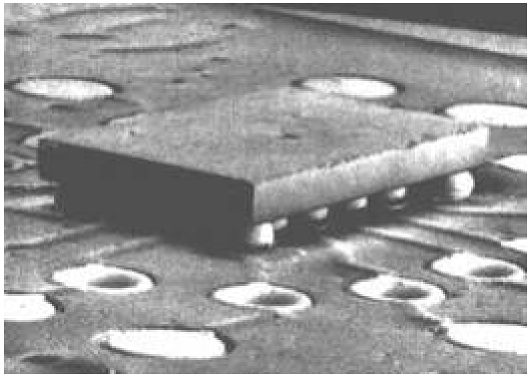


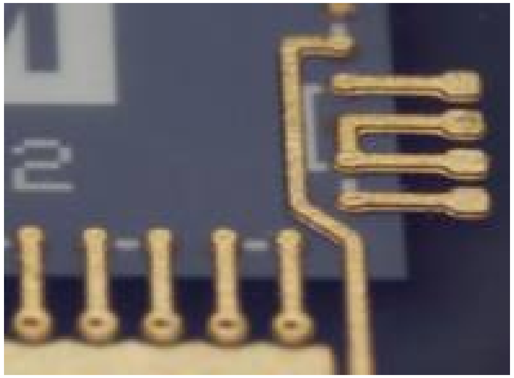




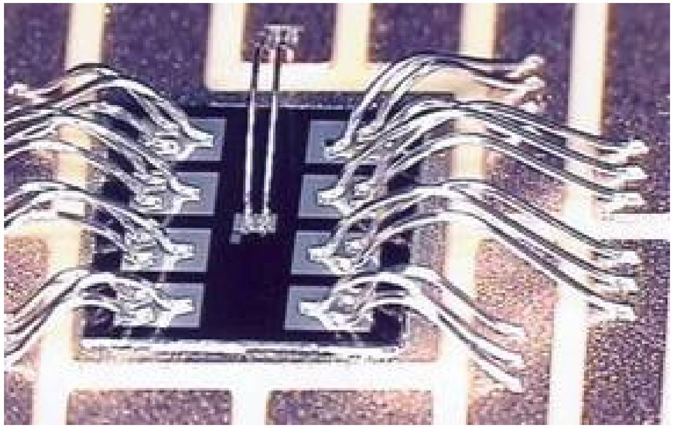
established → **smallest in 2D** → **smallest in 3D**



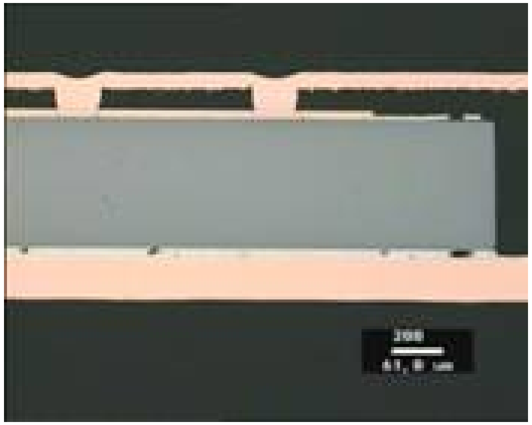


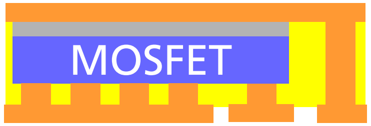


Power Electronics Packaging



wire-bonded power chips on DCB





planar packages & module with embedded power chips

Traditional Power modules

Planar Power Packaging

embedded MOSFET

single module manufacturing

large panel manufacturing

- ➔ low inductance
- ➔ high heat transfer
- ➔ high integration level
- ➔ high productivity

Power Embedding - Principle Features

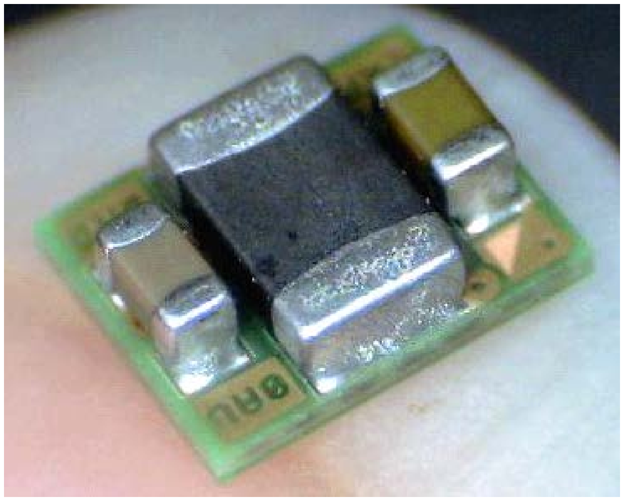
- Completely planar conductors
  - multiple wiring layers possible
  - **SMD assembly on top** allows driver integration
  - top side cooling possible
  - **very low parasitic effects**
- Direct connection by Cu conductors / no bond wires
  - high reliability by direct Cu to chip interconnects
  - shielding capability
- Embedding of power chips into Printed Circuit Board structures
  - **cost saving by large area process ➔ Panel Level Packaging**

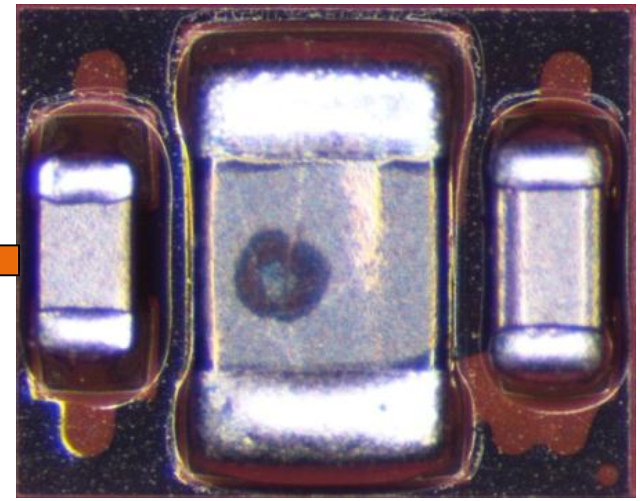
Products– DC/DC Converter SiPs

- ➔ 650 mA DC/DC converter System-in-Package with embedded chip
- ➔ volume manufacturing

Texas Instruments

ROHM SEMICONDUCTOR





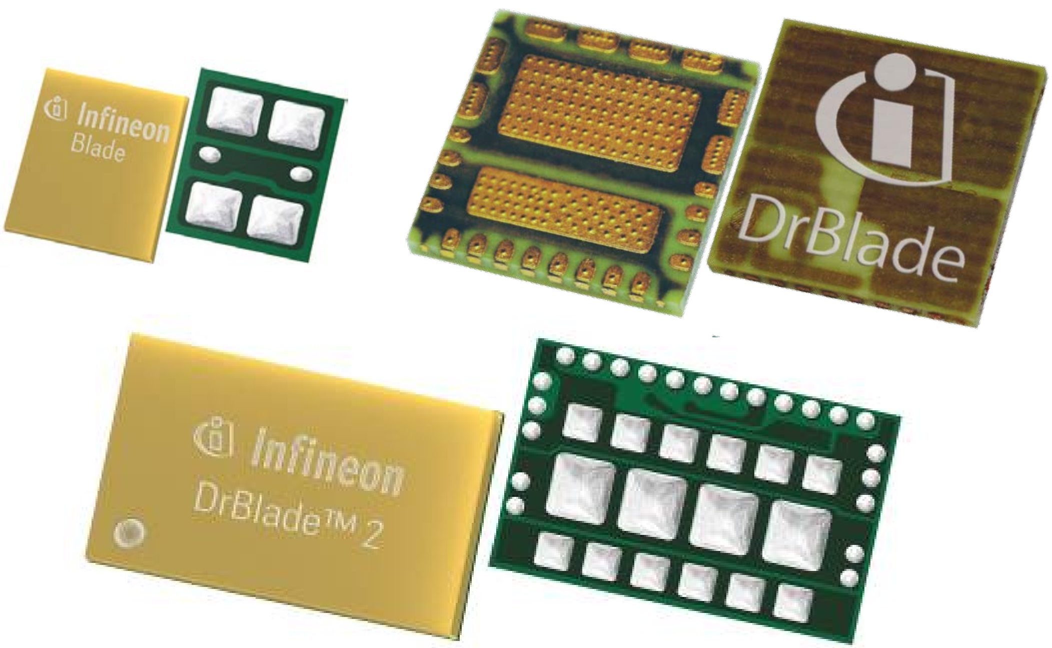
manufactured by AT&S

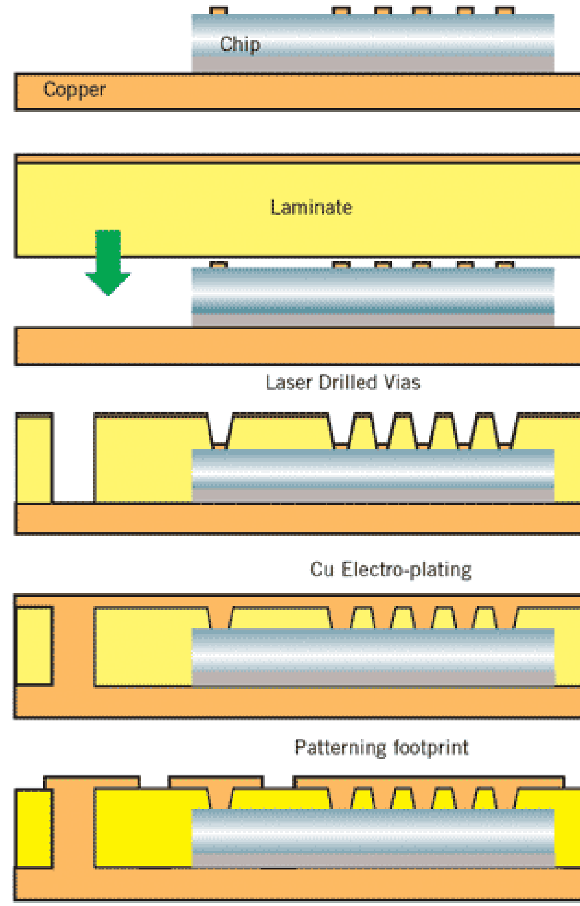
manufactured by TDK

Application – Infineon Blade Technology

SMD power package

- ➔ embedded Si MOSFET / Driver
- ➔ manufacturing on PCB format



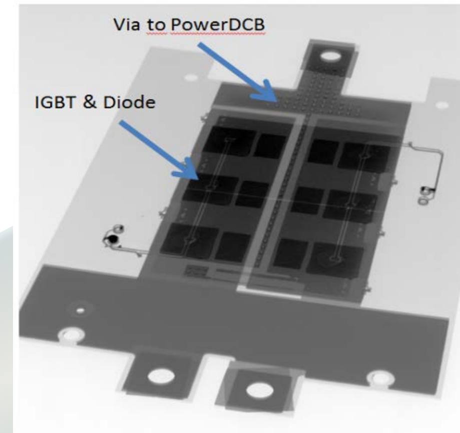


Products – GaN Power Chip Package

courtesy AT&S/GaN Systems

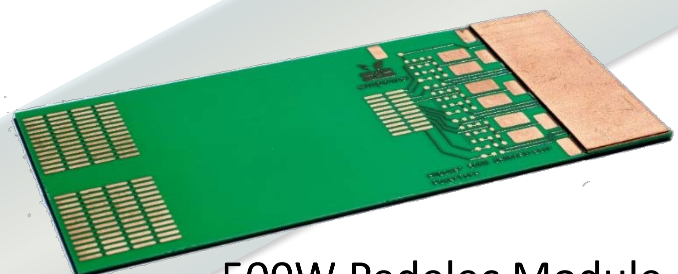
Embedded Die Packages/Modules for different power classes

- Reduction in volume and form factor
- Low inductive interconnect to embedded die
- Improved electrical performance due to optimized switching behavior and reduced switching losses
- Improved reliability, active and passive testing

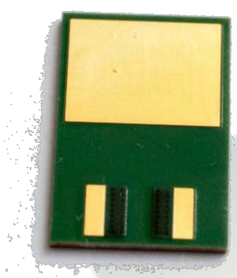


10kW+ Inverter modules

PROJECT HI-LEVEL



500W Pedelec Module



50W Schottky diode package

empower

The European EmPower Project

- Embedded power components for electric vehicle applications
- Started in September 2013, duration 3 years
- Project goals:
  - Industrialize double sided copper plating on wafer level
  - Industrialize next generation automotive power modules
- Benefits:
  - High performance power products with embedded MOSFET, IGBT, GaN, etc.
  - Smallest form factor power supplies
- Partners:

AT&S

ILFA Feinstleitertechnik

ATOTECH

Continental

TU berlin

TU WIEN

ST

http://catrene-empower.ats.net

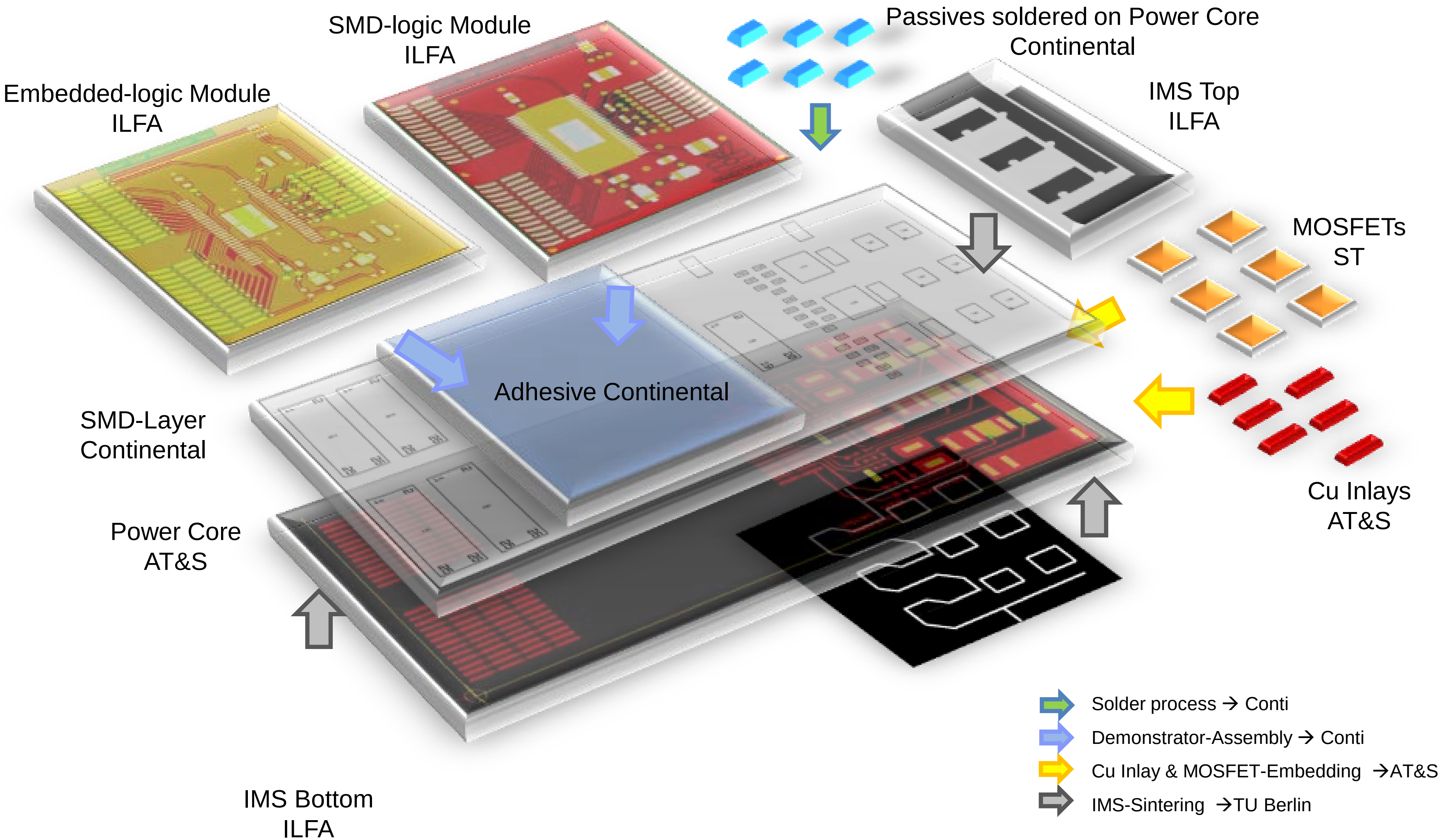
Project EmPower - Demonstrators

Diode Demonstrator
- double diode package
- 2 diodes embedded
- status: demonstrator realized, reliability tests ongoing

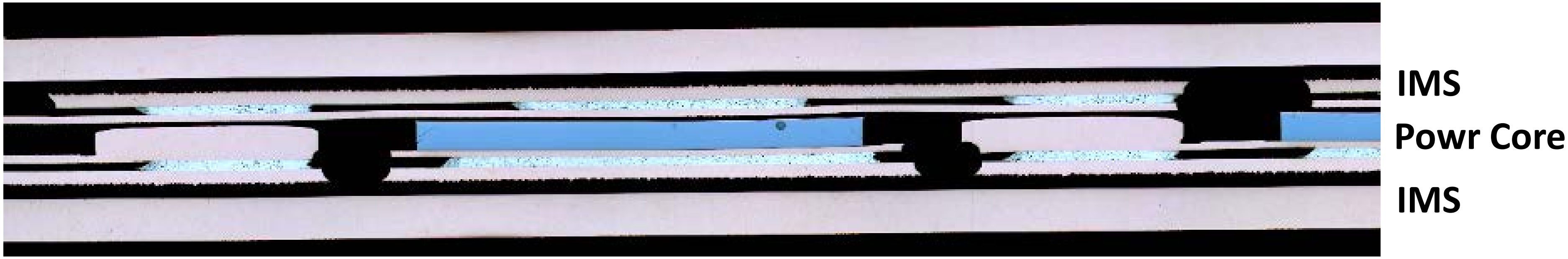
500 W Demonstrator
- pedelec inverter
- 24 V, 20 A
- 6 MOSFETs embedded
- control logic embedded in separate module
- status: demonstrator realized, reliability tests ongoing

50 kW Demonstrator
- automotive inverter
- 600 V, 200 A, 3 phases
- 24 IGBTs, 24 diodes embedded
- status: development ongoing

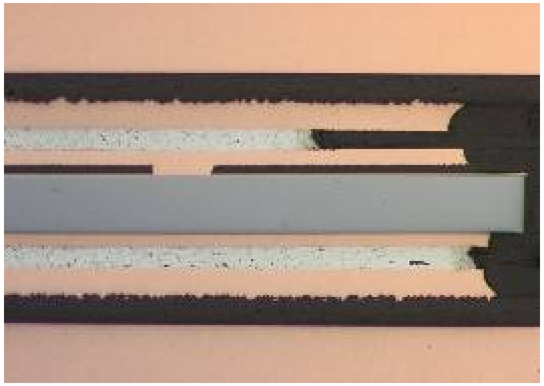
500 W Demonstrator – Concept



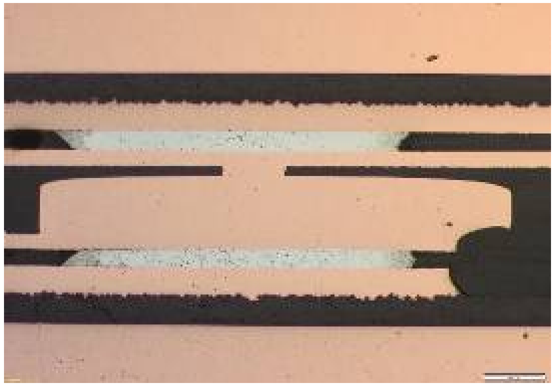
Sinter/Lamination Interconnection – Cross Section



cross section of IMS/power core/IMS sinter interconnects



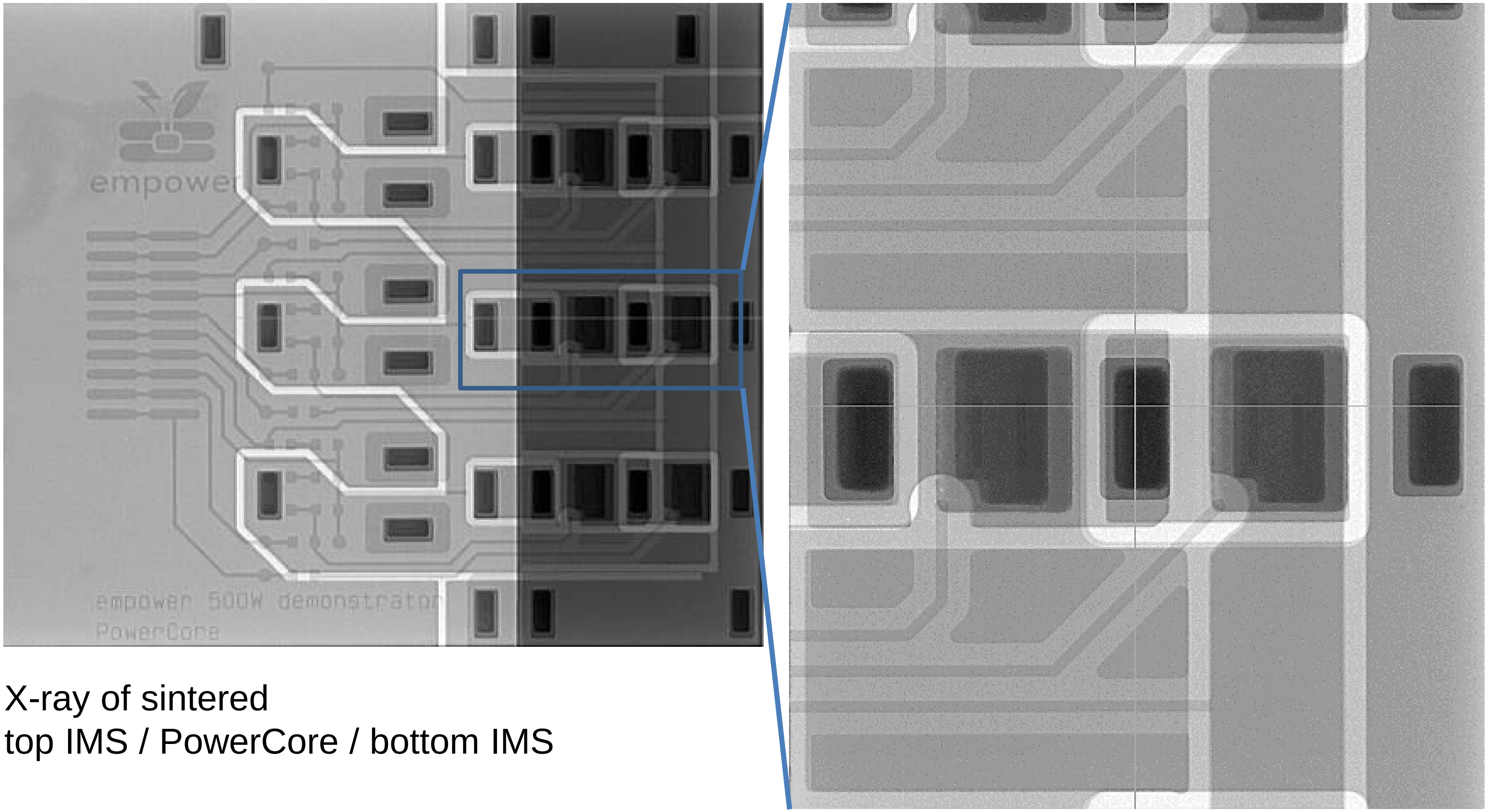
sinter connection die area



sinter connection copper inlay area

➔ no large voids in Ag sinter interconnects

Sinter Interconnects – X-Ray Inspection



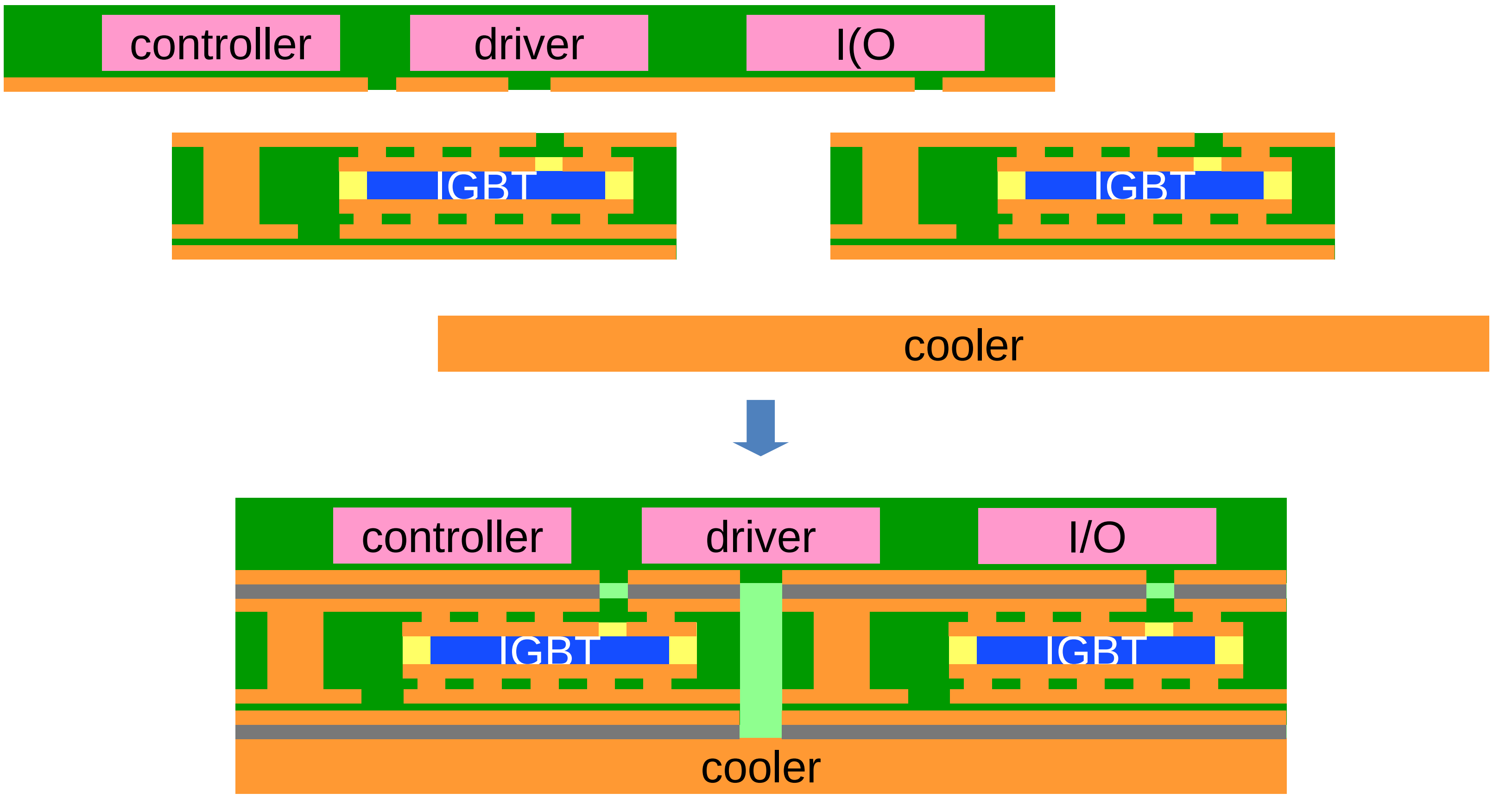
X-ray of sintered
top IMS / PowerCore / bottom IMS

➔ **good alignment (± 50 µm) of all sintered layers**

Concept 3D Stacking

What is a 3D Power Stack?

- Stacking of Functional Layers by combined sinter/lamination technology



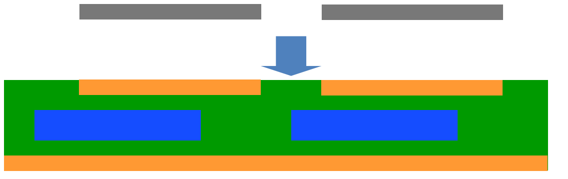
Rolf Aschenbrenner

Concept 3D Stacking

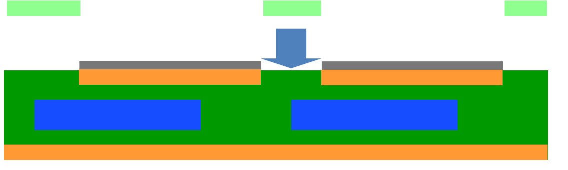
Stacking by combined sinter/lamination ➔ Process Flow

- Stacking of Functional Layers by combined sinter/lamination technology

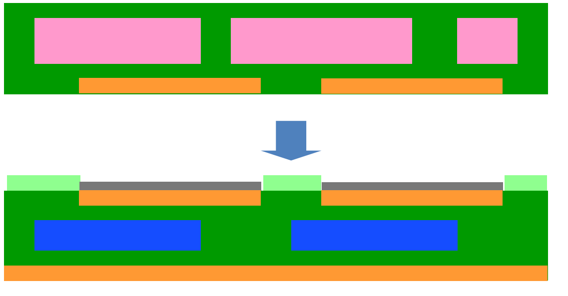
1. stencil printing of Ag sinter paste
   on Functional Layer, paste drying



2. lay-up of prepreg sheet with opening
   for paste locations

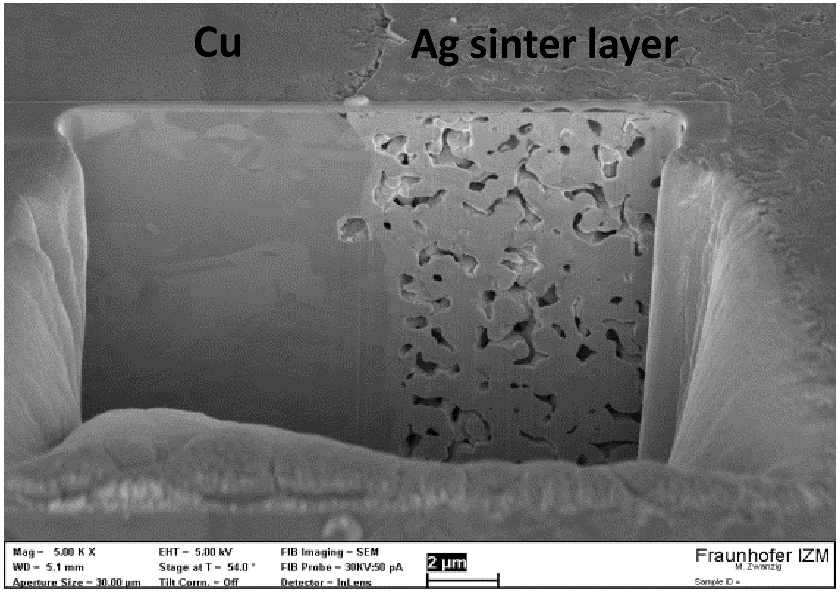


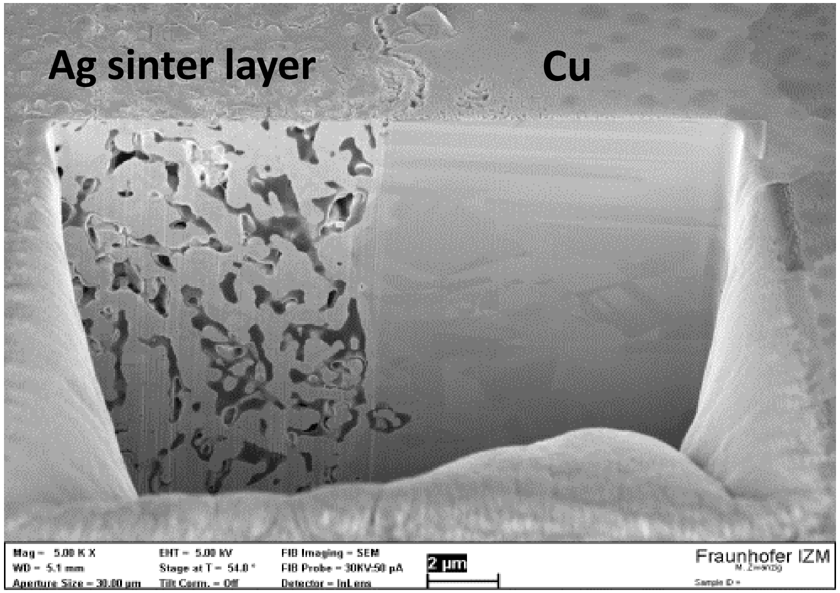
3. lay-up of 2. Functional Layer on top,
   vacuum lamination at 3 MPa,
   10 min./230 °C, 60 min./200 °C



Result: a monolithic stack, thermally and electrically interconnected by
high-reliable Ag joints, all gaps are filled by an isolating dielectric

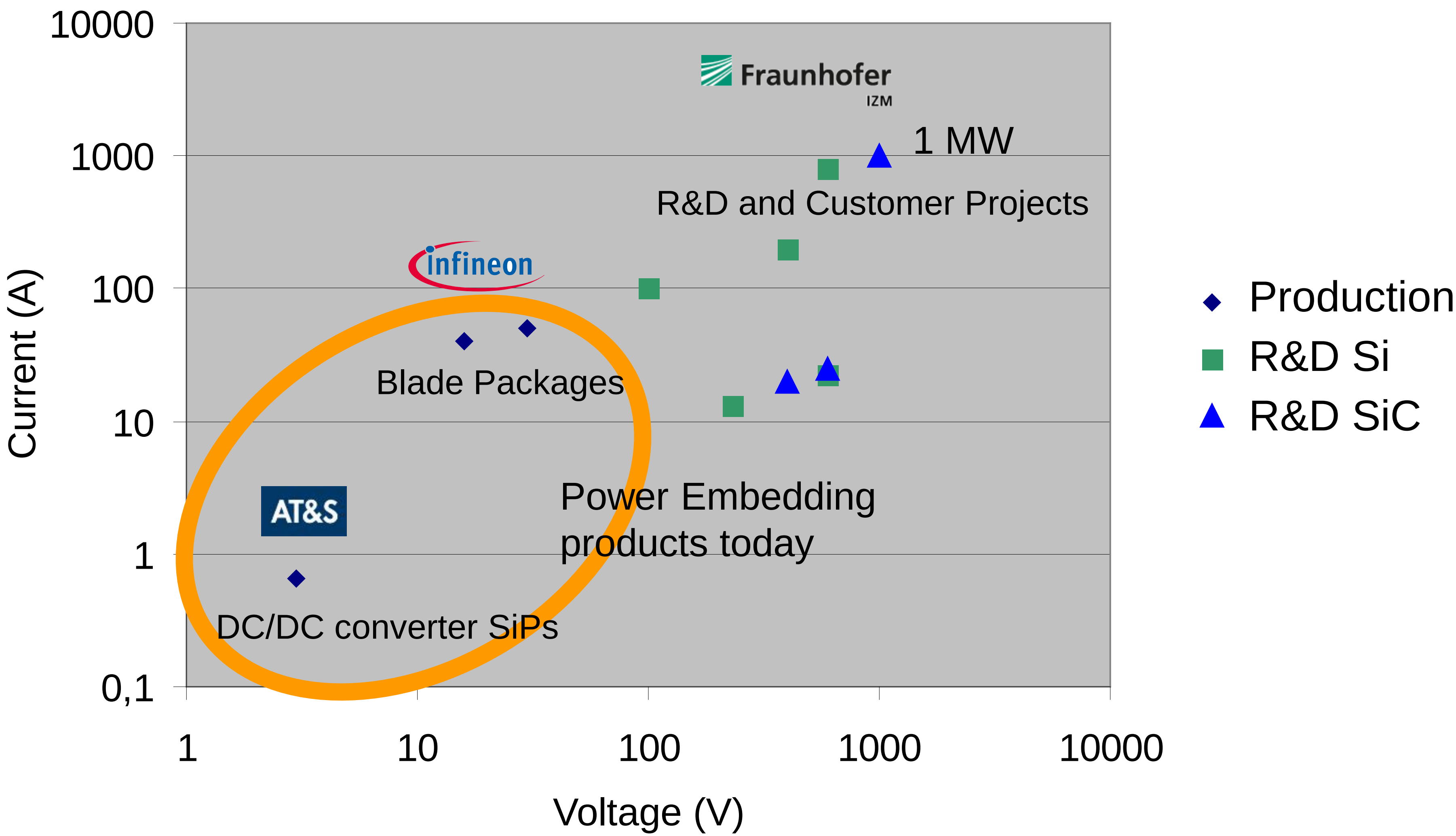
Sinter/Lamination Interconnection– FIB Analysis





➔ **sufficiently low amount of micro voids in sinterde Ag (< 30 %)**

Power Embedding – Production and R&D

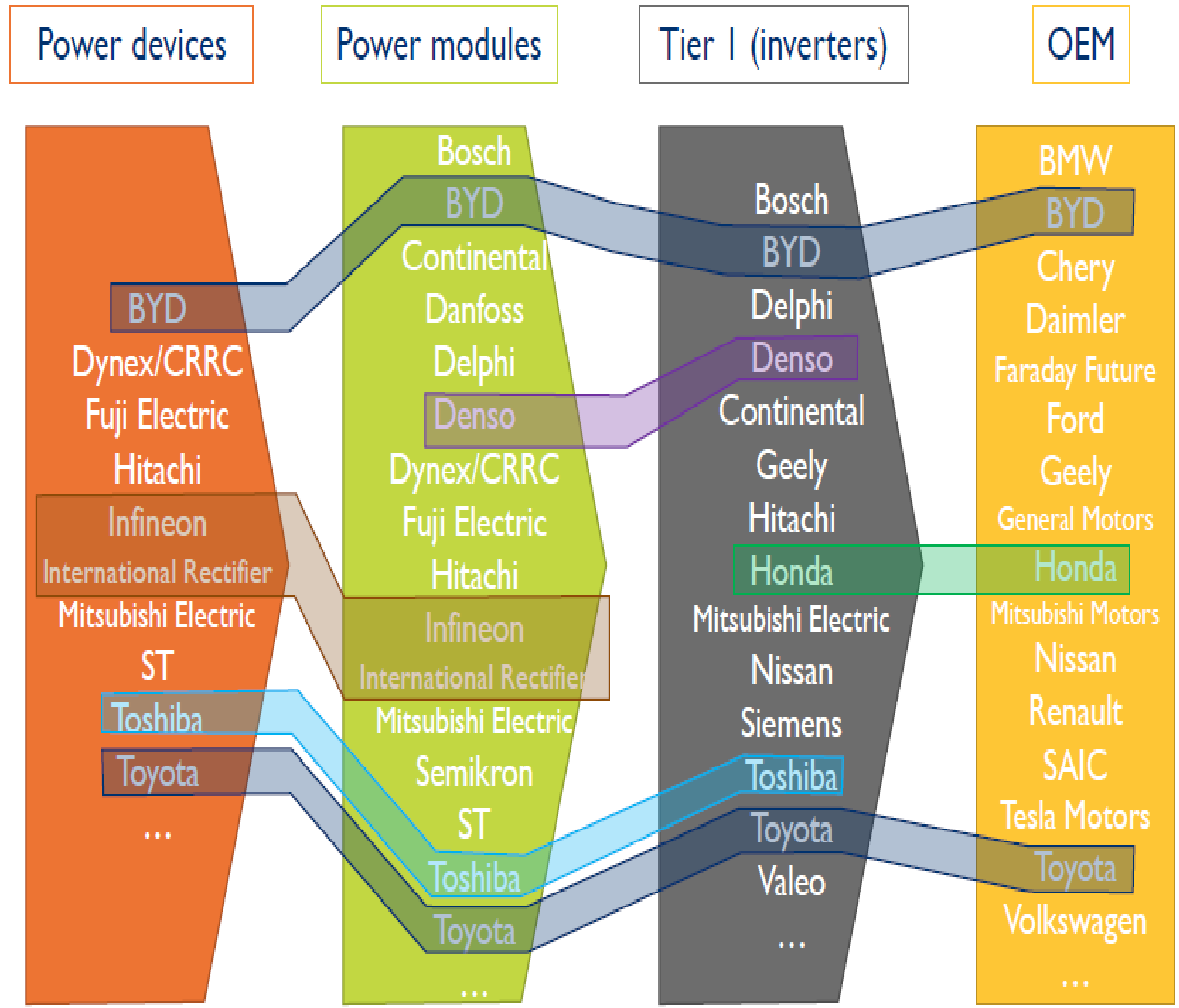


Fraunhofer IZM

Case study: automotive industry supply chain

Many companies are involved in the increasingly attractive market for electrified vehicles

- Electrified vehicles are seen as a very promising market, which is constantly attracting new players. For instance, Siemens is currently a major manufacturer or rail applications for power electronics. They have recently presented an inverter to be used in hybrid vehicles for the first time.
- Continental have proposed a fully integrated power electronics solution with its own power module.
- Apart from car makers, a very few companies are involved only at one level (power module for Danfoss or Semikron, inverter for Siemens).

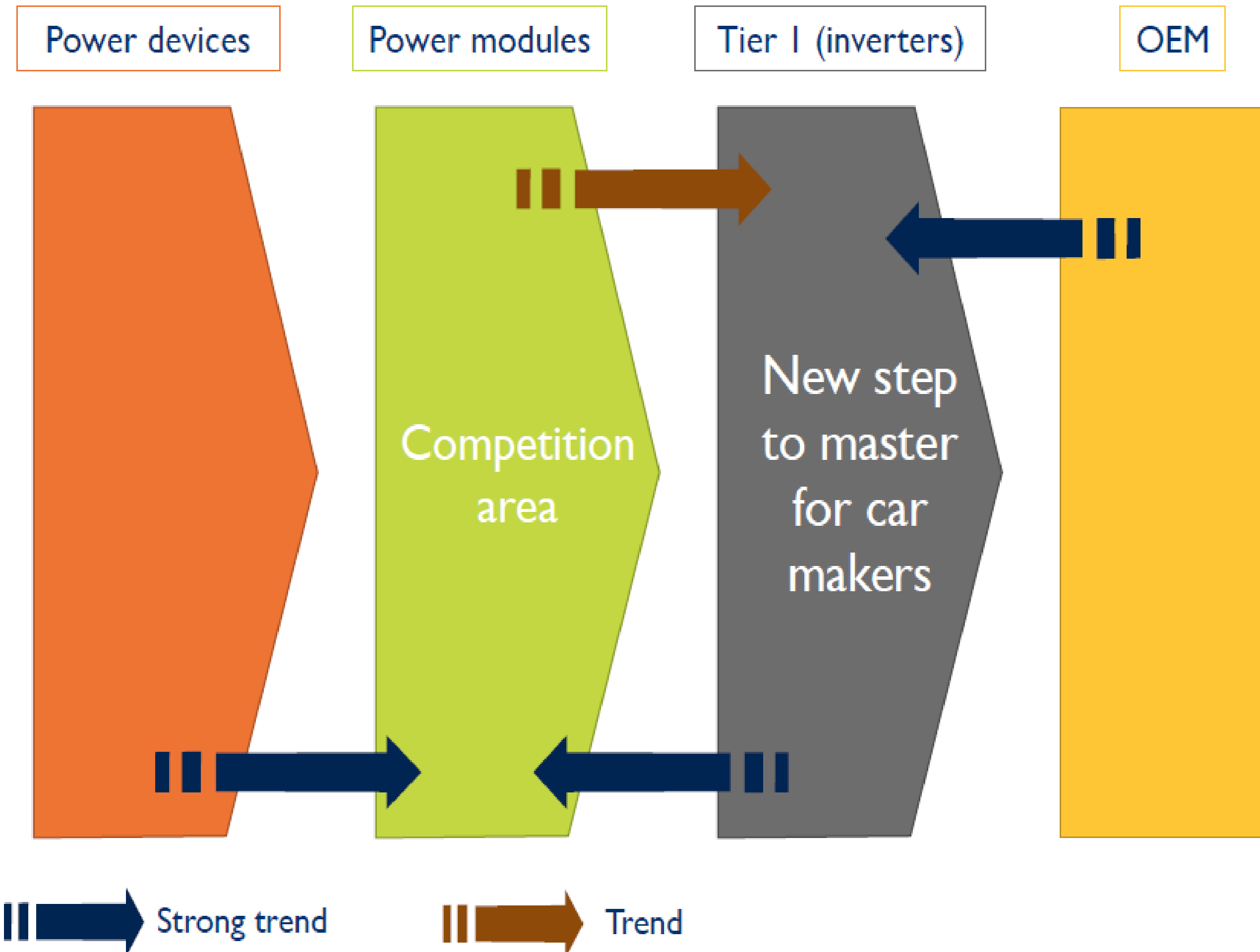


EVOLUTION OF POWER ELECTRONICS LANDSCAPE

Evolution of business models?

With such strong growth in the application, changes in business models are expected

- Power module manufacturing is an area of tough competition; module-only manufacturers must develop high performance products to stay competitive.
- Additionally, more and more car makers are willing to venture into the market at inverter level to differentiate themselves from competitors.

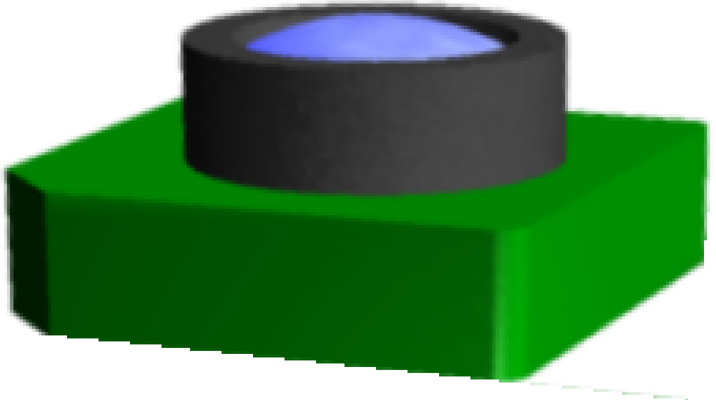


MoMiCa – Modular Camera Module

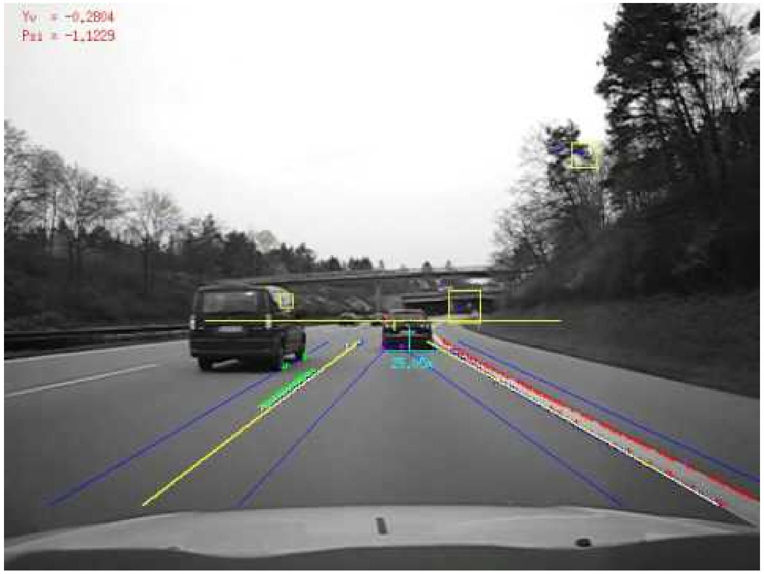
Motivation

•to develop a miniaturized camera module with integrated image processing

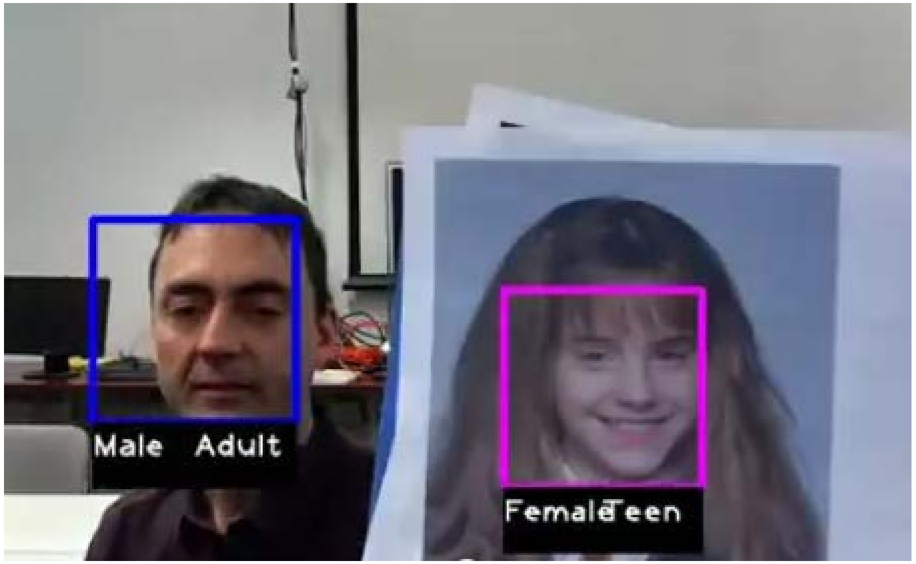
•using PCB PLP embedding



Potential Applications



traffic lane recognition



face / gender recognition

Rolf Aschenbrenner

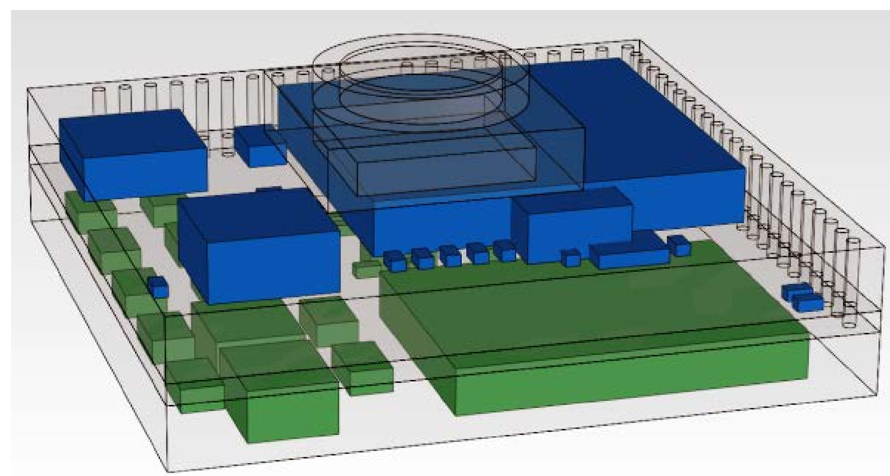
MoMiCa – Camera Module

Geometry
•16 x 16 x 3.6 mm³, weight 2 g w/o lens

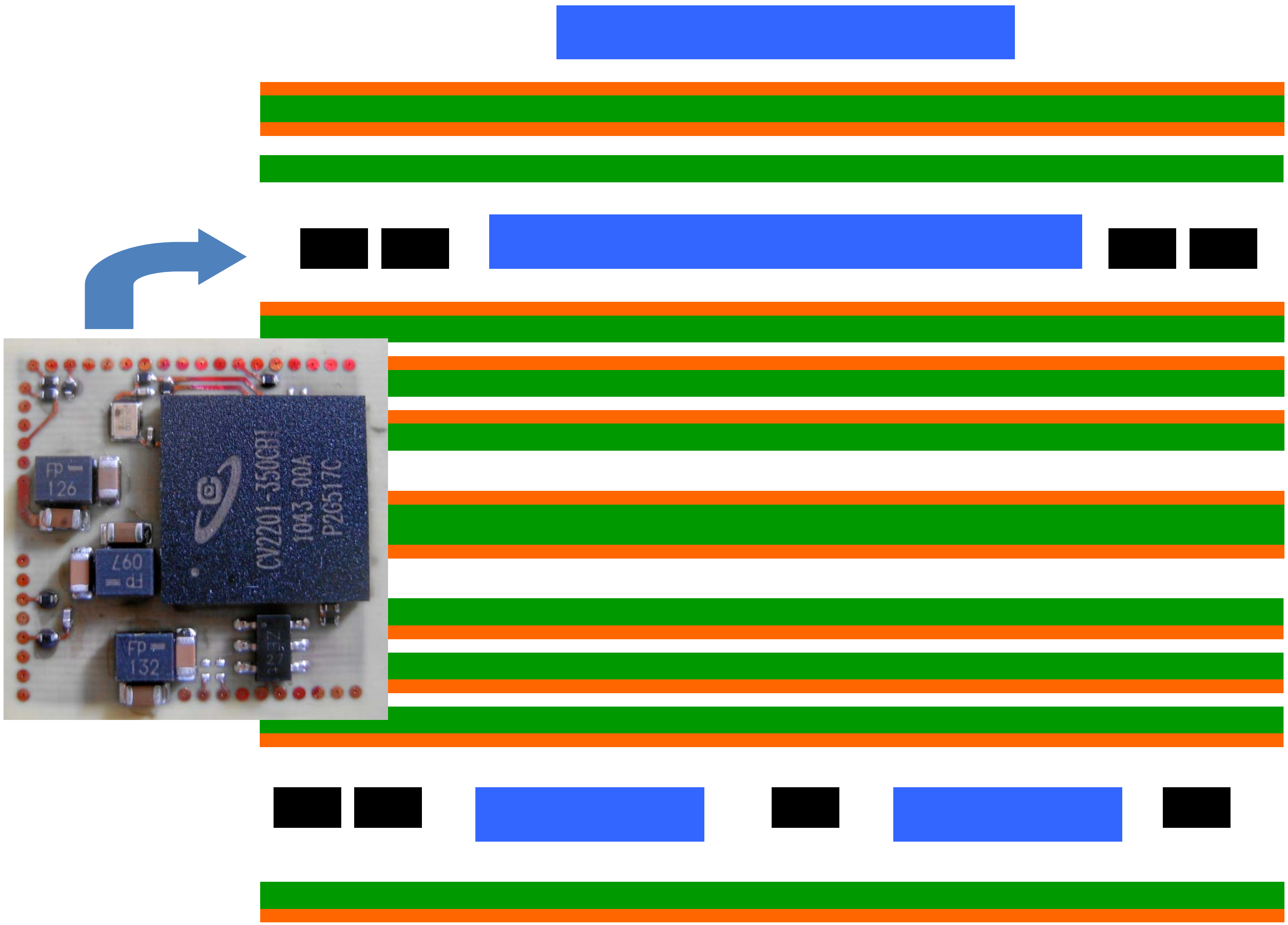
PCB Layers
•2 + 8 + 1 construction
•8 layer core with stacked mircrovias

Embedded Components
•32 bit microcontroller with image sensor interface (CogniVue CV2201 BGA 236)
•256 Mbit Flash Memory (Macronix 8WSON
•MOSFET switch (IRF SOIC)
•USB ESD protection (NXP SOT457)
•5 DC/DC-converters (Murata)
•oscillator 24 MHz (NXP
•2 LEDs (0402)
•34 capacitors (0201, 0603)
•25 resistors (0201)
•3 inductors (0603)

Components on top
•3 MPixel Image Sensor Omnivision 3642
•lens CMT746 + lens holder
•7 capacitors (0201)
•1 resistor (0201)
•1 inductor (0603)
•1 microswitch



MoMiCa - Layer Sequence



SMD Bildsensor

2 Lagen Kern

Bauelemente

3 Build-up Lagen

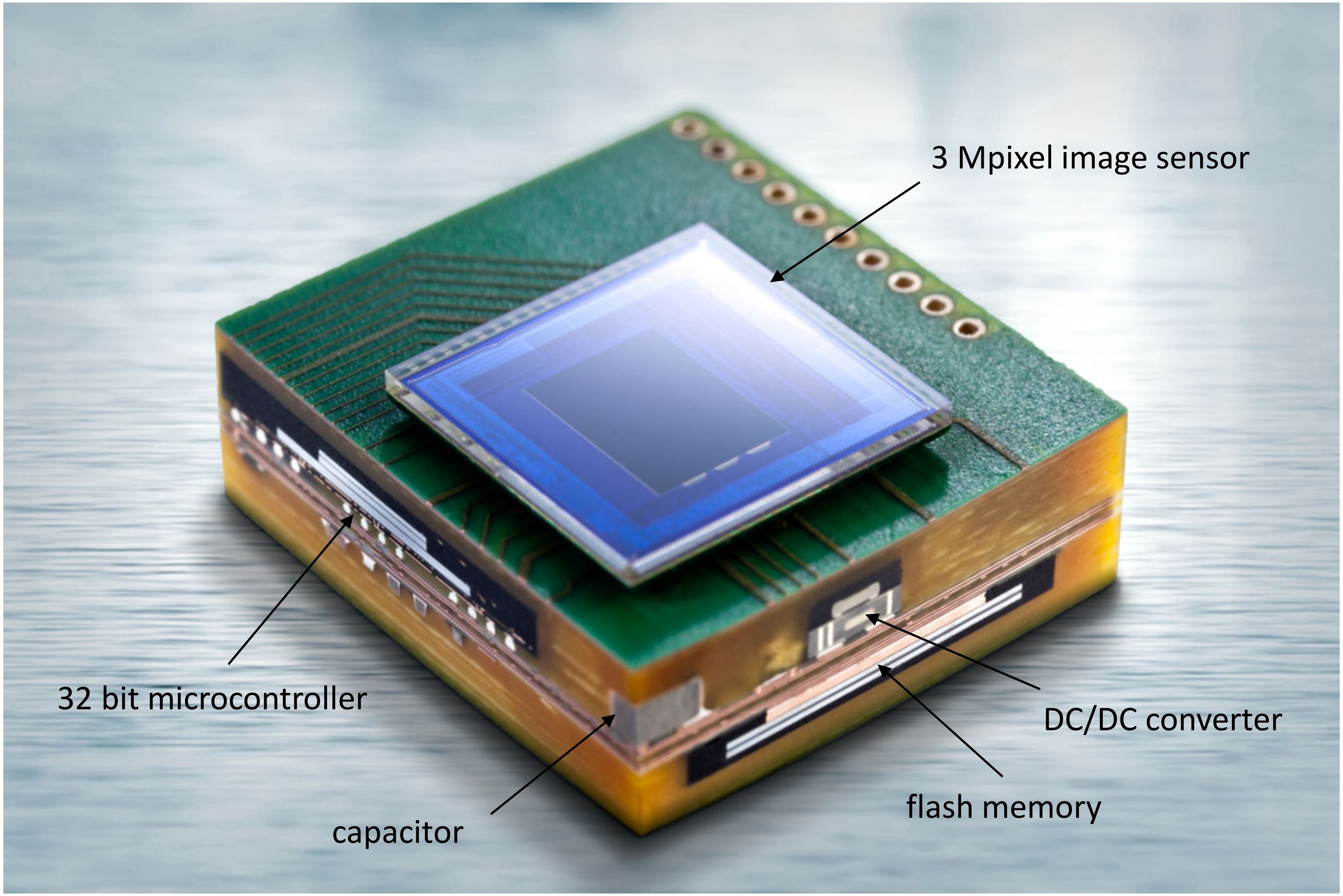
2 Lagen Kern

3 Build-up Lagen

Bauelemente

Außenlage

MoMiCa – Camera Module



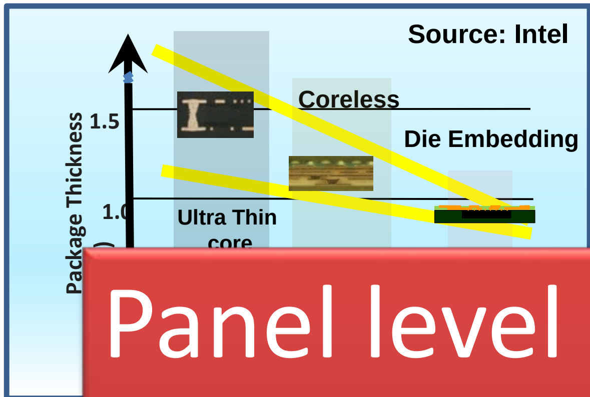
Modular camera with integrated 32 bit image processor and memory

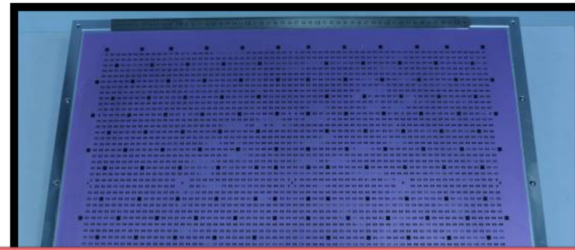
Panel Level - Embedding

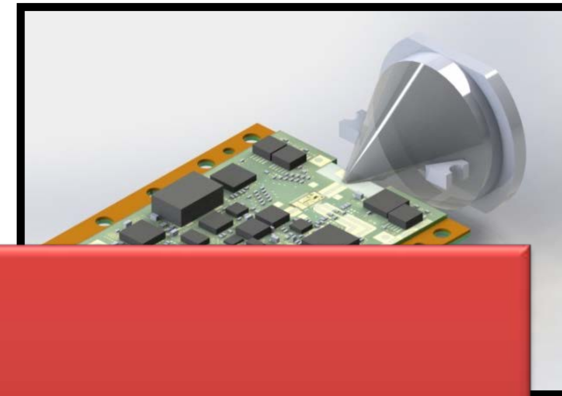
Miniaturization

Cost

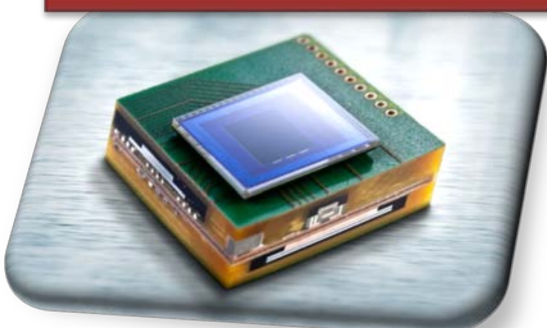
Electrical performance



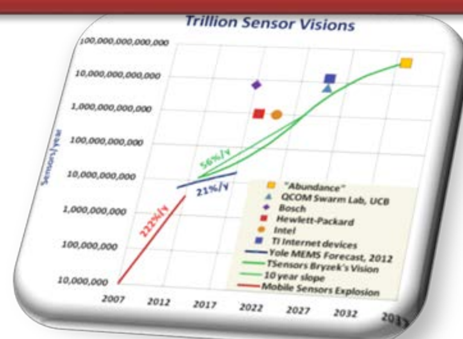




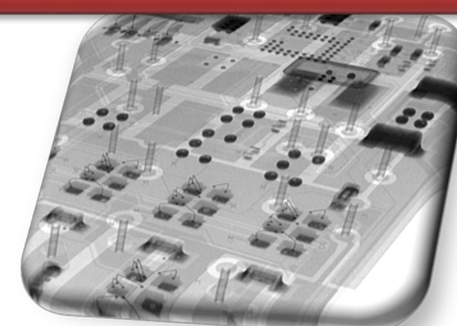
Panel level embedding:
A platform for many applications with improved reliability!



Camera with image processing



Trillion Sensor Vision



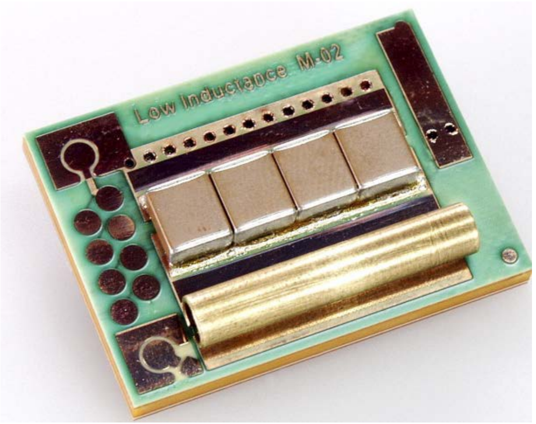
X-ray of embedded µSD

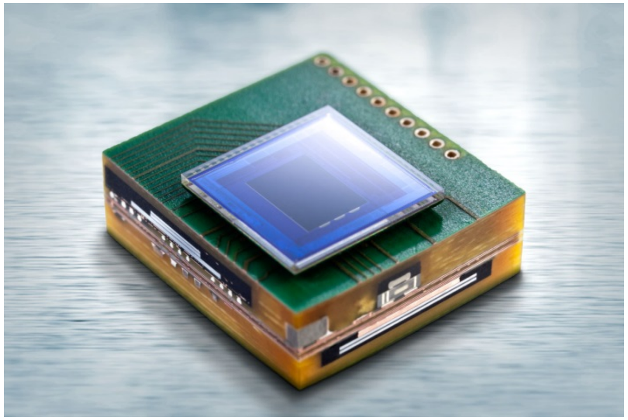
© Fraunhofer IZM

Conclusions

- Panel-level Packaging will gain a significant market share
- There will be a fusion of different technologies
- FO WLP will evolve towards large panels
- PCB technology will evolve towards very high density

. . . it just started - take the opportunity !






Thanks for your attention!