Characterization of *n*-Channel 4H-SiC MOSFETs: Electrical Measurements and Simulation Analysis

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***Abstract*— *n*-channel 4H-SiC MOSFETs were manufactured and characterized electrically at room temperature by current-voltage and Hall-effect measurements as well as by numerical simulations. To describe the observed electrical characteristics of the SiC MOSFETs, Near-Interface Trap (NIT) and charge carrier mobility degradation models were included in the simulation, performed with Sentaurus Device of Synopsys. For an accurate description of interface defects, their density versus trap energy was extracted from Hall-effect measurements. The result of the extraction indicates a continuous spreading of interface traps in the SiC conduction band, which was not reported before. For the first time also, the interface trap density as a function of trap energy as extracted from Hall-effect measurements was used directly in Sentaurus Device simulations. To check the applicability of the suggested model, it was used for the electrical simulation of MOSFETs with different channel lengths and widths but manufactured using the same technological processes. The developed simulation model shows excellent agreement with experimental results.**

I. INTRODUCTION

SiC is a semiconductor that possesses a favorable combination of physical properties [1] making it attractive for various applications in the electronic industry. Its wide bandgap makes it ideal for operation in high temperature environments. The high thermal conductivity of SiC and a roughly ten times higher breakdown field than in Si makes it the material of choice for high-power MOSFETs. In addition, the ability to form SiO_2 on SiC by thermal oxidation in a way similar to Si provides a good basis for the fabrication of SiC MOS-based electronic devices. Among the various polytypes of SiC, 4H-SiC is considered the most promising one for MOSFET development due to its high intrinsic carrier mobility. Unfortunately, commercial use of 4H-SiC MOSFETs is still limited by technological problems resulting in a low on-state current due to a low inversion-layer electron mobility and in a high leakage current of SiC MOSFETs.

A critical factor for the device performance of 4H-SiC MOSFETs with a surface channel is the quality of the interface between the semiconductor and the gate oxide which is believed to be directly related to the performance problems mentioned above. As it is known, 4H-SiC suffers from a high density of charge carrier traps near or at the interface [2]. The aim of this paper is to characterize 4H-SiC MOSFETs by applying different physical models in numerical TCAD simulations and comparing the simulation results with the measured transfer characteristics.

The Sentaurus Device software was used for numerical simulation of 4H-SiC *n*-channel MOSFETs. First, the device geometry and the doping distribution in SiC were set up. Second, the transfer characteristics were simulated and compared with the experimental results. The essential finding of this comparison is that the carrier mobility in the inversion layer of SiC MOSFETs and thus their observed electrical behavior is mainly influenced by Coulomb scattering of carriers at charged NITs and by surface-roughness scattering.

II. TEST MOSFETS

In this study, *n*-channel lateral MOSFETs have been fabricated on a *p*-type 4°-off 4H-SiC (0001) Si-face epitaxial layer with an aluminum concentration of $5 \cdot 10^{17}$ cm^{-3}. A 34 nm thick gate oxide was grown by thermal oxidation in N_2O atmosphere at 1553 K and annealed at the same temperature for 30 min under N_2 ambient. Phosphorus-doped polycrystalline silicon was deposited and patterned to form the gate electrode. Source and drain regions were box implanted with nitrogen (with a peak concentration of $5 \cdot 10^{19}$ cm^{-3}). Afterwards they were annealed under flowing Ar gas at a temperature of 1973 K for 30 min. For the fabrication of the source and drain contacts, SiC was alloyed with Ti at 1373 K for 2 min and thereafter a metallization stack containing Ti and Pt was deposited and patterned. The channel length and width of the transistors used in this study for model development are 500 µm and 80 µm, respectively. To characterize the MOSFETs electrically, current-voltage and Hall-effect measurements were performed at room temperature. The transfer characteristics were measured at drain-source voltages of 0.1 V, 0.6 V, and 1.1 V. The gate voltages were swept from 0 V to 20 V. Hall-effect measurements were already discussed elsewhere [3]. From that, only specific results are used for the simulations.

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However, a full description of the Hall-effect setup can be found in [4].

III. Simulation Results

A. Default Simulation

One of the main tasks for this numerical simulation is to explain the physical reasons for the low performance of MOS transistors based on 4H-SiC with a gate oxide fabricated by thermal oxidation in N_2O atmosphere. First, for reference, electrical properties of *n*-channel transistors were computed using the default simulation model that assumes an ideal interface between the gate oxide and the 4H-SiC semiconductor in the channel. This assumption means that neither fixed charges at the interface nor interface trapped charges are taken into account. The result of such a simulation for our SiC MOSFET is shown in Fig. 1 in comparison with the results of the measurements.

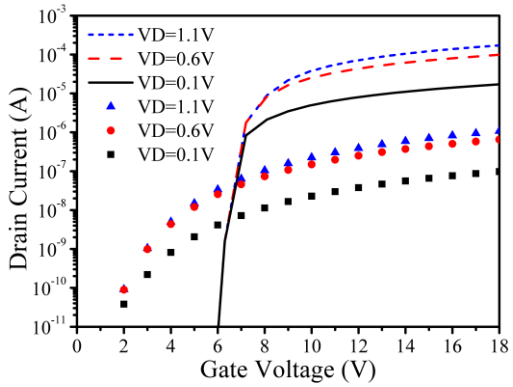

Figure 1. Comparison of default simulations (lines) and experiments (symbols) at different drain-source voltages.

As expected, the default simulation is insufficient and deviates from measurements significantly. The SiC MOSFET with an ideal interface, according to simulation, has a higher threshold voltage than measured and a significantly, i.e. about a factor of 50, higher current compared to the one measured. This result indicates the necessity to include appropriate models in the simulation for physical processes which must be considered in MOSFETs for achieving better agreement with experiments.

B. Fixed and Interface Trapped Charges

In order to identify the physical reasons for the lower performance compared to the ideal case, it is generally accepted as necessary to add interface traps between the gate oxide and the semiconductor material. Since *n*-channel MOSFETs are studied in this work, the interface trap densities at trap energies near the conduction band edge E_c are the most relevant ones. It is common practice in simulation to assume that the energy distribution of NITs can be described by an exponential tail distribution near the conduction band edge of SiC in the form [5]:

$$D_{it}(E_t) = D_{it}^{mid} + D_{it}^{edge} e^{(E_t - E_c)/\sigma}. \qquad (1)$$

Therein, D_{it}^{mid} is the midgap density of traps, D_{it}^{edge} is the band-edge density of traps, σ is the band-tail energy which determines the sharpness of the energetic profile, and E_t is the trap energy level. An important point of this model is that the distribution of interface traps is cut-off at E_c or even at a lower energy, i.e. D_{it} is assumed to be zero for higher energies. Although the parameters have a well-defined meaning, they are usually just fitting parameters to reproduce some characteristics of the electrical behavior of MOSFETs.

In order to avoid inaccuracies associated with a NIT model as in Eq.(1) in simulation, the interface trap density can be extracted directly from Hall-effect measurements. An important parameter in this procedure described in detail elsewhere [6] is a determination of the surface potential φ_s as a function of the applied gate voltage V_g. Based on the Hall-effect measurements, it can be obtained independently from the measured sheet carrier density. The interface trap distribution $D_{it}(E_t)$ can be determined from the change in the number of trapped electrons Δn_t for a small change in the surface potential $\Delta\varphi_s$:

$$D_{it}(E_t) = \frac{\Delta n_t}{\Delta \varphi_s} \qquad (2)$$

It should be emphasized that this method is self-consistent in the sense that the sheet carrier density of the electrons reflects all properties of the interface such as the electrons trapped in the NITs. To use this method for the calculation of the $D_{it}(E_t)$ distribution, the MOSFET described in the previous section was characterized by Hall-effect measurements. The results of the Hall-effect measurements and their interpretation are discussed in detail elsewhere [3]. Here we just use the resulting $D_{it}(E_t)$ distribution presented in Fig. 2. Please note that the sheet carrier density used for the extraction of $D_{it}(E_t)$ from Hall-effect measurements was obtained by assuming a Hall factor r_H determined in accordance with our new calculation method presented in [3]. It is important to point out that in this method the impact of different electron scattering mechanisms at the SiO_2/SiC interface on the effective values of the Hall factor were accounted for.

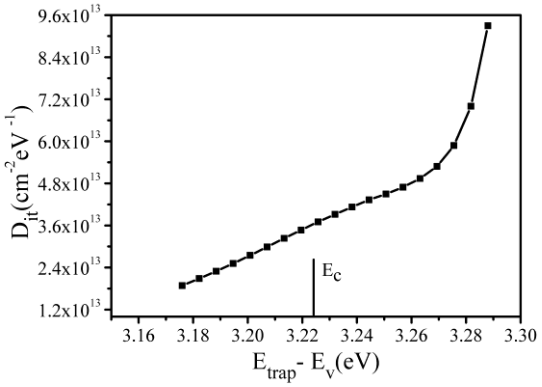

Figure 2. Interface trap density as a function of trap energy level, extracted from Hall-effect measurements.

The energy distribution of interface traps in Fig. 2 confirms the well-known continuous increase of the density towards the SiC conduction band edge E_c. In addition, as it can be seen in Fig. 2, the interface traps spread beyond E_c into the conduction band. Their density reaches a value of 9.3×10^{13} $cm^{-2}eV^{-1}$ at the highest trap energy of $E_t = E_v + 3.29$ eV accessible by this measurement method.

It should be noted that all traps for which the density was extracted from Hall-effect measurements are usually assumed to be acceptor-like states. These acceptor-like states store negative charge and have three effects on the device performance. The first effect is the trapping of electrons from the inversion layer, excluding them from participating in the electronic transport in the transistor channel. The second effect is the shift of the threshold voltage of *n*-channel MOSFETs to higher values due to the electrostatic pushing-off of the electrons in the inversion layer due to the negative charge trapped at the interface. The third effect is the scattering of electrons in the inversion layer at the trapped charges. The latter leads to a reduction of the mobility of the electrons in the inversion layer. All these effects contribute to the decrease of the MOSFET drain currents.

As reported elsewhere [7], in addition to negative charges due to electron trapping at the SiO_2/SiC interface, there are also positive charges at this interface. Furthermore, it was shown therein that this positive charge can be explained either by the presence of a large density of positive fixed charges at the interface or by the presence of donor-like states located close to the conduction band of SiC. The positive charge at the SiO_2/SiC interface lowers the threshold voltage and its amount was chosen in this simulation so that the simulated threshold voltage of the MOSFET agrees with the measured threshold voltage.

C. Mobility Degradation Model

In order to obtain an agreement between simulated and measured results, in addition to the NIT model which modifies the electrostatics of the transistor, mobility degradation due to scattering of the electrons at the interface defects has to be accounted for. It is widely accepted that the inversion electron mobility in 4H-SiC *n*-channel MOSFETs is limited due to electron scattering at the interface charges and ionized bulk impurities as well as at the surface roughness and at phonons [8, 9]. It should be noted here that including phonon-related and bulk-related components [9] into the mobility model did not result in a significant mobility reduction in our 4H-SiC *n*-channel MOSFETs. The dominant scattering mechanisms which lead to the low mobility in the inversion layer are surface-roughness scattering and Coulomb scattering at the interface charges. In our work, the contribution attributed to surface-roughness scattering is modeled in the form [10]:

$$\mu_{sr} = \left\{ \frac{\left(F_\perp / F_{ref}\right)^2}{\delta} + \frac{F_\perp^3}{\eta} \right\}^{-1} \qquad (3)$$

where $F_\perp$ is the component of the electric field perpendicular to the oxide/semiconductor interface, with a reference field of $F_{ref} = 1$ V/cm. The values of the model parameters δ and η were modified from the default values taken from silicon by bringing the simulated and experimental transfer characteristics at higher gate voltages into agreement and are listed in Table I.

TABLE I. MODEL PARAMETER VALUES FOR THE SURFACE-ROUGHNESS COMPONENT OF THE ELECTRON MOBILITY

Parameter	Units	Value
δ	$cm^2/(V\cdot s)$	$1.8\cdot10^{13}$
η	$V^2/(cm\cdot s)$	$1.8\cdot10^{29}$

The reduction of the electron mobility near the interface due to Coulomb scattering at $T = 300$ K was included in the form [10]:

$$\mu_c = \frac{\mu_1 \left\{ 1 + \left[c / \left(c_{trans} \left(\frac{N_c}{N_0} \right)^{\eta 1} \right) \right]^{\upsilon} \right\}}{\left(\frac{N_c}{N_0} \right)^{\eta 2} f(F_\perp)} \qquad (4)$$

where μ_1 is the mobility without the effect of Coulomb scattering, c is the concentration of electrons near the interface, and N_c is the interface charge density. The dependence on the perpendicular field $F_\perp$ is modeled by:

$$f(F_\perp) = 1 - e^{\left[-(F_\perp / E_0)^\gamma\right]} \qquad (5)$$

with default values from Sentaurus Device used for the parameters E_0, γ, c_{trans}, N_0, $\eta 1$, υ, and $\eta 2$ [10]. The Coulomb scattering model takes into account scattering of mobile electrons at the positive and negative interface charges.

A comparison of the measured and fully simulated transfer characteristics for the transistor implemented in this work is presented in Fig. 3.

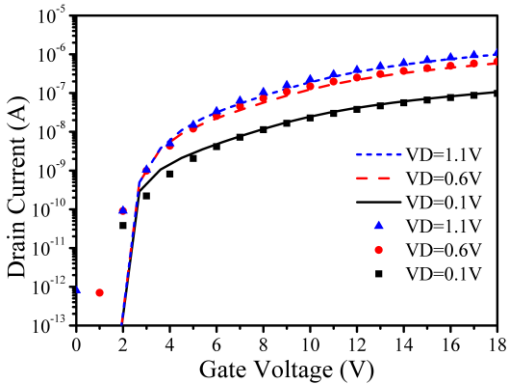

Figure 3. Comparison of transfer characteristics simulated with NIT and mobility degradation models (lines) with measurements (symbols) for a 500×80 μm^2 4H-SiC MOSFET at different drain-source voltages.

The final numerical simulation includes all the effects of the positive and negative interface charges as well as accounting for the mobility degradation due to the interface defects as described before. The $D_{it}(E_t)$ distribution of interface trap states shown in Fig. 2 was introduced into Sentaurus Device via a table function. It can be seen that the simulations with the developed NIT and the calibrated mobility models for 4H-SiC reproduce the measurements of transfer characteristics for different drain-source voltages (VD = 0.1 V, 0.6 V and 1.1 V) in the range of gate voltage from 2 V till 20 V excellently. The deviation of simulated and measured current-voltage characteristics at gate voltages between 0 V and 2 V could be explained by quantum mechanical effects, e.g. surface-defect-assisted tunneling, which were not included in this simulation. A further more detailed analysis of the simulation results indicates that the main reason for the low performance of 4H-SiC MOSFETs is the mobility reduction due to significant Coulomb scattering at the interface charges and surface-roughness scattering.

For a practical application of the developed simulation model, its scaling properties were checked. For this purpose, the electrical characteristics of *n*-channel MOSFETs manufactured with the same technological processes as the one described before but with a channel length and width of 5 µm and 100 µm, respectively, were simulated. Since the channel length was reduced by a factor of 100, and the channel widths for both transistors are similar, the current of the smaller one is about 100 times higher. This is well justified by the measurements of the transfer characteristics.

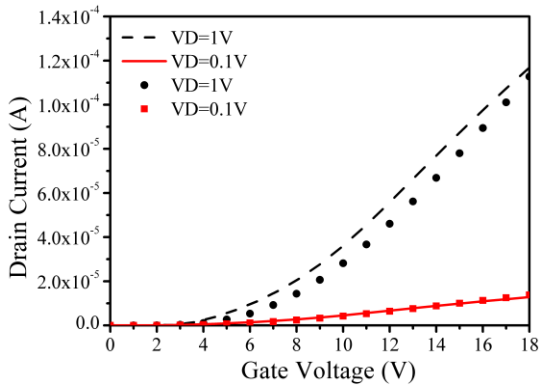

Figure 4. Comparison of transfer characteristics simulated with NIT and mobility degradation models (lines) with measurements (symbols) for a 5×100 µm^2 4H-SiC MOSFET at different drain-source voltages.

A comparison of the simulation for the 5 µm length *n*-channel MOSFET with the measurements of transfer characteristics for this transistor is presented in Fig. 4. The transfer characteristic at the lower drain-source voltage VD = 0.1 V is well reproduced in the simulation, while for higher VD = 1 V a small discrepancy is observed between the measured and simulated results. The deviation of the simulated maximum transistor current from the measurement amounts to about 4%. Taking into account that neither the model parameters for trap distribution nor for mobility models were modified, this is an excellent agreement. It means that the developed model has excellent scaling properties and the assumption of a non-uniform distribution of the near-interface traps which was applied in the simulation is also supported by the measurements on transistors with different channel dimensions.

IV. Conclusion

A TCAD simulation analysis has been performed to understand the physical mechanisms determining the electrical performance of *n*-channel 4H-SiC MOSFETs. Hall-effect measurements were used to calculate the interface trap density versus trap energy. For the first time, the experimentally measured energetic distribution of interface traps was used directly in TCAD simulation. In addition to the NIT model, mobility degradation models were applied in the simulations to characterize the electrical properties of 4H-SiC MOSFETs. A very good agreement between measured and simulated transfer characteristics was achieved. Moreover, the developed simulation model has excellent scaling properties, it can reproduce the transfer characteristics of transistors with different channel dimensions manufactured using the same technological processes.

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