Aixtron user meeting at ICSCRM 2015

Quality control of SiC materials by optical detection of defects

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Acknowledgment

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Outline

- Motivation and aims for UVPL imaging
- Measurement setup
- UVPL imaging on bare wafers and epiwafers
- UVPL imaging on partially processed wafers
- Optical stress test for material testing
- Conclusions

Motivation and aims for UVPL imaging

- **Find** structural and technological **defects*:**
  - in substrates, epilayers and partially processed **SiC wafers**
  - with **non-destructive, inline** measurements!

- **Tracking defects** from substrate to epilayer and to device
  - Discard defective material specifically ?

- **Improve reliability** testing of devices
  - Optical stressing of base material and devices possible?
  - Discard defective devices specifically ?

* structural defects: dislocations, stacking faults, …
* technological defects: scratches, downfalls, …

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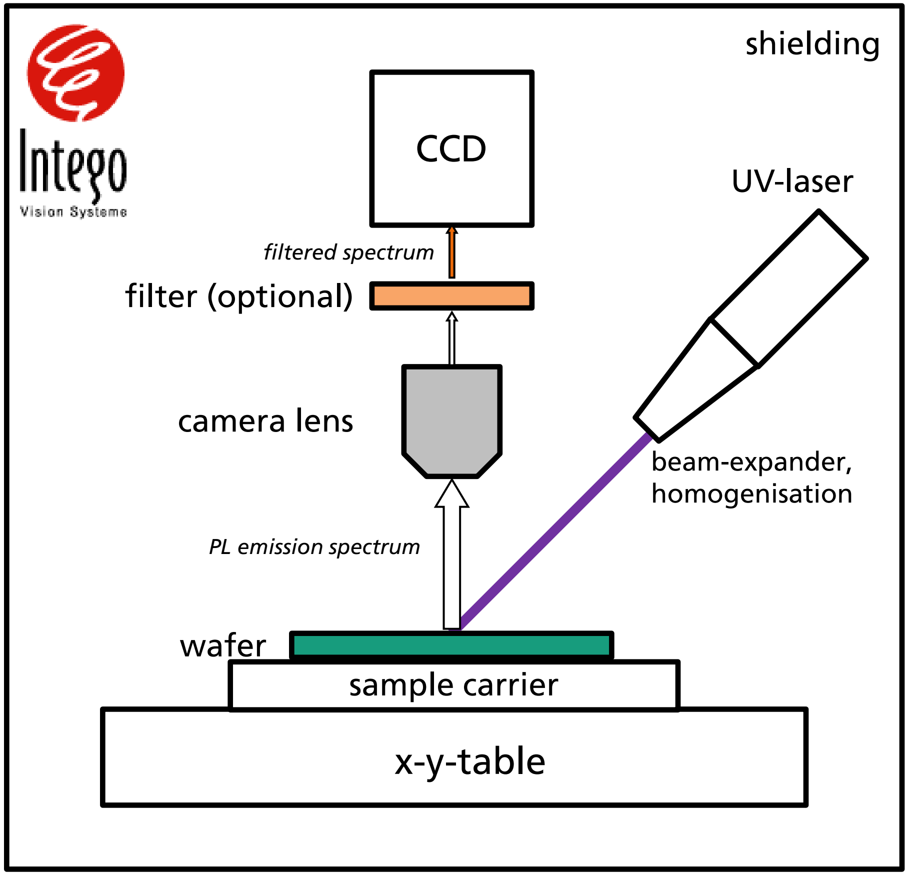
Measurement setup: Defect Luminescence Scanner (DLS)



Class 1 laser system

- UV-Laser: 325 nm (cw, 100 mW)
- Penetration depth: approx. 8 µm
- CCD-camera (400 - 1000 nm)
- Band-pass filters ($\lambda \pm 50$ nm)
- Narrow-band filters ($\lambda \pm 5$ nm)
- Long-pass filter: $\lambda > 590$ nm
- Camera lens: **2.8x** or 6.3x

- Lateral res.: **5 µm** or 2.2 µm
- x-y-table (up to **6''**)
- Meas. time: **5 - 30 min**

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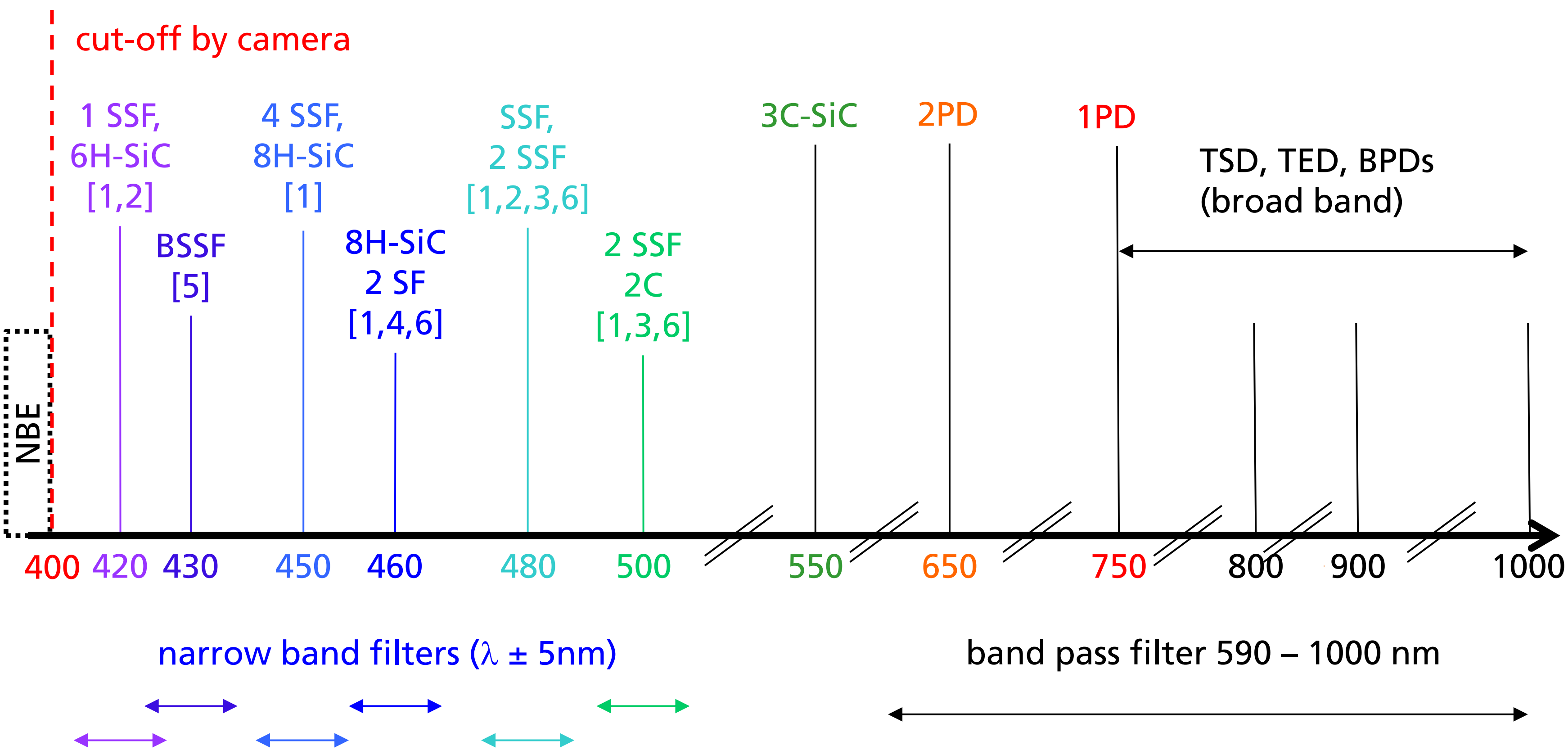
Identification of defects by their spectral fingerprints

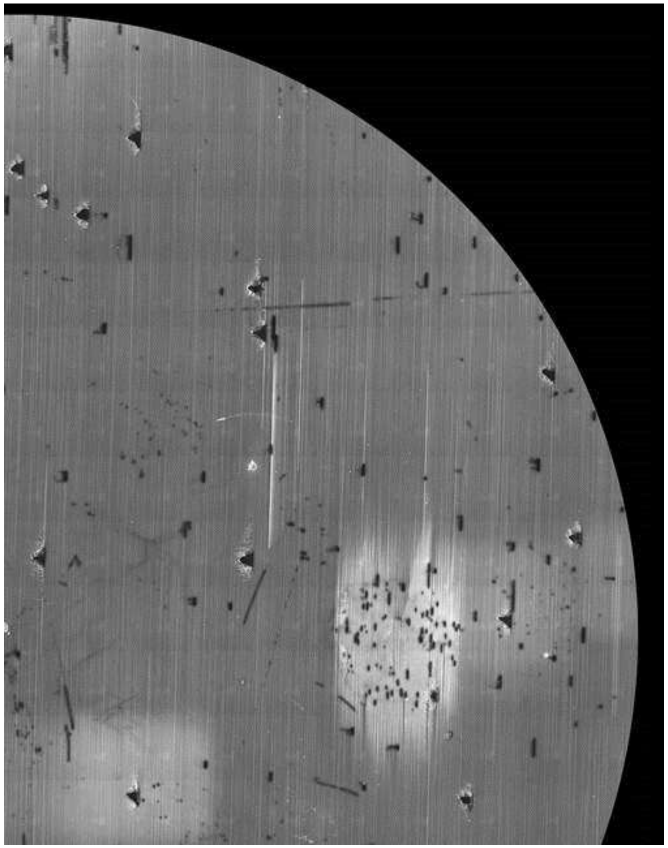
NBE = Near Band Edge emission



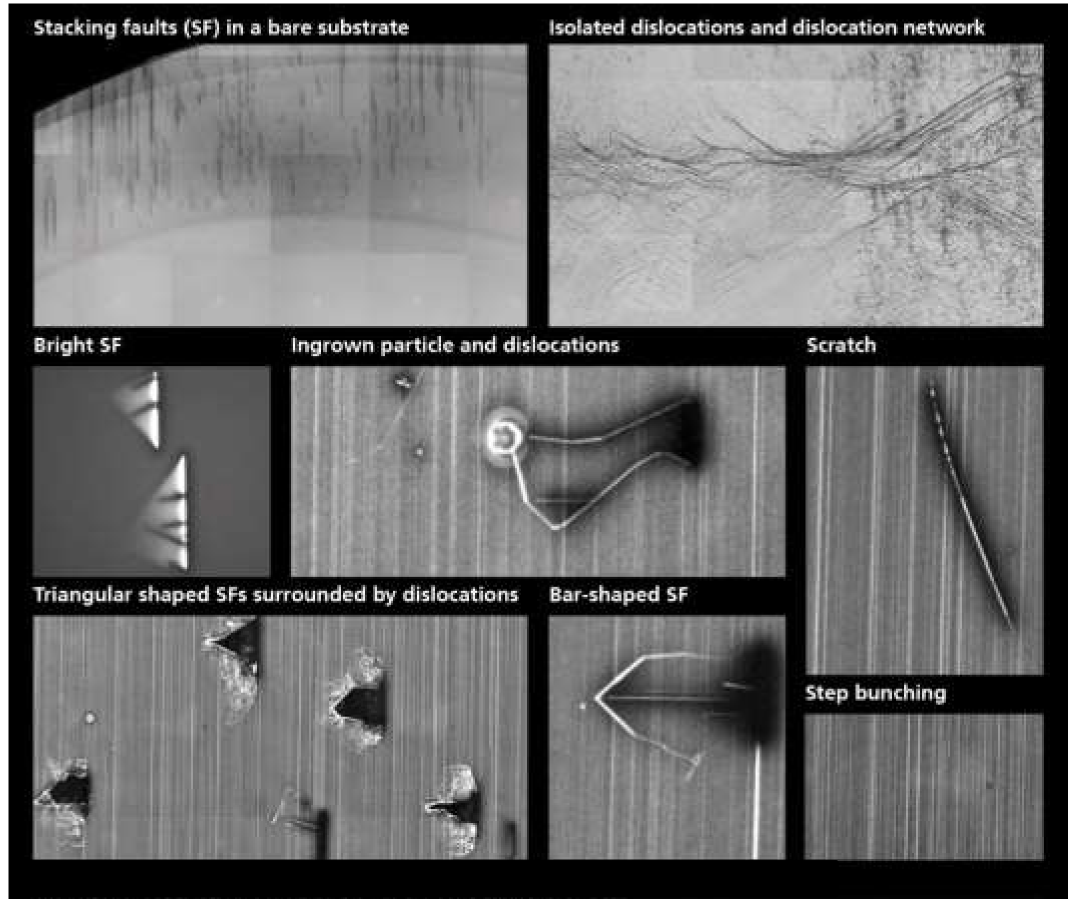
[1] Thierry-Jebali et al. AIP 2015; [2] Kamata et al AIP 2010; [3] Bluet et al. AIP 2003; [4] G. Feng et al. APL 2008; [5] Camarda et al. AIP 2011; [6] Feng et al. Physica B 2009

UVPL IMAGING OF SUBSTRATES AND EPIWAFERS

UVPL image processing: typical defects in epiwafers



Part of a 100 mm epiwafer with 30 µm thick epilayer.
mag: 2.8x; exposure: 1 s; PL spectrum: 400 – 1000 nm.



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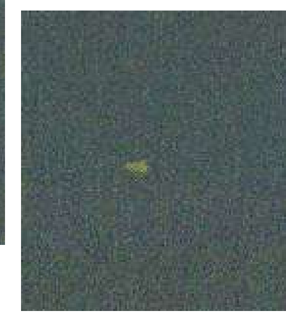
UVPL imaging: identification of stacking faults

1. UVPL imaging (400 – 1000 nm)



2. stacking fault types

Part of a 100 mm epiwafer with 5 µm thick epilayer.
mag: 2.8x; exposure: 1 s; different narrow band filters.

1) UVPL imaging with different narrow band filters (approx. 15 min./filter)
2) Compilation of overview to stacking fault types: immediately.

→ Size of different stacking fault types? Origins of different stacking fault types?

→ Which ones are critical defects?

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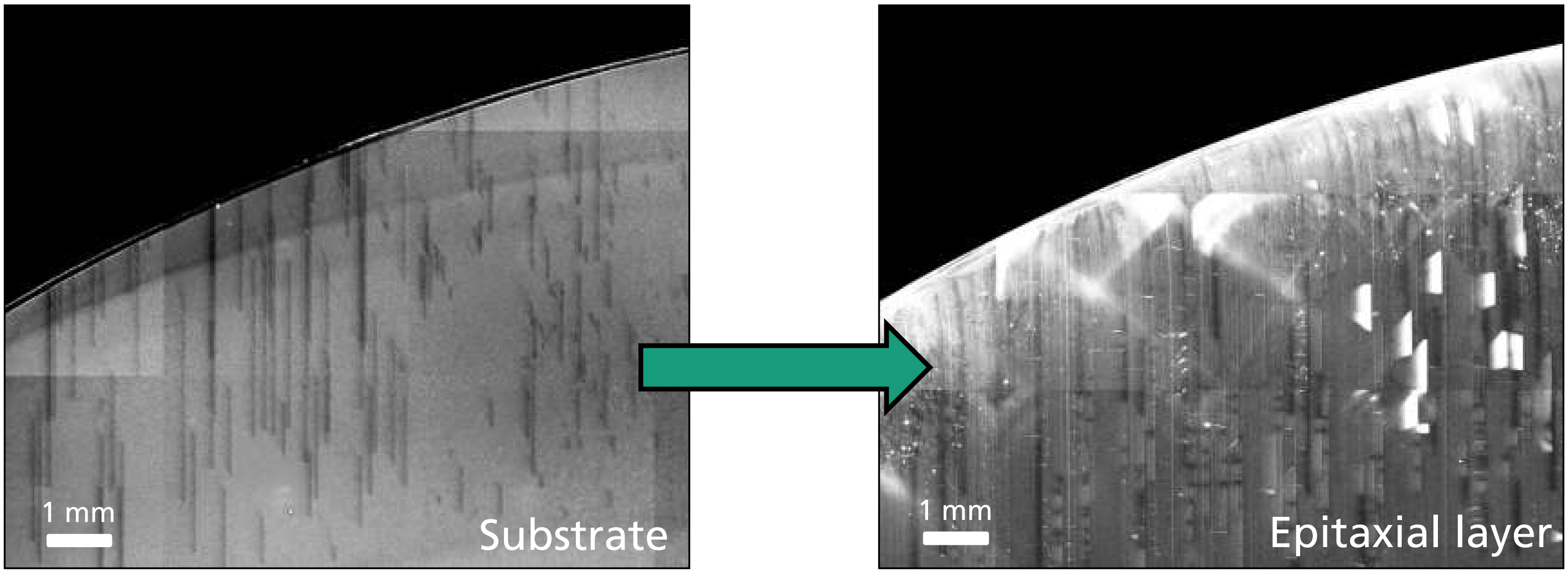
UVPL of substrates and epiwafers: stacking faults

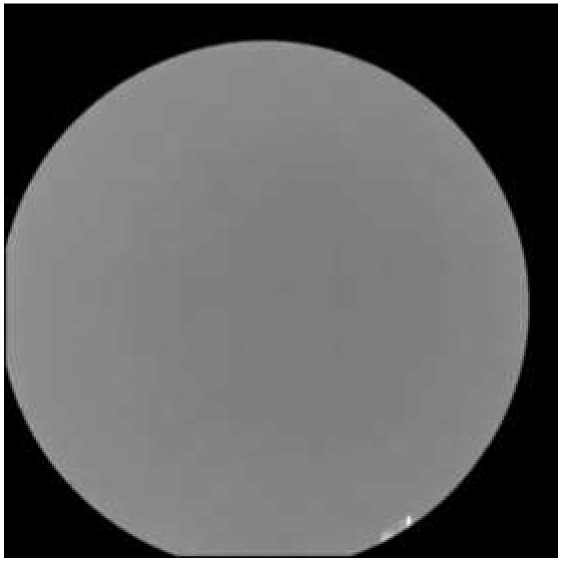


- Stacking faults (dark bar-shaped) already present in substrate
- Increased amount of dark bar-shaped stacking faults in epitaxial layer

→ Propagation and expansion in epitaxial layer during epitaxial layer growth

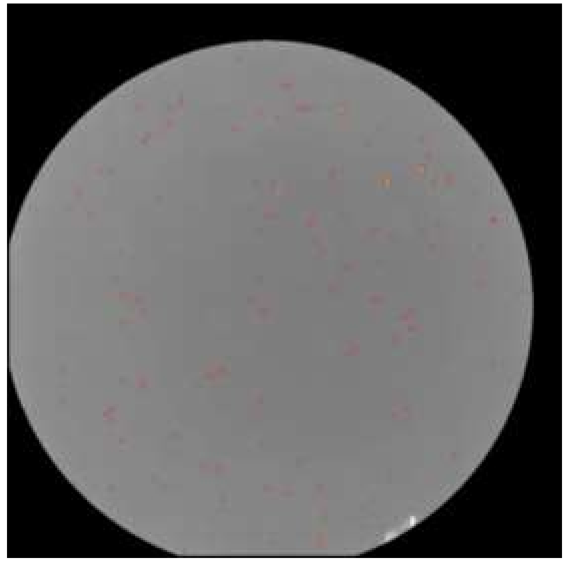
- Even more details of defects visible with higher magnification

UVPL image processing: yield prediction



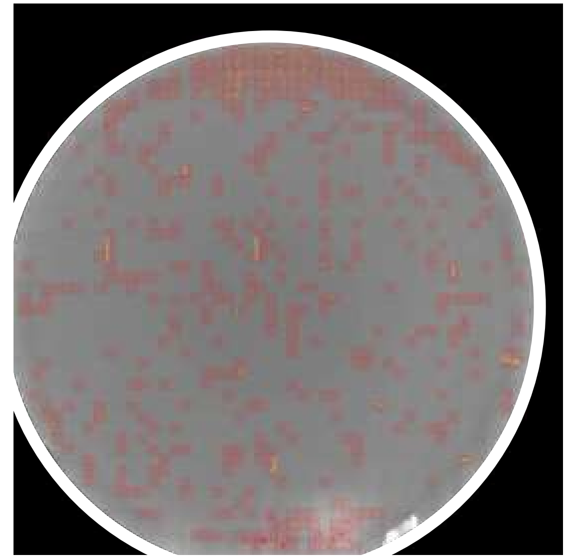
1. UVPL imaging (400 – 1000 nm)

100 mm epiwafer from vendor.
mag: 2.8x; exposure: 1 s; PL spectrum: 400 – 1000 nm.



2. yield prediction (e.g. 1 x 1 mm²)

100 mm epiwafer from vendor.
mag: 2.8x; exposure: 1 s; PL spectrum: 400 – 1000 nm.



2. yield prediction (e.g. 2 x 2 mm²)

100 mm epiwafer with 45 µm epilayer from vendor.
mag: 2.8x; exposure: 1 s; PL spectrum: 400 – 1000 nm.

1) UVPL imaging of 100 mm epiwafer and defect recognition/classification: ~ 15 min.
2) Yield prediction according to selected defect classes and die size: immediately.

→ Export geometrical data (x-y position, size, shape, …) for each individual defect

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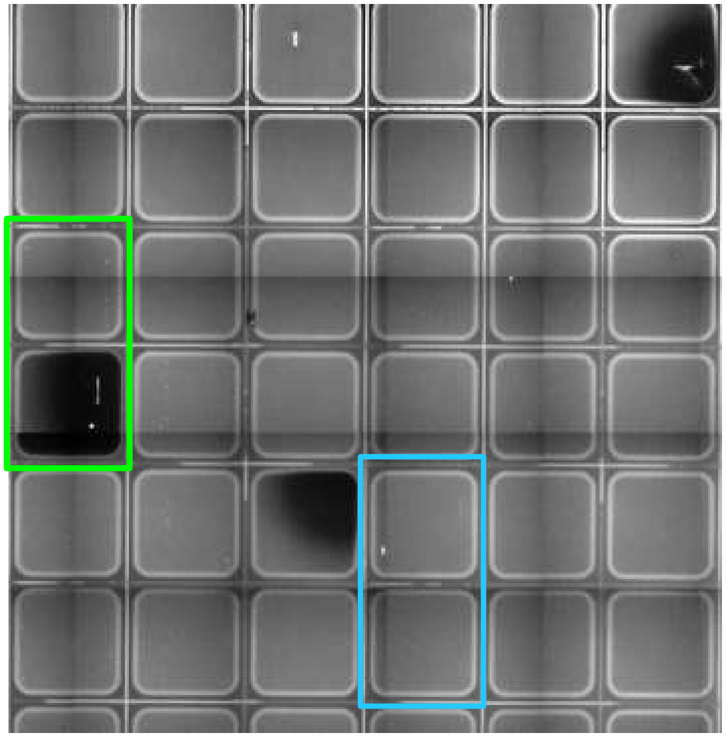
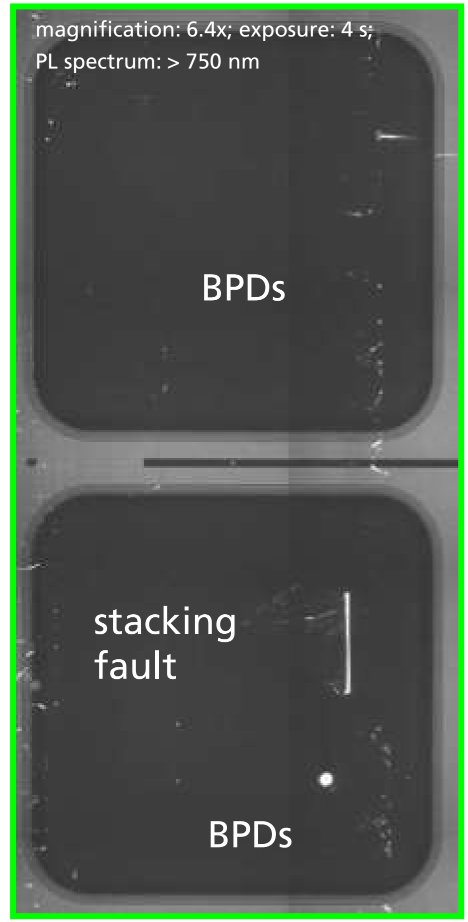
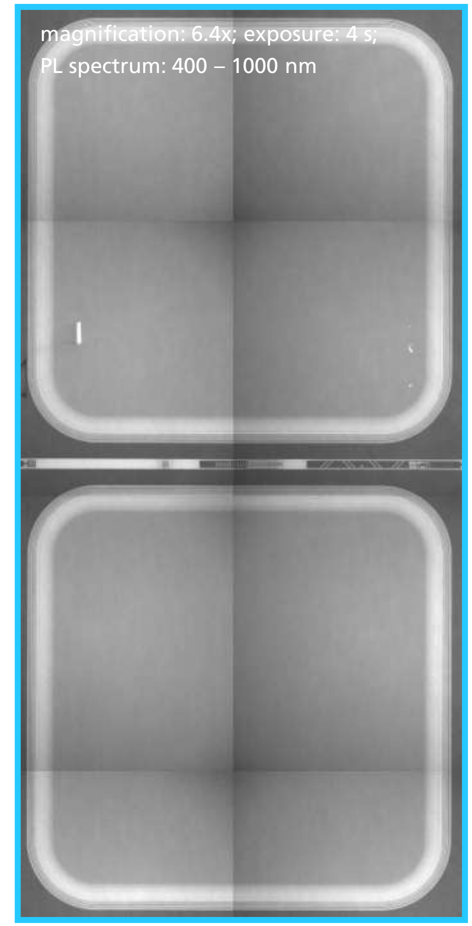
UVPL IMAGING OF PARTIALLY PROCESSED WAFERS

UVPL imaging of partially processed wafers



6.5 kV PiN diodes fabricated within „SiC-WinS“ project;
diode size 3.5 x 3.5 mm².
magnification: 6.4x; exposure: 4 s; PL spectrum: 400 – 1000 nm.





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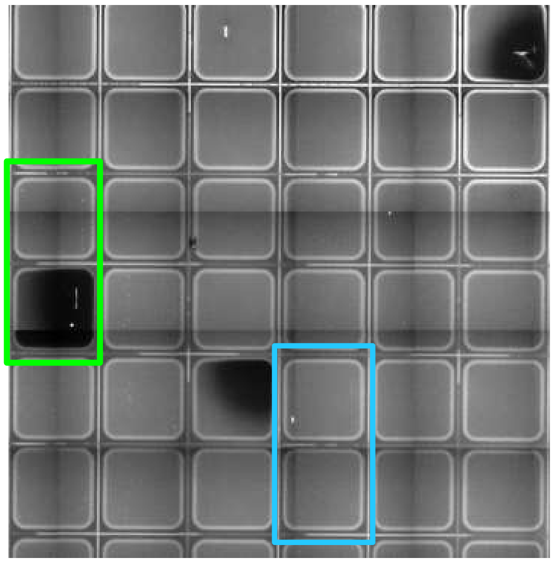
UVPL imaging of partially processed wafers



6.5 kV PiN diodes fabricated within „SiC-WinS“ project; diode size 3.5 x 3.5 mm².
mag: 6.4x; exp: 4 s; PL spectrum: 400 – 1000 nm.

- Defects can be tracked from bare epi to partially processed wafer
- Defective devices can be identified by UVPL
- Bipolar degradation of PiN diodes can be *predicted* by UVPL

  → L. Wehrhahn et al.: Bipolar degradation of 6.5 kV SiC pn-diodes: result prediction by photoluminescence; Th-2B-4

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OPTICAL STRESSING BY UVPL

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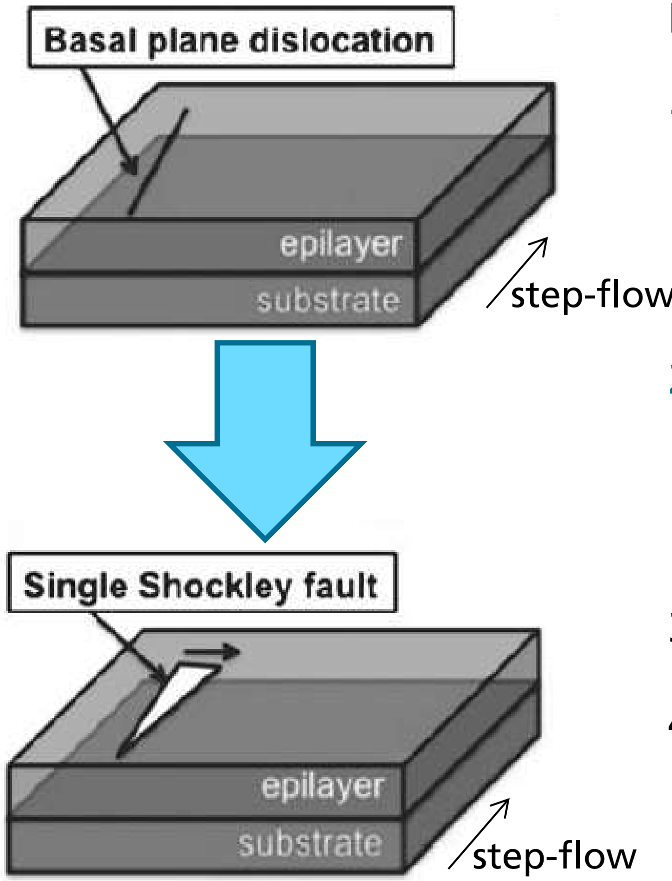
Optical stressing of the material: idea



Provoke “bipolar degradation” on wafer level

→ Discard susceptible material specifically

1. root cause: Basal Plane Dislocation (BPD) in material
2. trigger: recombination of excess carriers at BPD. origin of excess carriers: by bipolar device operation or optical excitation
3. consequence: BPD converts to stacking fault
4. continued recombination: expansion of stacking fault

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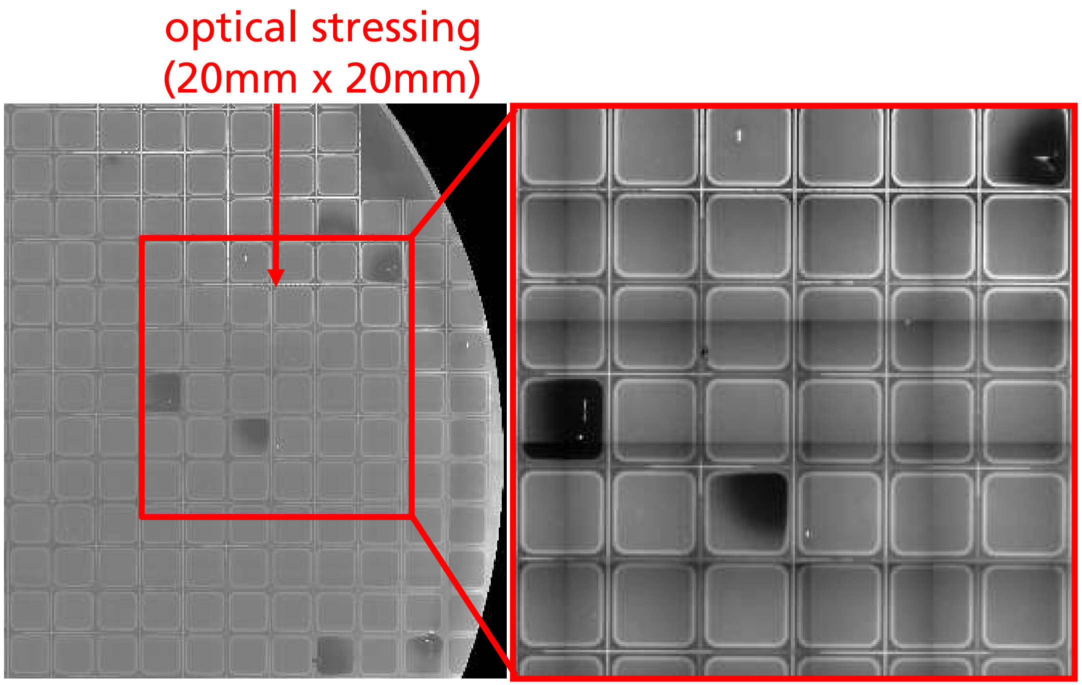
Optical stressing of the material: procedure



6.5 kV PiN diodes fabricated within „SiC-WinS“ project; diode size 3.5 x 3.5 mm².
mag: 2.8x; exp: 5 s; PL spectrum: 400-1000 nm.

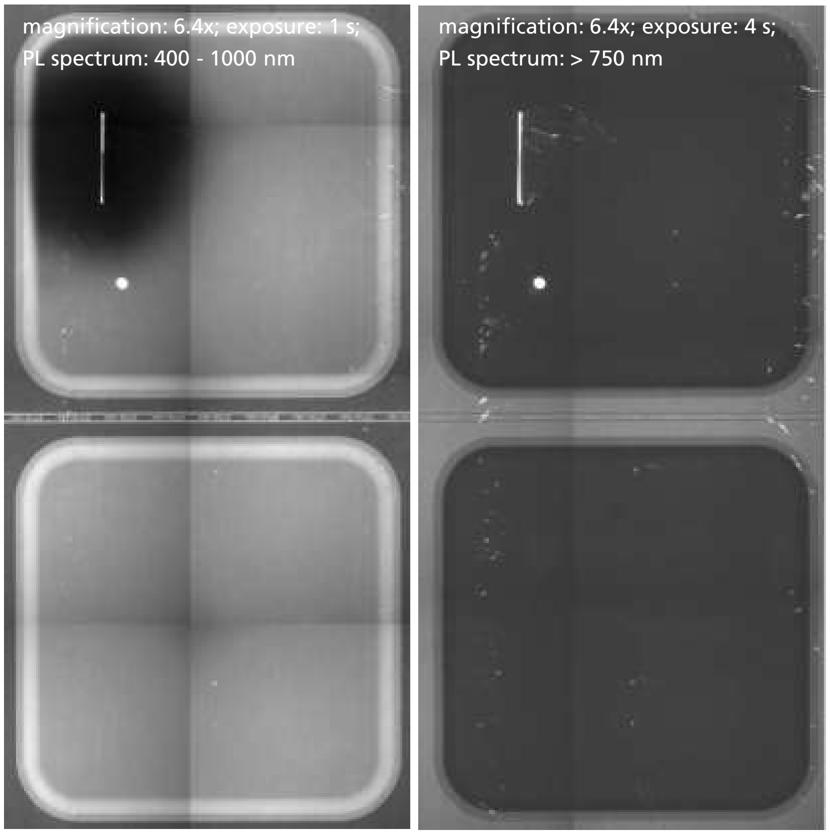
mag: 6.3x; exposure: 5 s; PL spectrum: 400-1000 nm.

Procedure:

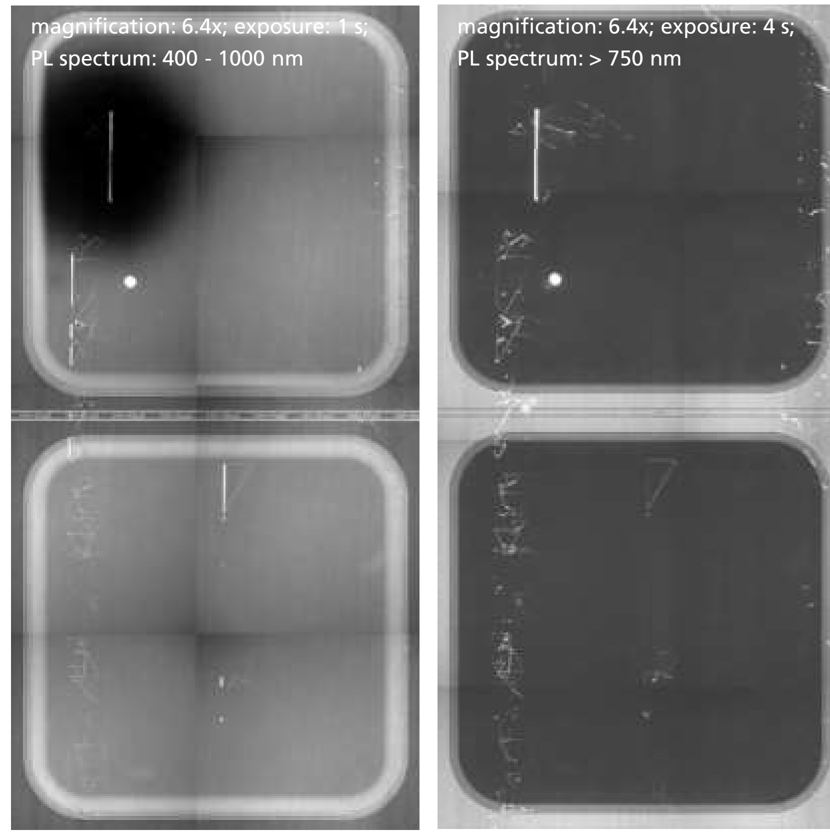
1. Detailed mapping with higher magnification (6.3x)
2. Optical stressing (beam width FWHM ca. 500 µm, scan speed 100 µm/s)
3. Repeat detailed mapping with higher magnification (6.3x)

Optical stressing: generation of stacking faults (1/3)

BEFORE optical stressing



AFTER optical stressing



6.5 kV PiN diodes fabricated within „SiC-WinS“ project; diode size 3.5 x 3.5 mm².

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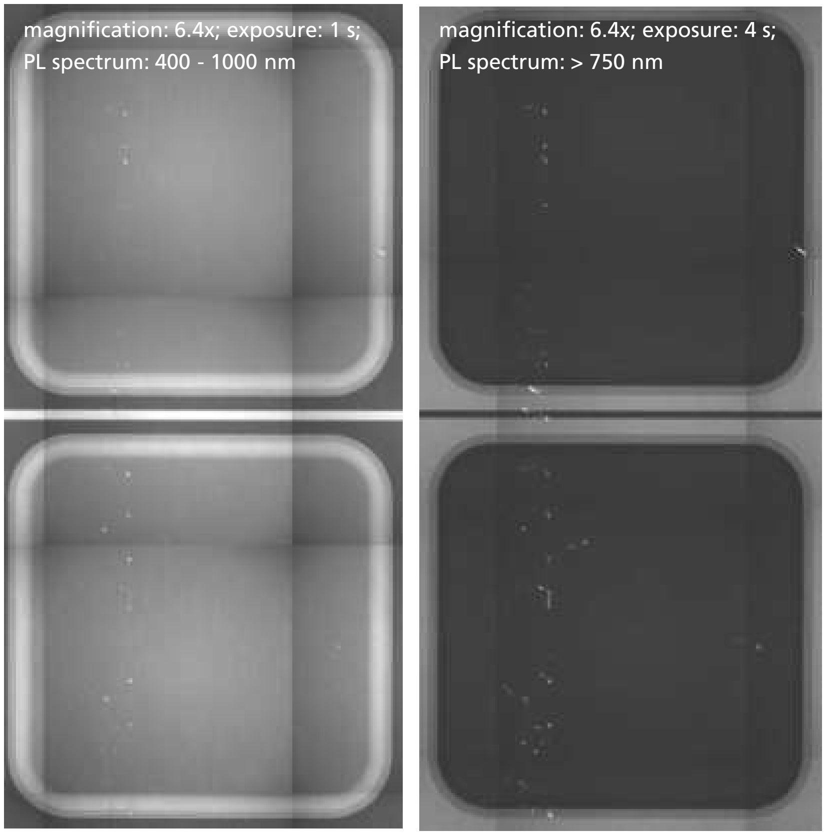
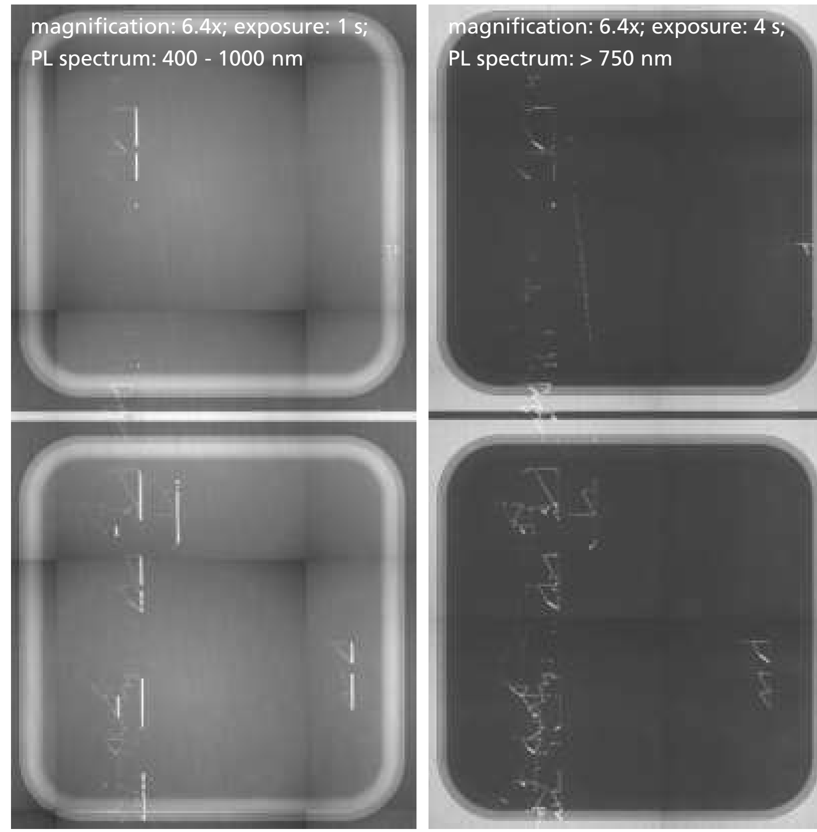
Optical stressing: generation of stacking faults (2/3)

BEFORE optical stressing



AFTER optical stressing



6.5 kV PiN diodes fabricated within „SiC-WinS“ project; diode size 3.5 x 3.5 mm².

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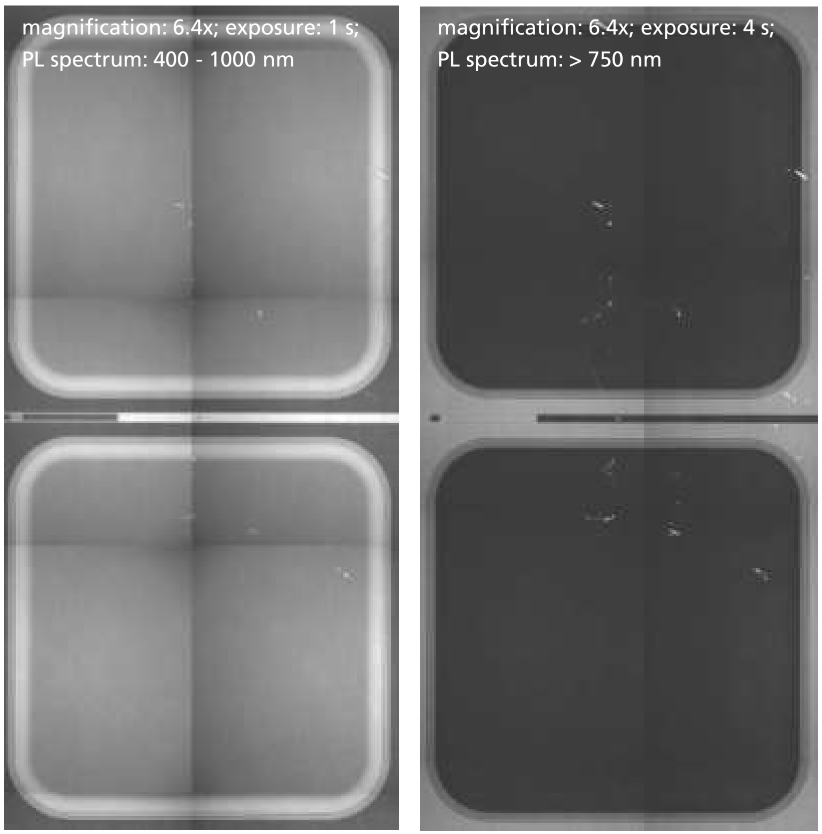
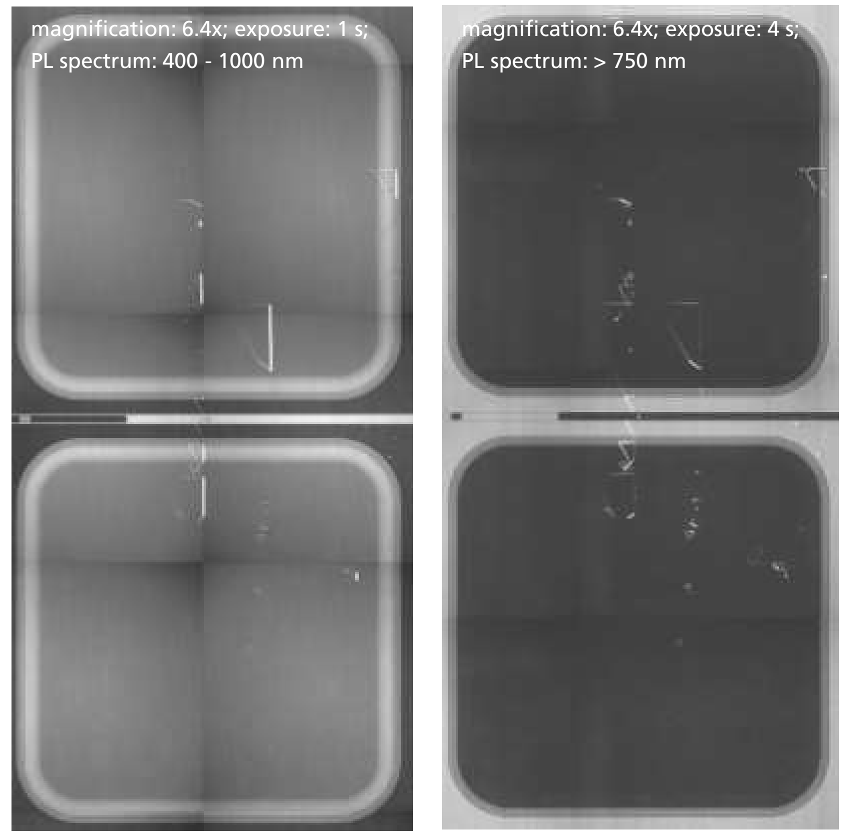
Optical stressing: generation of stacking faults (3/3)

BEFORE optical stressing → AFTER optical stressing





6.5 kV PiN diodes fabricated within „SiC-WinS“ project; diode size 3.5 x 3.5 mm².

Conclusions

- **Find** structural and technological **defects***
  - in substrates, epilayers and partially processed **SiC wafers**
  - with **non-destructive, inline** measurements!

- Tracking defects from substrate to epilayer and to device
  - Learn about defect behavior during growth processes and technology
  - Discard defective material specifically → **save costs!**

- Improve reliability testing of devices
  - Optical stressing of base material and devices
  - Discard defective devices specifically → **enable bipolar devices!**

* structural defects: dislocations, stacking faults, … ; technological defects: scratches, downfalls, …

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