Charge/Discharge effects and ESD prevention at the example of RFID smart card manufacturing

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Zusammenfassung – Die Herstellung von Chipkarten-Inlays auf Trägerfolie stellte aus ESD Sicht schon immer eine Herausforderung dar, zumal die Folien normalerweise aus nicht ableitfähigen Kunststoffen bestehen. Mit der Einführung von Zweiband-RFIDs (Funkschlüssel) in Chipkarten sind jetzt neue ESD Risiken mit unkonventionellen Entladungspfaden entstanden. Auf die eine Hälfte der Plastikfolie wird eine Spulenantenne (LF) aufgedruckt. Um diese elektrisch zu schließen, sind an der Stelle der Rückleitung beide Seiten der Folie metallisiert. Auf der anderen Hälfte befindet sich – für den UHF Bereich – ein offener Faltdipol, der keine Durchkontaktierung benötigt und daher elektrisch floatet, bzw. produktionsbedingt durch Reibung aufgeladen wird. Wird nun ein RFID-Chip in Fliptechnik auf die Antenne assembliert, so entsteht ein harter Entladekanal zwischen UHF- und HF-Antenne durch den Chip hindurch. In einem solchen Fall sind die ESD Schutzstrukturen nur von begrenztem Nutzen. Das Paper befasst sich im ersten Teil mit der Problemdarstellung und den Grundlagen. Im zweiten Teil geht es um Abhilfemaßnahmen, gezeigt an einer beispielhaften Prozessanlage. Teil 3 befasst sich mit dem vertieften Verständnis der Entladepfade und –formen, sowie einer geeigneten Testmethodik. Im letzten Teil wird ein Folienprüfstand zur Evaluation verschiedener Trägerfolien vorgestellt und ein Ausblick auf künftige Entwicklungen gegeben.

Abstract – Already for long time, the manufacturing of chip card inlays on carrier foil tape is a challenge from ESD point of view, since these carrier foils usually are made from non-dissipative plastics. The introduction of dual-band RFIDs (Radio Frequency Identification Devices) in chip cards created new ESD risks with unconventional discharge paths. On a plastic foil, a more or less grounded coil antenna for radio frequency (RF) is aluminum-printed on one-half of the card. On the other half, an electrical floating, but thus, highly electrostatic charged folded dipole for ultrahigh frequency (UHF) is arranged. When the chip is placed by a flip-chip assembly process, a strong discharge takes place through the RF-UHF-path of the chip. Usual ESD protective structures are only of limited use in these cases. In its first part, this paper describes the problems and introduces into the basics. The second part deals with in-process improvements in order to minimize ESD risks, presented at the example of a typical process equipment. Finally, the third part deals with a deeper understanding of discharge characteristics and verification/ testing methods. In the last part of the paper, a special setup for the characterization of carrier foils is presented and an outlook on future developments is given.

1 Introduction

RFID devices become one of the most numerous manufactured devices worldwide. They are used in access cards, money cards, product labels and numerous further applications. In principle, we distinguish between two main groups of RFIDs: the low frequency RFIDs, which are connected to a coil antenna and the ultrahigh-frequency RFIDs, working with a multiple-folded open dipole. LF-RFIDs operate in a primarily magnetic field, allowing only a low range but are less sensitive against nearby metals and liquids than UHF RFIDs. On the other hand, UHF-RFIDs allow significantly enhanced ranges and – due to higher frequencies – a higher bandwidth, meaning high data transfer rates. However, in presence of nearby water or metals, they suffer severe resonance shifts, which limit their fields of application. With new dual-band RFID (Radio Frequency Identification Device) chips coming up, some basic new ESD scenarios challenge the production of RFID smart cards. Within the same antenna foil inlay, two antennas – one for low, one for ultra-high frequency (UHF), are printed. While the low-radio-frequency (RF-) antenna is a printed coil, of which the return path needs line printing on both sides of the inlay, the UHF path

is an open multiple folded dipole, printed only on one side. During foil transportation, the foil charges itself to high electrostatic voltage. While the LF antenna is grounded through its backside, the UHF antenna takes the full charge, provoking new and unusual discharge paths through the device.

2 New ESD scenarios

To resolve the problem, dual-band RFIDs have been designed within one chip, which needs to be connected by two pads to the LF coil antenna and further two pads to the UHF antenna. The chip is connected in a flip process to these two antennas, which are printed (usually in aluminum) onto a thin foil inlay to be processed later into a foil stack, which becomes hot laminated to credit card thickness and thereafter cutted accordingly.

In the assembly process, the antenna carrier foil has a width of about half a meter or more and is unrolled under defined conditions to the assembly point (Figure 1). This unrolling generates significant electrostatic charging. Without useful countermeasures, the foil charges up to 2-digit kilovolts [1]. At the placement point, the foil is stopped and supported by a conductive or (sometimes) electrostatic dissipative plate underneath the foil. Due to the backside line, the LF coil antenna is grounded while the open dipole became highly charged during the foil movement. Since the UHF dipole on the thin foil surface becomes highly charged, the LF antenna is grounded via the backside. The related discharge takes place at the moment when the chip is placed.

Figure 1: Unrolling the antenna inlay foil, which enters through the slit on the right hand side into the assembly chamber. The foil is highly charged at the assembly point, if no countermeasures are made.

2.1 Discharge paths when placing the RFID chip onto the antenna foil

The following discharge scenarios have been observed, depending on the support plate as well as from the nozzle type (Figure 2 - 5):

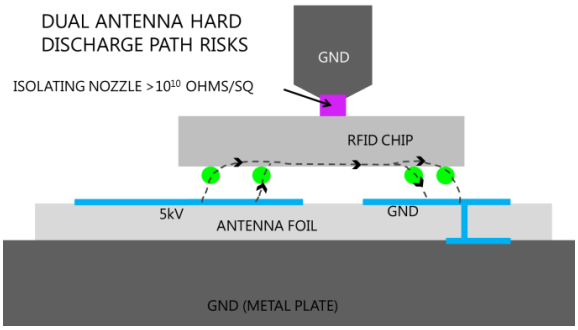

Figure 2: The UHF-antenna (left) is highly charged and forms a capacitor to the grounded metal support. This capacitor suffers discharging through the chip and the (grounded) RF-antenna. The green balls are the solder balls or glue connects or welding bumps (depending on the technology), by which the RFID-chip is connected in a flipped manner to the antenna. Since in this scenario, the picker head (nozzle) is made from isolating rubber, it will not contribute to the discharge path. In many cases the discharge path includes surface metal lines and, such, bypasses ESD pad protective ciruits, which usually discharge into silicon substrate. Active circuitry within the device is highly at risk. Although this discharge scenario looks somehow similar to the human body model (HBM) discharge, it is a different one: no re-resistor reduces the current flow, when discharging the capacitor in a hard manner, which stores more energy than a person's body surface capacitance. The outstanding high voltage (without countermeasures, even more than 10 kV can be reached at this process step!) allows to punch through interlevel dielectrics between metal layers and to severely generate damage throughout the whole vertical device structure.

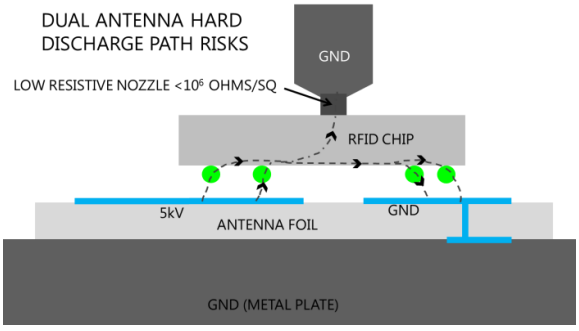

Figure 3: When a low-resistive rubber nozzle is used, a part of the voltage is discharged through the silicon substrate, where the ESD pad protective structures help bypassing sensitive circuitry. However, due to the low-resistive nozzle type, it is still a dangerous hard discharge scenario.

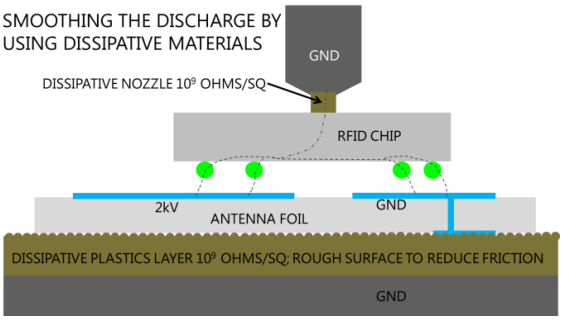

Figure 4: In this case, the nozzle is made from high-ohmic dissipative (about 10^9 Ohms/sq) rubber and the support includes a surface layer (>2 mm) of dissipative plastics. By this, the discharge is smoothed to very low current in order to avoid damaging the device.

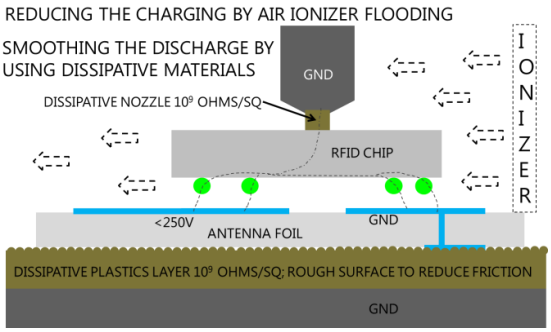

Figure 5: In addition to the scenario of Figure 4, the process chamber is flooded with ionized air, which makes the discharge very smooth and starts it already long before the device approaches to critical sparking distance to the antenna foil. Only very small charge remains in that case, being uncritical for the chip.

RFID chips need only each two terminal pads per band (RF respectively UHF). However, looking at an RFID chip, often more than two pads (resp. four pads in case of dual-band chips) can be seen when inspecting the device. These pads are normally for wafer-level-testing purpose: e.g. to bypass the internal voltage regulation or to access specific test points within the circuitry. Or, they are just connected to a chip-top-metal pad without further connection to the internal circuitry. These pads, as well as sometimes test pads may be used to serve as additional fixation points of the chip onto the foil. However, these pads also open additional discharge paths, accordingly to the scenarios described in Figure 2 - 5. For instance, a pad without internal connection to the circuitry may become a target to ESDFOS damage [2] by sparking through the interlevel dielectrics into the circuitry underneath. Therefore, support pads should best be directly connected to the substrate, such helping to bypass potential discharge paths through the circuitry. In some machines, hard plastic baseplates were mounted in the assembly chamber, where the chip is placed onto the antenna. In these cases, the discharge path to ground via the antenna was blocked; however, the voltage measured on the antenna reached a 2-digit kV order-of-magnitude.

3 Process machine ESD risk evaluation and debug

3.1 Brief process description

The tool debug and improvements were made on a Mühlbauer 15000 inlay production system (Figure 5). Since from tool manufacturer side, no useful ESD precautions were installed, significant yield drops between 7% and 30% have been reported by the machine user, who asked for engineering support. The machine setup construction takes the bare die from the diced wafer on a framed sticky blue tape. For the chip picking from the foil, a black dissipative nozzle has been used and this nozzle hands over the chip to another – isolating – nozzle, which puts it from the backside. This nozzle lands the device onto the antenna foil in a flipped manner (frontside down, connecting to the antenna pads).

Figure 6: Mühlbauer 15000 system

3.2 ESD Risks and Countermeasures

In principle, three main steps of the process on the machine include ESD risks, see also [3]:

a) picking the die from the blue foil
b) handover the die from the picker nozzle to the placement nozzle
c) placing the die onto the antenna foil

In details, the charging situations in these three steps present themselves as following:

In step a), every time when a die is picked from the blue foil, the foil with the remaining dies on it will be charged a little bit more. Remaining silicon dust from wafer sawing sometimes connects some chips to “charge clusters” [4]. In whole, if no countermeasures are taken, the foil may reach a potential of some kV. When the next chip is picked by a grounded or low-ohmic-dissipative nozzle, a risk of surface discharge (ESDFOS) from charged dies into the nozzle may appear. Since the capacitance behind such

discharge is between the surface capacitance of a single die and an unknown number of (via silicon dust) connected dies, this discharge is not limited to a just "one-single-die" CDM-like discharge. Therefore, at this point, it is important to continuously avoid the slowly (with the number of picked dies) increasing charging of the foil during the whole picking process. This can be achieved best by a continuous air flow of ionized air by an ionizer fan, directed to the foil surface. This air ionizer has been found on some – but not all – Mühlbauer machines of the 15000 series, although it should be mandatory here.

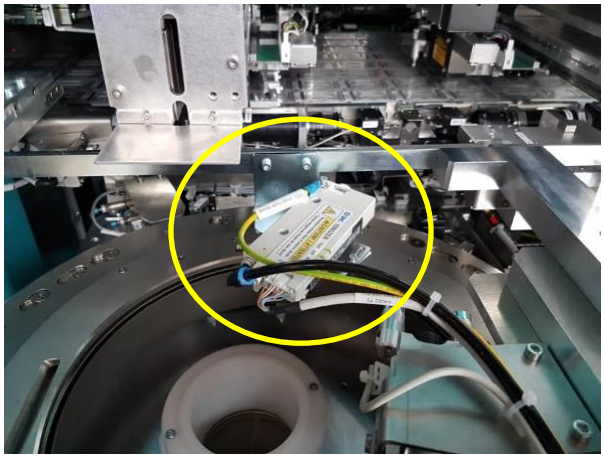

Figure 7: Die picking station, here with air ionizer.

Considering the picker nozzle, it should be dissipative in order to avoid a charging of the single die during picking. When picking the die from the foil, electrostatic charging is generated just by the pull force needed to draw the die from the sticky blue tape. If an isolated nozzle is used (as delivered in the standard version without ESD protection), this charge would be taken at least to the handover point, where the placement nozzle (Figure 8) takes the chip from the backside.

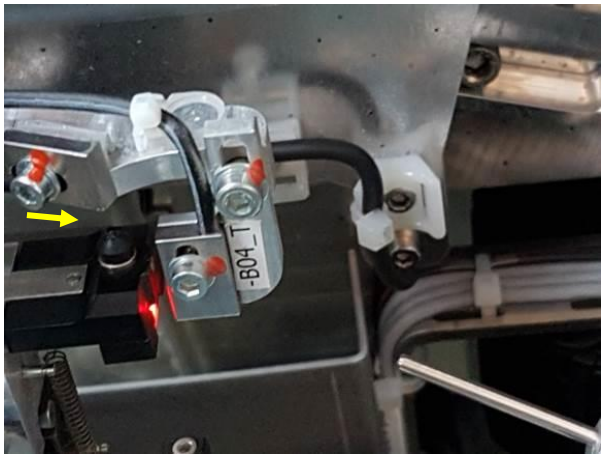

Figure 8: Picking nozzle to take the dies from the blue tape.

At this moment, we are at step b), the handover step. For the placement, in standard versions, a white isolating nozzle is used. The potential risk of this step is that the nozzle might have been charged from previous placement (contact electricity) and transfers this charge to the device to be handed over from the picker nozzle (and through the chip surface – ESDFOS – via picker nozzle to ground). Although the energies to be transferred could be assumed rather low, in general devices with very high sensitivity might suffer damage or reduction in lifetime (e.g. LEDs). The question, why no dissipative material is used for the placement nozzle, has been replied with the reason that dissipative nozzles would be too soft for the placement process. However, this response couldn't convince, since a variety of dissipative plastics and rubbers are available, especially constructed for such placing nozzles.

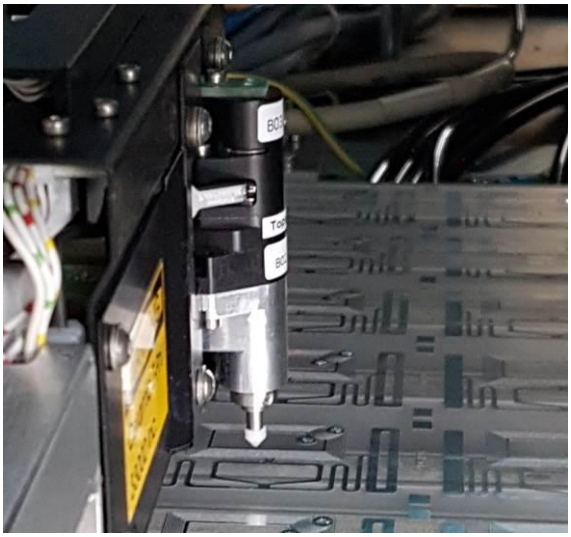

Figure 9: Placement unit with non-dissipative nozzle; no ionizer in place, although it should be at this process step.

The by far most critical step c) is the placement of the die onto the antenna (Figure 9). Ideally, all participating parts should be at earth potential respectively discharged. However, in practice, huge potential differences were measured.

The main contributor and ESD-risk is given by the antenna carrier foil, as already described in detail in chapter 2. Considering the foil-transport and -discharge scenario, the support material in this section plays a decisive role. Looking at the two extreme situations, metal vs. plastic support, the result is as following: When using a grounded metal support, the foil still suffers charging by friction when it is moved. However, due to the small foil thickness, the charging voltage is limited. On the other hand, such setup forms a

perfect high-capacitance foil capacitor between the UHF dipole antenna (not grounded) and the support, which is connected to the HF coil antenna. This low ESR (electrical series resistance)-capacitor is discharged with its full power at the very moment when the chip is placed. The discharge path is UHF antenna – UHF antenna pad – chip – HF antenna pad – HF antenna (=ground).

Replacing the metal support by a non-dissipative plastic support will convert the capacitor in a nearly pure conductive capacitance, determined by the overall surface of the HF- and UHF antenna. Also the HF antenna would not be grounded. And the ESR of this capacitor would be nearly infinite. However, in such case, the charging potential is more or less only limited by surface corona discharge from plastics. With such setup, usually up to 2-digit kV charging can easily be reached to which many chip-internal ESD protections cannot cope with.

Therefore, the – materials-point-of-view – best solution is provided by a high-resistive support plate. Like in case of the metal support, this setup will form a capacitor, however, now with a very high ESR, which limits the discharge current significantly. Figure 10 shows the replacement of a metal frame bar prior to curing by a dissipative version.

Figure 10: Inlay support conversion from metal (left) to a dissipative version (right).

Experiments by covering the metal supports by paper in order to reduce the risk of hard discharge improved the output yield but cannot be considered as a permanent solution. Figure 11 shows such an approach. Figure 12 shows the new indexer plate made from dissipative material, which gave very good results in yield.

Besides the placements section, we need to do a careful reviewing of the numerous rollers in the whole equipment setup. Certainly, it can be accepted that the foil charges as long as the antenna is not connected to the ESDS. However,

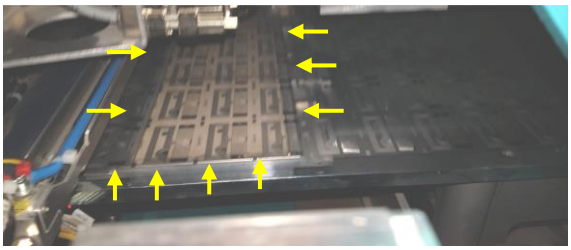

Figure 11: Vacuum tube support Al-blocks which can be proven to be the root cause for hard discharges and low yield at position 3 and 5 of a 6x inlay matrix. Covering them with paper tape/masking tape improves the yield on these positions, but a hard discharge path remains due to the Al-frame (yellow arrows) of the die placement vacuum support plate under the inlay.

Figure 12: The improved indexer plate – frame out of dissipative material – gave already very good results in the trial runs – no main failing position (3 and 5 for 6x antenna matrix) any more.

before reaching the die placement point, such setup needs to be discharged, for instance by an air ionizer. In principle, this would be a good solution, but can it cope with the high process speed and throughput? Unfortunately, frequently, the answer is “no”. First, we need to do some considerations about the carrier foil and the use of air ionizer bars: As long as the foil suffers friction electricity by transportation, the use of ionizers is always a critical issue. If we consider a transportation roller, at which the charge separation takes place, the ionizer will be directed to a point after this charge separation, so that at this point, in fact, the charge will be neutralized. Unfortunately, the more distance the foil gains from this neutralization point by ongoing transportation, the more the voltage will increase again. This effect is well known as the “capacitor effect”, where a plate capacitor, once charged to a charge Q, increases in voltage by just increasing the distance of the capacitor plates. Thus, when working with ionizers in such setup, the ionizers need a self-control feedback sensor (which checks the voltage exactly at the point where the die placement will take place). The sensor itself controls the needle high-voltage power supply of the ionizer, so that the ionizer voltage is automatically adjusted in a manner where the antennas, printed on the foil, are completely neutralized at the die placement point. Besides

this aspect, ionizer types need to be carefully selected, since it has been observed that some types even acted as a charging instrument to the antenna foil, especially if the roller is not coated by dissipative material.

However, we must not forget that such solutions may drift in voltage, are expensive and need a continuous ESD-coordinator survey on effectiveness. In addition, the problem has been observed, that, if once an air ionizer has been correctly measured and adjusted, even small changes as humidity or antenna carrier foil change, may give completely deviating results. Therefore, we did additional experiments using grounded discharge brushes. In a first approach, we noted that the material of many discharge brushes is rather hard, so that the foil may suffer mechanical scratching. Smoother brushes are available and fulfil the requirements. However, the interesting point here is, that, following to the principles of a van-de-Graaff generator, the brushes don't need to touch the foil. A distance of about 5 mm is completely enough to reliably discharge the foil by corona discharge. Figure 13 shows such brushes, which are very useful in the process sections after the chip placement.

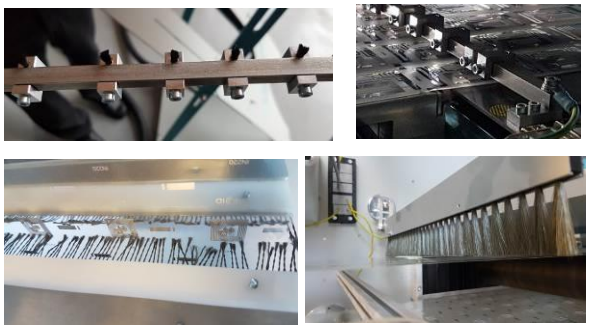

Figure 13: Soft dissipative brushes can be used both in a touching manner as well as non-touching corona dischargers. If the foil rollers are made from dissipative material, too, most air ionizers can be replaced by brush solutions.

In both air ionizer and brush solutions, it is very important to do it from both sides or, where not possible by cylinder rolls, to coat them with dissipative material.

In sum, we noted that the charge cannot be completely removed, but by a combination of precautions, it can be suppressed in the placement point to an acceptable level. Figure 14 shows the end section of the Mühlbauer 15000 machine in its old version (left image) with air ionizer and new version (right image) with new dissipative rollers and brushes.

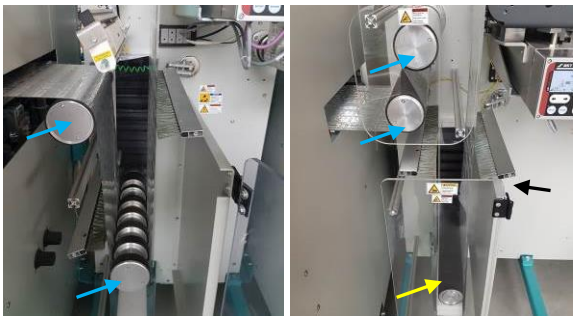

Figure 14: Blue arrows = old wheels, yellow arrow = new wheel construction with internal brushes to guarantee earth connection, black arrow = new soft dissipative brushes which can be used contactless as long as the distance to the surface to be discharged is < 3 mm.

3.3 Antenna layout precautions

Besides the assembly equipment aspects, additional ESD precautions can be done with respect to the antenna design and the chip robustness. Considering the antenna design, a significant improvement would be given by one of the following improvements:

a) Design a dummy hole into the UHF antenna, so that also the UHF antenna has a small contacted metal piece at the baseplate side of the foil. This will cause discharging of the UHF antenna, too, if a dissipative support plate is used.

b) Provide a dummy connect on the foil between the HF and the UHF antenna. However, this dummy connection needs to be designed in a high-frequency compatible manner in order to avoid restrictions in the RFID functionality. An alternative could be to design this connect in a manner that it is located outside the later card format, so that it disconnects itself in subsequent cutting/ stamping process steps.

Looking to the chip itself, a careful evaluation of "undesired functions" of pads, just serving as mechanical supports, should be mandatory: frequently, test pads to access unregulated voltages or other functions used at wafer level testing, are re-used in the assembly as mechanical supports, without considering their potential role as possible entries for ESD.
Finally, facing the assembly of bare dies to a triboelectric foil, in general, a high level of ESD robustness of the chip itself would be desirable. In order to cope with the special discharge scenarios in such assembly process, we need to better understand ESD pulses in the placement section, since they are not reproducible by the "classic" discharge models. Within our team, this was the part of the colleagues from Fraunhofer EMFT.

4 Investigation of potential ESD scenarios and hypothesis of failure mechanisms during the assembly

4.1 Introduction

The third part of our paper investigates potential ESD-scenarios and hypothesis of failure mechanism during the flip chip assembly of two frequency RFID inlays. In a first approach, Very-Fast Transmission-Line Pulsing (VF-TLP) [6] was used to stress the bare die. However, a gap of correlation was observed regarding the failure signatures which occurred in the assembly line. In order to consider the stress current path of the antennas, we therefore measured corresponding current transients by performing CDM tests directly on the antenna traces of the flex. Besides a deeper insight into the ESD-event itself, our findings provide required information for ESD-relevant countermeasures as already described in detail in section 3.3 (Antenna layout precautions).

4.2 Potential ESD scenarios and ESD-related countermeasures

This section deals with potential ESD scenarios that can take place in a flip chip assembly line and highlights the corresponding failure mechanism.

4.2.1 Flip chip die attach

a) The charging mechanism

An ESD-event during the flip chip die attach is the main subject of our investigations. The hypothesis of failure mechanism is the following: By means of the repetitive pick-and-place sequence, charges are separated caused by the triboelectric effect and parts of the system may accumulate charges like a Van de Graaff generator. The chip may charge up through contact with the isolated pick-and-place nozzles during it is picked up and passed over. Caused by friction electricity due to unwinding, transportation and incorrectly adjusted air ionizer (see section 3.2 ESD Risks and Countermeasures), the foil as well as the printed traces of two antennas can be charged on different electrical potentials.

b) Discharge between antenna and chip

The charged chip is placed between the four antenna pads (two pads on each of the two antennas). In the microsecond range, the antenna pads are connected with their respective pads on the chip at the same time. In the CDM domain, the time domain in which ESD is occurring (nanoseconds), one antenna pad contacts first. Assuming that the capacitance of the antenna is large enough, the chip discharges into the antenna. The resulting ESD event can be described by the Charged Device Model (CDM). In its worst-case scenario, the corresponding antenna owns a double-sided metallization connected through a via and is placed on a grounded metal layer. Therefore, the chip assembly should take place on a dissipative underground. The usage of dissipative pick-and-place nozzles can be used to prevent the charging of the chip. Both air ionizer and brush solutions can neutralize accumulations of charges on the system.

Alternatively, the metallization of the antenna that is contacted first can be charged. Due to charge balancing of electrostatics loads and dependent on the chip capacitance, the chip could be stressed through the one antenna pad that contacts first. To prevent this ESD-event, a complete discharge of both antennas before the die attach is necessary.

c) Capacitive compensation currents between the antennas through the chip

A third possible ESD-mechanism could be the following: During the assembly, the chip connects the antennas by one pad on one side and one or two pads on the other side (two pads on both sides should not be possible due to consecutive contacting in the CDM-domain). If both antennas are on a different electrical potential, a discharge current will flow through the chip. As a countermeasure, both antennas have to be discharged or at an equal potential during the chip assembly.

4.2.2 Hard grounding of a double-sided metallized inlay

The chip assembly on the foil is followed by the process of final epoxy curing, testing and marking of bad units, cutting and winding of the foil. Since the foil is permanently exposed to friction electricity during transportation through the assembly line, the charging of the foil and its antennas is hardly to prevent. If the metallization of a double-sided antenna is grounded due to a material change of the underlying supporter, a hard discharge of the capacitance of the other antenna via both pads through the IC to the grounded antenna via both pads may occur. The covering of the metal as a measure against the hard grounding is described in 3.3 Antenna layout precautions.

4.2.3 Summary of potential ESD scenarios

Table 1 classifies the potential ESD failure scenarios in the assembly line. It shows the possibility of a discharge scenario through each combination of the two antenna pads on both sides. If the capacitances of both antennas are high enough, the stress current is mainly determined by the current path of the discharged antenna and by its number of involved antenna pads. This means that the scenarios can be divided into discharges of the antenna via one or two pads.

Failure scenario	Current Discharge Path
4.2.1 Flip chip die attach	b) IC ⇄ (1)Antenna
	c) Antenna(x) → IC→ (y)Antenna x = 1 ⇒ y ∈ {1,2}; x = 2 ⇒ y = 1
4.2.2 Hard grounding of one antenna	Antenna(2) → IC → (2)Antenna (Gnd)

Table 1: Possible ESD failure scenarios of two frequency RFID inlays in the flip chip assembly line. The number in brackets denote the number of involved antenna pads.

4.3 VF-TLP on bare die

As first approach, VF-TLP (5 ns pulse width) on the bare die was performed as it characterizes the capacitive discharge of one antenna via one pad through the chip to one specific pad of the other antenna. For discharges via more than one antenna pad per side, each discharge path can be investigated separately. Figure 15 shows an exemplary VF-TLP current transient.

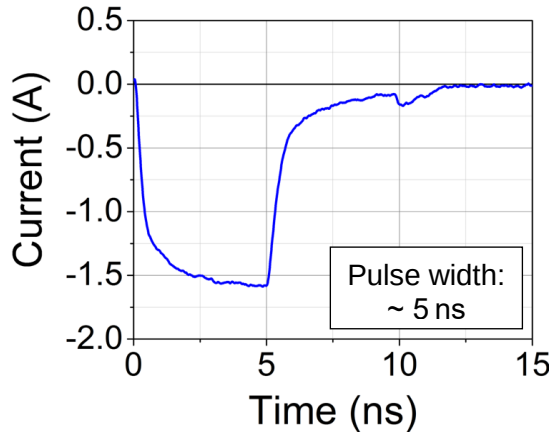

Figure 15: Current transient of VF-TLP on bare die.

However, the performed VF-TLP tests were not able to address the failures signature observed in the assembly line. Thus, it was necessary to investigate the occurring discharge waveforms in more detail.

4.4 CDM on flex

4.4.1 Test setup

The following section describes the emulation of the potential ESD-scenarios (Table 1) by CDM testing on flex referring to Figure 16. The RFID inlay can be regarded as a Chip-on-Flex (COF) assembly, which contains a very large scale package exceeding the size of the Ground Plane (GP) in CDM [7]. To measure the discharge current of the dipole antenna capacitance (green arrows) via two pads through the IC, the CDM stress of one coil antenna pad (☆) is measured while the rest of the coil antenna is removed (red area). For the investigation of the antenna discharge via one pad, one of the dipole antenna pad has to be cut (dashed blue line).

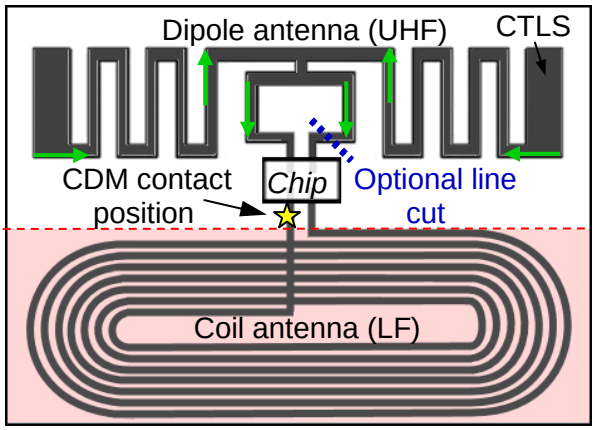

Figure 16: Exemplary schematic of a dual frequency RFID inlay with a multiple-folded open dipole (top) and a coil antenna (bottom). The discharge of the capacitance of the dipole antenna via two pads is measured by performing CDM on a coil antenna pad (☆), while the rest of the coil antenna is cut (red area).

4.4.2 Waveform analysis

Figure 17 and Figure 18 show the CDM waveforms for the discharge of the dipole and coil antenna capacitance via one and two antenna pads through the chip. It was measured under test condition TC 125 of ANSI/ESDA/JEDEC JS-002-2014 [8] by a 33 GHz oscilloscope. The "pulse width" of the main stress by discharging the capacitance of the dipole (~1.5 ns) and coil antenna (<1.0 ns) is much shorter than the previously applied VF-TLP stress pulses (~5 ns) (Figure 15). This is most probably the reason why

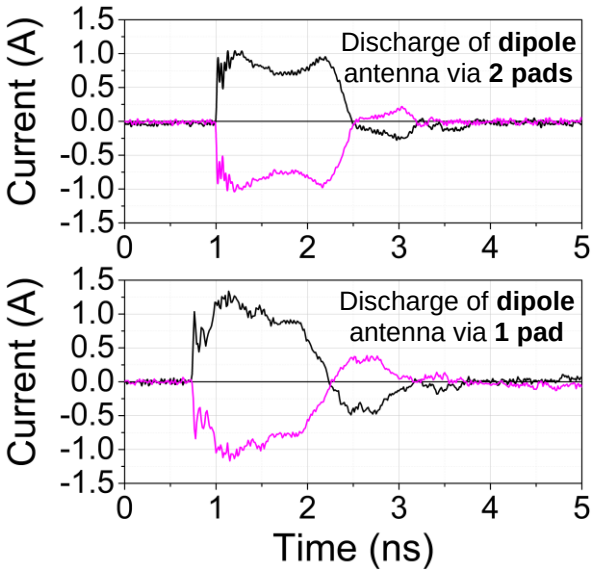

Figure 17: CDM stress of one coil antenna pad, discharging the capacitance of the dipole antenna via both pads (top) and via only one pad (bottom) through the chip under test condition TC 125 of ANSI/ESDA/ JEDEC JS-002-2014 [8]. The corresponding setups for the discharge via two or one antenna pad are illustrated in Figure 16 without or with the optional line cut.

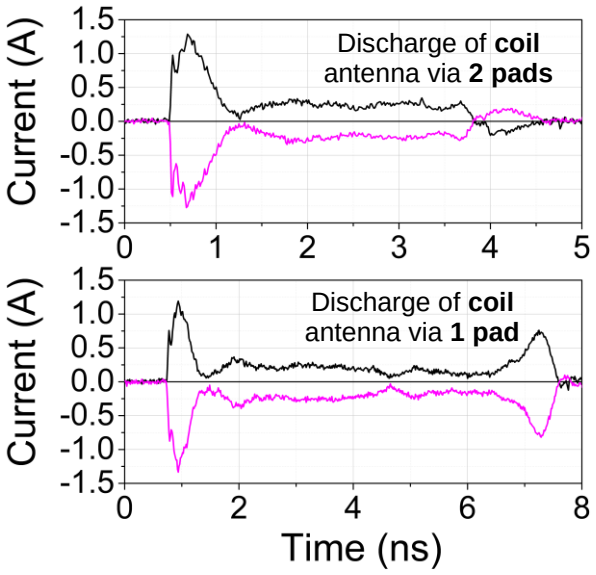

Figure 18: CDM stress of one dipole antenna pad, discharging the capacitance of the coil antenna via both pads (top) and only via one pad (bottom) through the chip under test condition TC 125 of ANSI/ESDA/ JEDEC JS-002-2014 [8].

the VF-TLP pulses have not addressed the observed failure signatures after the assembly. Besides the typical first peak of the CDM stress current transient, a second one is appearing at the end of the current waveform. In the case of the coil antenna discharge via one pad (Figure 18, bottom), this arises from the capacitances of the two contact pads which are placed close to the antenna pads (left out in Figure 16 to simplify the schematic). The charge stored in the contact pad capacitance which is cut from the chip has to propagate through the whole coil antenna in the beginning of the pulse. This is the reason why the coil discharge via one pad (Figure 18, bottom) is around two times longer than via two pads (Figure 18, top). For the coil antenna discharge via two antenna pads, the second peak vanishes as both contact pad capacities discharge directly via the two antenna pads through the chip to the pogo pin. In the case of the dipole antenna discharge, the second peak occurs due to "Capacitive tip loading structures" (CTLS) (Figure 16). Because the capacitance and the size of the antenna are inversely proportional to the resonant frequency, CTLS are used to reduce the size of dipole antennas for a given resonant frequency [9].

The short "pulse width", together with the short rise time and double peak structure of the stress current imposes high demands on the ESD protection structures on chip.

4.4.3 Capacitive coupling of the foil

As recommend in JS-002-2014 [8], the foil under test is held in place against the field plate by means of vacuum holes. Although the foil is thus more flattened, arched areas especially between the vacuum holes exist. The foil tension makes it very difficult to create a uniform flattening of the entire foil, even by attaching the foil ends with adhesive tape. We found that the magnitude of the second peak current strongly depends on the capacitive coupling of the CTLS. For illustration, the waveforms for the discharge of a half dipole antenna (a) with a flattened CTLS placed directly above a vacuum hole, (b) with an arched CTLS and (c) without CTLS (cut off) are demonstrated in Figure 19.

A stronger capacitive coupling of the CTLS results in a stronger magnitude of the second peak current of the double-peak dipole discharge waveform via two pads. Accordingly, the worst-case scenario would occur for the strongest capacitive coupling of the whole foil. To simulate this worst-case scenario in the CDM test, the dielectric FR4 plate is removed and the foil is placed on the insulating surface coating of the metal chuck. Thus, the peak current of the resulting waveform (Figure 20) almost doubles compared to the current waveform with the dielectric FR4 plate between chuck and foil (Figure 17, top).

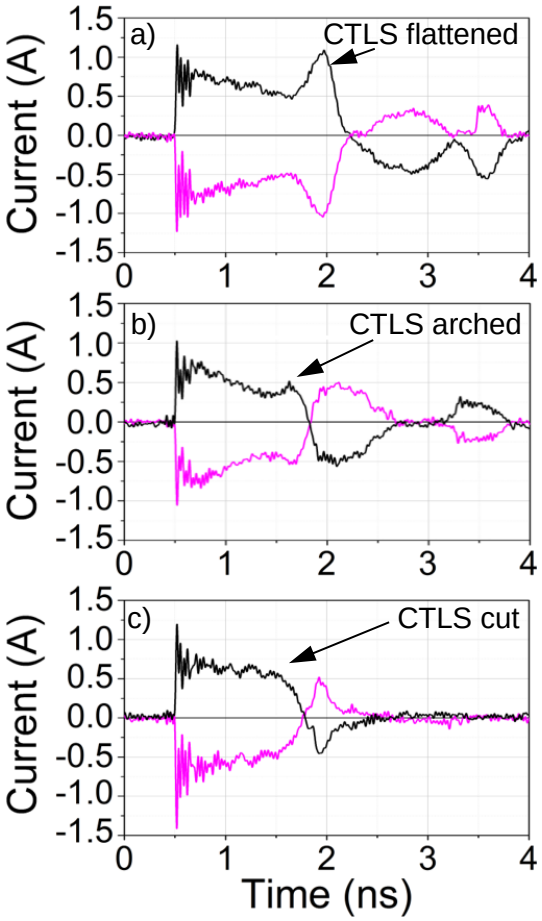

Figure 19: Current waveforms of the discharge of a half dipole antenna for different curvatures of the "Capacitive tip loading structure" (CTLS) (Figure 16) measured under test condition TC 125 of ANSI/ESDA/ JEDEC JS-002-2014 [8].

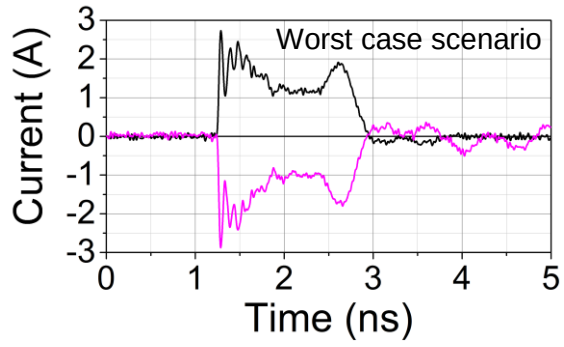

Figure 20: Worst-case scenario of the dipole antenna discharge via both pads through the chip by placing the foil on the insulating surface coating of the metal chuck. Apart from the lack of the dielectric FR4 plate, the test is performed under test condition TC 125 of ANSI/ESDA/ JEDEC JS-002-2014 [8].

However, if the capacitive coupling of the foil only increases after it is already charged, the voltage as well as the discharge current will be suppressed (V=Q/C). Thus, this scenario will not correspond to the worst-case scenario discussed before.

4.5 Outlook

By means of CDM testing on flex, we analyzed the discharge waveforms of the antennas and gained new information about their short "pulse widths" and double-peak characteristics. The results suggest that the pulse widths of previous VF-TLP tests have been probably too long to address the observed failures after assembly. This offers to repeat VF-TLP with a lower pulse width as it would provide a transient evaluation of the ESD protection performance. In this context, the influence of the second peak current magnitude on the current failure threshold could be examined. In order to verify that the CDM and VF-TLP measurements on flex induce the same failures as those which were observed in the assembly line, a physical failure analysis is required.

It could also be beneficial to investigate the antenna discharges by means of Capacitively Coupled Transmission Line Pulsing (CC-TLP) [11]. It is a contact-mode test method and combines the narrow-pulse high current stress pulses known from CDM with the reproducibility of VF-TLP, by directly connecting only one spot of the antenna. CC-TLP can also be used to determine the chip robustness on wafer level. To find pros and cons of the different test methods which can be used to characterize the ESD-behavior of a Chip-on-Flex (COF) assembly, a correlation study between these different test methods on the RFID inlay would be reasonable. In this course, ESD-critical parameters (e.g. charging of the foil, second peak current magnitude, pulse width) can be identified and different antenna and chip designs can be investigated.

5 Validation of countermeasures and periodic tool survey

It is mandatory to verify the success of countermeasures – not only after their implementation – but also periodically: electrostatic effects are strongly depending on materials and environmental conditions as humidity, temperature and degree of ionization of the air (ozone level). For validation, a specific measurement setup is needed [5]. For field strength measurements and simple order-of-magnitude- surface voltage measurement, an electrostatic field meter can be used. However, these meters usually provide voltage values, which can be erratic if the measurement distance is not correctly kept and the measurement subject is too small (from their measurement sensor, they

integrate the field through a virtual 90° cone towards the measurement surface). A better solution is to use either a distance-compensated contactless voltmeter, working with separate small probes, which allow a better physical approach to the position-of-interest. The measurement distance should not be more than 1cm in order not to overburden the distance compensation. However, such contactless voltmeters are limited to a range of 2-3 kV. A rather new approach are contacting electronic electrostatic voltmeter, which have a small ceramic tip to touch the surface of even very small subjects to be measured. In our case, the decisive voltages are measured on the antenna metallizations and on the chip surfaces, because their electrostatic potential difference at the point of "marriage" between chip and antenna is crucial considering the severity of discharge.

In general, electrostatic voltage differences between locations where a hard discharge can happen (marriage point) should not exceed 250 V [3], while in process sections before (where the foil is without chip), ESD cannot cause destruction of chips, so that charging is uncritical.

Considering the electric dissipation of materials, it can be measured best by using a small high-voltage bar-ohmmeter, giving the area-resistance in Ohms/square. These small handheld meters provide a range from $0\text{-}10^{12}$ displayed in a raw of LEDs (1 LED per order of magnitude). In order to avoid hard discharges into an electrostatic dissipative material, the best practice choice - besides existing standards - would be a material of about 10^9 Ohms resistance. If it is lower, the conductivity is too high and a risk of hard discharge of charged devices applies. If it is more than 10^9 Ohms, triboelectricity may apply, which means that the material can be charged by friction and keep the surface voltage for too long time.

A detailed instruction of all measurement locations, possible results and countermeasures on the tools would be beyond the scope of this paper but is included in the updated version of [3], previously available in November 2017 or, if needed before, it can be received from the authors directly.

Considering the antenna carrier foil, Empa is working at present on a foil characterisation tool. The foil – a sample of about 1,5 m length - is fixed at its ends between two fixing bars under a constant tension. A slide rail carries a moveable triple holder of three rollers, through which the foil is guided. This triple roller holder can be moved from one end of the test setup to the other (distance about 1 m). On this moveable holder, also variable/ adjustable settings for accessories as ionizer bars, corona brushes and voltage measurement probes are mounted. This setup allows a comparative characterisation of different foils with respect to their electrostatic behaviour.

6 Conclusion

New ESD mechanisms in Dual-band-RFID assembly processes create a dangerous ESD risk situation, consisting of a charged (dipole antenna) foil capacitor and a grounded coil antenna - with the ESD-sensitive RFID chip in-between. The risk of a hard discharge can be minimized, if dissipative materials are used for the baseplate where the chip is placed onto the antenna, if nozzles are made from dissipative rubber with enough space to metal parts and if a useful placement of discharge brushes and air ionizers is applied as described in detail in the paper in order to pre-discharge the setup at critical process-steps. With this, a significant yield enhancement has been achieved. Based on typical dual band antenna layouts and different tool setups, resulting ESD's have been reproduced and characterized in order to develop realistic testing scenarios which are not reproduced by existing ESD models. These test procedures serve to improve ESD robustness on RFID device design of ESD protection circuitries.

All tool-related countermeasures need a careful evaluation and continuous survey. The latest version of the ESD Forum e.V. guideline 1013 has been extended to a practical example of the foil processes described in this paper.

For optimization of ESD debugging considering the characterization of tool and carrier materials, a multi-use foil/ roller setup is under construction at present, which allows comparative electrostatic characterisation of carrier foils and tapes.

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