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Influence of Aluminum Compensation Effects in 4H-SiC on the Performance of VDMOS Transistors

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Al Compensation Effects in 4H-SiC

- Compensation of free charge carriers in Al implanted areas in SiC is a long known phenomena
- It may be dependent on implantation and annealing process as well as Al concentration [1, 2]
- This compensation effects can influence electrical characteristics like the sheet resistance of implanted layers [3]
- Here, the influence of compensation on electrical characteristics of SiC MOSFETs have been determined by adjustment of simulations to measurements

Experimental Setup

- Lateral and vertical MOSFET were fabricated on n-doped 4H-SiC Epilayer
- Implantation of N and Al (RT), post implant HT annealing @ 1700° C for 30 minutes (in Ar atmosphere)
- Gate oxidation in O_2 atmosphere (@1300° C) with post treatment in N_2 and NO (@1300° C) resulting in 51 nm gate oxide
- Measurement of transfer characteristic of lateral MOSFET and blocking characteristic of vertical MOSFET
- Comparison of simulation to measured characteristics

Simulation

- „Synopsis Sentaurus TCAD“ was used as a simulation tool, device structure was implemented with structure editor („SDE“) including implantation profiles created by process simulation (Fig.1)
- In addition, similar shaped, calculated N-profiles have been added to the structure to account for donor like compensation centers $N_{comp,D}$ in the Al-doped regions (Fig. 2)
- Transfer and Blocking characteristics were simulated with device simulation („sDevice“)

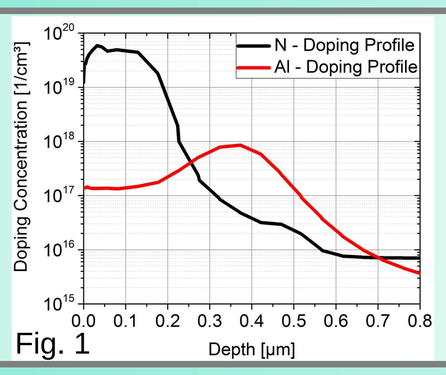

Fig. 1

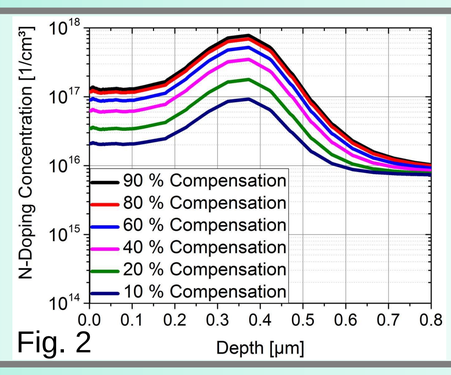

Fig. 2

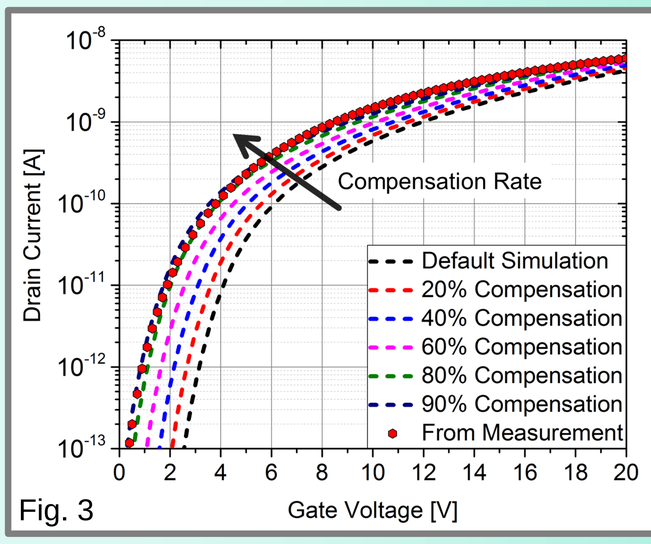

Fig. 3

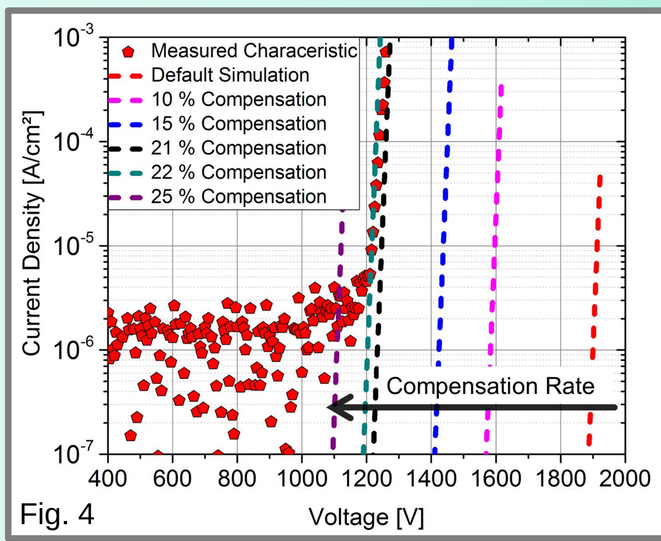

Fig. 4

Transfer Characteristic

- Physical properties at the SiO_2/SiC interface have to be taken into account for simulation of transfer characteristic (mobility degradation, interface states etc.) in the default simulation:
- Distribution of $\mathbf{D_{it}}$ have been implemented via a Gaussian distribution suggested by Hauk et al [4] and fitted to values evaluated by CV-measurement
- Fixed oxide charge $8 \cdot 10^{11}$ cm^{-3} and donor concentration at the interface have been added (evaluated by CV-measurement)
- Different N-profiles were added to account for donor-like compensation centers $N_{comp,D}$
- Simulated characteristics for different compensation factors and a measured one for comparison are shown in Fig. 3
- Best fit found at compensation values between **80 % and 90 %**
- It has been suggested that this shift comes from the presence of positive fixed charges at the SiO_2/SiC interface or by the presence of donor states located energetically close to the conduction band of SiC within the first 2 nm below the SiC-surface [5], in addition, it is proposed, that compensation effects have to be taken into account to achieve correct simulation results
- When gate voltage is applied, the depletion layer, in which drain source current flows, can reach deeper regions (where the influence of defects in the bulk SiC material, that act as charge carrier traps and extend the depletion layer, is stronger)

Blocking Characteristic

- Measured VDMOS blocking characteristic and associated simulation curves with different factors for compensation is depicted in Fig. 4
- In the default simulation, breakdown voltage is significantly higher than in the measured device
- Rapid increase of current can be explained by reach through effect [6]: the depletion region reaches through the p-well region of the VDMOS, before an avalanche breakdown occurs (dependent on the Al doping density in the p-well region as well as spacing of shielding region and n-drift region)
- Best fit of the simulation is achieved at compensation values around **22 %**
- Simulation characteristic is improved towards the measured breakdown voltage by 700 V
- Difference in compensation values for transfer and blocking because of different Al concentrations

Comparison to Previous Results

- The compensation factors found in this work match the values for compensation found by Weisse et al (Fig. 5) [2]
- Compared model takes different defect centers within the band gap into account to fit the neutrality equation and shows good agreement with hall-measurement over a wide range of temperatures [2]
- For the transfer characteristic, a lower $N_{comp,D}$ value would be expected, compared to the value determined at 10^{17} cm^{-3} from Weisse et al [2]
- This can be explained by the uncertainty of the exact properties of the N distribution at the SiC/SiO_2 interface that, in the simulation, can shift the transfer characteristic in a similar manner like $N_{comp,D}$ in the bulk SiC

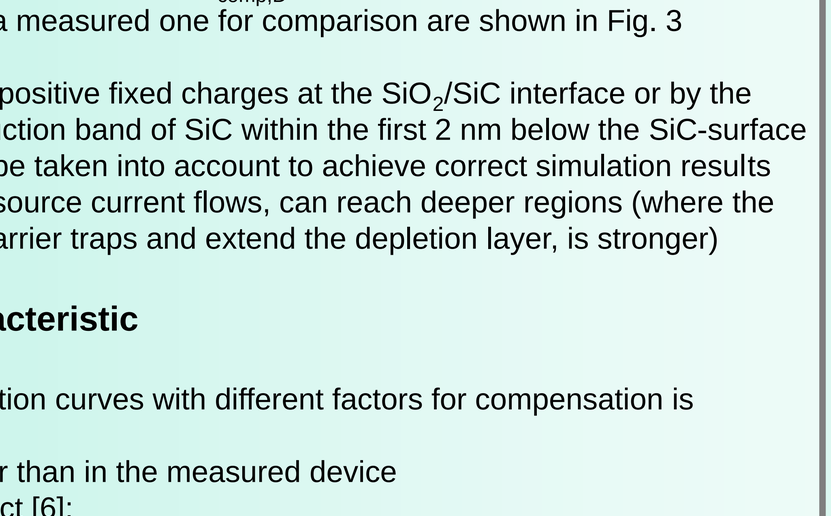

Fig. 5

Conclusion and Outlook

- The found compensation values were approx**. 80 %** in the surface near channel region with Al concentration of $1.5 \cdot 10^{17}$ cm^{-3}
- Compensation of approx. **23 %** in the deeper implanted shielding region (Al peak at $7.5 \cdot 10^{17}$ cm^{-3})
- The simulation results for blocking- and transfer-characteristic of 4H-SiC VDMOS can be significantly improved

References

- [1] M. Rambach et al, Phys.Stat.Sol.(b) 245, No. 7, pp. 1315-1326, 2008.
- [2] J. Weisse et al, Mat. Sci. F., 1662-9752, Vol.963, pp 433-436, 2018.
- [3] M. Kocher et al, Mat. Sci. F., Vol. 963, pp. 445-448, 2019.
- [4] M. Hauck et al, Communications Physics, Volume 2, Article number: 5, 2019.
- [5] V. Uhnevionak, Doctoral Thesis, “Simulation and Modeling of Silicon Carbide Devices”, urn:nbn:de:bvb:29-opus4-61975, 2015.
- [6] L. Zhao et al, DOI 10.1109/piers.2017.8262041, Prog. Electromag. Res. Symp., Spring (PIERS), St Petersburg, 2017.