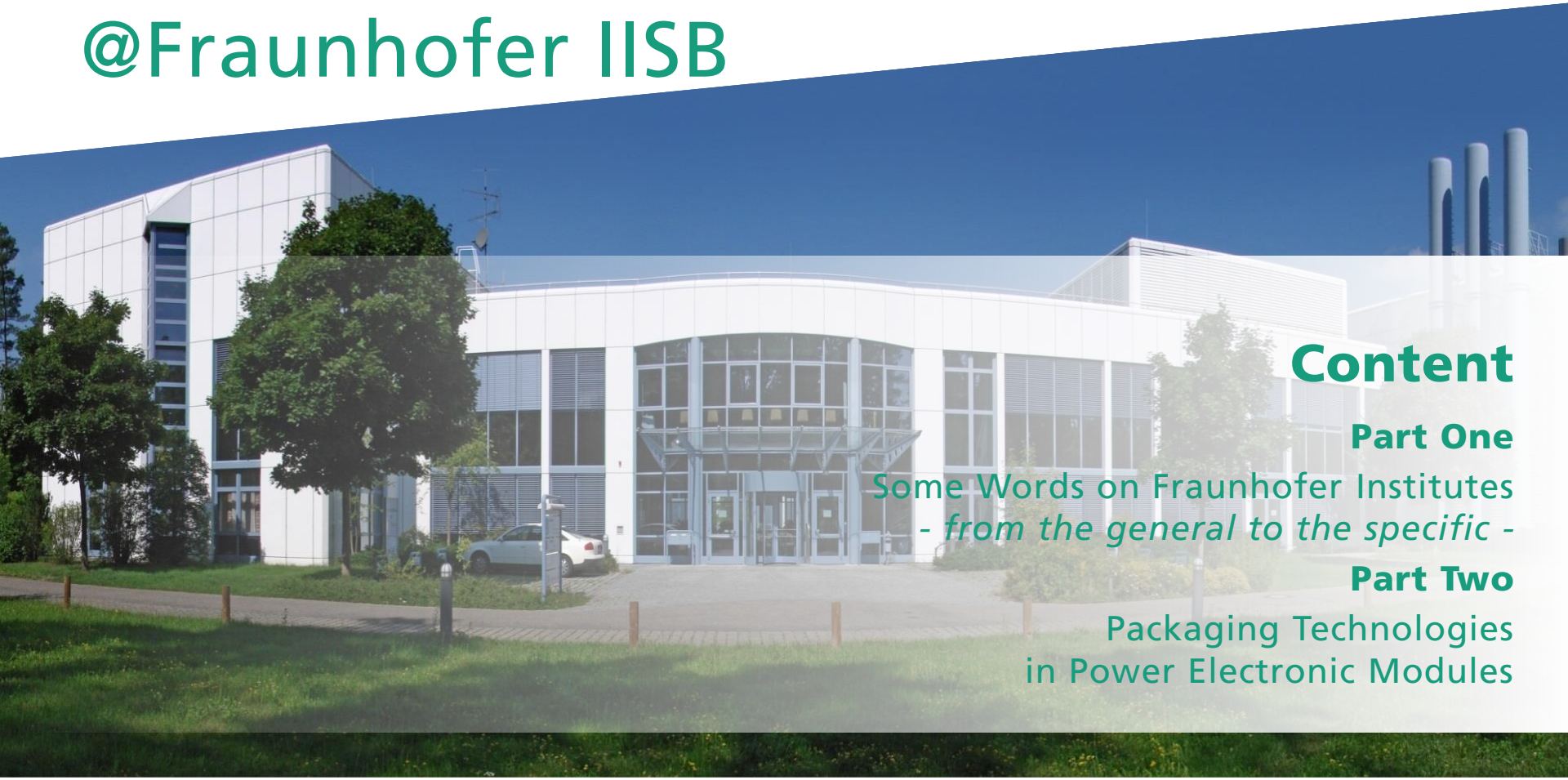
Packaging Technologies in Power Electronic Modules @Fraunhofer IISB



Content

Part One

Some Words on Fraunhofer Institutes
- from the general to the specific -

Part Two

Packaging Technologies
in Power Electronic Modules

Fraunhofer IISB

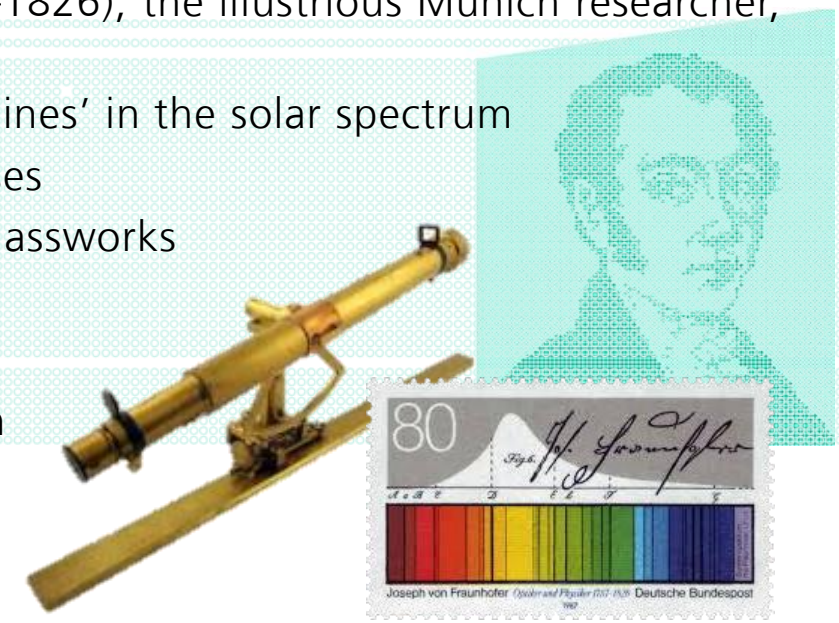
JOSEPH VON FRAUNHOFER
(1787 – 1826)

The **Fraunhofer-Gesellschaft** is a recognized non-profit organization that takes its name from '**Joseph von Fraunhofer**' (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

- **Researcher** – discovery of the 'Fraunhofer lines' in the solar spectrum
- **Inventor** – new processing method for lenses
- **Entrepreneur** – director and partner in a glassworks

- **Fraunhofer foundation in 1949**

  → from military to recent industrial research and engineering (today's staff 24,500)



Dr. Christoph F. Bayer et al., Packaging and Modules
Departement DEVICES AND RELIABILITY

Fraunhofer IISB

FRAUNHOFER GESELLSCHAFT

INSTITUTES AND RESEARCH ESTABLISHMENTS IN GERMANY

Fraunhofer Research Institutes

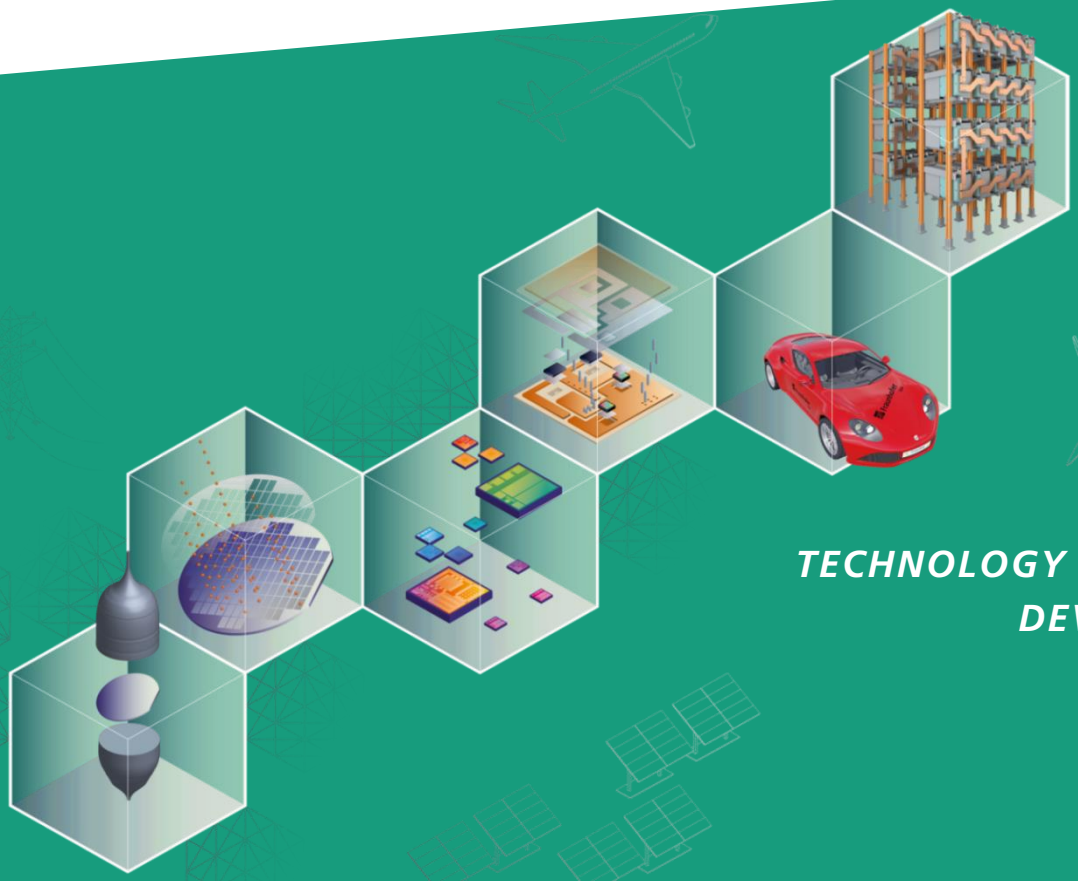
- Legal status: Non-profit association (e.V.)
- Mission: Application-oriented R&D
- 72 institutes with approx. 2.1 billion euros budget
- Through contract research 1.9 billion euros
- About 70 pct. of the Fraunhofer-Gesellschaft's contract research revenue comes from publicly financed research projects

Dr. Christoph F. Bayer et al., Packaging and Modules
Departement DEVICES AND RELIABILITY © Fraunhofer IISB

Fraunhofer IISB

POWER ELECTRONIC SYSTEMS

From Material to Power Electronic Applications

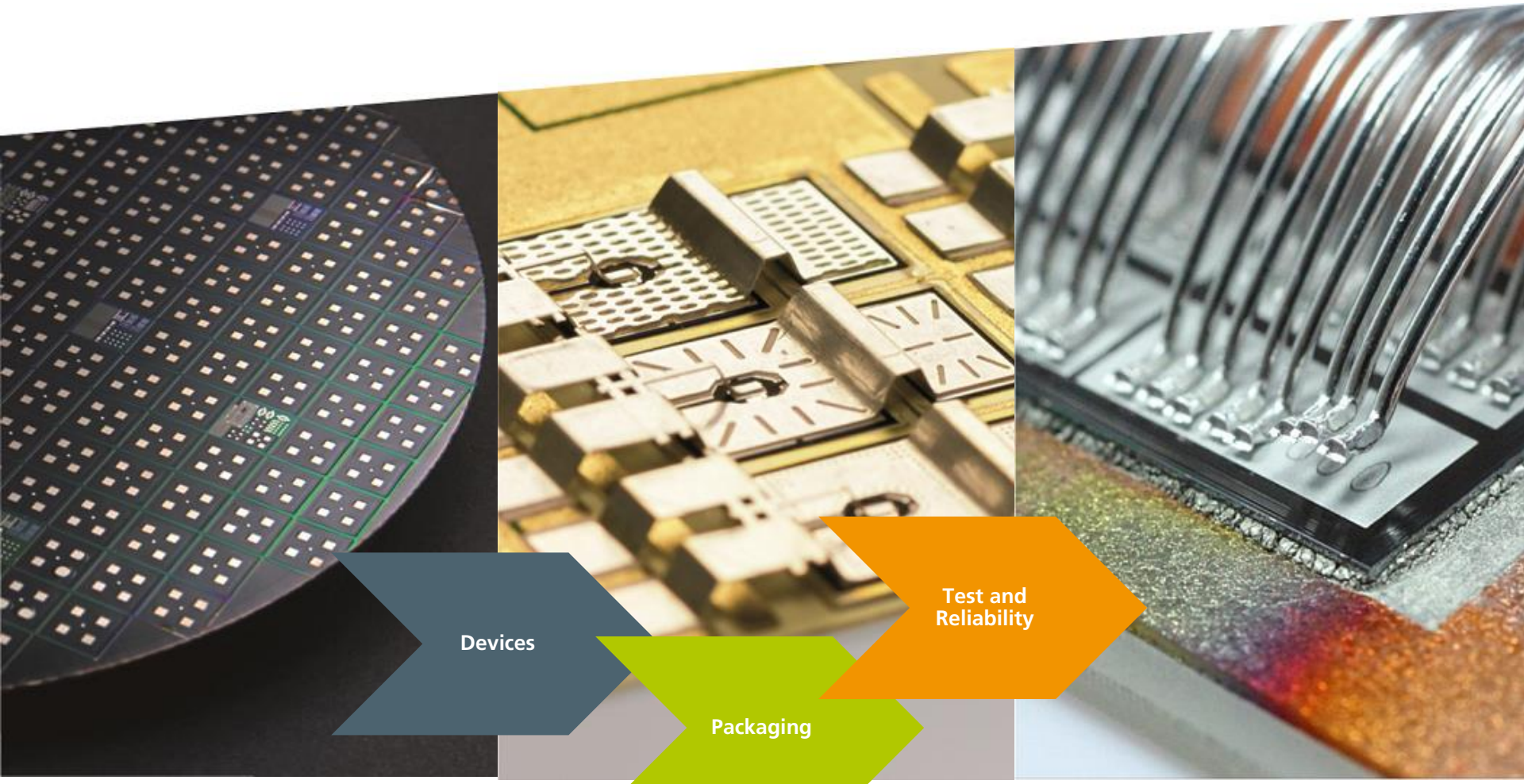


SIMULATION
MATERIALS
TECHNOLOGY AND MANUFACTURING
DEVICES AND RELIABILITY
VEHICLE ELECTRONICS
ENERGY ELECTRONICS

Dr. Christoph F. Bayer et al., Packaging and Modules
Departement DEVICES AND RELIABILITY

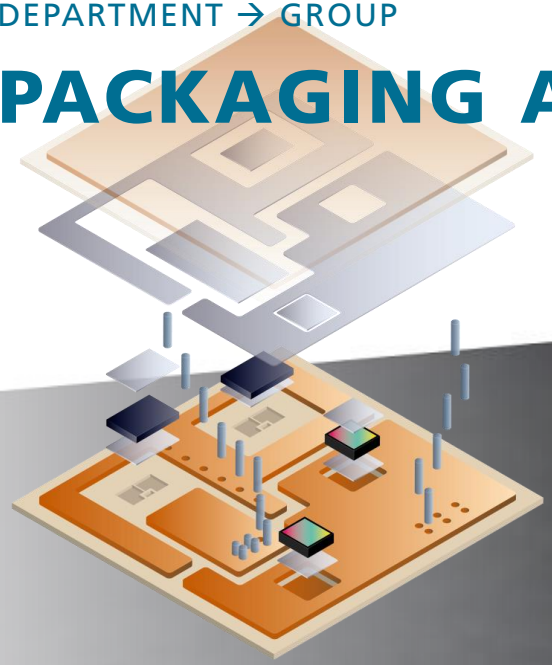
Fraunhofer IISB

DEVICES AND RELIABILITY



Fraunhofer IISB

PACKAGING AND MODULES



- New Concepts and Materials for Packaging
- High Performance Joining Technologies, Sintering
- Thermal, Electrical, and Mechanical Characterization
- Lifetime Characterization, Statistical Analysis
- Analysis of Failure Mechanism
- Lifetime Modeling

Packaging Technologies in Power Electronic Modules

- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - Packaging concepts
  - Interconnection technologies
  - Packaging at Fraunhofer IISB
  - Thermal design and insulation coordination
- Simulation process and theoretical consideration
- Test procedure and analysis
  - General
  - AQG 324 (LV 324)
- Test setups and parameters
- Summary

Packaging Technologies in Power Electronic Modules

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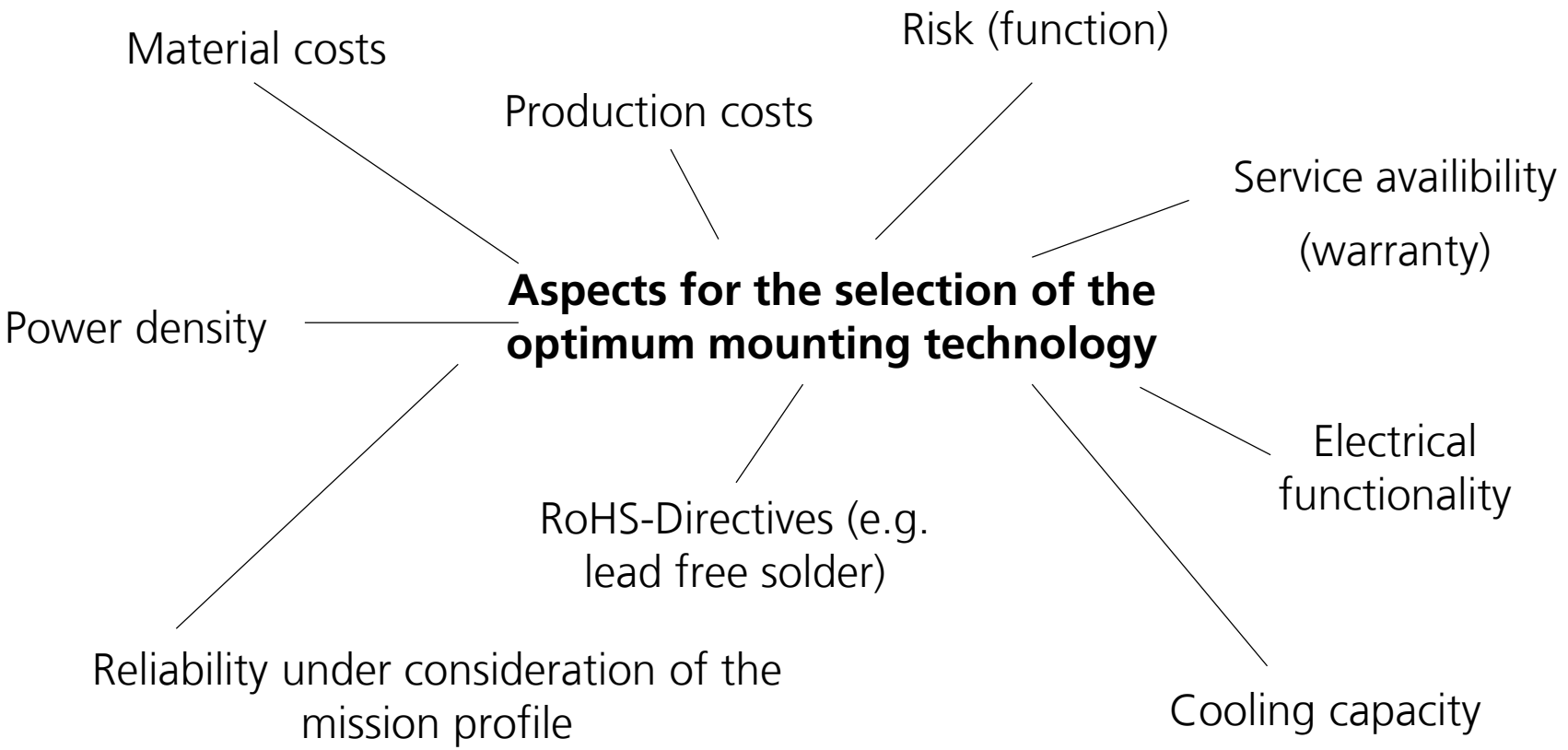
Packaging and interconnection technologies for power electronics

Basics and materials

- **What should be considered?**



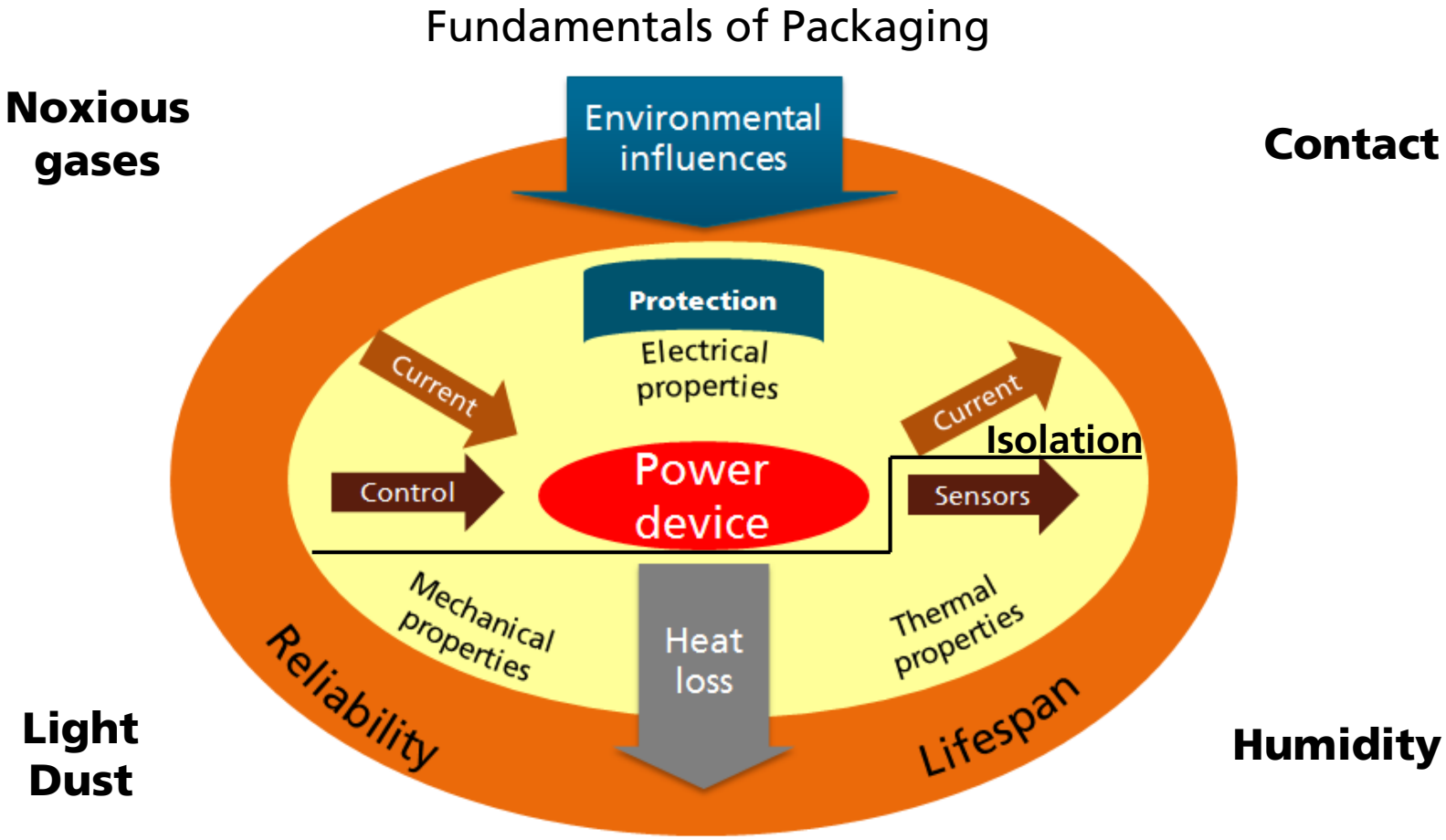
Packaging and interconnection technologies for power electronics

Basics and materials

Material costs	Production/process costs	Risk costs
Semiconductor (Diode, MOSFET, IGBT, etc.) **Die attach** (Solder, Sinterpaste, etc.) **Substrate/ circuit carriers** (PCB, DCB, IMS, etc.) **Bonding wires** (thin/thick wire, Cu, Al, etc.) **Heat sink, base plate** (Al, Cu, Graphite, etc.) **Housing**	**Machinery and equipment** (stencils, soldering adapters, bonding tool, etc.) **Employee** (preliminary tests, main tests, optimization, quality control, etc.)	**Failure** (malfunction after assembly, damage during assembly, pre-damaged components due to delivery, etc.) **Reserve** (backup stock of semiconductors, die attach, tools, etc.)

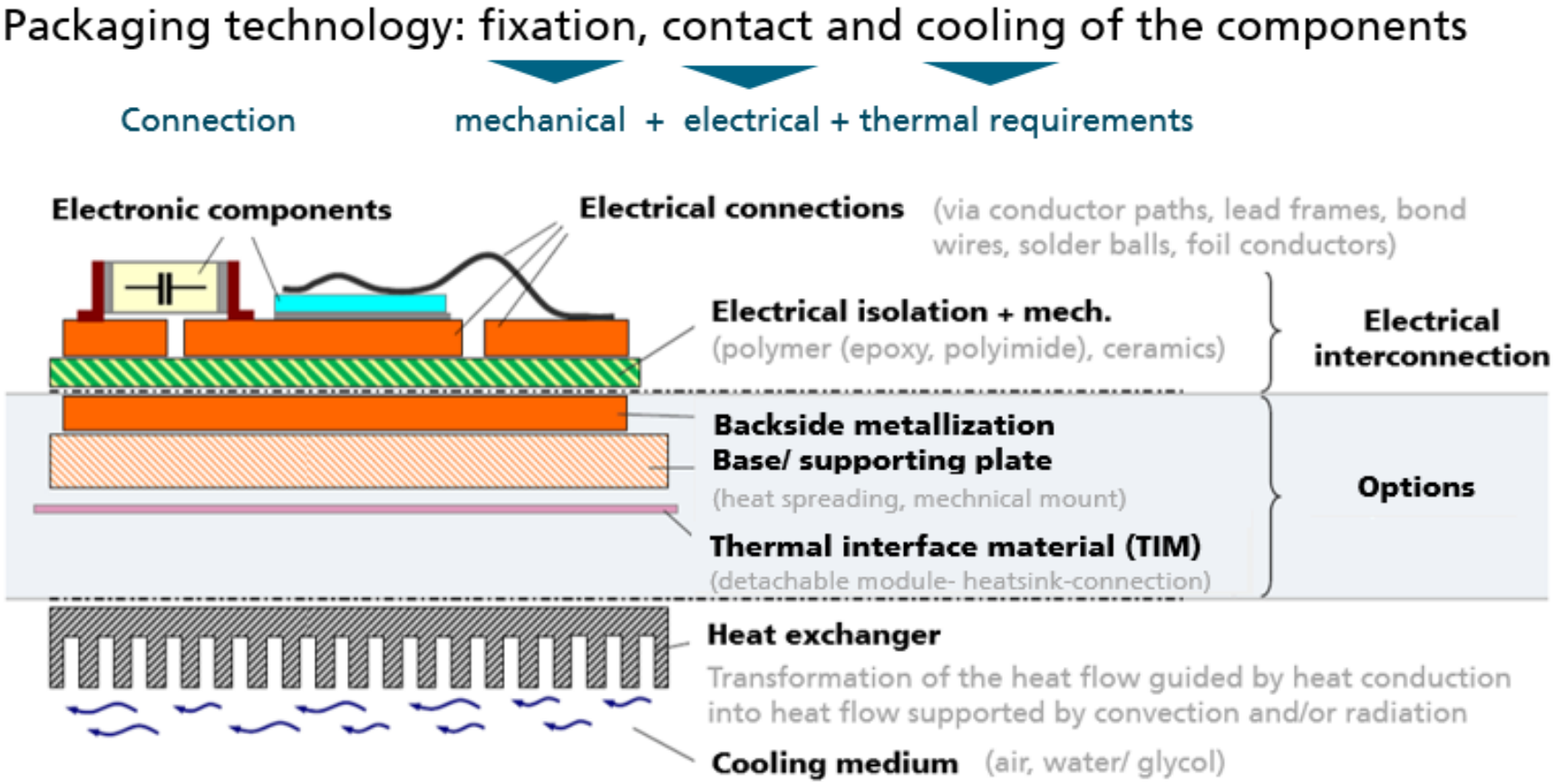
Packaging and interconnection technologies for power electronics

Basics and materials



Packaging and interconnection technologies for power electronics

Basics and materials



Packaging and interconnection technologies for power electronics

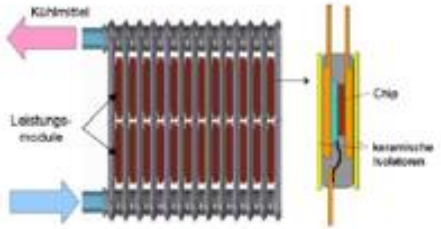
Basics and materials

- Cost reduction through better cooling and/or higher chip temperatures

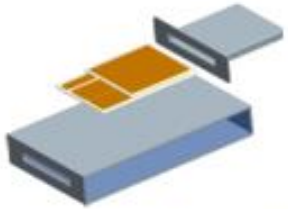
Cooling on both sides

Chip costs $\propto I \cdot \frac{R_{th}^{(A)}}{\Delta T}$ (@IGBT)

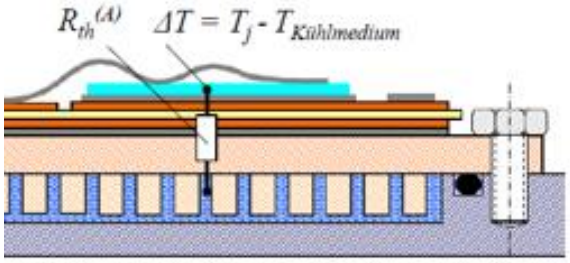
More cycle resistant



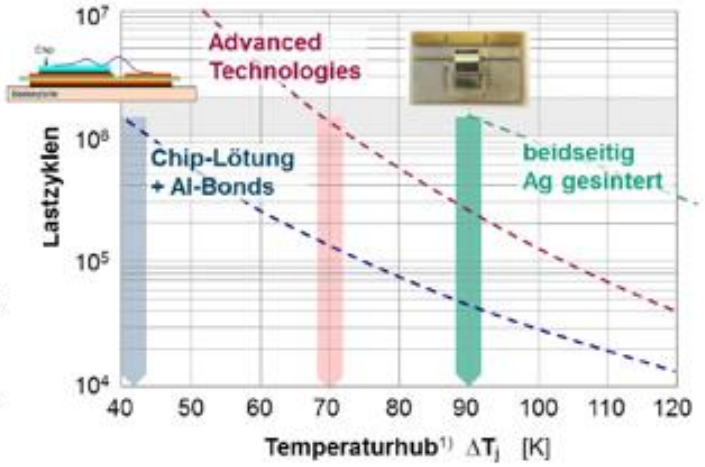
Toyota Lexus LS600h



Slot-Modul (FhG IISB)



However, the additional expenditure required for this in the area of substrate and connection technology must not overcompensate the chip cost savings. Not every technology is economical.



Packaging Technologies in Power Electronic Modules

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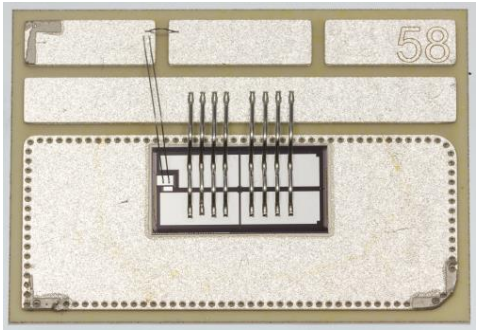
Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic



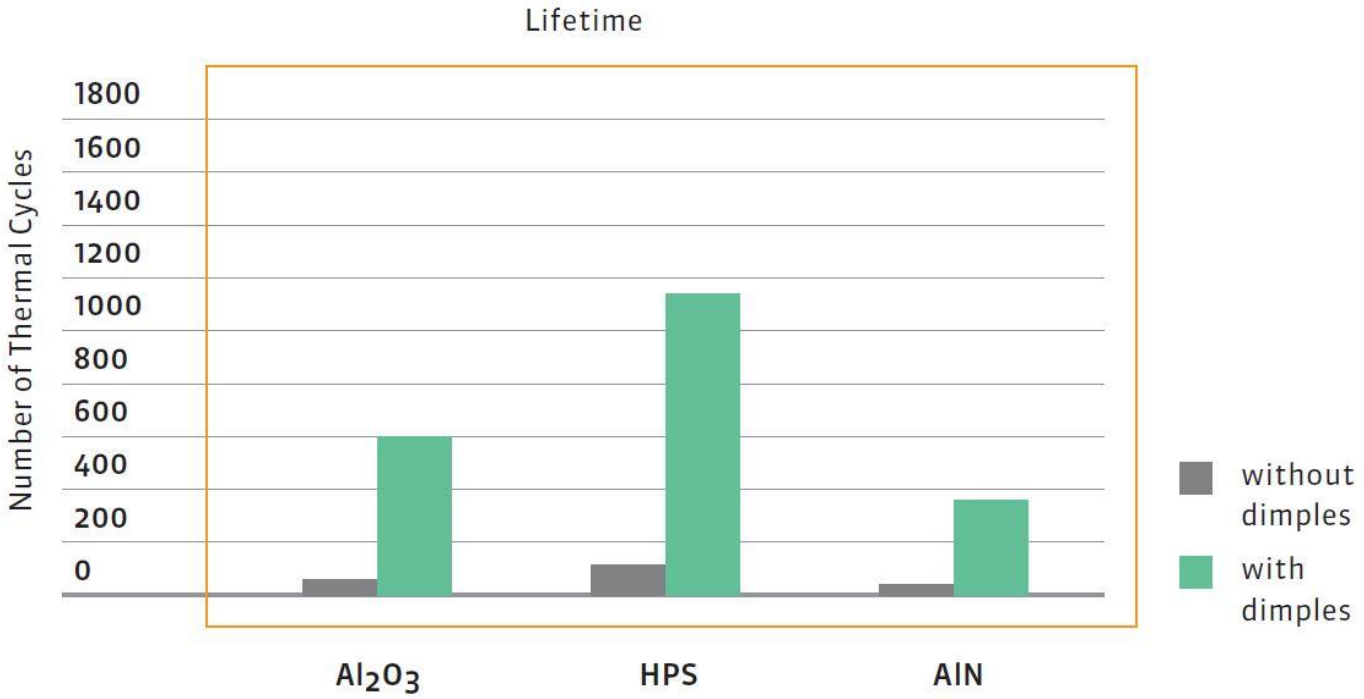
- **D**irect **C**opper **B**onded (DCB)
- Composite of ceramic and metal
- Very often used for PE applications
- Ceramic → Al_2O_3 / ZTA / AlN / Si3N4
- Metallization → Cu / Al

	Al_2O_3	ZTA	AlN	Si_3N_4
K1C in MPa·m$^{1/2}$	4 - 5.5	4.4 - 5	2.7	5 – 8.5
Elastic modulus in GPa	400	380	310	290 - 330
Flexural strength in MPa	230 - 580	400 - 480	200 - 360	700 - 1100
Thermal conductivity in W/mk	15 - 30	15	180 - 220	15 - 85
CTE in 10^{-6}K^{-1} (30 - 1000 °C)	6 - 8	9 - 11	4.5 - 5.6	2.5 - 3.5
Dielectric strength in kVmm^{-1}	15 - 17	--	> 20	20

Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic

- **D**irect **C**opper **B**onded (DCB)
- DCBs with dimples → up to 10 times longer service life
  - Test condition from -50 °C to +150 °C

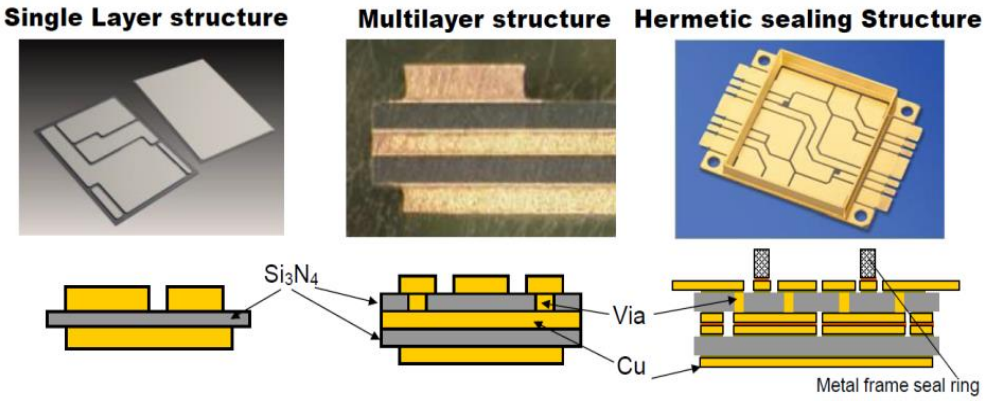


CURAMIK ELECTRONICS GMBH: DBC technology : Design Rules Version 12/2014, 2014

Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic

- **A**ctive **M**etal **B**razing (AMB)
- Composite of ceramic and metal with active solder
- Alternative to DCB
- Ceramic → Al_2O_3 / AlN / Si3N4
- Metallization → Cu



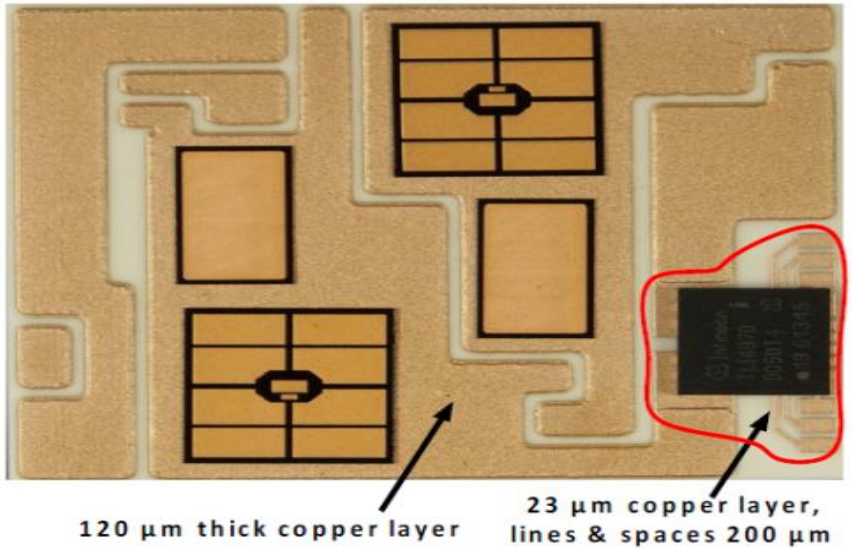
	Cu thickness in mm	Cycles from -40 to 125 °C
Si_3N_4 (0.32t)	0.2	> 3000
	0.3	> 3000
	0.4	> 3000
	0.5	> 3000
AlN (0.635t)	0.2	300
	0.3	200
	0.4	Crack at AMB Process
	0.5	Crack at AMB Process
Al_2O_3 (0.635t)	0.2	500
	0.3	300
	0.4	200
	0.5	100

KYOCERA: AMB Cu-Bonded Ceramic Substrates for Power Modules, 2014

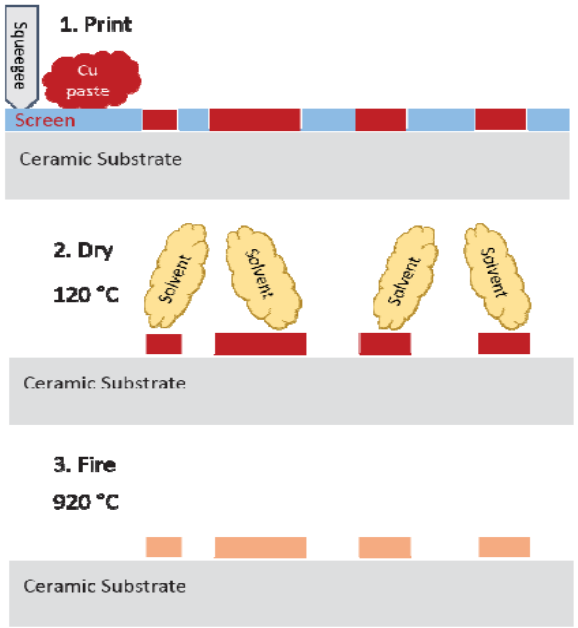
Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic

- **T**hick **F**ilm **T**echnology (TFT)
- Copper paste metallization
- Steps in metallization possible for signal and power
- Ceramic → Al_2O_3 / ZTA / AlN



BLANK, Thomas et al.: Copper thick-film substrates for power electronic applications., 2014

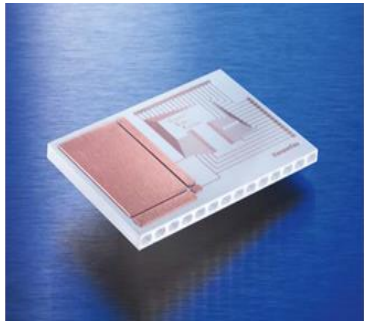


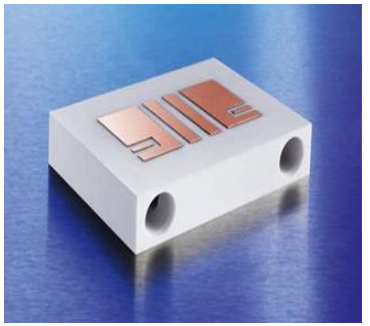
GUNDEL, Paul et al.: Thick Printed Copper as Highly Reliable Substrate Technology for Power Electronics. In: PCIM Europe 2015

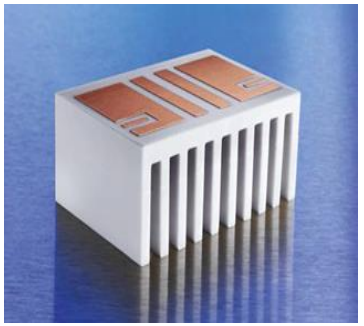
Packaging and interconnection technologies for power electronics

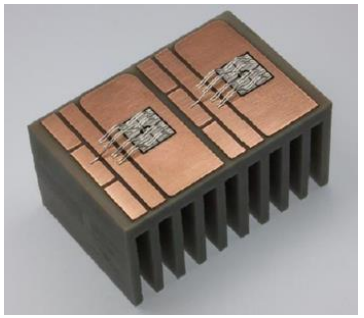
Substrate technologies - Inorganic

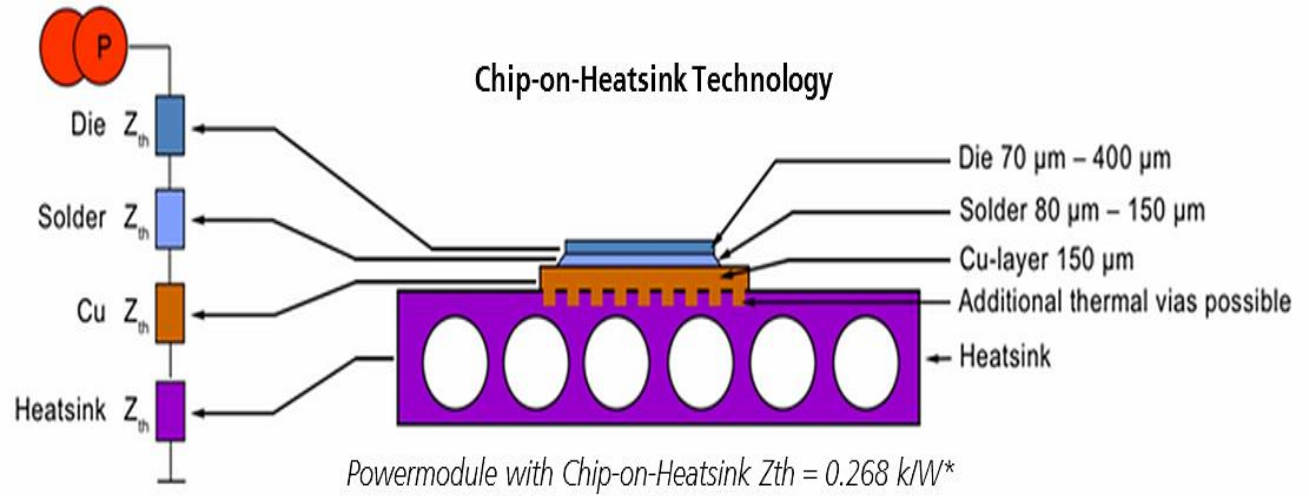
- **S**tructured **C**opper **T**echnology (SCT)
- Copper paste metallization
- Ceramics as substrate **and** heat sink
- Saving of the connection levels
- Ceramic → Al_2O_3 / AlN









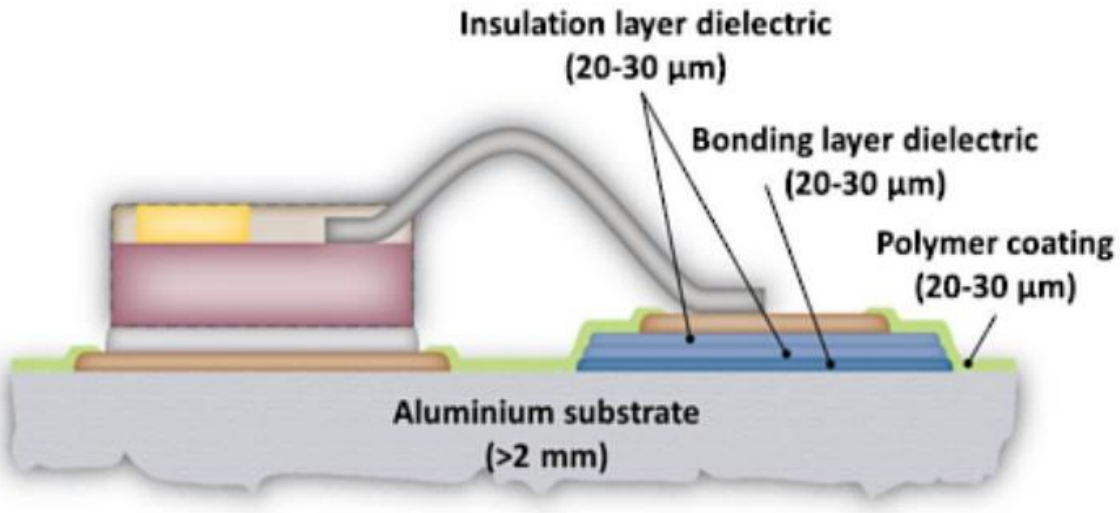


CERAMTEC: Advanced Ceramic Material Properties for the Electronics Industry

Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic

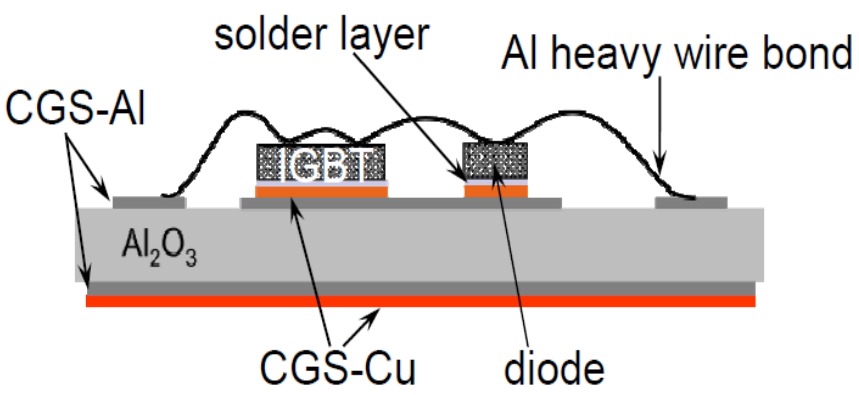
- **Anotherm**
- Copper paste metallization
- Ceramics as substrate **and** heat sink
- Saving of the connection levels
- Ceramic → Al_2O_3 / AlN

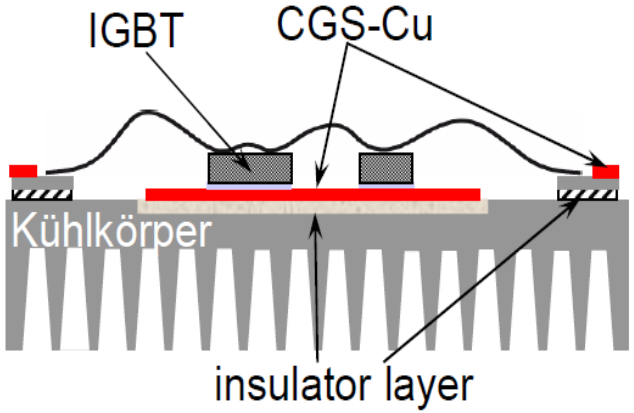


Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic

- **C**old **G**as **S**praying (CGS) → under development
- Apply metal powder to ceramic substrate
- Electrical conductivity ~ 80 % of DCB metallization
- R_{th} → ~ 13 % higher than DBC
- Metallization → Cu / Al
- Ceramic → Al_2O_3



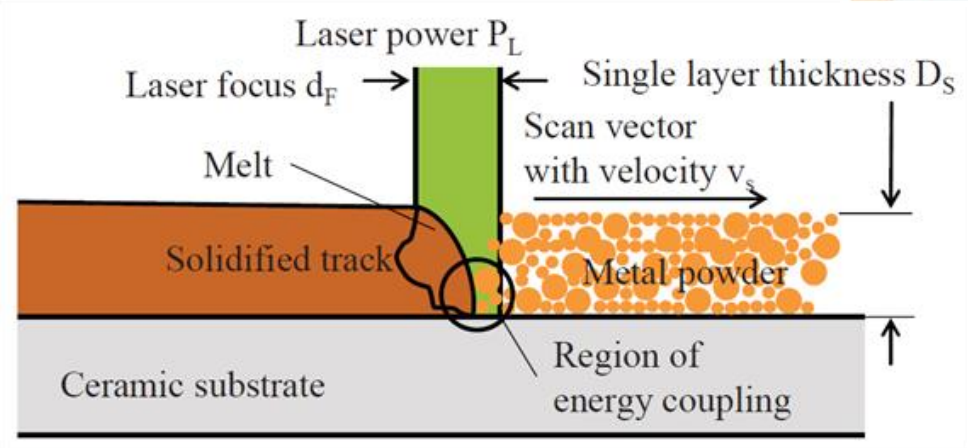


WILDE, J. ; WIELAGE, B.: Case Study: Cold Gas Spraying (CGS) Metallization Based Ceramic Substrates., 2010

Packaging and interconnection technologies for power electronics

Substrate technologies - Inorganic

- **S**elective **L**aser **M**elting (SLM) → under development
- Applying metal powder to ceramic by means of laser technology
- Steps in metallization possible
- Metallization → Cu
- Ceramic → Al_2O_3



SYED-KHAJA, Aarief ; PEREZ, Philip Patino ; FRANKE, Joerg: Production and Characterization of High-temperature Substrates through Selective Laser Melting (SLM) for Power Electronics. 2016

Packaging and interconnection technologies for power electronics

Substrate technologies - Organic

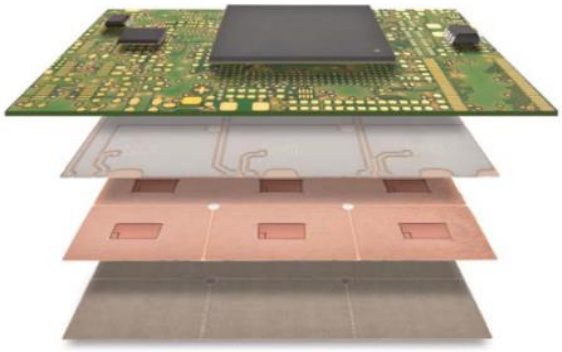
- **P**rinted **C**ircuit **B**oard (PCB)
- Organic materials → FR4, Polyimide, Epoxide, Teflon, etc.
- Metallization → Cu
- Less expensive than ceramic substrates

	Standard FR4	Polyimide	BT-Epoxy	CE-Epoxy	Teflon (PTFE)
Glass transition temperature in °C	125 – 140	220 – 260	~ 200	~ 250	200 – 230
CTE in ppm/K	< 70	< 55	< 40	< 25	< 70
Dielectric constant **1 MHz** **1 GHz** **10 GHz**	 4.7 4.3 -	 4.0 3.8 3.8	 4.4 4.1 -	 3.9 3.7 3.5	 2.6 2.4 2.2
Dielectric strength in kV/mm	50	45	70	65	45
Copper adhesion in N/mm	1.5	1.0	1.6	1.6	1.3
Cost comparison with standard FR4	1.0	~ 3 – 5	~ 2.5	~ 2.5	~ 4 - 8

Packaging and interconnection technologies for power electronics

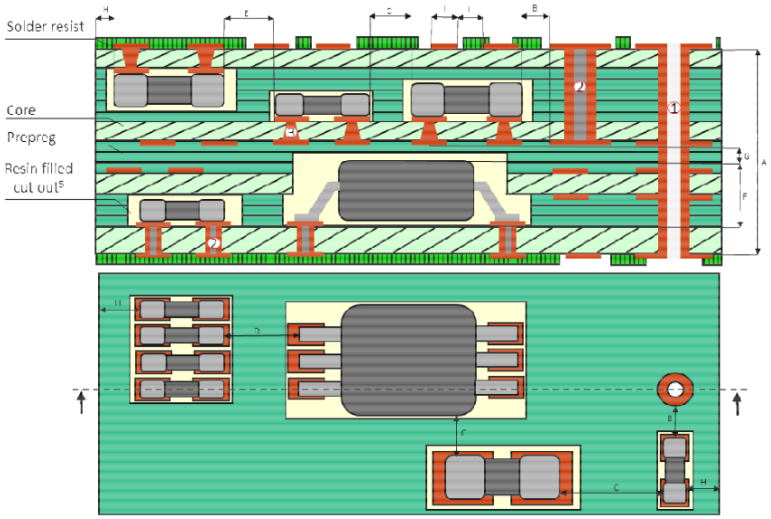
Substrate technologies - Organic

- **P**rinted **C**ircuit **B**oard (PCB) Embedding
- Semiconductor embedded in multilayer PCBs with vias
- Metallization → Cu
- Flexible 3-D designs



Smart p^2 Pack layup

SCHWEIZER ELECTRONIC: PCBs - Products and Solutions, 2015



ILFA Feinstleiter Technologie: Embedding Datasheet., 2020

Packaging and interconnection technologies for power electronics

Substrate technologies - Organic

- **High temperature PCB**
- For applications at 175 °C or higher
- PCB material temperature resistant up to ~ 220 °C

*Differential scanning calorimetry
**Dynamic mechanical analysis

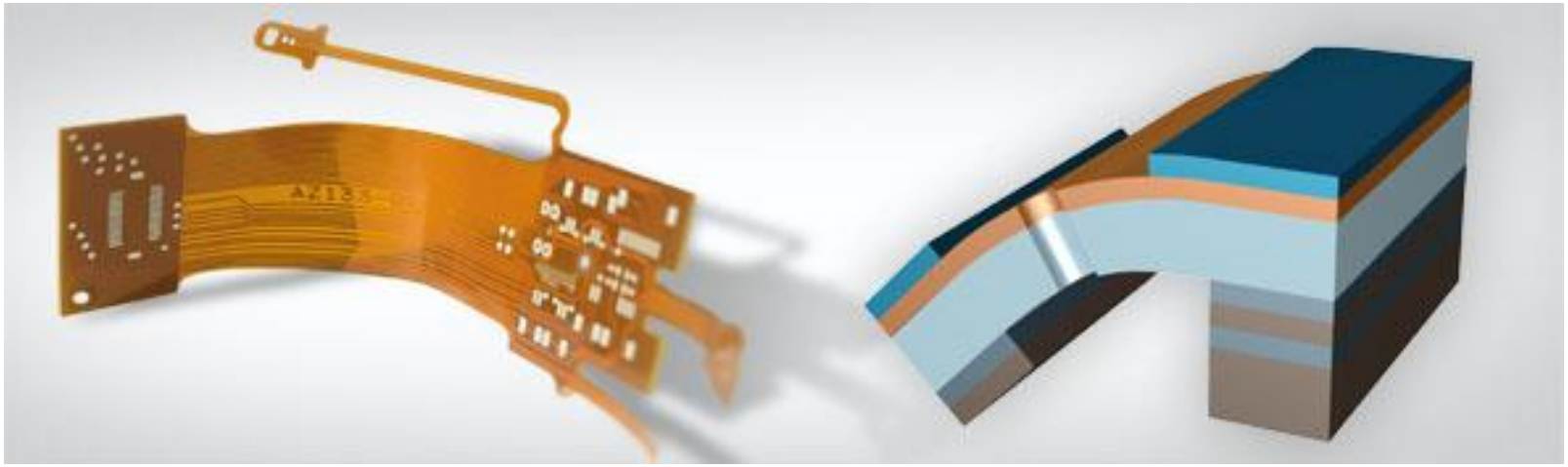
	Isola B	Benzo
Resin manufacturer	Isola	Huntsman
Polymer basis	Epoxy	Benzoxazine
Halogen-free	yes	yes
T_g (DSC)* in °C	~ 175	~ 200
T_g (DMA) in °C**	~ 195	~ 220
CTE-z (below T_g) in ppm/K	40	38
Soldering bath at 288 °C (with Cu) in min	> 10	> 10
Thermal conductivity in W/mK	0.7	0.7
Copper adhesion (35 µm/HTG) in N/mm	≥ 1.4	≥ 1.4

TROEGER, K. et al.: Tailored Benzoxazines as Novel Resin Systems for Printed Circuit Boards in High Temperature E-mobility Applications, 2014

Packaging and interconnection technologies for power electronics

Substrate technologies - Organic

- **Flexible printed circuit boards**
- Suitable for compact, complex, space/weight minimizing superstructures
- Base film → Polyimid, PET, PEN
- Metallization → Cu / Ag / Au

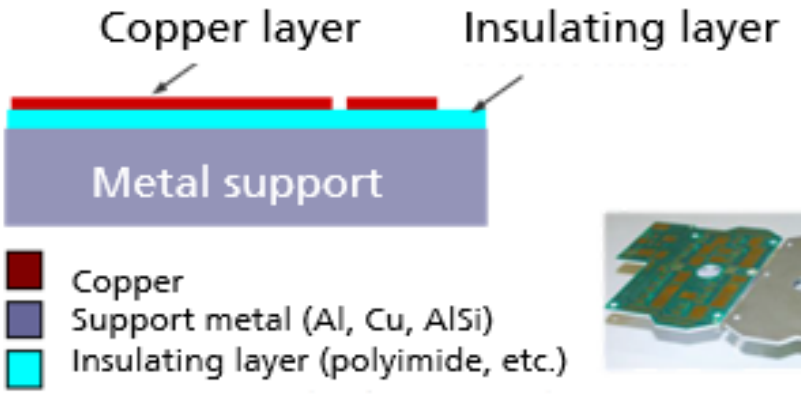


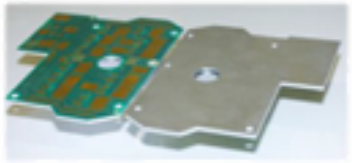
https://ats.net/de/produkte-technologien/produkt-portfolio/flexible-starr-flexible-leiterplatten/flexible-leiterplatten/

Packaging and interconnection technologies for power electronics

Substrate technologies - Organic

- **I**nsulated **M**etal **S**ubstrate (IMS)
- Organic materials → see PCB
- Less expensive than ceramic substrates
- Base material Al / Cu / stainless steel





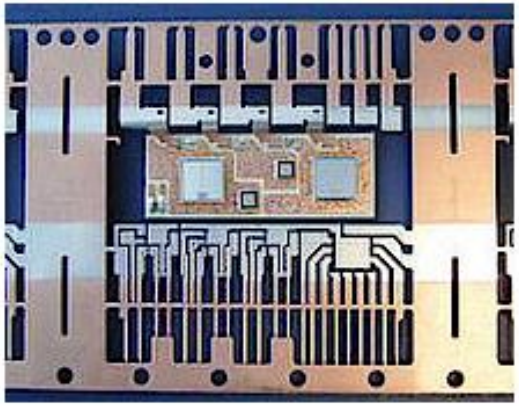
Bildquelle: aurel s.p.a.

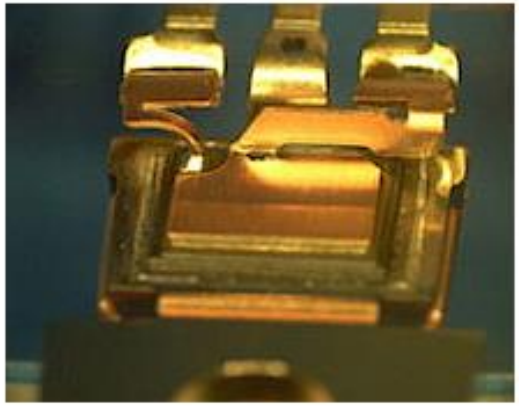
Bildquelle: Schweizer AG

Packaging and interconnection technologies for power electronics

Substrate technologies - Metallic

- **Copper leadframe**
- Cost-effective (Cu as carrier material)
- No substrate-internal CTE mismatch (substrate made of Cu only) → good for substrate lifetime
- But high CTE mismatch to bare dies
- Very high flexibility in terms of design





https://www.zestron.com/de/anwendungen/leistungselektronik/reinigung-von-leadframes.html

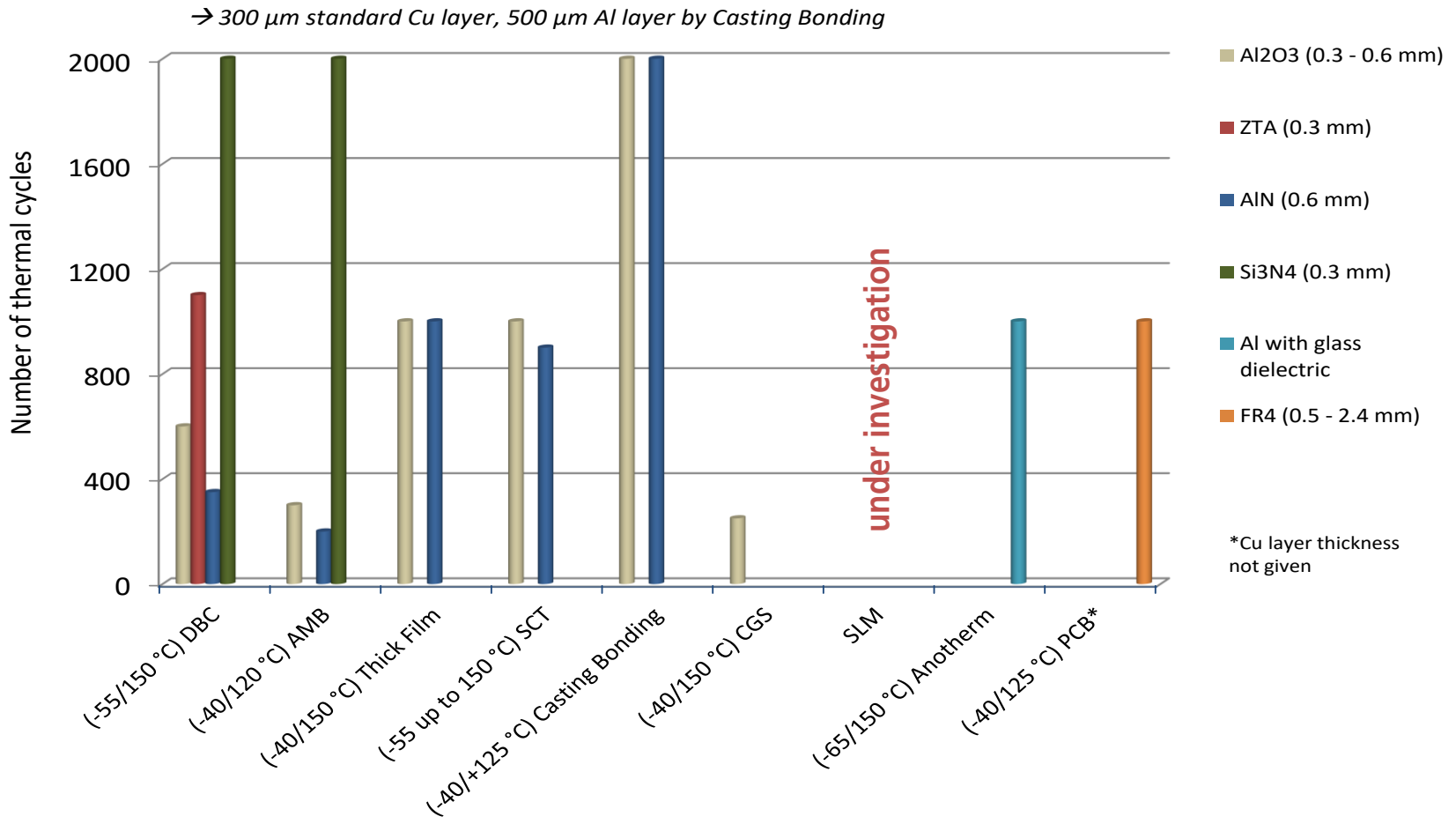
Comparison and Evaluation of packaging methods

Substrate Technologies - Summary

	Special features	Service life or TWB strength	Current carrying capacity	Steps in metallization	Thermal conductivity in W/mK	Dielectric strength in kV/mm	Temperature resistance
LTCC	Good electrical conductivity; through-connection possible; expensive	Adapted to Si	Medium, max. layer thickness 0.2 mm	Not possible, but not absolutely necessary, due to layer structure	2.8 – 5	20 - 40	**Good**
HTCC	Mechanical stability; through-connection possible	Adapted to overall structure	Bad, because electrical conductivity is poor		13 – 25 (Al2O3) 140 – 200 (AlN)	> 22	**Good**
DCB/ AMB Al_2O_3	Different metallizations possible; distance between conductor tracks is larger than on printed circuit boards	medium	Good	Possible, but step height limited	15 - 30	15 – 17	**Good**
DCB/ AMB AlN		Poor passive TC, thick AlN necessary			180 – 220	> 20	
DCB/ AMB Si_3N_4		Very good passive TW	Very good, thick copper layers	Possible, due to experience based large tolerances	15 - 85	~ 20	**Good**
SCT/ Thick-film	Different ceramics & metallization possible	Passive TW very good, possibly CTE smaller compared to Al_2O_3 DCB/AMB	Cu-paste, electrical conductivity 50% of bulk copper	possible	20 – 30	10 – 20	Good
Copper lead-frame	No CTE mismatch, low cost	High CTE	Good, depending on the thickness	possible	30 – 380		Good
Flex printed circuit board	Flexible design possible Through-connection possible	Not suitable for high temperature, high CTE	Good	Not possible, but not absolutely necessary, due to layer structure	1.3 – 2.2 depending on material	120 – 150 depending on material	Up to approx. 210 °C depending on material
IMS	Mechanical stability, Structure is like printed circuit board; Rth worse than DCB	Not suitable for high temperature, high CTE	Good	Not known	0.4 - 12	60 depending on dielectrics	Not known

Comparison and evaluation of packaging methods

Substrate technologies - comparison of thermal stability



Dr. Christoph F. Bayer et al., Packaging and Modules
Departement DEVICES AND RELIABILITY © Fraunhofer IISB

Fraunhofer IISB

Packaging Technologies in Power Electronic Modules

- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - **Packaging concepts**
  - Interconnection technologies
  - Packaging at Fraunhofer IISB
  - Thermal design and insulation coordination
- Simulation process and theoretical consideration
- Test procedure and analysis
  - General
  - AQG 324 (LV 324)
- Test setups and parameters
- Summary

Packaging and interconnection technologies for power electronics

Packaging concepts

- Cova et al., 2016: "Thermal design optimization of novel modular power converter assembly enabling higher performance, reliability and availability"
- Zhong et al., 2014: "Design & Analysis of Novel IGBT Package with Double-Sided Cooling"
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- Brinkfeldt et al., 2014: "Modeling of SiC Power Modules with Double Sided Cooling"
- Chen et al., 2015: "Design and Testing of the World's First Single-Level-Press-Pack IGBT Based Submodule for MMC VSC HVDC Applications".
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- Zhang et al., 2016 : "A Wirebond-less Package for High Votlage Cascode Gallium Nitride Devices"
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- Marcinkowski, 2014: "Dual-sided Cooling of Power Semiconductor Modules"
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- Ivanova et al., 2006: „Heat Pipe Integrated in Direct Bonded Copper (DBC) Technology for Cooling of Power Electronics Packaging"
- Liang, 2015: „Integrated Double Sided Cooling Packaging of Planar SiC Power Module"
- Saeed et al., 2014: „High Current Density Air Cored Inductors for Direct Power Module Integration"
- Grassmann et al., 2015: „Double Sided Cooled Module Concept for High Power Density in HEV Applications"
- Stahr et al., 2016: „Investigation of a Power Module with Double Sided Cooling Using a New Concept for a Chip Embedding"
- Berry et al., 2016: "Thermal Characterization of Planar High Temperature Power Module Packages with Sintered Nanosilver Interconnection"
- Brinkfeldt et al., 2016: "Design and Fabrication of a SiC-Based Power Module with Double-Sided Cooling for Automotive Applications"
- Vagnonet et al., 2010: "A Bus-Bar-Like Power Module Based on Three-Dimensional Power-Chip-on-Chip Hybrid Integration"
- Nakatsu et al., 2013 : "A Novel Direct Water and Double-Sided Cooled Power Module and a Compact Inverter for Electrified Vehicles"
- Duchesne et al., 2013 : "Interconnection Technology for New Wide Band Gap Semiconductors"
- Rhee Min Woo et al., 2014: "High Power SiC Inverter Module Packaging Solutions for Junction Temperature over 220°C"
- Yamanari et al., 2016: "Smaller Size and Higher Reliability for Vertical Chip Mounted Type Power Device"
- Wunderle et al., 2014: "Double-Sided Cooling and Transient Thermo-Electrical Management of Silicon on DCB Assemblies for Power Converter Modules: Design, Technology and Test"
- Johnson et al., 2007: "Compact Double-Side Liquid- Impingement- Cooled Integrated Power Electronic Module"
- Chang et al., 2006: "Novel Dual-Side Thermal Interfacing of IPM for Elevated-Temperature Application"
- Stockmeier et al., 2011: "SKiN: Double side sintering technology for new packages"
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- Hoene et al., 2013: " Ultra-Low- Inductance Power Module for Fast Switching Semiconductors"
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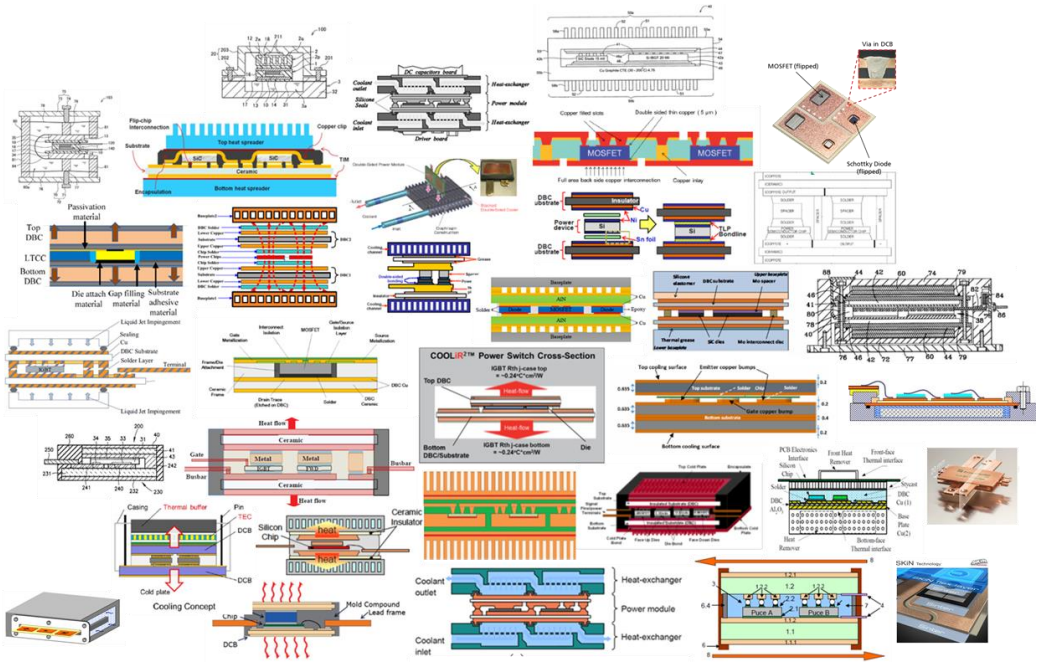
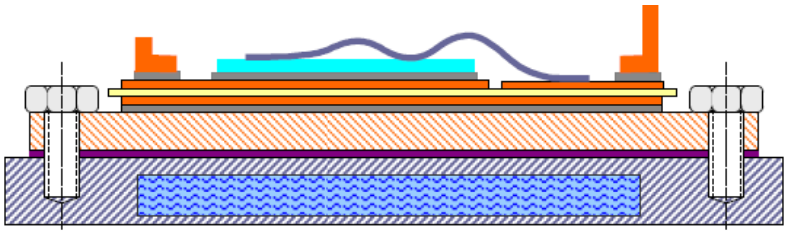


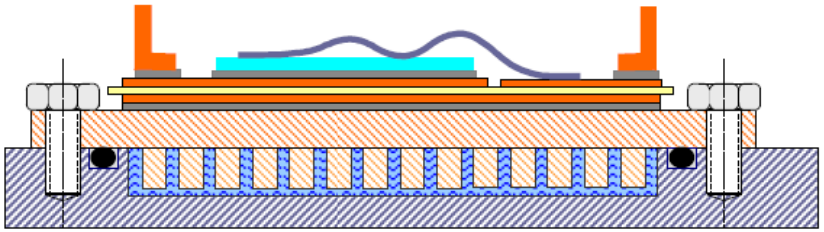
Packaging and interconnection technologies for power electronics

Packaging concepts

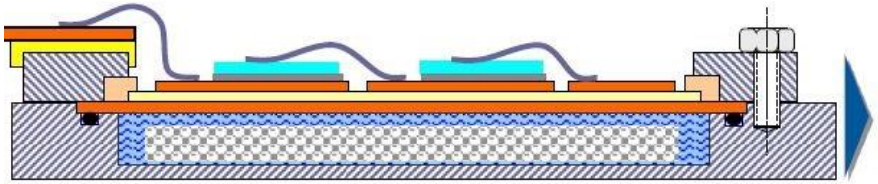
Single-sided cooled power modules - basic concepts



Indirect cooling
- Module (with or without base plate) on heat sink
- The mechanical separation point also represents a significant thermal barrier with thermal interface material (TIM)
- CTE's of a wide range of materials must be matched
- Error prone (TIM) and expensive assembly



Directly cooled base plate
- Low thermal resistance
- CTE's of a variety of materials are have to be matched to each other
- Seal required

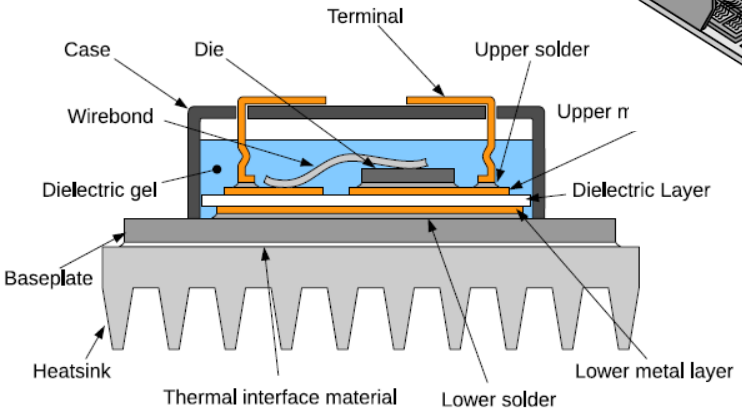


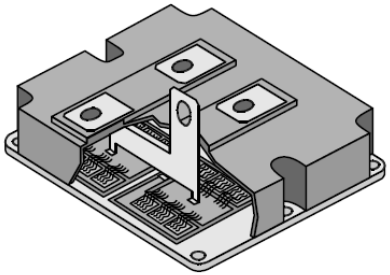
Directly cooled substrate
- Smallest number of interfaces and materials
- Low thermal resistance e.g. by means of turbulence bodies in the cooling oil channel (see ShowerPower™)
- Low heat capacity in case of coolant flow disturbances (e.g. air bubbles)
- Seal required

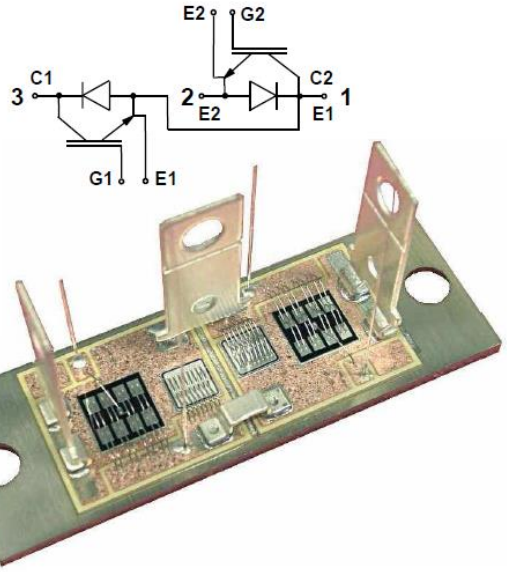
Packaging and interconnection technologies for power electronics

Packaging concepts – assembly standard

- Standard assembly







- Aufbau- und Verbindungstechnik in der Leistungselektronik, Wahlfach-Vorlesung, Wintersemester 2008/09, Friedrich-Alexander-Universität Erlangen-Nürnberg, Dr. Uwe Scheuermann
- Packaging for Power Electronics, Laboratoire Ampère, Lyon, France, 2015, Cyril BUTTAY

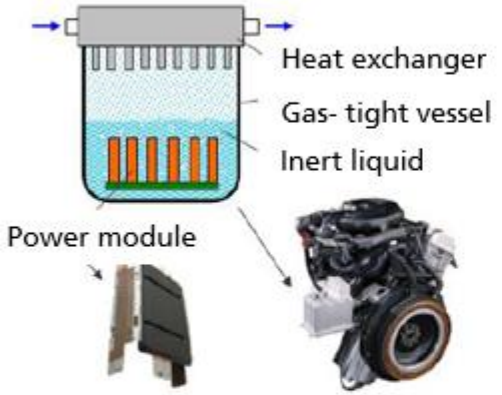
Packaging and interconnection technologies for power electronics

Packaging concepts

- **Double-sided cooled power modules - Basic concepts**

Boiling-bath cooling

Conti-Temic

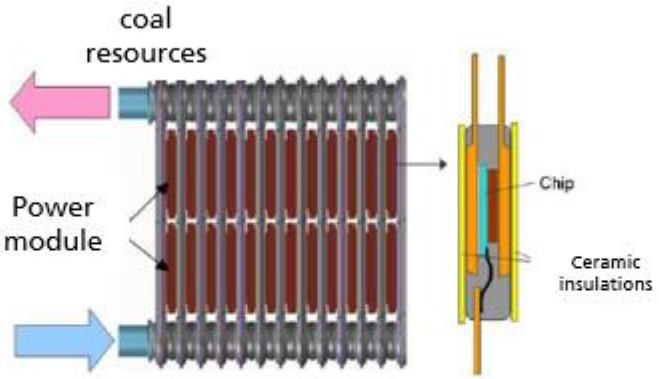


- highest cooling capacity
- gas tight housing and
- inert liquid required

Problems: service, disposal, media compatibility of all components

Pressure plates

Toyota Lexus LS600h

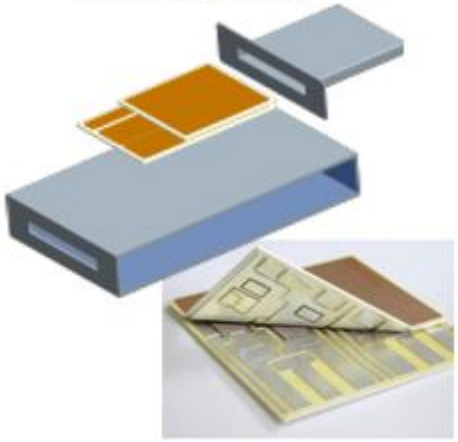


- Not much better than one-sided cooled Pin-Fin module due to double-sided thermal interface material
- Considerable mechanical overhead (clamping device))

1) TIM: Thermal Interface Material (z.B. Wärmeleitpaste)

Slot- module

Fraunhofer-IISB

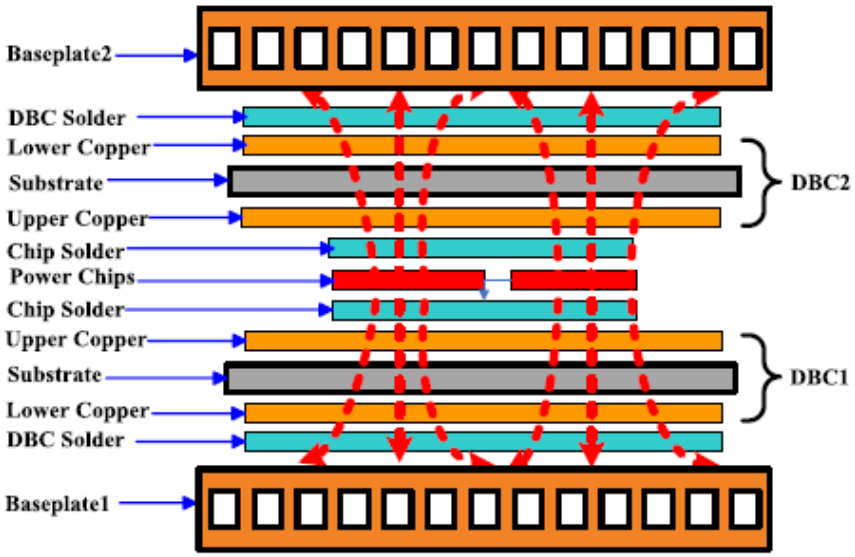


- very high power density
- no TIM
- no mechanical pressing devices

Packaging and interconnection technologies for power electronics

Packaging concepts

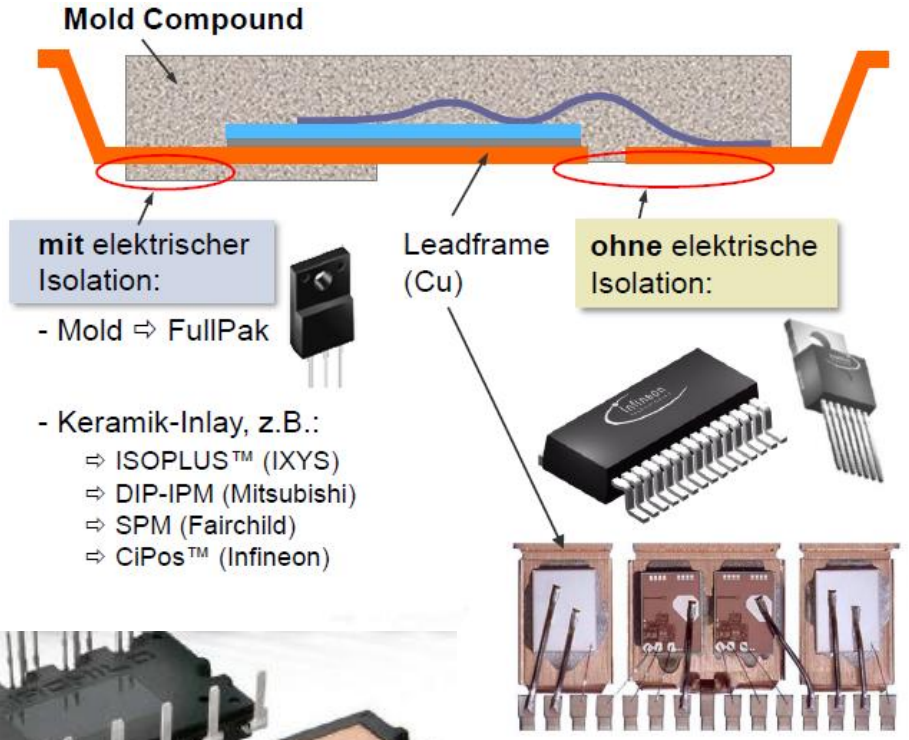
- **Double-Sided Ceramic Substrate Technology**
- Sandwich concept, chips connected on both sides with DCBs and base plate
- Requires extra insulation layer on the heat sink
- Challenge regarding layout design and production process
- Better power distribution
- High thermal conductivity, R_{th} up to -50 %
- Low inductive, short switching times
- Reduction of volume and weight
- Stackable cooling concept
- Highest integration and power density



Packaging and interconnection technologies for power electronics

Packaging concepts

- **Leadframe-Molded Module**
- Overmoulded stamped grid structure as circuit carrier
- Mold mass or ceramic inlay as electrical insulation
- Very cost-effective, high volume production
- High protective effect (dirt, mechanical stress, etc.)



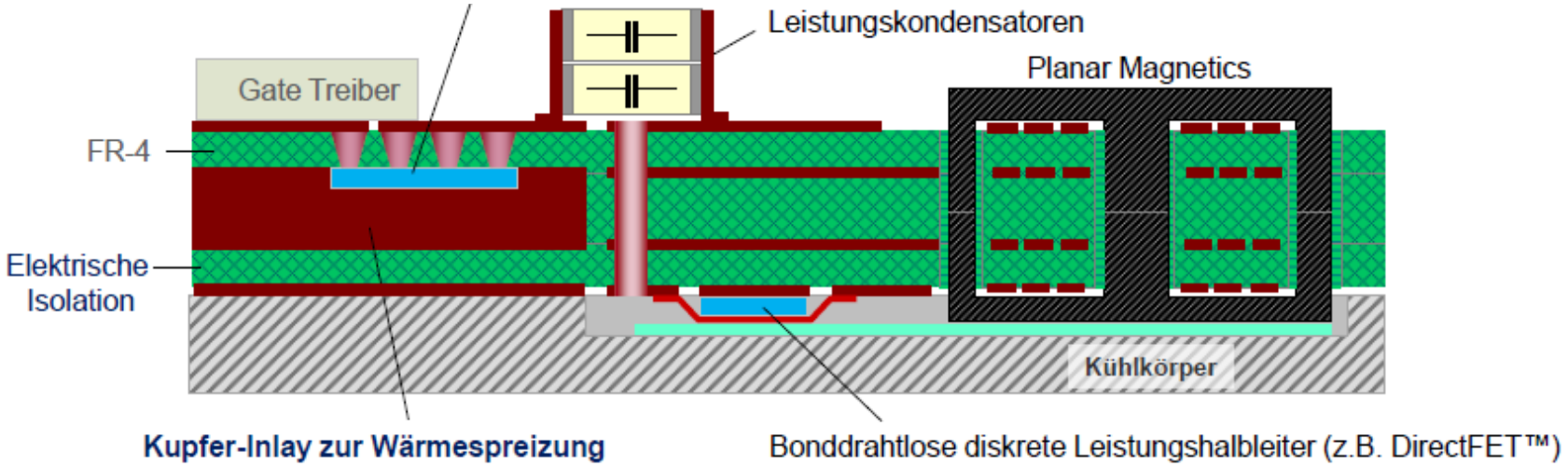
Infineon, Fairchild, STM

Packaging and interconnection technologies for power electronics

Packaging concepts

- **Embedding Technology**
- Chips embedded in insulating substrates
- Miniaturization → Elimination of bonding wires and housings
- Low inductive designs → short current paths, electrical vias, 3D integration
- Double-sided cooling, thermal vias → up to 60 % R_{th} improvement for double-sided liquid-cooled embedded packages

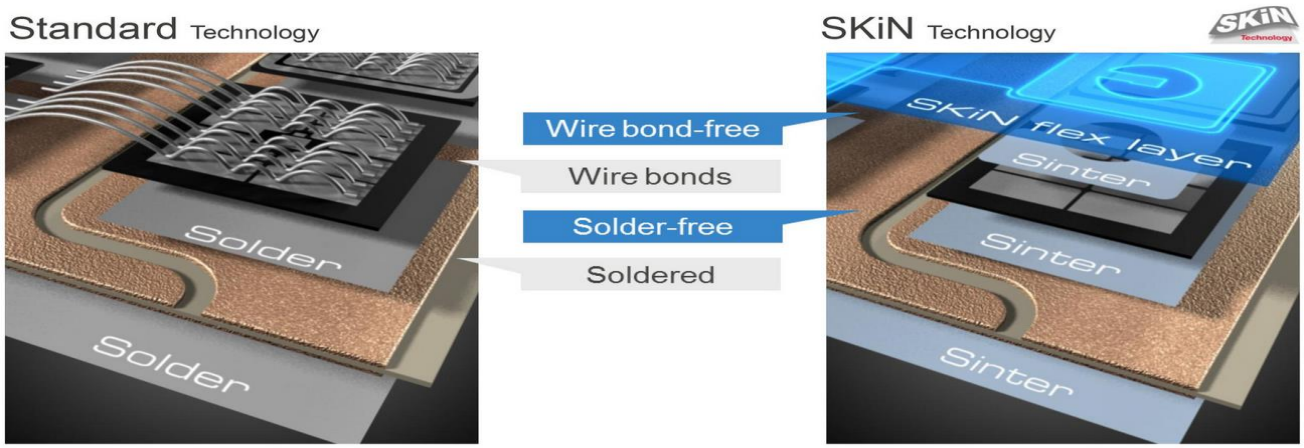
Power semiconductor chips embedded in the circuit board



Packaging and interconnection technologies for power electronics

Packaging concepts

- **SKiN Module (SEMIKRON International GmbH)**
- Use of flexible conductor foils
- R_{th} reduction compared to classic power modules
- Elimination of solder layers and bonding wires
- Increased service life by factor ~200 compared to classic power modules
- Lifetime increase by factor ~40 compared to state-of-the-art industrial power modules
- Reduction of volume and weight (to ~ 40 % of classic power modules)

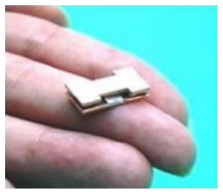


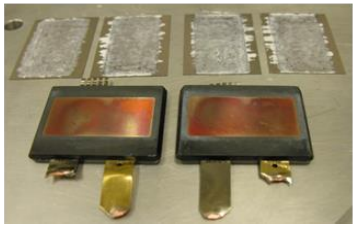
Packaging and interconnection technologies for power electronics

Packaging concepts

Further packaging concepts and products

- Toshiba TPW1R306PL; 5.0 mm × 6.0 mm × 0.73 mm; MOSFET; 60 V 260 A; 2015/2017
  http://www.powerelectronicsworld.net/article/0/101041-toshiba-adds-double-sided-cooling-to-60-v-power-mosfets.html
- Infineon HybridPACK™ DSC; 42 mm x 42.4 mm x 4.77 mm; IGBT; 700 V 200/400 A; 15 nH; 0.1 K/W (0.12 K/W HybridPACK 1); PCIM 2016
  http://www.infineon.com/cms/de/about-infineon/press/market-news/2016/INFATV201605-056.html
- International Rectifier/Infineon COOLiR²Module™; 50 mm x 45 mm x 7 mm; IGBT; 680 V 300 A; <15 nH; down to 50 % R_{th}; Bodo's Power Systems 2012
  http://www.powerguru.org/coolir2%E2%84%A2-high-power-semiconductor-platform/
- Hitachi DCPM Double-sided-cooling Full-SiC Power Module; Tokyo Motor Show 2015
  http://www.hitachi.com/New/cnews/month/2015/09/150928a.html
- Fuji LS600h Lexus power module; 47.9 mm x 38.1 mm x 5.3 mm; vol. 54 no 2 fuji electric review 2008 or Oak Ridge National Laboratory 2009





Packaging Technologies in Power Electronic Modules

- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - Packaging concepts
  - **Interconnection technologies**
  - Packaging at Fraunhofer IISB
  - Thermal design and insulation coordination
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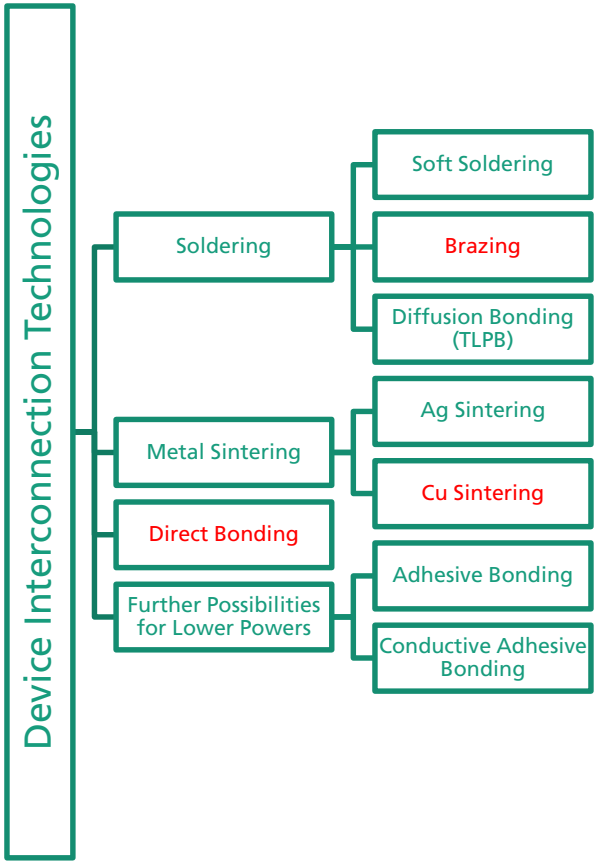
Packaging and interconnection technologies for power electronics

Interconnection technologies

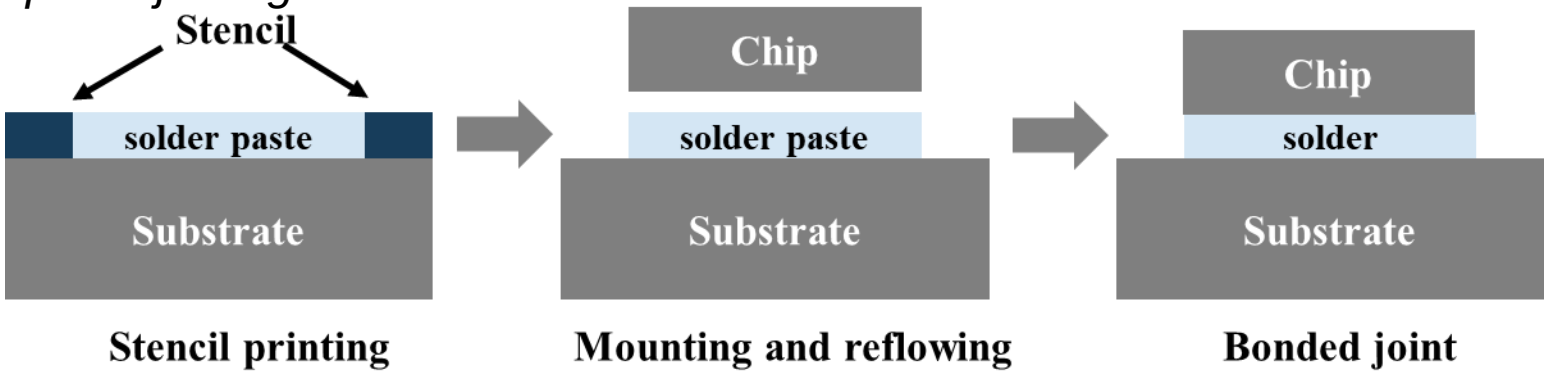
- Besides everlasting interest in further integration, minimization, modularization, high temperature and high voltage capability, new materials such as wide bandgap semiconductors come up and find their way into recent application.
  Thus it appears that SiC semiconductor devices are now used in power electronics mainly for switching high electrical currents (up to several 100 A) and high voltages (≥ 1 kV) in automotive drives, energy transmission and traction applications.
- Possible device interconnection technologies
  in power electronics packaging (red: research topics)



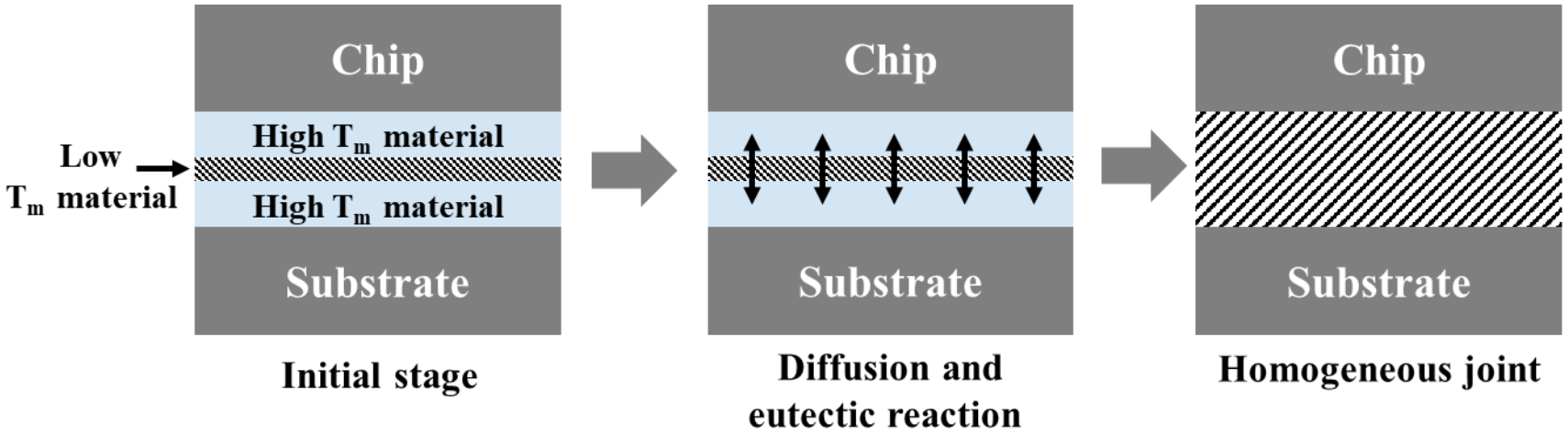
Packaging and interconnection technologies for power electronics

Interconnection technologies

1. Solder paste joining



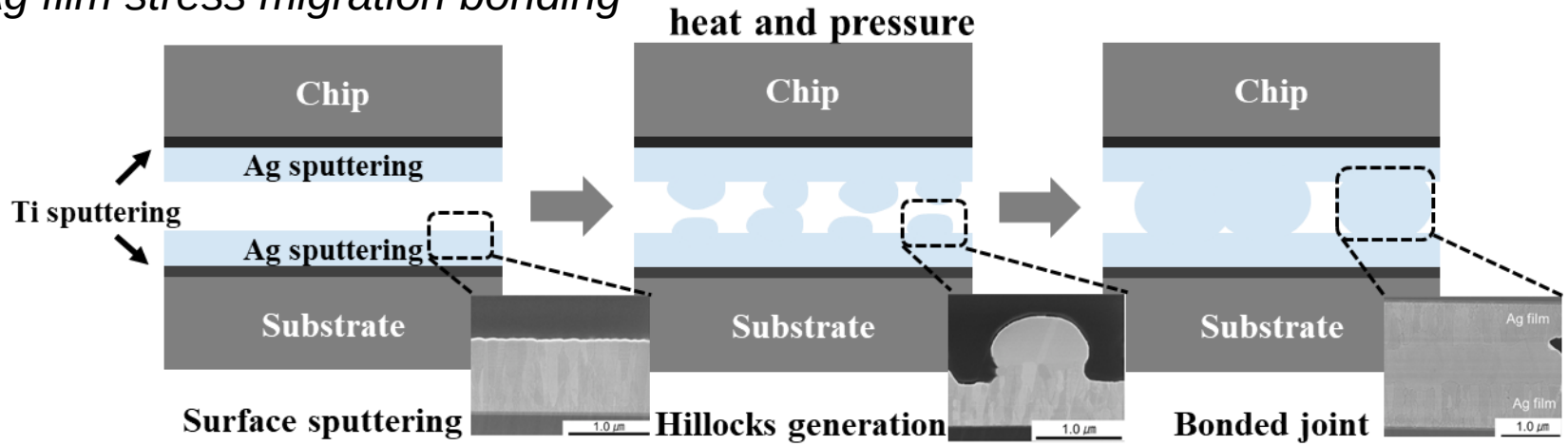
2. Transient liquid phase (TLP) bonding



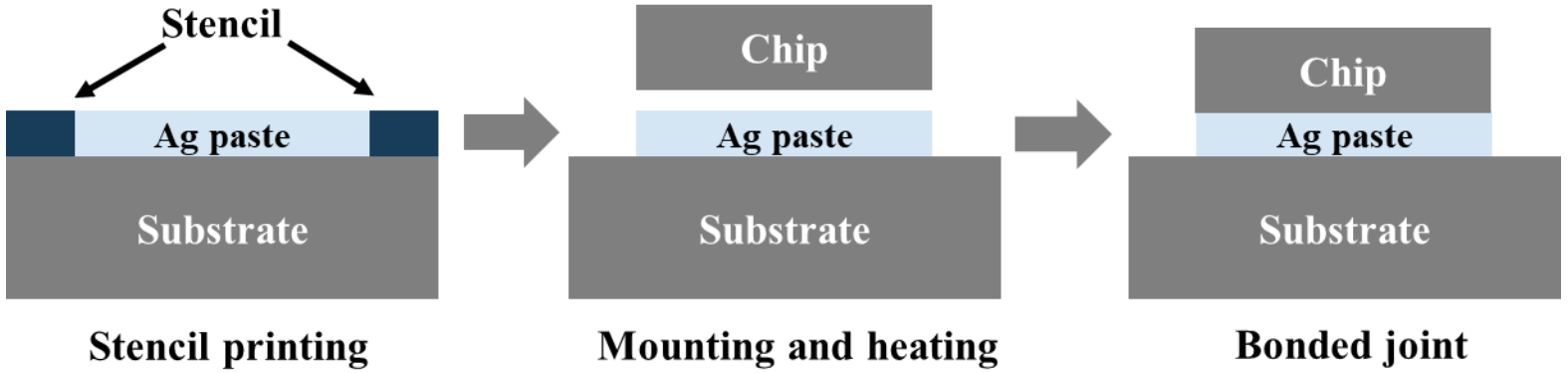
Packaging and interconnection technologies for power electronics

Interconnection technologies

3. Ag film stress migration bonding



4. Ag paste sinter joining



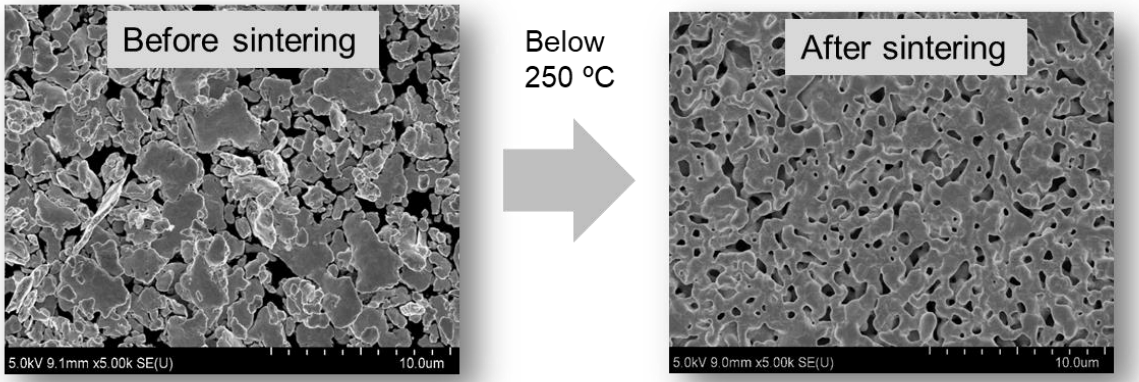
Packaging and interconnection technologies for power electronics

Interconnection technologies

- A comparison of different bonding materials

Series	Processing Temperature in ºC	Maximal Temperature in ºC	Electrical Resistivity in mΩ·cm	Thermal Conductivity in W/m·K	Bonding quality
Ag paste	200~250	Up to 900	≤ 0.005	≥ 200	High
Conductive adhesive	120~175	250	~7[1]	~ 3 – 10	Low
High-temperature solder	50 ºC above Tm	50 ºC below Tm	~15[2]	≤ 100	High

A: MG Chemicals 8331 Silver Epoxy Adhesive; B: Pb-Sn solder



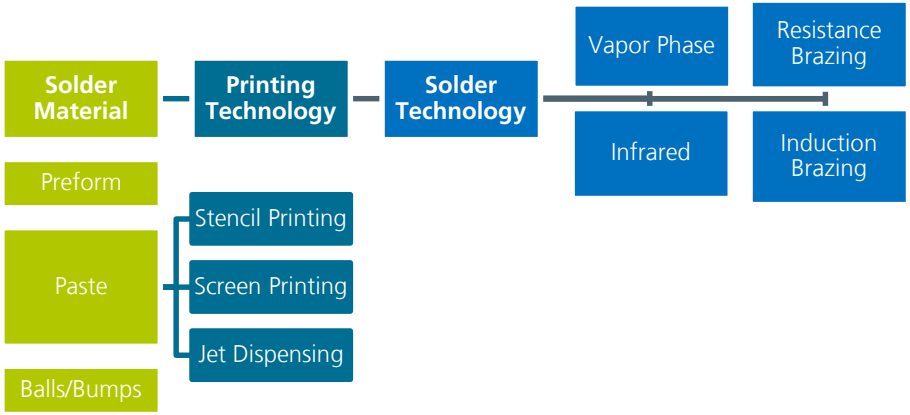
Ag particles and solvent

Micron-porous Ag structure

Packaging and interconnection technologies for power electronics

Interconnection technologies

- Overview of soldering technology for power modules
- Selection of solder materials for power electronics applications

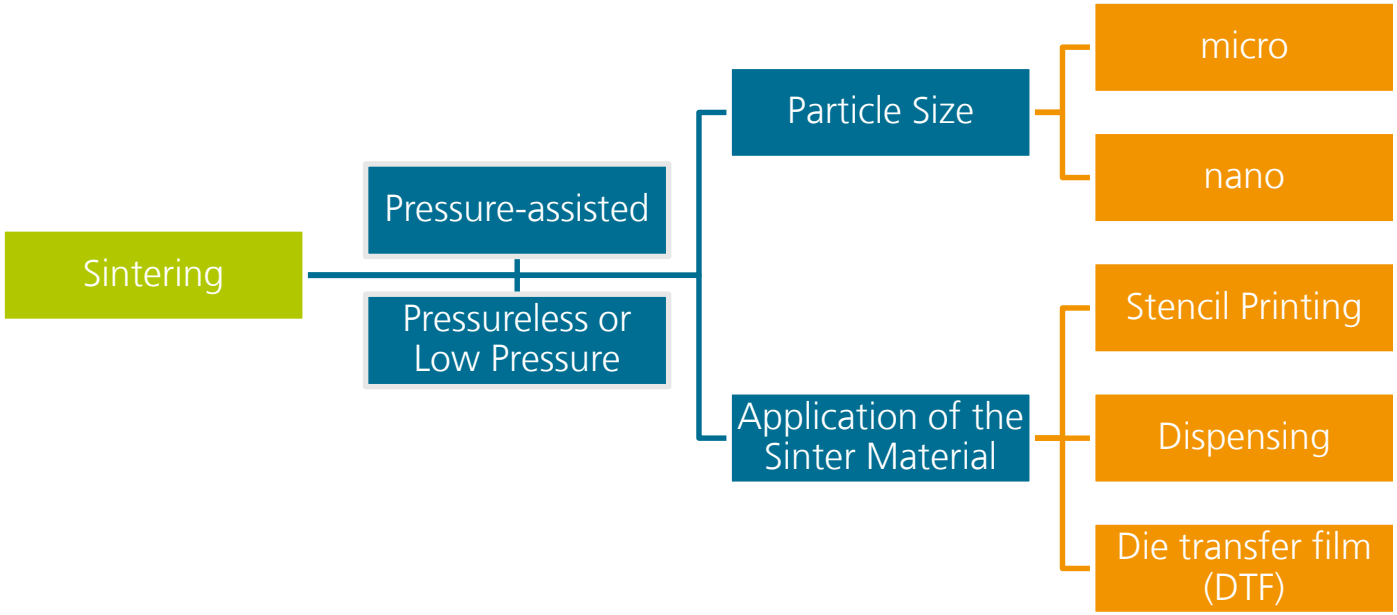


Solder composition	$T_{Liquidus}$ in °C	Electrical Conductivity in m/Ωmm²	Thermal Conductivity in W/mK	CTE in ppm/K
BiPb(32)Sn(15.5)	95	1.5	--	16.6
BiSn(43)	139	--	19	--
InPb(50)	215	3.3	22	24.4
SnPb(37)	183	7.4	70	24.3
SnAg(3.5)Cu(0.9)	217	--	60	--
SnCu(1)	227	8.8	60	--
Sn(96.5)Ag(3.0)Cu(0.5)	217/221	--	--	--
Sn(96.5)Ag(3.5)	221	--	--	--
Sn(95)Ag(5)	221/245	--	--	--
Sn(99.3)Cu(0.7)	227	--	--	--
Sn(97)Cu(3)	227/300	--	--	--
Sn(100)	232	--	--	--
PbIn(19)	276	--	--	--
PbSn(5)Ag(2.5)	280	< 5	44	29
PbSn(5)	315	< 5	45	29
PbSn(2)	325	4.9	--	--
Pb(100)	327	--	37	29.3
AuSn(20)	280	< 5	46	16
AuGe(12)	356	7	34	13.4
AuSi(3)	363	25	26	--

Packaging and interconnection technologies for power electronics

Interconnection technologies

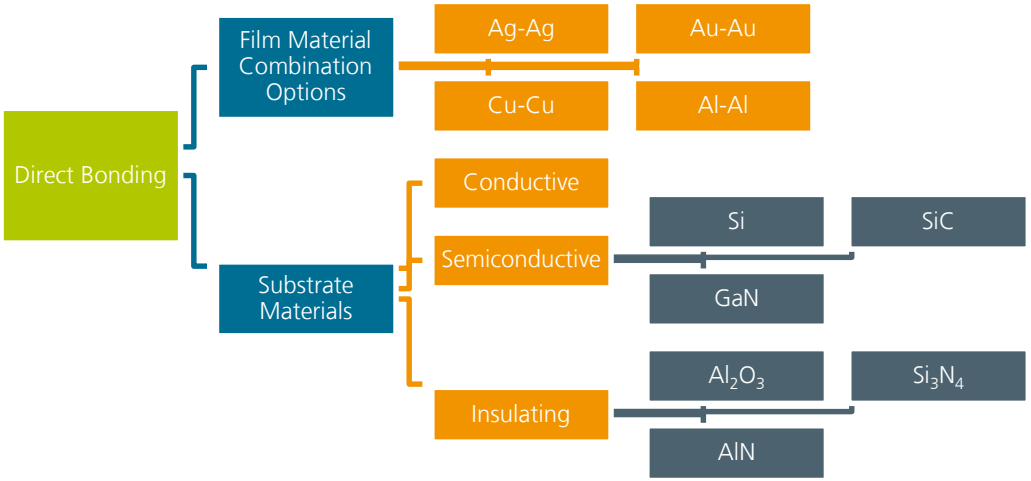
- Variety of metal sintering technology for die attach, e.g. mainly silver but also copper or copper-silver sinter paste

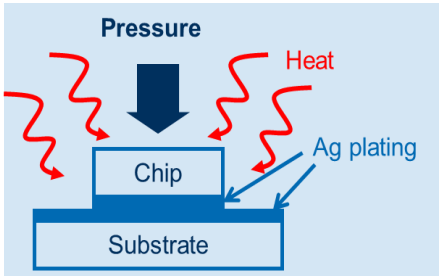


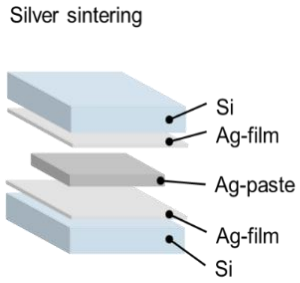
Packaging and interconnection technologies for power electronics

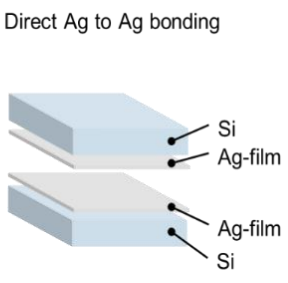
Interconnection technologies

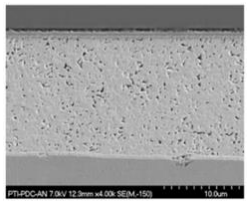
- Direct bonding examples in power electronics – substrate materials rank as carriers of the needed metallization

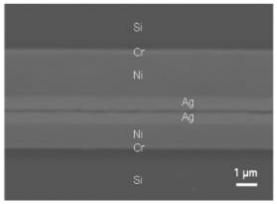






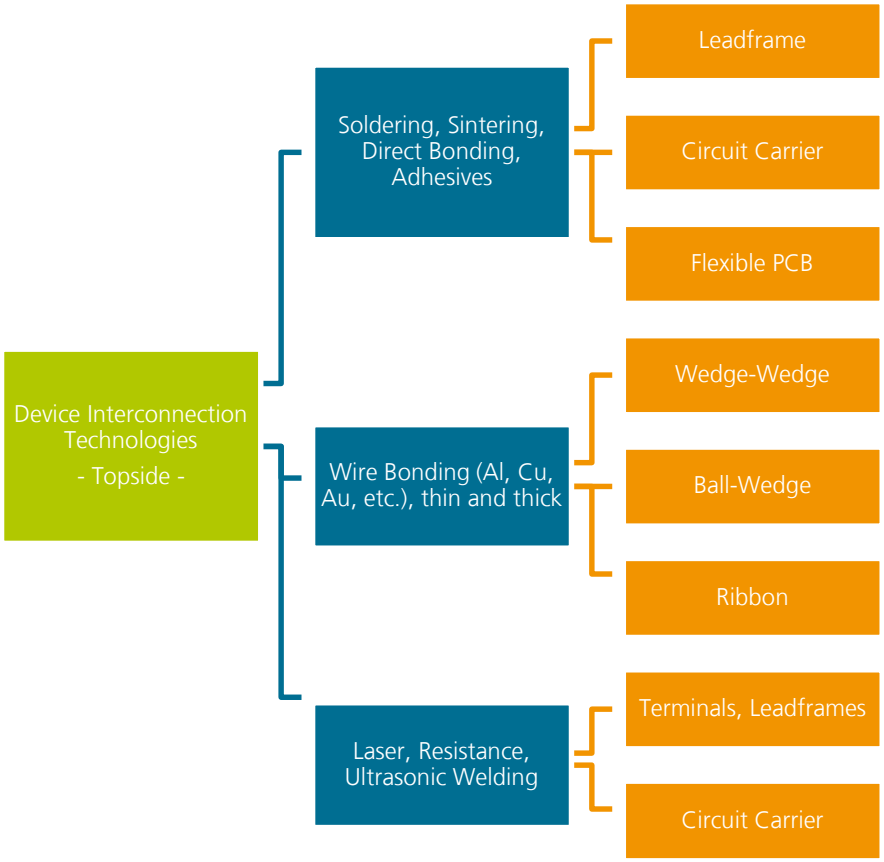


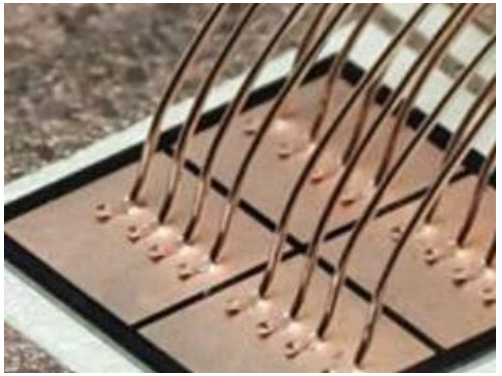




Packaging and interconnection technologies for power electronics

Interconnection technologies





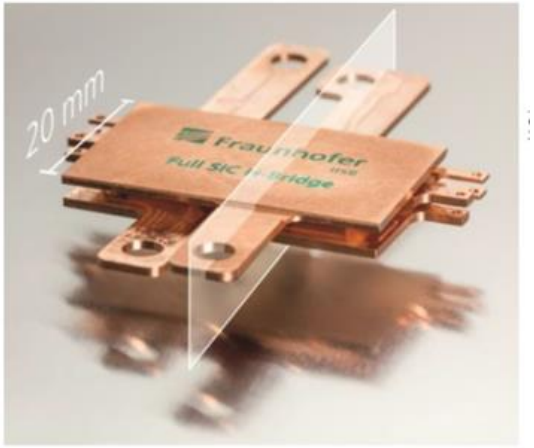
Packaging Technologies in Power Electronic Modules

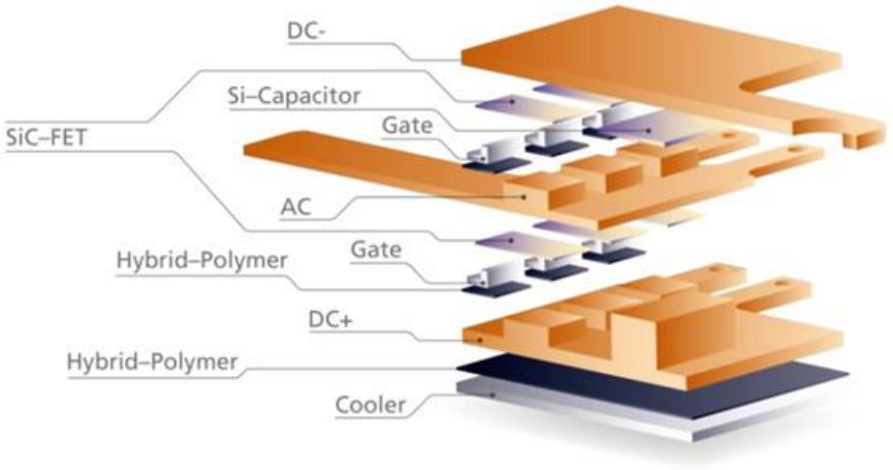
- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - Packaging concepts
  - Interconnection technologies
  - **Packaging at Fraunhofer IISB**
  - Thermal design and insulation coordination
- Simulation process and theoretical consideration
- Test procedure and analysis
  - General
  - AQG 324 (LV 324)
- Test setups and parameters
- Summary

Packaging and interconnection technologies for power electronics

Packaging at Fraunhofer IISB

- **Fraunhofer IISB concepts from public projects**
- **Project EMILE** (Full SiC Busbar Power Module)
- Double-sided assembly concept by means of Ag-sintering
- Chips on copper bus bar in the smallest space high power density
- Very high switching speed Inductance < 1 nH
- Cooling on both sides possible
- Cost-effective → no ceramic circuit carriers, only copper

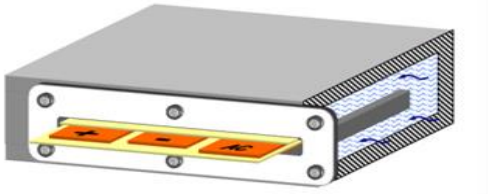


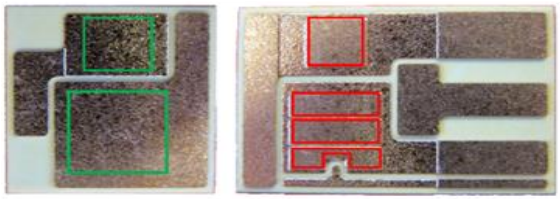


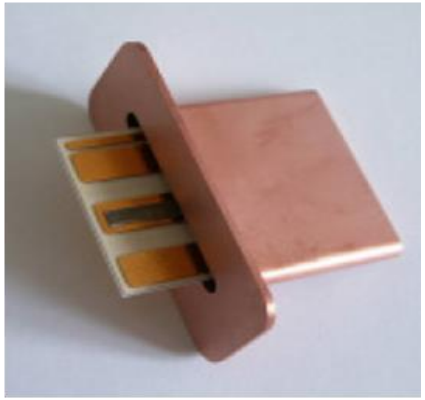
Packaging and interconnection technologies for power electronics

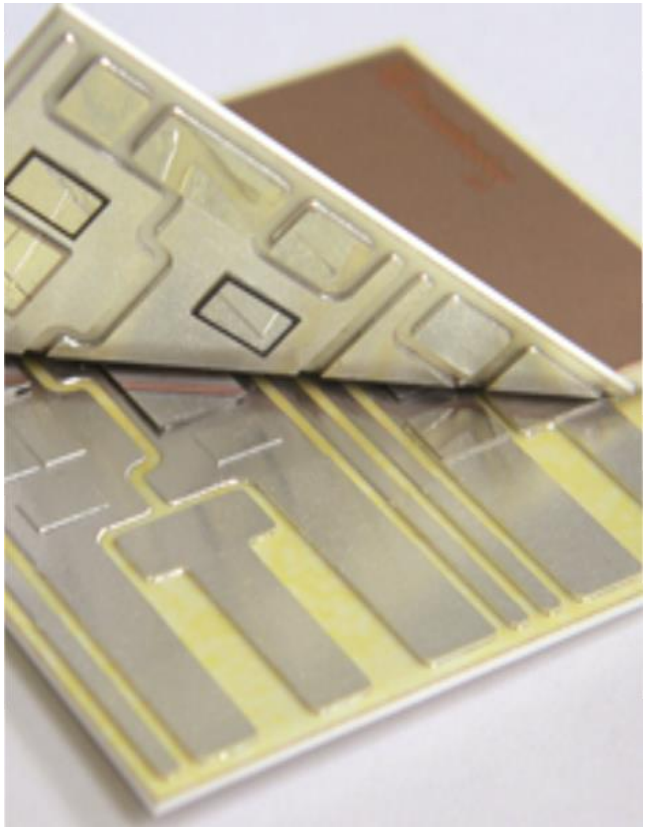
Packaging at Fraunhofer IISB

- **Fraunhofer IISB concepts from public projects**
- **Project ULTIMO** (Double-sided Power Module)
- Chips sintered on both sides in DCBs
- High power density
- Low number of different materials
- Cooling on both sides possible



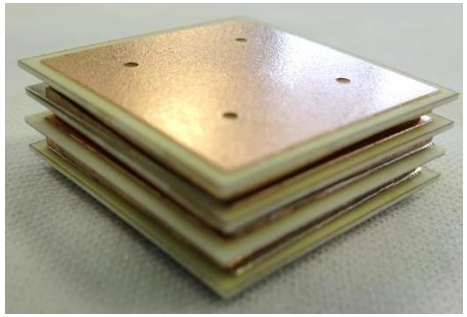




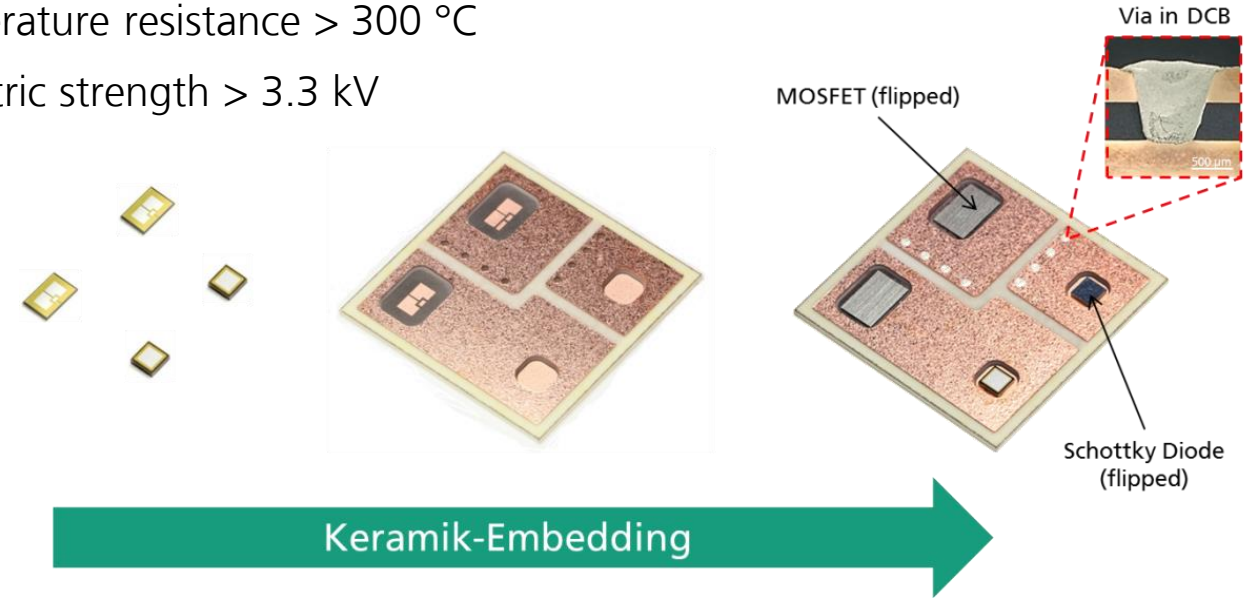


Packaging and interconnection technologies for power electronics

Packaging at Fraunhofer IISB



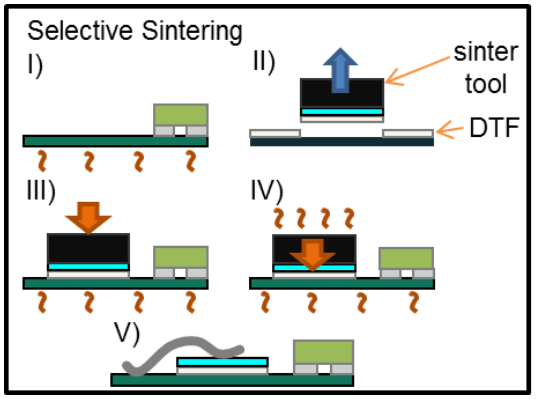
- **Fraunhofer IISB concepts from public projects**
- **Projekt DiaLe** (Ceramic/ DCB Embedding)
- WBG components embedded in DCBs
- Multilayer DCB stack realizable
- Flexible generation of vias in DCB
- High temperature resistance > 300 °C
- High dielectric strength > 3.3 kV

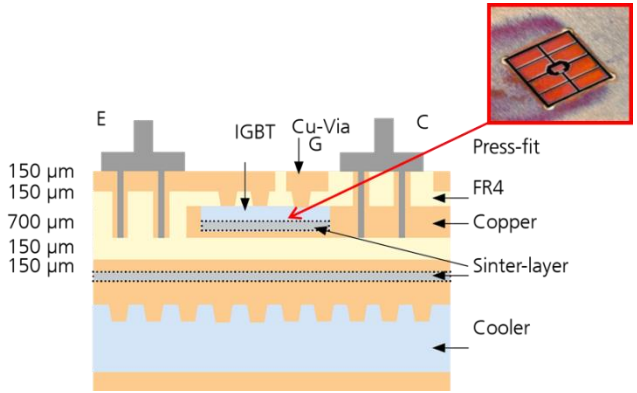


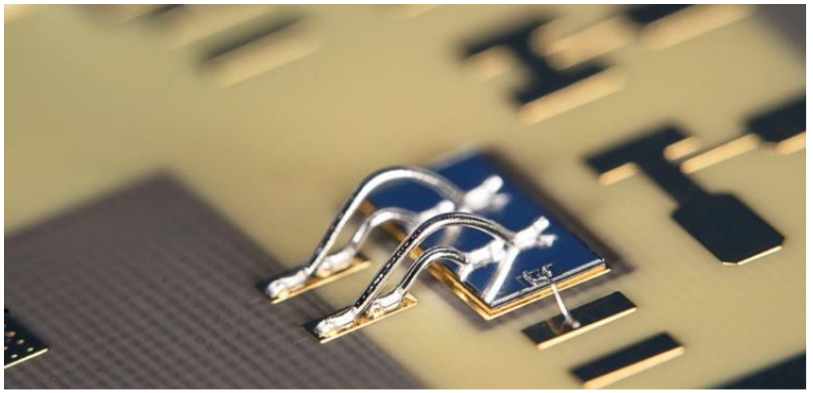
Packaging and interconnection technologies for power electronics

Packaging at Fraunhofer IISB

- **Selective silver sintering**
- Sintering of bare dies or SMD components on PCB
- Sintering on leadframe for chip embedding



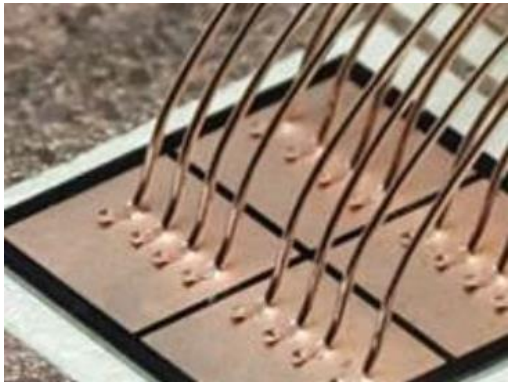


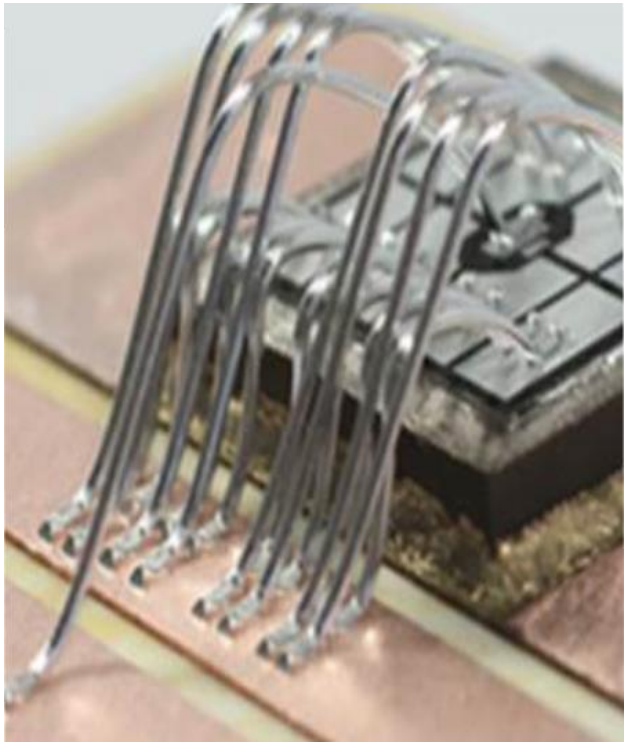


Packaging and interconnection technologies for power electronics

Packaging at Fraunhofer IISB

- **Chip metallization and wire bonding**
- Bonding wires Al, Cu, AlCuCore, Au...
- Metallization as desired for bonding, soldering, silver sintering, etc...





Packaging and interconnection technologies for power electronics

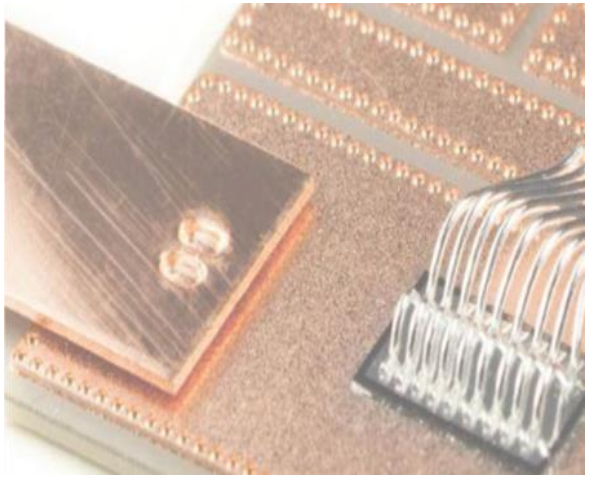
Packaging at Fraunhofer IISB

- **Top side chip contacting**
- Pressureless silver sintering with leadframe
- High current carrying capacity and reliability

Packaging and interconnection technologies for power electronics

Packaging at Fraunhofer IISB

- **Resistance spot welding of copper terminals on DCB**
- Cu-Cu bonding
- No intermediate / connection layer
- Low thermomechanical stress formation during the process
- High reliability



Packaging Technologies in Power Electronic Modules

- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - Packaging concepts
  - Interconnection technologies
  - Packaging at Fraunhofer IISB
  - **Thermal design and insulation coordination**
- Simulation process and theoretical consideration
- Test procedure and analysis
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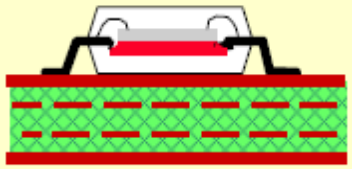
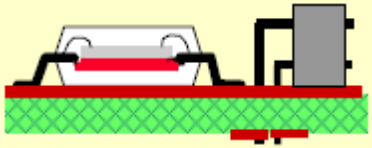
Packaging and interconnection technologies for power electronics

Thermal design

- **Thermal optimization possibilities of the assembly technology**

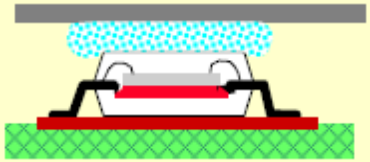


Heat Spread

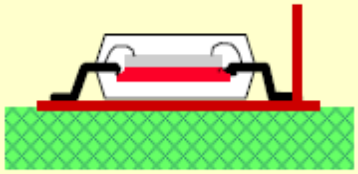


Heat dissipation

Heat sink



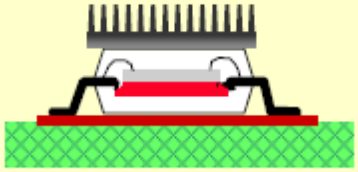
Gap filler



Extra heat sink or heat pipe

Convection

Thermal vias



Double sided cooling

Packaging and interconnection technologies for power electronics

Insulation coordination - principles, terms and standards

- Aim of the insulation coordination
  - Prevention of hazards to people and malfunctions in electrical equipment during its entire service life in the intended environment
    - Sparkover of airgap
    - Leakage currents on insulating material surfaces
    - Breakdowns of solid insulating materials
- Procedure
  - Dimensioning of insulating sections to the voltage stress, which is expected during operation
  - Standards for insulation coordination for minimum values

Packaging and interconnection technologies for power electronics

Insulation coordination - principles, terms and standards

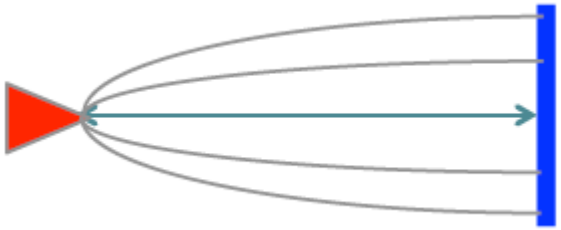
European Standards

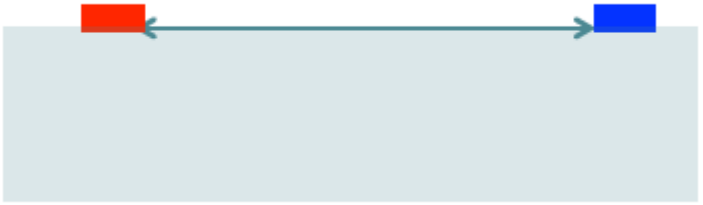
- Basic standards **EN 61140 / protection against electric shock**
  - Field of application → Electrical installations, systems and equipment without limitation of voltage, current, type of current and for frequencies up to 1 kHz
- Product family standards **EN 60664-... / Insulation coordination for electrical equipment in low voltage systems**
  - Application range → Up to 1000 V AC with rated frequencies up to 30 kHz and 1500 V DC up to an operating altitude of 2000 m above sea level
- Product standards **EN 61800-... / Variable-speed electrical drives**
  - Field of application → Excluded are railway drives and electric vehicle drives

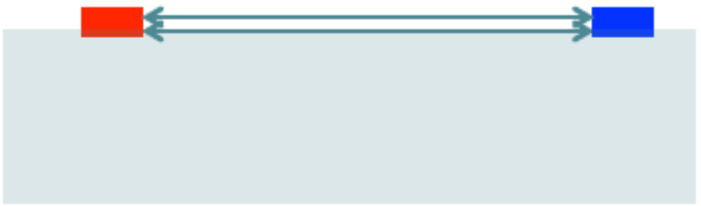
Packaging and interconnection technologies for power electronics

Insulation coordination - principles, terms and standards

- Air gap
  - Shortest distance in air between two conductive parts
- Creepage distance
  - Shortest distance along the surface of an insulating material between two conductive parts
- A creepage distance must not be smaller than the associated clearance
  - The smallest possible creepage distance is at least as large as the associated clearance







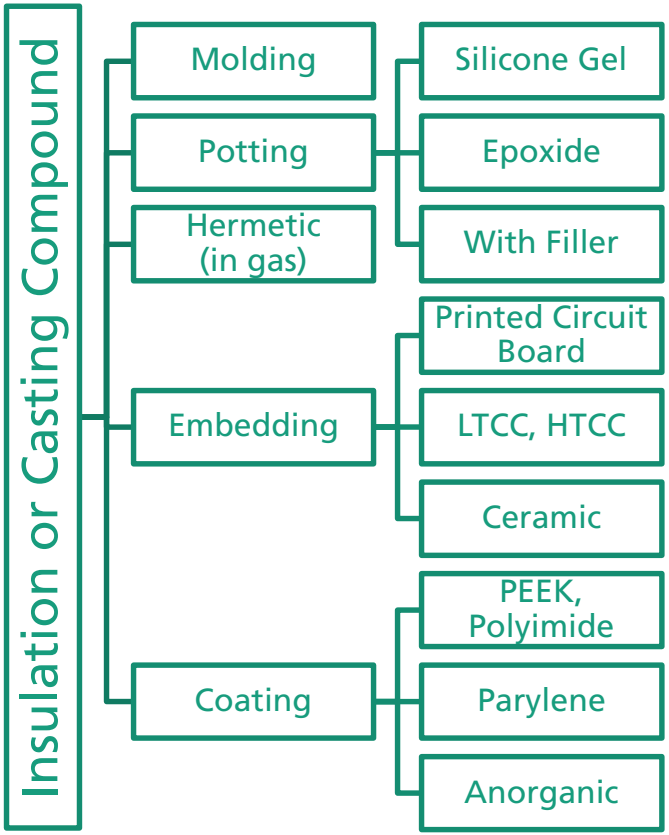
Packaging and interconnection technologies for power electronics

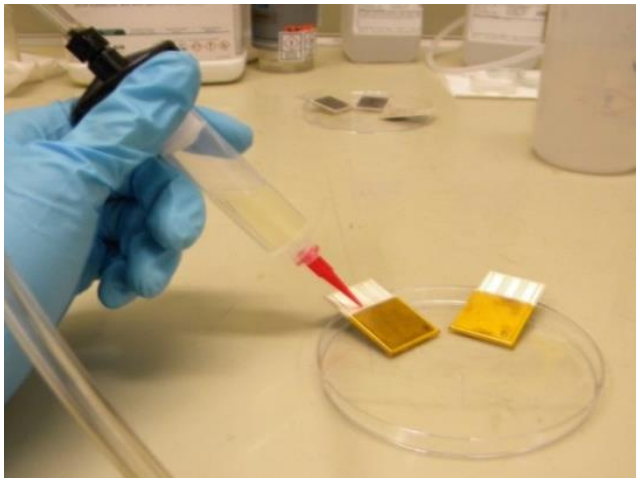
Insulation coordination - principles, terms and standards

- Further remarks on insulation coordination
  - The determination of clearance and creepage distances requires not only knowledge of the standards but also a great deal of knowledge of circuit technology, the function and the operating conditions of the equipment
  - With complex circuit boards or substrates, the dimensioning of the clearance and creepage distances can be a very confusing and tedious challenge
  - Software support is a good facilitation for the control of clearance and creepage distances

Packaging and interconnection technologies for power electronics

Insulation concepts





Potting examples	Silikone gel	Epoxide	Polyimide	PEEK
Dielectric strength in kV/mm	14 … 25	18 … 45	22 … 25	20
Electric conductivity σ in $(\Omega m)^{-1}$	10^{-13} … 10^{-14}	10^{-13} … 10^{-14}	10^{-12} … 10^{-13}	10^{-14}
Relative permittivity ε_r	2,7 …3,0	3,3 … 7,2	2,8 … 3,6	3,2
CTE in 10^{-6} K^{-1}	290 … 400	40 … 170	54	50
Flexural strength in MPa		55 … 125	116	
Modulus of elasticity in Gpa		1,1 … 5,0	3,3	3,0
Thermal conductivity λ in W $m^{-1}K^{-1}$	0,20 … 1,10	0,48 … 2,1	0,35	0,25
Operating temperature in °C	<260	<240	<300	<260

Packaging and interconnection technologies for power electronics

Insulation concepts – risk of corrosion

Electrochemical Migration ECM – clip (https://www.iisb.fraunhofer.de/en/research_areas/packaging_reliability/corrosion.html)

Thank you for your attention!

- Packaging at Fraunhofer IISB
- New Concepts and Materials for Packaging
- High Performance Joining Technologies, Sintering
- Thermal, Electrical, and Mechanical Characterization
- Lifetime Characterization, Statistical Analysis
- Analysis of Failure Mechanism
- Lifetime Modeling

Packaging Technologies in Power Electronic Modules

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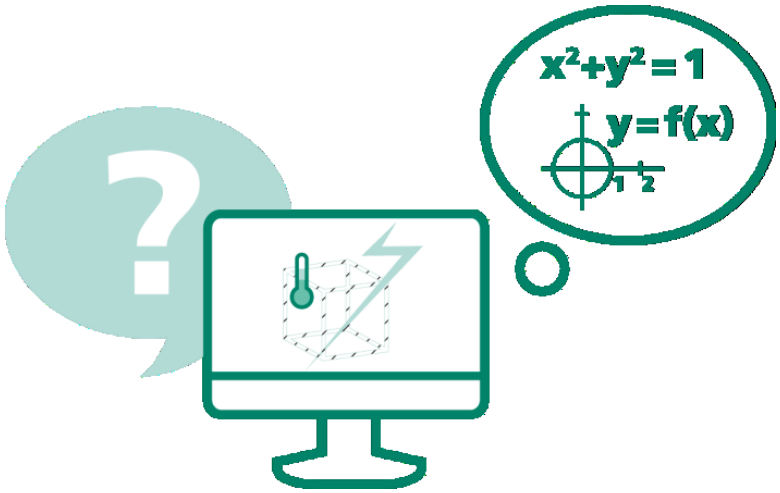
Simulation methods and theoretical consideration

Fundamentals of simulation

What is simulation?

“The simulation or simulation is...



...a procedure for the analysis of systems that are too complex for theoretical or formulaic treatment. In simulation, experiments are carried out on a model to gain knowledge about the real system. The procedure of the simulator with concrete values (parameterization) is called simulation experiment. Its results can then be interpreted and transferred to the system to be simulated.“

Simulation methods and theoretical consideration

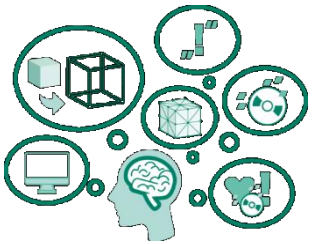
Fundamentals of simulation

- **Expectations**
- Building understanding of the problem and the materials involved
- Extension of the understanding of the effects of physical processes and behavioral prediction
- Reduction of development time, development costs and production costs, saving of material, reduction of test series
- Early detection of weak points, failure prediction
- Quality improvement and optimization of the construction
- Flexible adaptation to subsequent constructions
- Further training
- And much more...

Simulation methods and theoretical consideration

Fundamentals of simulation

- **Requirements**
- Modelling understanding (experiment → calculation model)
- FEM theory: Knowledge of the basics
- Training period for the software
- Powerful and problem specific software (ABAQUS, COMSOL, PLM, CST, ANSYS, JMAG, ISAFEM, MECHANICA, NASTRAN, PERMAS, CD-Adapco, FEMM, OpenFOAM, Keysight ADS, 6SigmaET, and many more)
- Powerful hardware (PC, Workstation, Mainframe, Cluster, Cloud)
- Expert or engineering knowledge for critical evaluation of the results



Simulation methods and theoretical consideration

Fundamentals of simulation

- **Simulation possibilities**
- Static and dynamic strength calculations, electrical, electromagnetic, magnetic, thermal, mechanical, thermomechanical, vibration mechanics problems
- Chemical and physical reactions, separation or combustion processes
- Vibration analysis on electrical machines, stresses and deformations (elastic and plastic, e.g. virtual crash tests using finite element methods), flow simulation
- Semiconductor devices, heat conduction processes, optical systems, fusion reactors, accelerators and nuclear reactions, doping and diffusion, electromigration
- Electrical properties, circuit simulations
- Couplings, reductions, optimizations, and much more...

Simulation methods and theoretical consideration

Parasites in power module

$$\Phi_j = \sum_i \frac{q_i}{4\pi\varepsilon|\vec{r_i} - \vec{r_j}|}$$

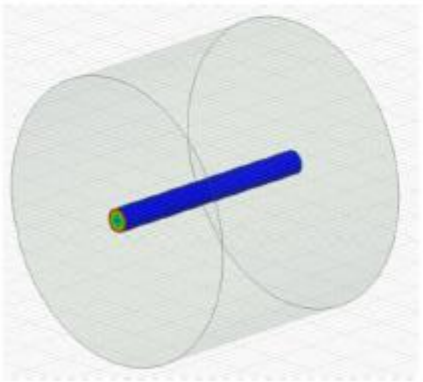
- **Physical basics**
- Calculation of internal and coupling capacities in FEM
  - Calculation of the charge distributions in conductors and the induced charge distributions on the surface of dielectrics
  - Ratio of voltage to charge gives the capacity $C = \frac{Q}{U}$
- Calculation of inductances and resistances
  - DC: Calculation of current distribution (FEM) and vector potential (FMM) Inductance and resistance
  - AC: All currents are considered as surface currents (BEM), but are corrected with a skin effect correction factor depending on frequency (magnetic field distribution, current distribution and vector potential result in inductance and resistance)

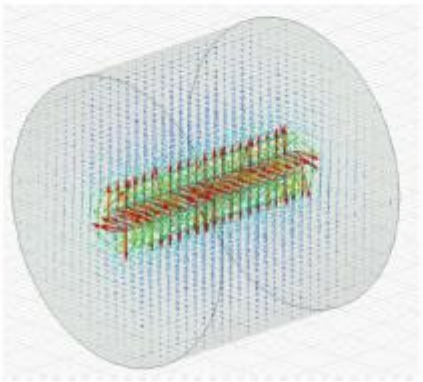
Simulation methods and theoretical consideration

Parasites in power module

- **Physical basics**
- FEM versus BEM (e.g., here Ansys Maxwell versus Ansys Q3D)

Ansys Maxwell (FEM)	Ansys Q3D (BEM)
- Berechnung der Umgebung/ Plenum benötigt - Felddarstellungen in dem umgebenden Material möglich - Künstliche Randbedingungen möglich	- Berechnung der stromleitenden Volumen - Stromdichte/ Felder nur in (DC) oder auf (AC) berechneter Geometrie - Ziemlich schnell…





Simulation methods and theoretical consideration

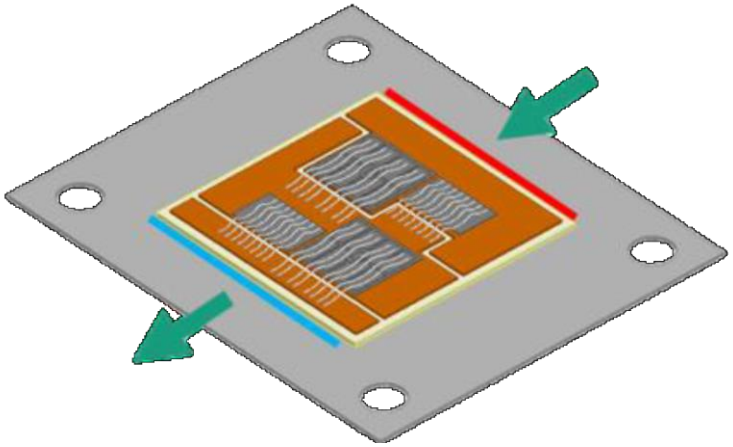
Parasites in power module

- **What can be simulated?**
- Calculation of the own capacities and coupling capacities of the individual conductors → Capacity matrix
- Low-frequency (DC) and high-frequency (AC) inductors and resistors → Inductance matrix
- ➢ C, L and R are simulated for different conductor and dielectric arrangements for two-dimensional and three-dimensional problems
- Export of component properties for circuit simulations
- ➢ Creation of equivalent circuit diagrams for Maxwell Spice, Berkley Spice, HSPICE, PSPICE, Spreadsheet Format, IBIS Package Model, Ansoft Serenade, Cadence DML, etc.

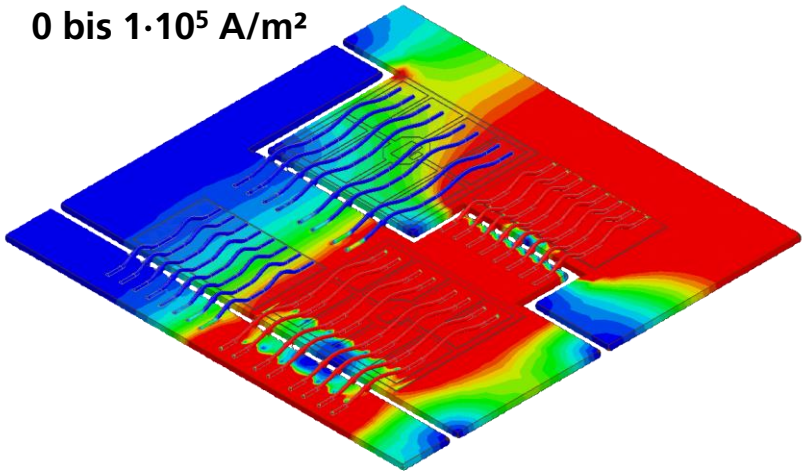
Simulation methods and theoretical consideration

Parasites in power module

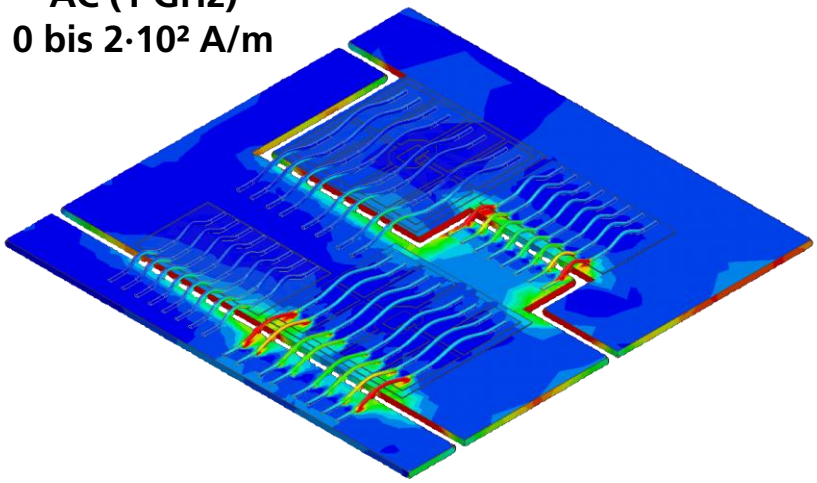
- **What can be simulated?**
- Frequency dependent current density distribution



DC
0 bis $1 \cdot 10^5$ A/m²



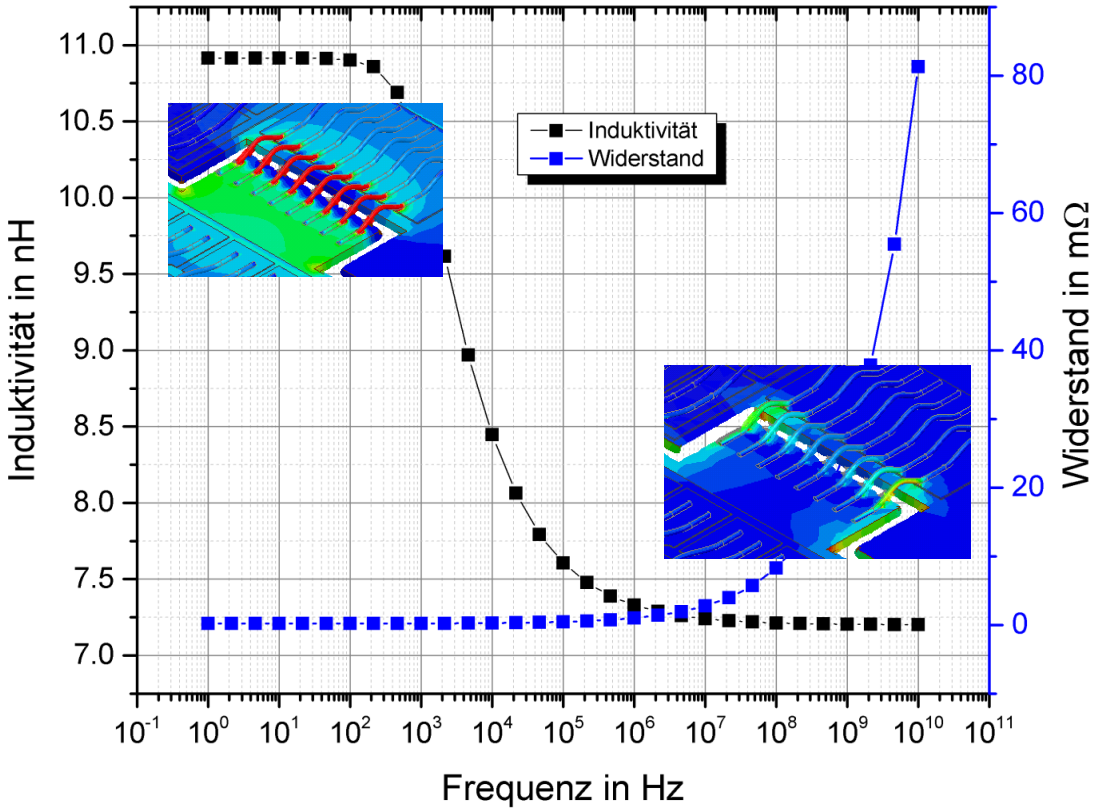
AC (1 GHz)
0 bis $2 \cdot 10^2$ A/m



Simulation methods and theoretical consideration

Parasites in power module

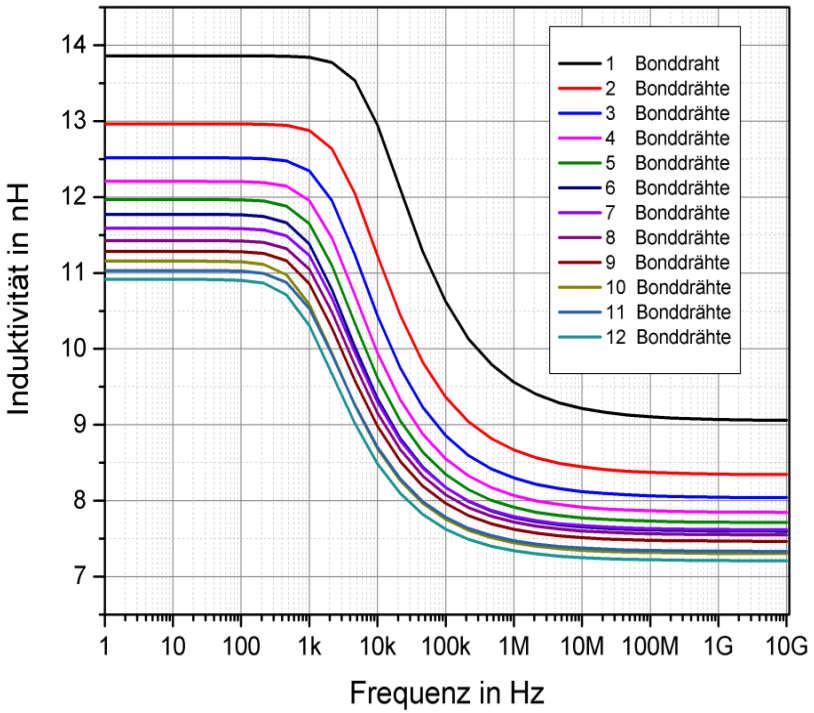
- **What can be simulated?**
- Frequency dependent inductance

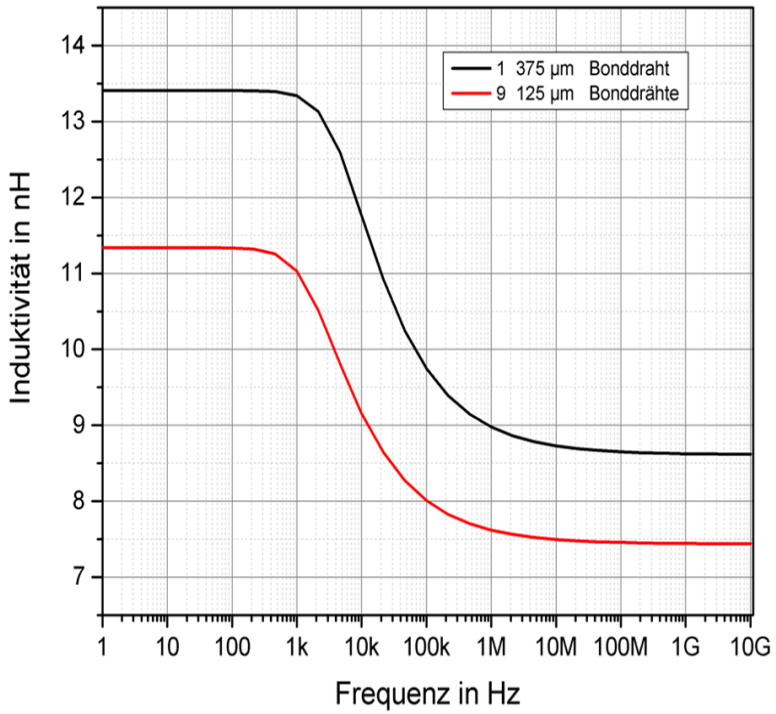


Simulation methods and theoretical consideration

Parasites in power module

- **What can be simulated?**
- Example Variation of the number and thickness of bond wires in the power module

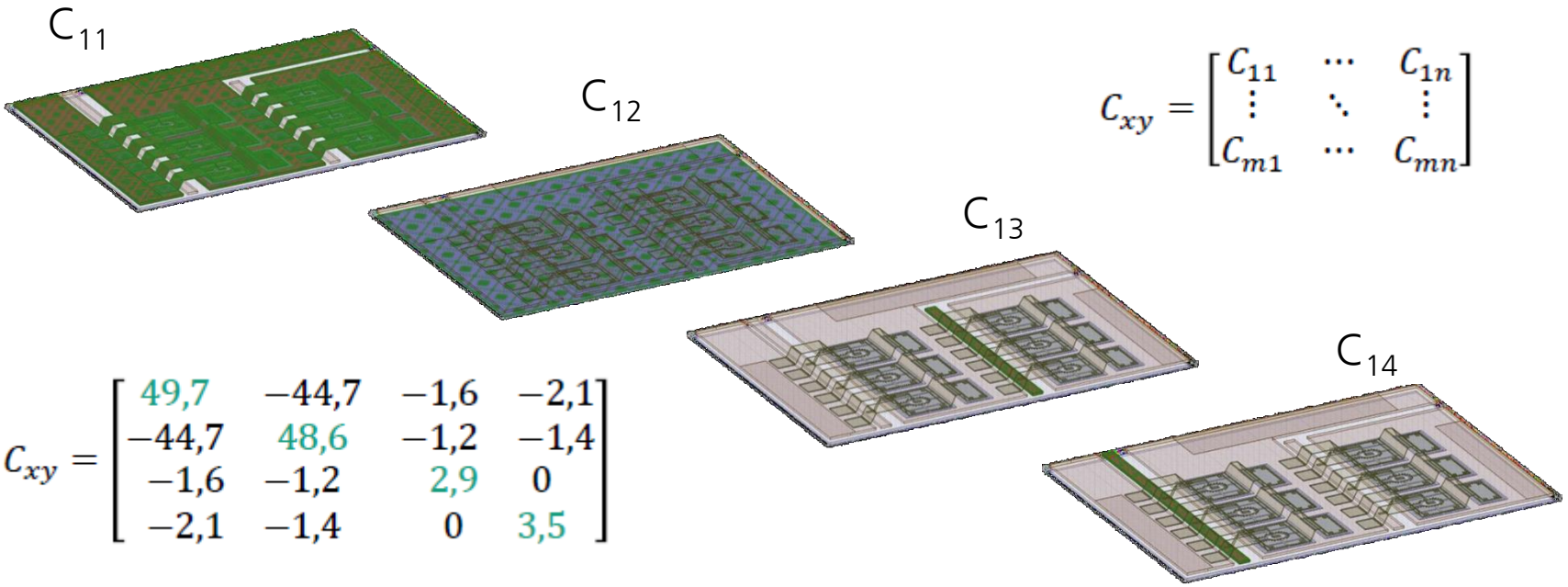




Simulation methods and theoretical consideration

Parasites in power module

- **What can be simulated?**
- Capacity and coupling capacitances in pF
- Frequency dependence only with loss factor tan(δ) in the dielectric



Simulation methods and theoretical consideration

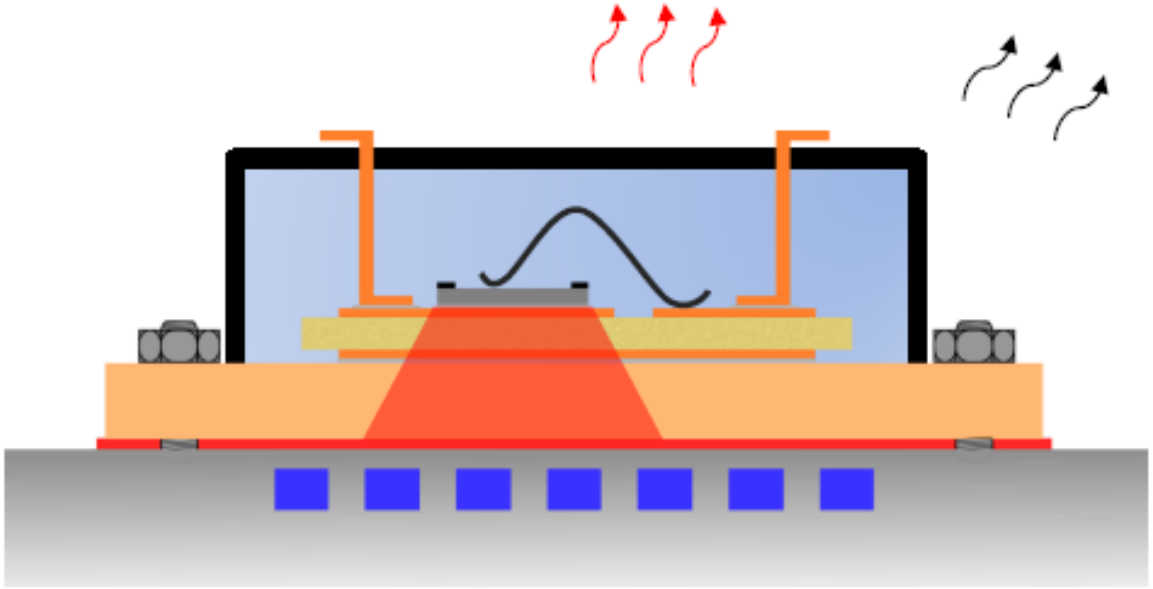
Parasites in power module

- **Risks, problems and inaccuracies**
- Disregard of the simulation restrictions
  - Explicit calculation for 'good' electrically conductive materials only for very low frequencies (DC) and very high frequencies (AC)
    - ➢ Estimate skin effect for materials used
    - ➢ Observe distances of conductive components (due to wave propagation HFSS)
- Inaccuracies in networking
  - Self-generated short circuits due to 'surface-penetrating' cross-linking
  - Insufficient networking or poor aspect ratio
    - ➢ Checking the current density distribution

Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Physical basics**
  - Heat transfer mechanisms



$$E_{in} + E_{gen} - E_{out} = E_{res}$$

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Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Physical basics**
- Unsteady/ transient heat conduction

➢ $\boldsymbol{\rho \cdot cp \cdot \left(\frac{dT}{dt}\right) + \lambda \cdot \nabla^2 \cdot T = P_V}$

- Calculation of thermal behaviour in case of overloads/ surge currents
- Thermal capacity C_{th} of a structure

$$C_{th} = c_{th} \cdot \rho \cdot V$$

- Thermal diffusivity α

$$\alpha = \frac{\lambda}{\rho \cdot c_{th}}$$

	ρ kg/m³	c_{th} kJ/kgK	λ W/mK	α 10^{-6} m²/s
Al	2,7	0,88	237	98,8
Cu	8,9	0,382	399	117

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Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Physical basics**
- Coupling of a temperature field with structural mechanics
- Temperature increase of a material causes a change in length $\Delta\varepsilon$ or thermal expansion as a function of the thermal expansion coefficient CTE

$$\Delta\varepsilon = CTE \cdot \varepsilon_0 \cdot \Delta T$$

- (Thermo-)Mechanical stress σ as a function of elastic modulus E and thermal strain $\Delta\varepsilon$

$$\sigma = E \cdot \Delta\varepsilon \quad \Rightarrow \quad F = \sigma \cdot A$$

Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **What can be simulated?**
- Temperature distribution (in electronic components)
  - Thermal expansion and thermal influence zones
  - Calculation of the maximum temperatures of semiconductors and derivation of the thermal resistances of different assembly concepts
  - Analysis of heat flows
- Transient temperature distribution
  - Cooling curves (Z_{th})
  - Accidents/impulse loads
- Thermo-mechanical (stationary/instationary)
  - Deformations
  - Mechanical stresses and strains (elastic/plastic)

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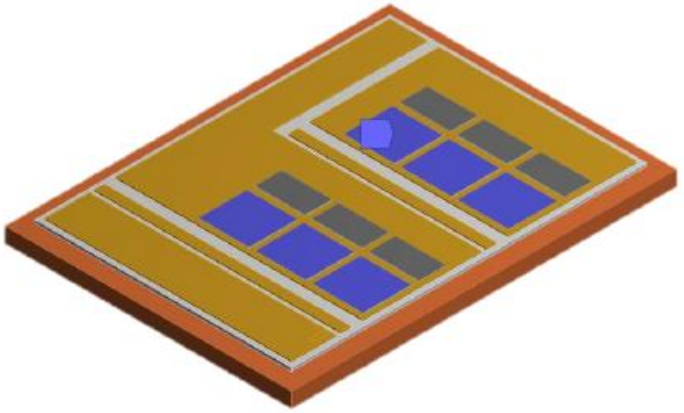
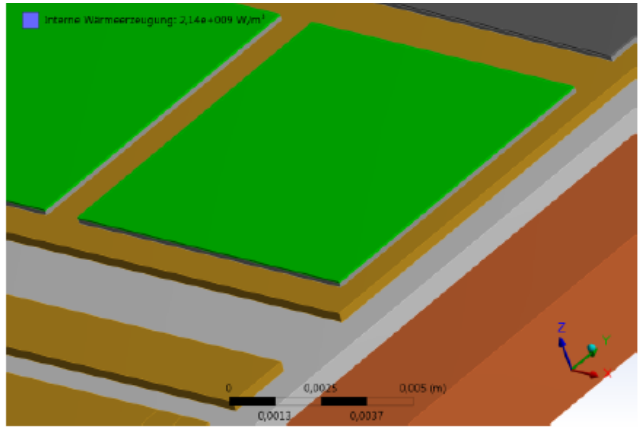
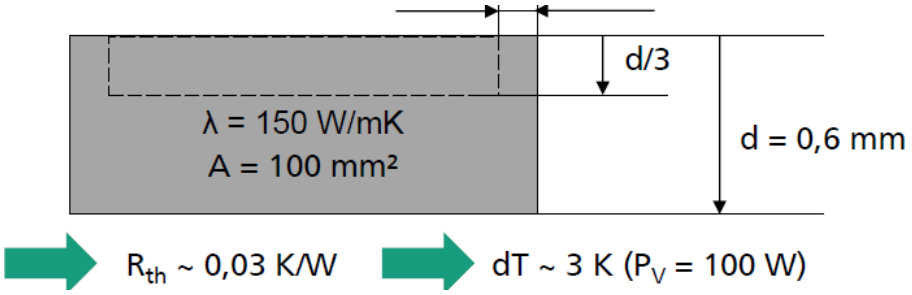
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Defining boundary conditions**
- Obtaining power dissipation
  - Heat flow (on surface)
  - Heat flux density (on surface)
  - Internal heat generation (volume) e.g. 150 W Chip volume
- Differentiation active/passive chip area useful for HV chips







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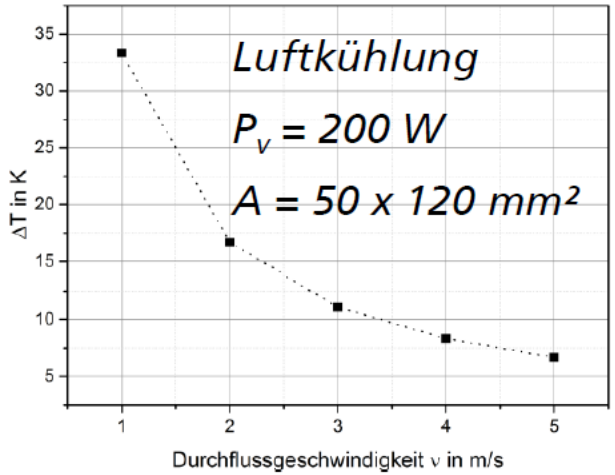
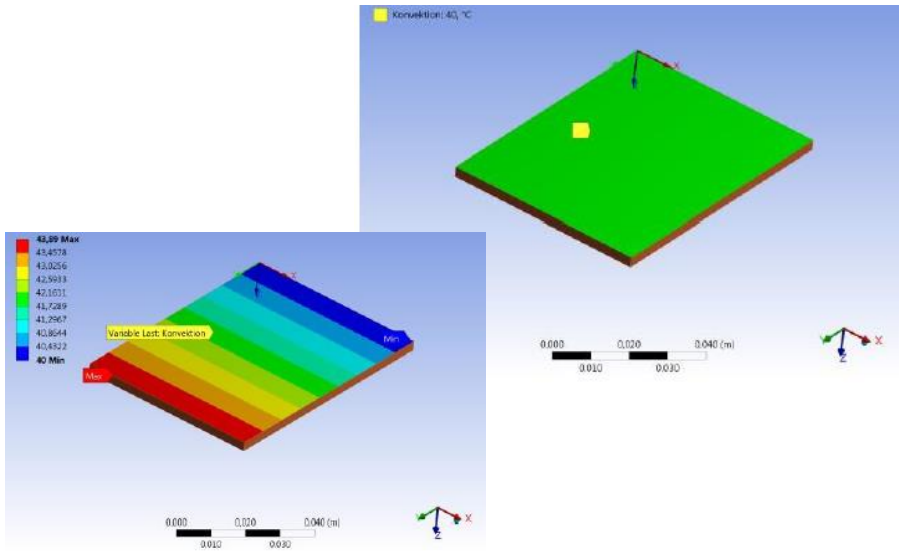
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Defining boundary conditions**
  - Assumption of cooling capacities by heat transfer coefficients (αK)
  - Constant coolant temperature
  - Variable coolant temperature
    - Consideration of heat input and inlet/outlet temperature

$$P_V = A \cdot v \cdot \rho \cdot c_p \cdot (T_{out} - T_{in})$$

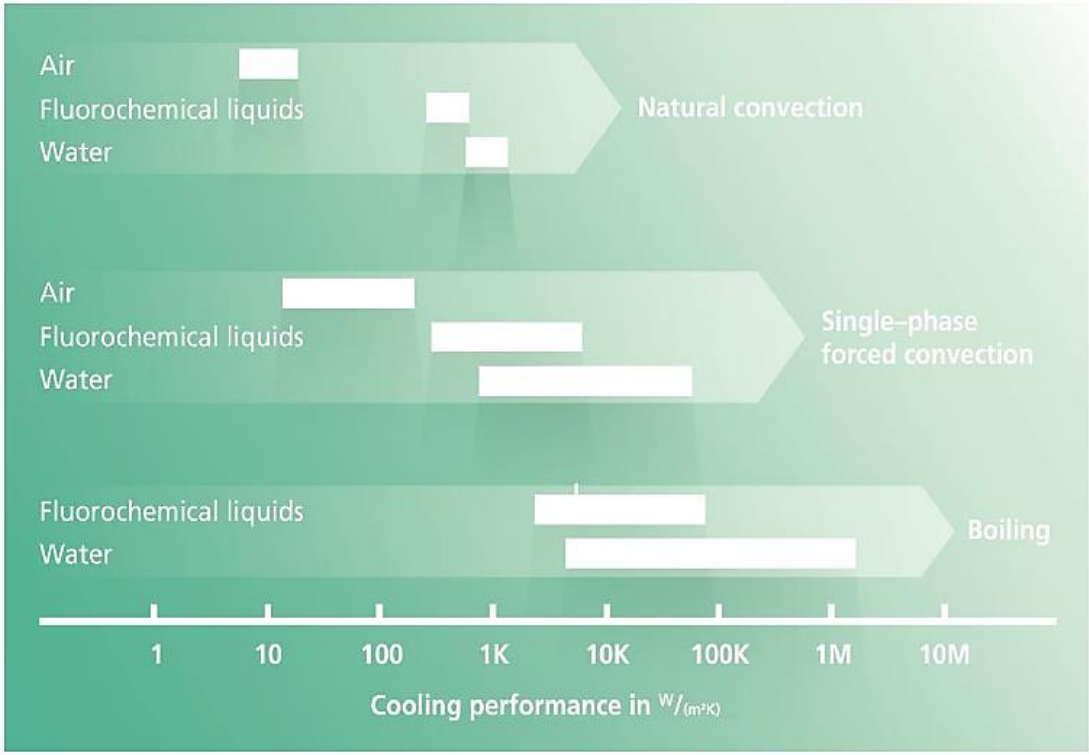




Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Defining boundary conditions**
  - Assumption of cooling capacities through heat transfer coefficients (αK) versus coolant temperature
  - Air cooling
    - 5 W/m²K (natural horizontal)
    - 20 W/m²K (natural vertical)
    - 500 W/m²K (forced, fins)
  - Water-cooling
    - 5,000 W/m²K (4 l/min)
    - 20,000 W/m²K (12 l/min)
  - 2-phase cooling*
    - 80,000 W/m²K



* S. N. Joshi, E. M. Dede; Thermal management of future WBG devices using two-phase cooling – PCIM 2016

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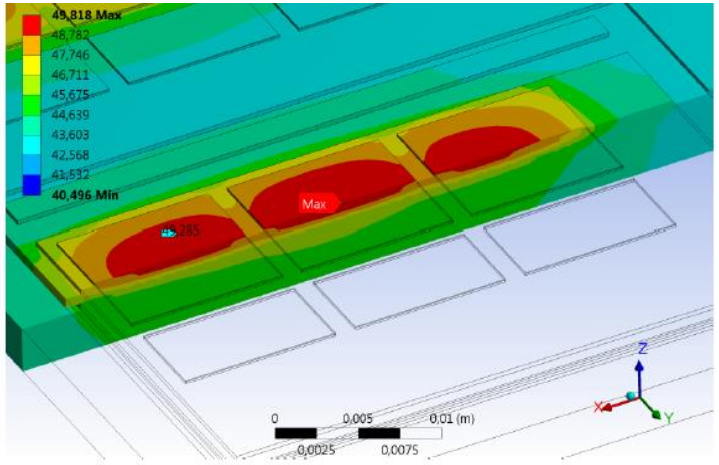
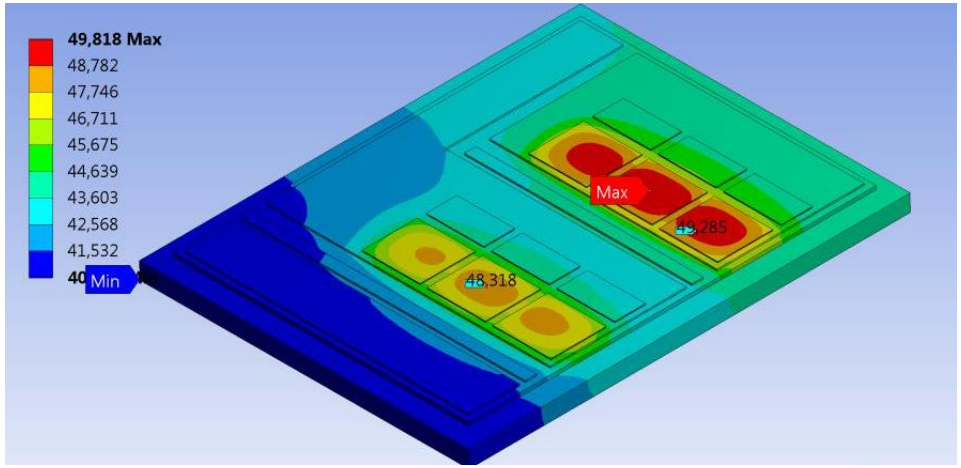
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **What can be simulated?** (Example in Ansys Workbench)
- Temperature distribution in the power module
- 150 W/chip (internal heat generation)
- α_K = 20,000 W/m²K against T_{min} = 40 °C

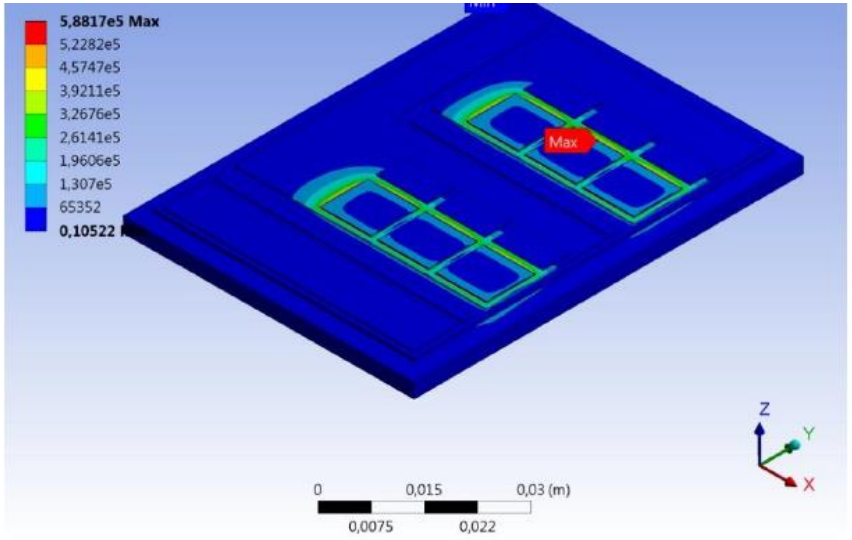


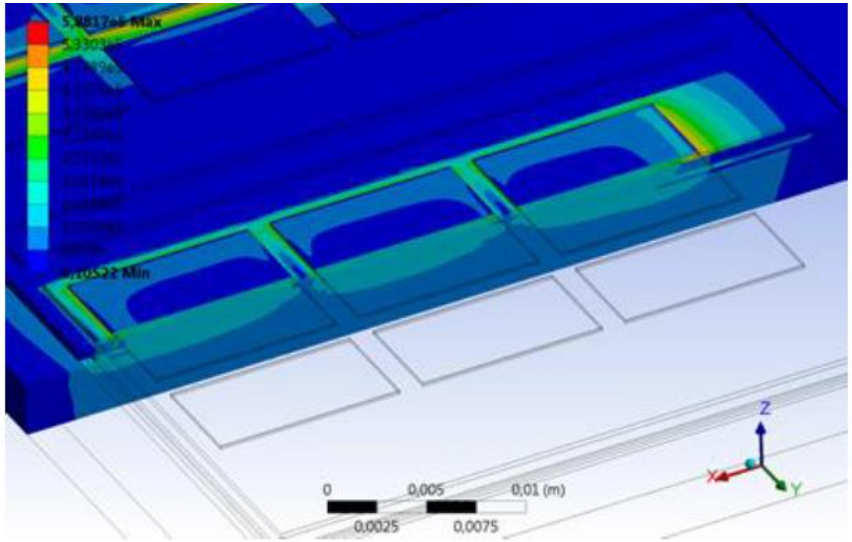


Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **What can be simulated?** (Example in Ansys Workbench)
- Heat flow
- 150 W/ chip (internal heat generation)
- αK = 20,000 W/m²K against T_{min} = 40 °C

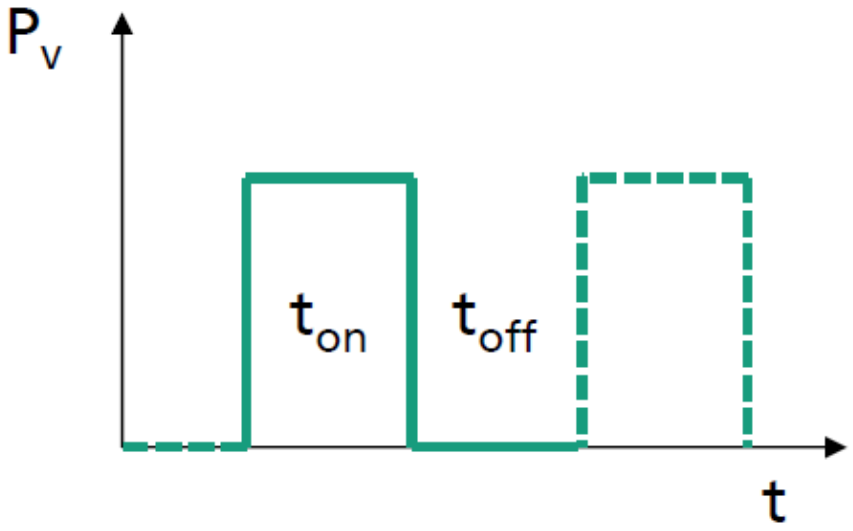




Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

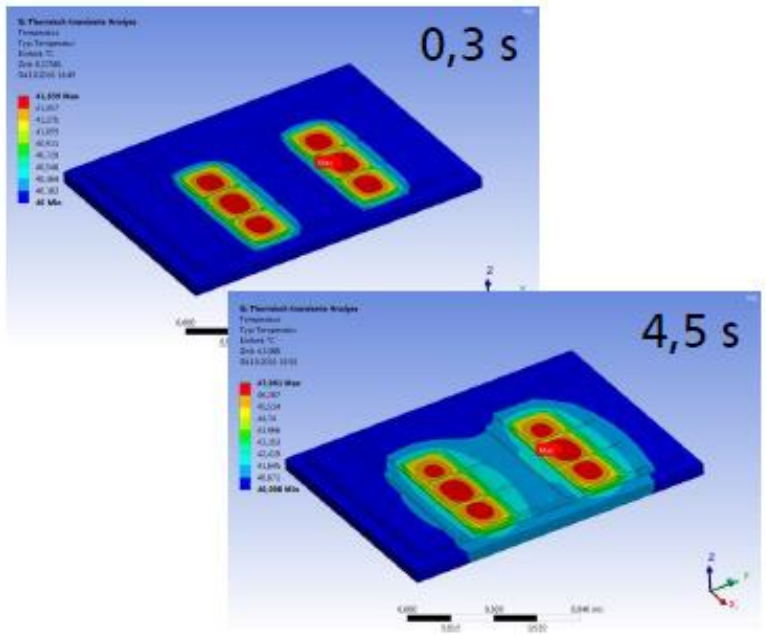
- **What can be simulated?**
- Transient temperature distribution
- Simulation of a power cycle
  - t_{on}/ t_{off} every 5 s
  - 150 W/ Chip
  - T_{min} = 40 °C
  - α_K = 20 kW/m²K
- Consider material data
  - Spec. thermal capacity
  - Density
- Time dependent internal heat generation
  - Formula → e.g. sinus function
  - Chart → Definition of load steps

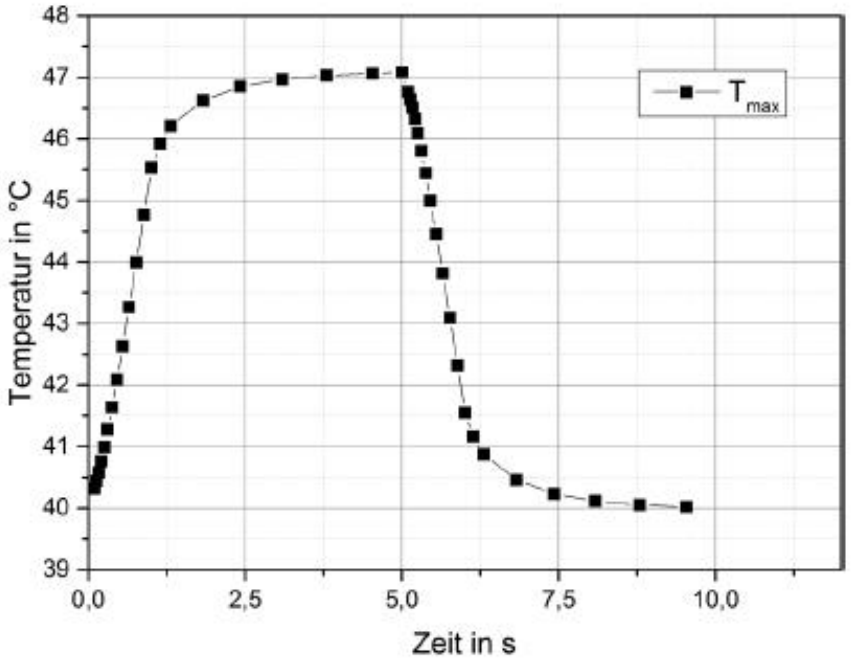


Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **What can be simulated?**
- Transient temperature distribution
- Graphical and chart temperature evaluation as a function of time

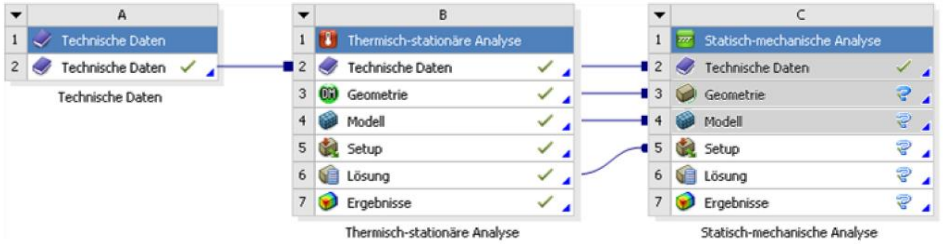




Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

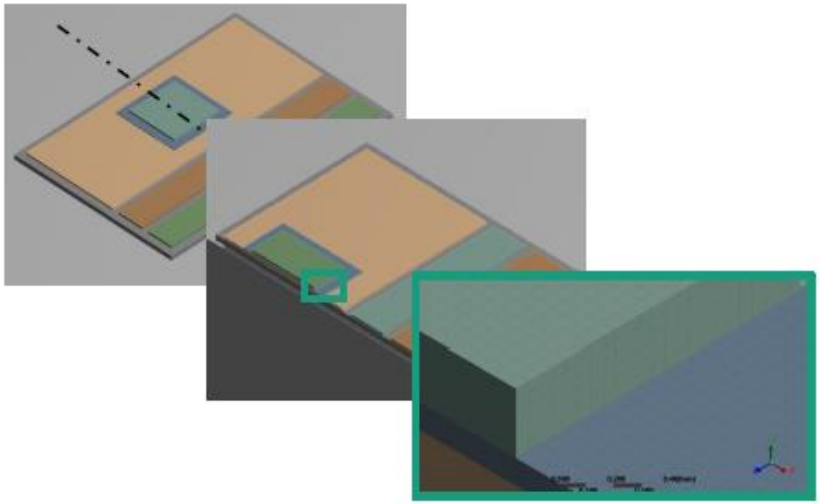
- **What can be simulated?**
- Coupling of a temperature field with structural mechanics
  - The thermal simulation results in a change in length of the individual components (deformation), which leads to mechanical tensions/strains
  - Contact areas of the individual components influence the stress/strain distribution (example: bond versus frictionless)
  - Output temperature and resulting temperature distribution of the bodies serve as input parameters for the mechanical simulation

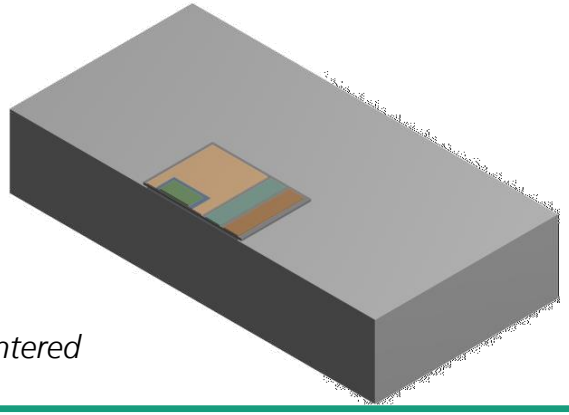


Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **What can be simulated?**
- Static-mechanical analysis
  - Temperature field = Imported load
  - Bearings
    - Model friction-free on base plate
    - Base plate fixed
    - Gravitational acceleration on geometry
  - Technical data
    - CTE
    - E-Modulus



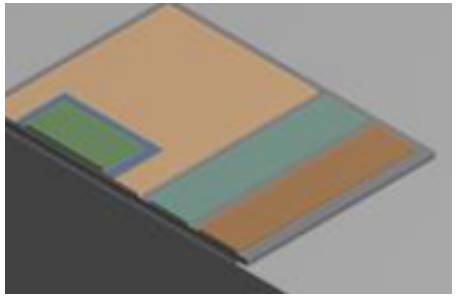


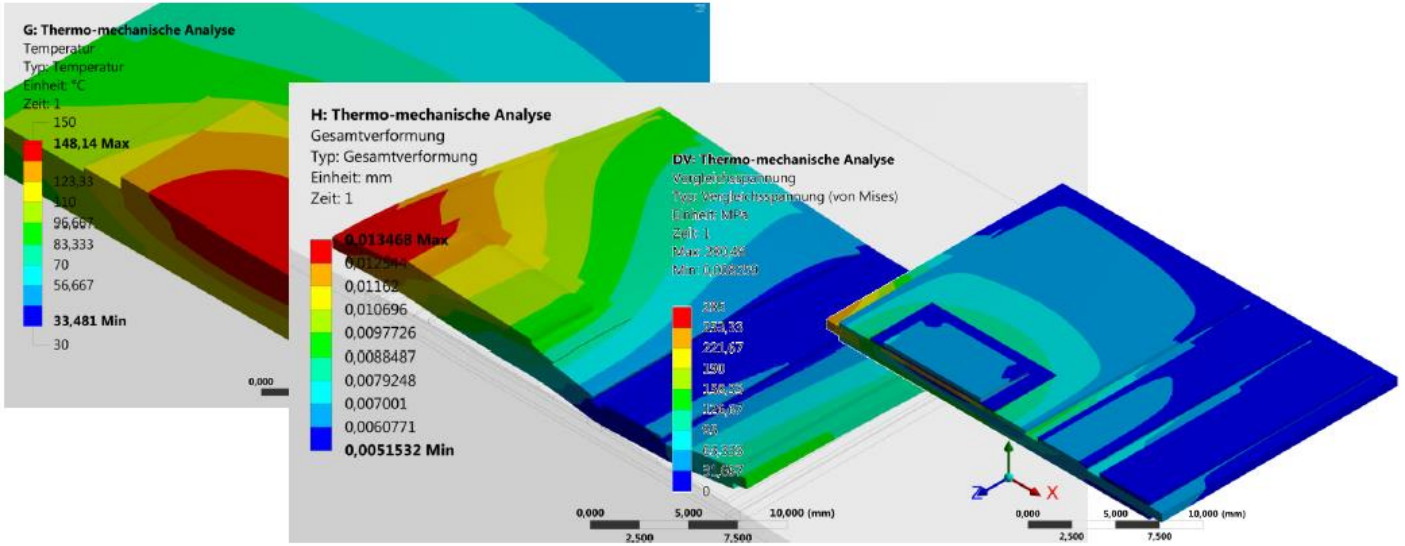
Beispiel:
Chip on DCB sintered

Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **What can be simulated?**
- Static-mechanical analysis
- CTE- Mismatch of the individual layers leads to
  - Deformation of the model
  - Occurrence of mechanical stresses in the model





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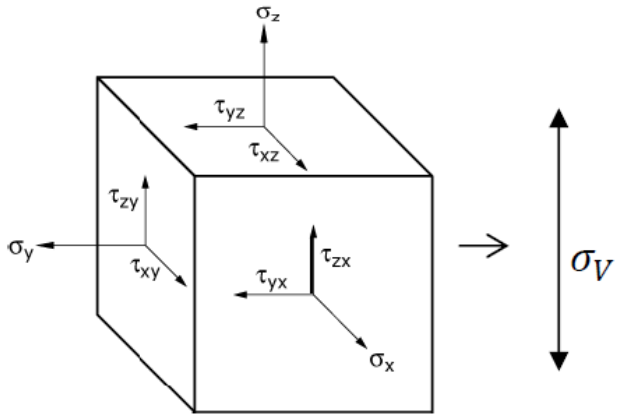
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Evaluation**
- Mises equivalent stress (GEH hypothesis)
  - The stress tensor

$$\begin{bmatrix} \sigma_x & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_y & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_z \end{bmatrix}$$



with elements of the normal stress σi and the shear stress τij can be reduced to a uniaxial stress by means of a comparative stress σV → Comparison with tensile strengths possible

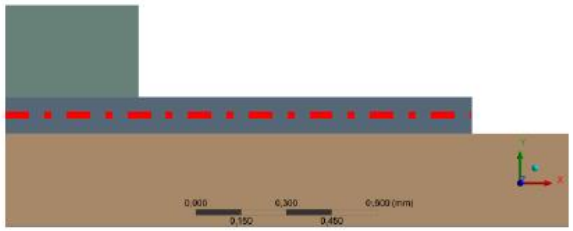
$$\sigma_V = \sqrt{\sigma_x^2 + \sigma_y^2 + \sigma_z^2 - \sigma_x\sigma_y - \sigma_x\sigma_z - \sigma_y\sigma_z + 3(\tau_{xy}^2 + \tau_{xz}^2 + \tau_{yz}^2)}$$

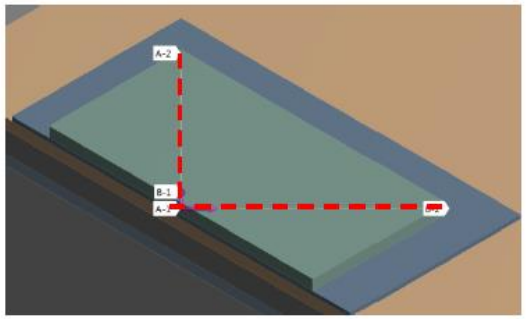
- Application for ductile materials → Solder/sinter connections, Cu, etc.

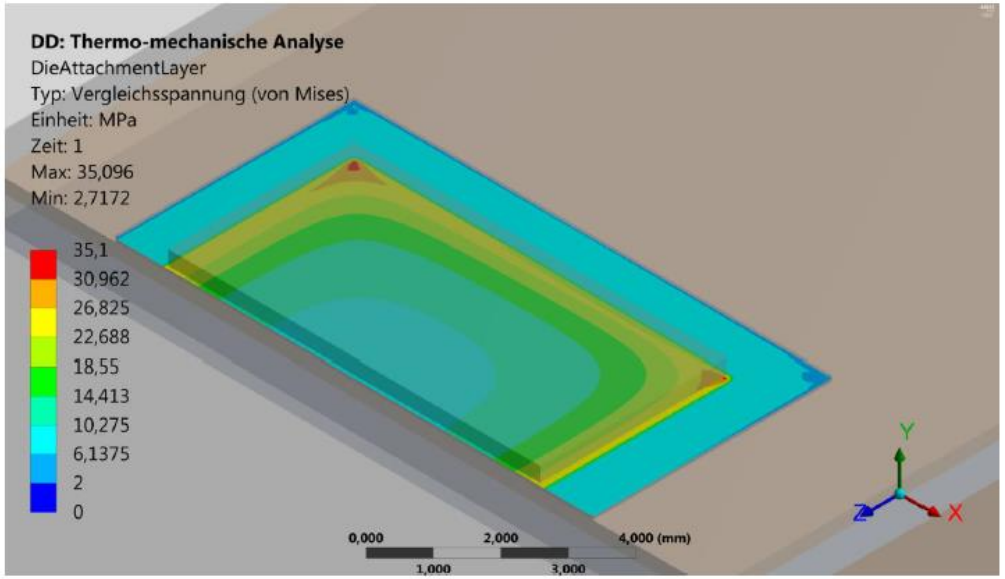
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Evaluation**
- Mechanical stresses in ductile compound layers
  - Cutting planes
  - Paths



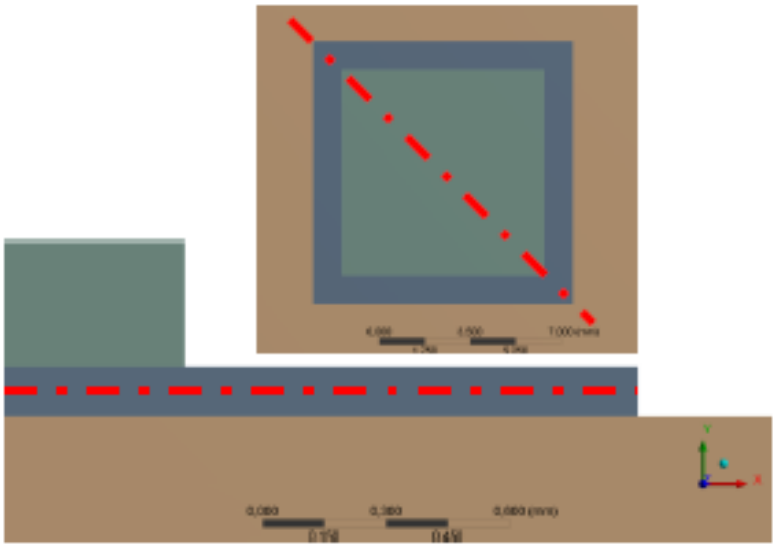


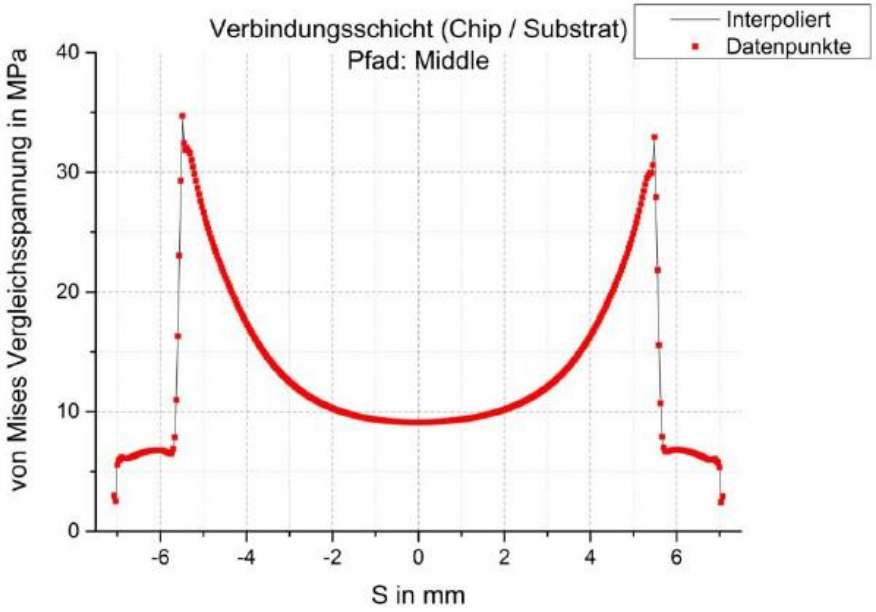


Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Evaluation**
- Mechanical stresses in compound layers along diagonal
  - Evaluation in the middle of the layer → Boundary layer network-dependent
  - Margin area not evaluable → singular





Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Evaluation**
- Normal stress hypothesis (plane stress state)

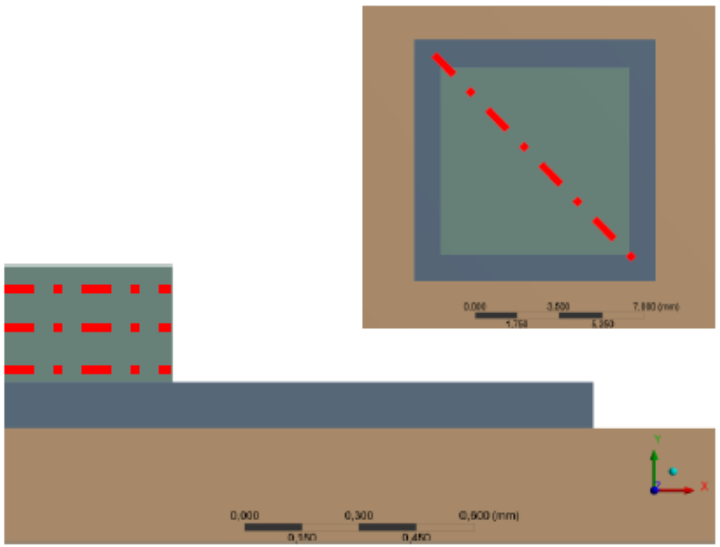
$$\sigma_v = \sigma_{1,2} = \frac{1}{2}\left[(\sigma_x + \sigma_y) \pm \sqrt{((\sigma_x - \sigma_y)^2 + 4{\tau_{xy}}^2)}\right]$$

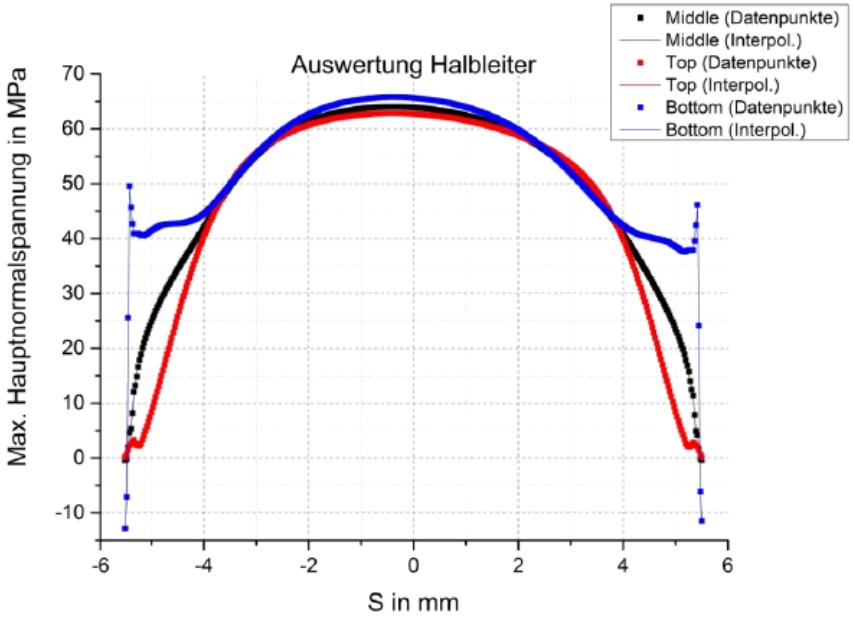
- Greatest normal stress = 1. Main stress
- Application for brittle materials → Si-Chip, Ceramic
- Tensile fracture strength of a Si chip is approx. 50 - 200 MPa* → Borders not taken into account!
- Evaluation (in Ansys):
  - Positive normal stress = tensile stress
  - Negative normal stress = compressive stress

Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Evaluation**
- Mechanical stresses in semiconductors along diagonal
  - Evaluation on diagonals in several planes of the chip
  - Margin area not analyzable→ singular

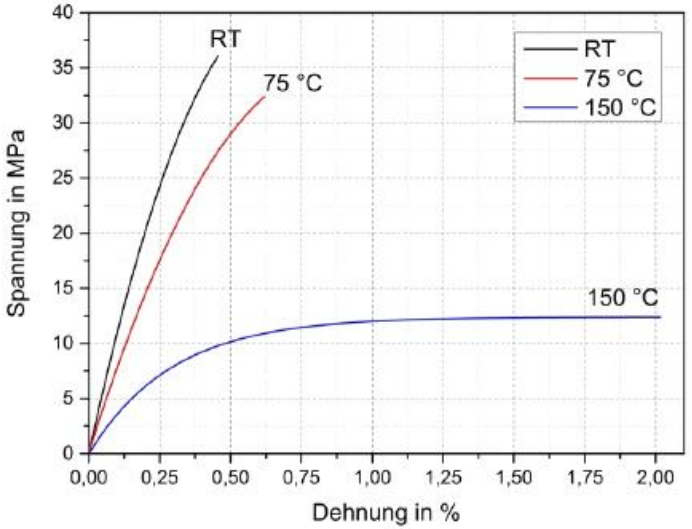




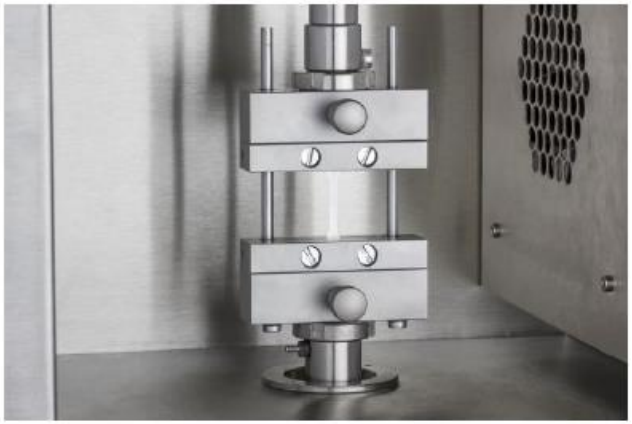
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

- **Further possibilities**
- Thermal simulation
  - Unsteady material properties
    - Phase transitions
      - Latent heat storage
      - 2 2 Phase cooling
  - Flux simulations (CFX/CFD)
    - Pressure drop in the cooling channel
    - Optimization of cooling structures
- Mechanical simulation
  - Plastic properties
  - Lifetime modelling
  - Crack propagation



Quelle: S.Letz – CIPS 2016



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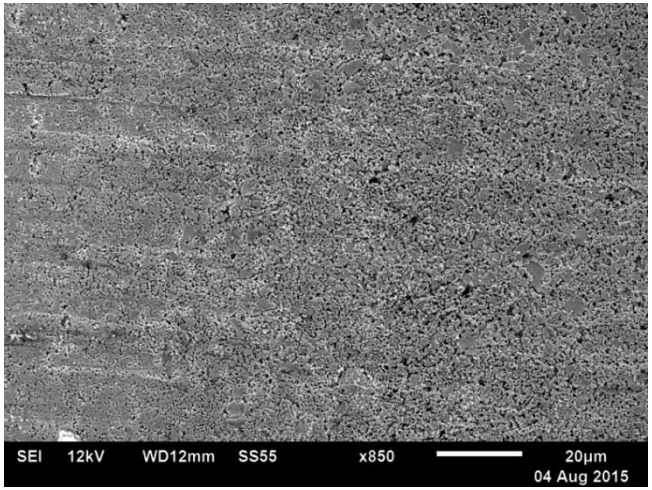
Simulation methods and theoretical consideration

Heat dissipation and deformation in power modules

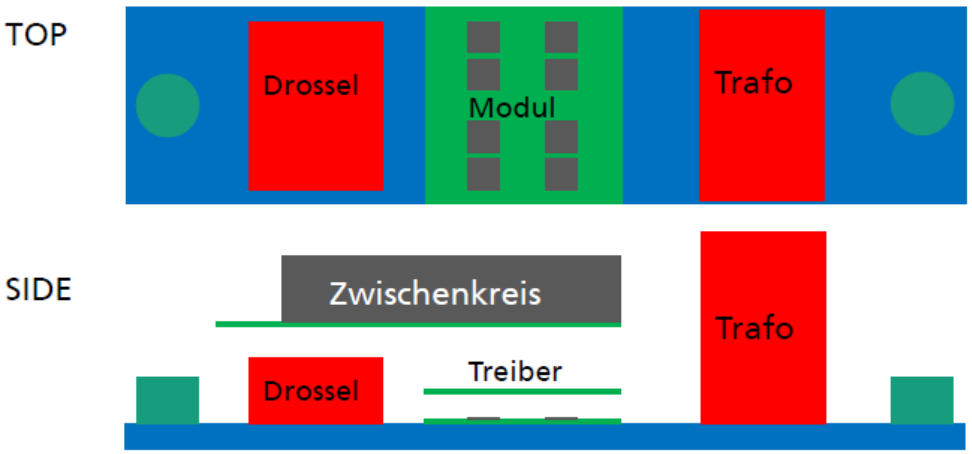
- **Risks, problems, inaccuracies**
- Material data
  - Temperature dependence
  - Plastic material data difficult to obtain (e.g. "What copper do I really have?"→ Cu-OFE? Cu-HCP? Cu-ETP? Cu-DHP?)
  - Influence of manufacturing processes? → Recrystallisation
- Network fineness (vs. computing time)
- Cooling capacities/ inflow conditions
- Evaluation at singular points not practical
- Idealization
  - Active volume in the chip
  - Layer thickness / homogeneity
  - Constant heat dissipation via cooling surfaces
  - Neglect of temperature-related process steps

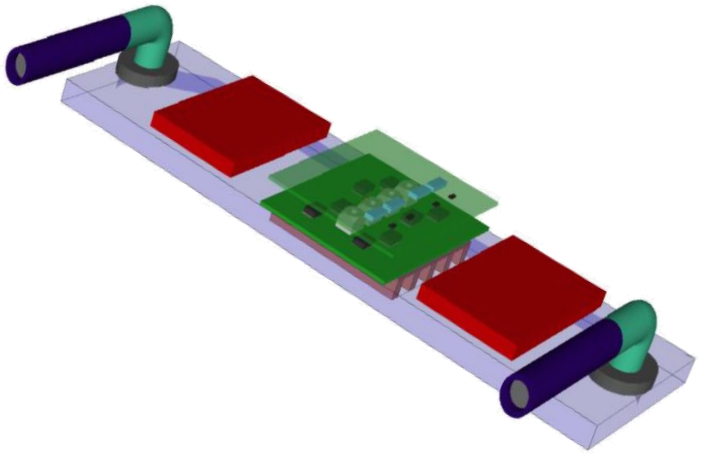


Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- **Example simulation with 6SigmaET**
  - Simulation of an isolating DC/DC converter
- Goals
  - Compliance with the component-specific boundary conditions
  - Identify challenges early on and develop solutions





Simulation methods and theoretical consideration

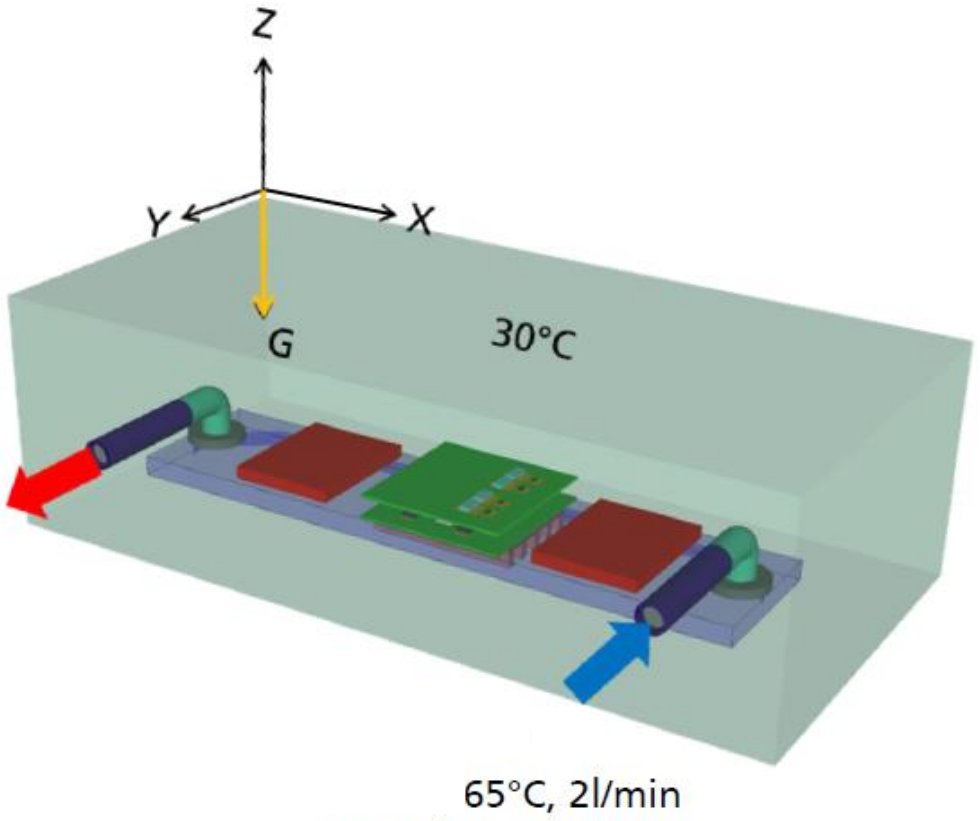
Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- Idealization
  - Right-angled edges
  - Ideal contact surfaces, solid-solid and fluid-solid
  - No roughness (with restriction)
  - No rounding (special networking)
  - Classification of the components according to their relevance
    - Detailed, Flow obstruction, Decorative
- Material data
  - Characteristic values for each material suitable for the desired simulation
  - See data sheet information
  - Verification of the data

Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

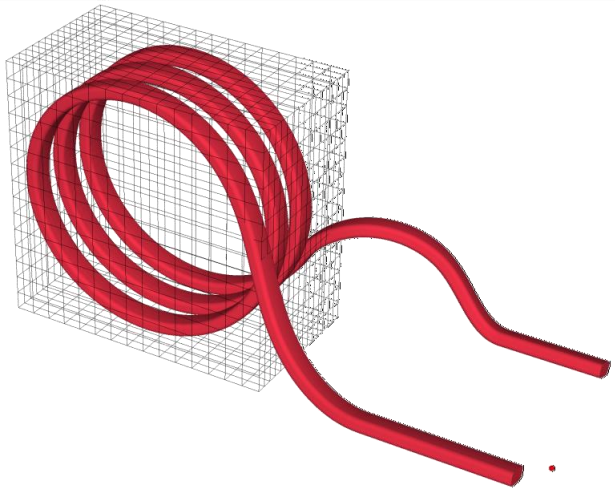
- Boundary conditions
  - Temperature
    - Environment
    - Coolant
  - Current
    - Components
    - Speed
    - Volume flow
  - Gravitation
  - Radiation

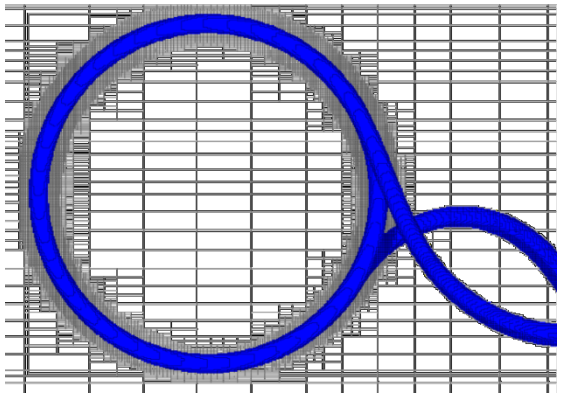


Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- Networking
  - Cartesian grid
  - Too large elements can lead to unwanted contact points
  - Grid Control Variants
    - Direction
      - Quantity
      - Size
    - Approximating the geometry
      - Size of the cells in the structure
      - Size of the cells in the surrounding fluid
      - Inflation

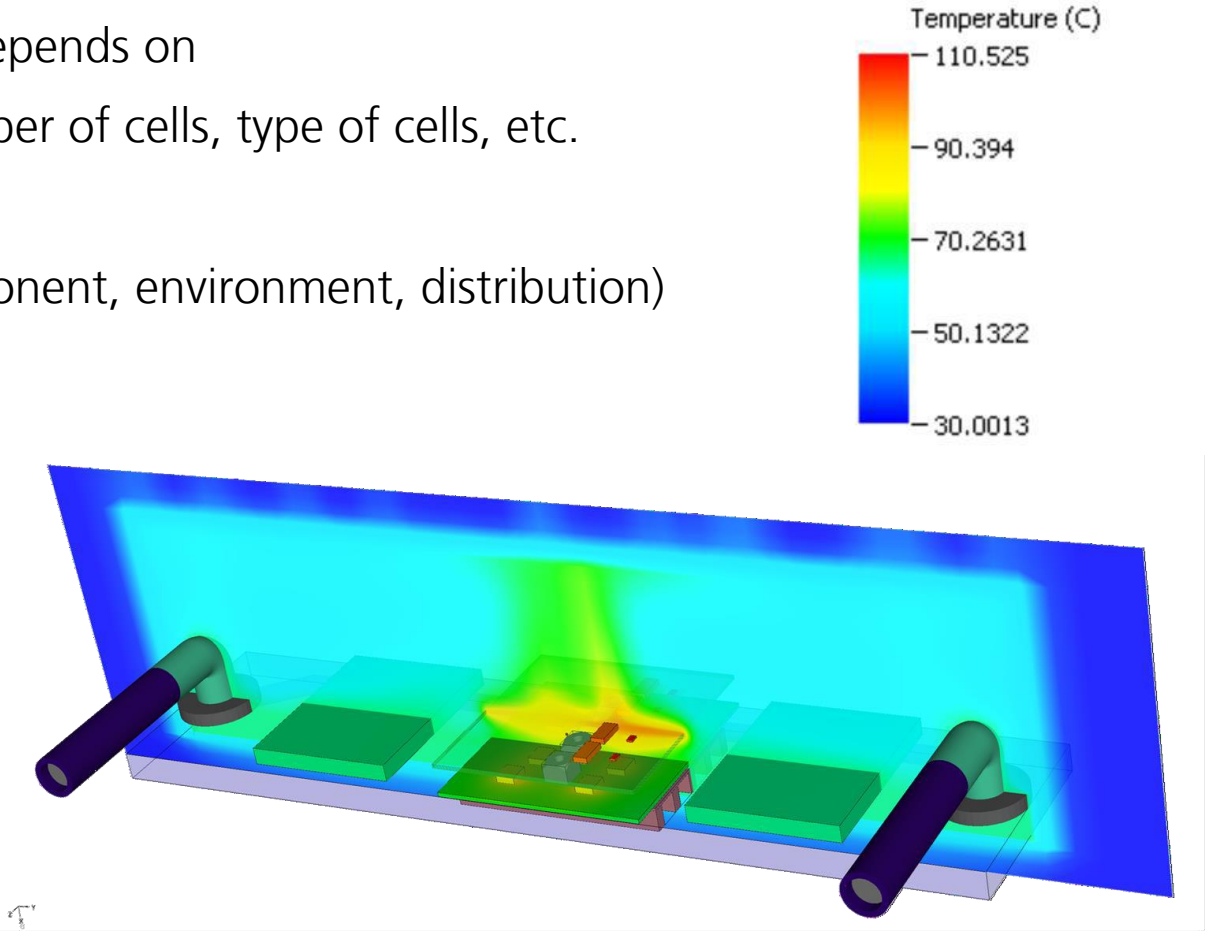




Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- The computing time depends on
  - parallelization, number of cells, type of cells, etc.
- Display of results
  - Temperature (component, environment, distribution)
  - Speed, pressure
  - Ohmic losses

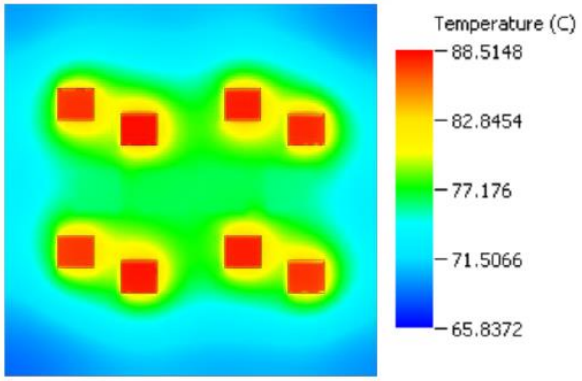


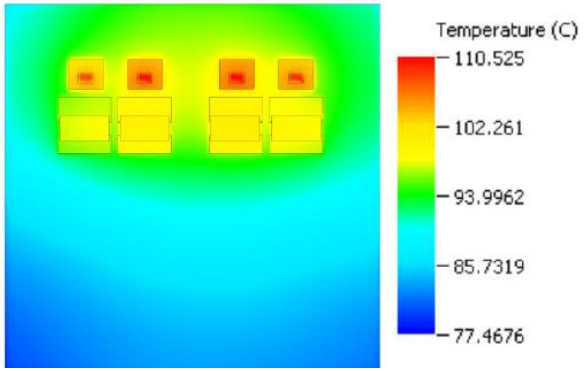
Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- Simulation result (example 6SigmaET)
  - List of the temperature of each component

	Owner PCB	Junction Temperature	Mean Volume Temperature
Gate_switch_1 (Case)	Driver_Board	108.1	108.1
Gate_switch_2 (Case)	Driver_Board	110.1	110.1
Gate_switch_3 (Case)	Driver_Board	110.6	110.6
Gate_switch_4 (Case)	Driver_Board	109.2	109.2
Switch_1 (IPT020)	Module	87.89	87.89
Switch_2 (IPT020)	Module	87.39	87.39
Switch_3 (IPT020)	Module	87.83	87.83
Switch_4 (IPT020)	Module	87.2	87.2
Switch_5 (IPT020)	Module	87.99	87.99
Switch_6 (IPT020)	Module	87.4	87.4
Switch_7 (IPT020)	Module	88.43	88.43
Switch_8 (IPT020)	Module	87.69	87.69
Gate_Resistor_1 (Resistor)	Driver_Board		97.97
Gate_Resistor_2 (Resistor)	Driver_Board		100
Gate_Resistor_3 (Resistor)	Driver_Board		100.5
Gate_Resistor_4 (Resistor)	Driver_Board		99.07

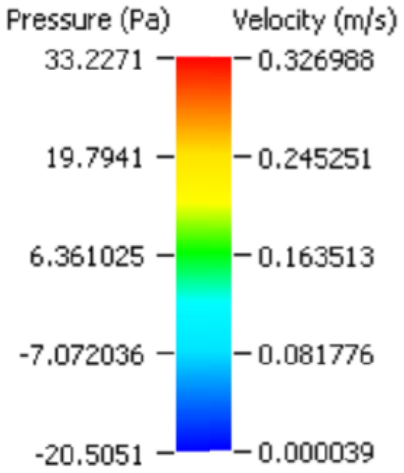


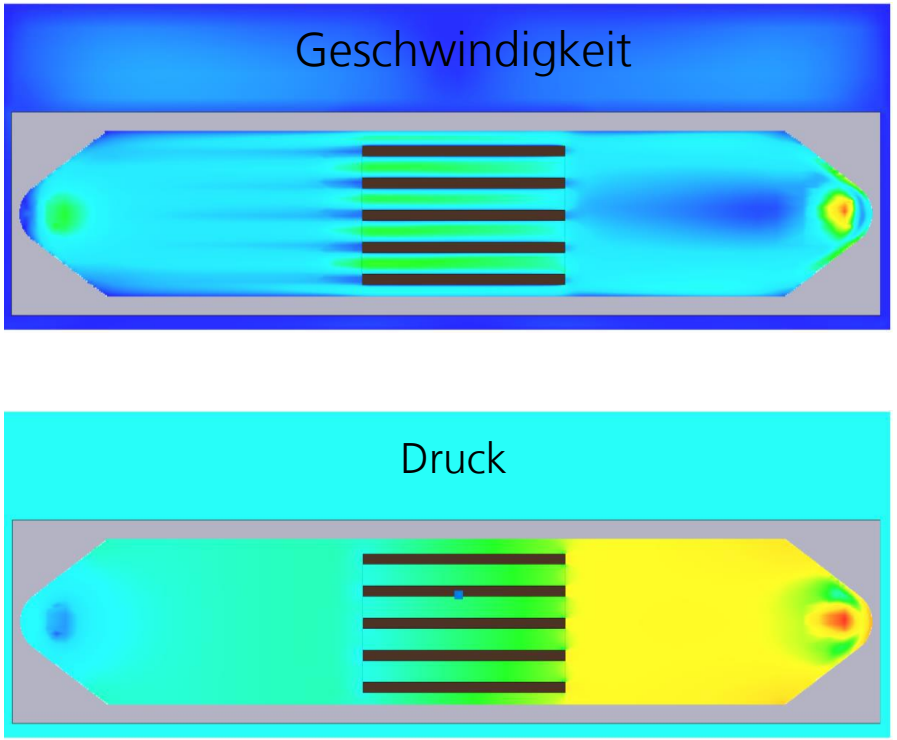


Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- Simulation result (example 6SigmaET)
  - Flow simulation





Dr. Christoph F. Bayer et al., Packaging and Modules
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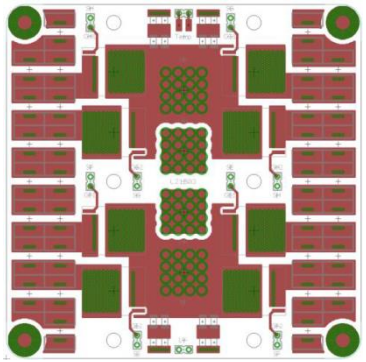
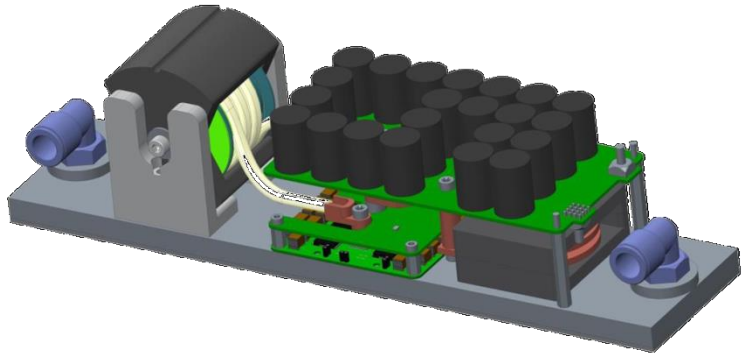
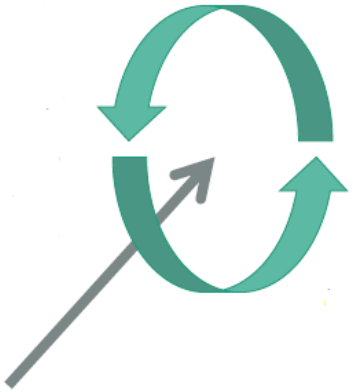
Simulation methods and theoretical consideration

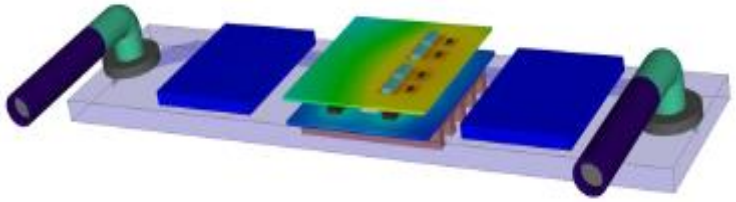
Thermal simulation of electronic systems during design - Conjugate Heat Transfer

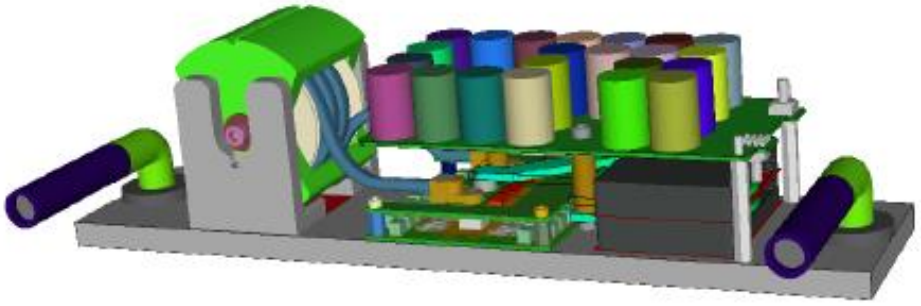
- Model iterations → Import of CAD data, layout programs







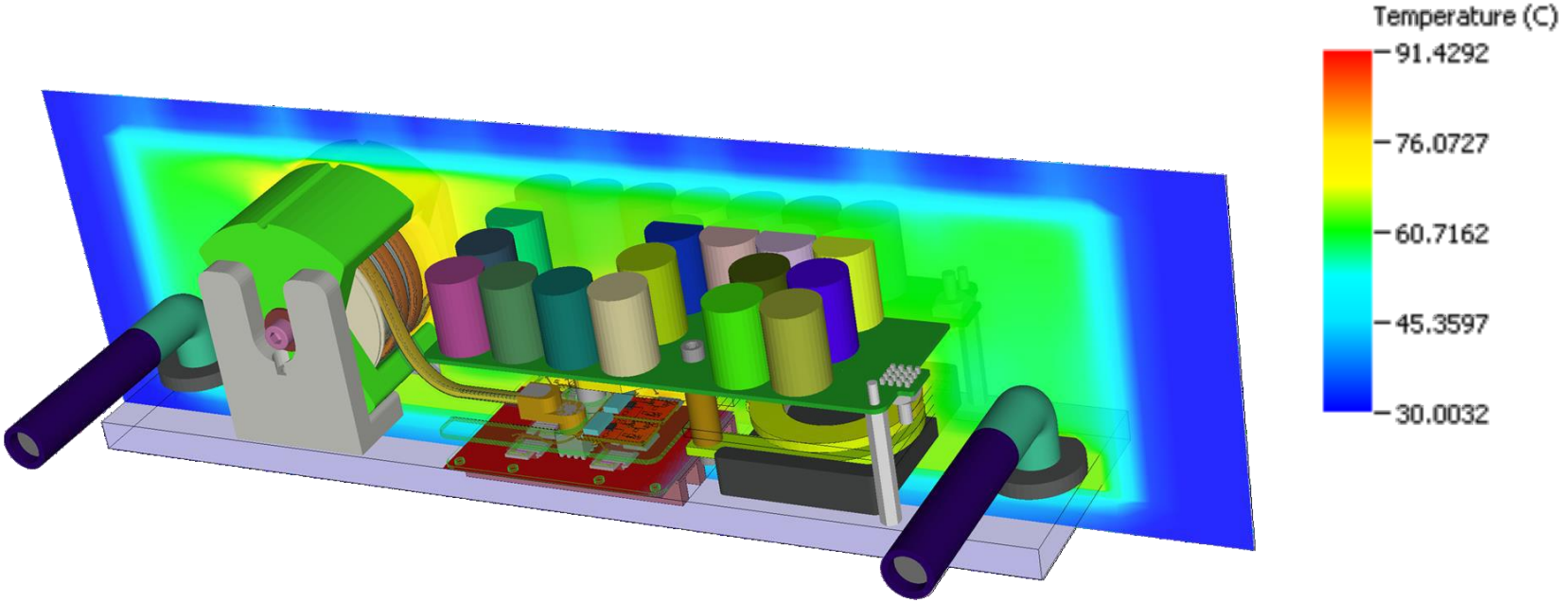




Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

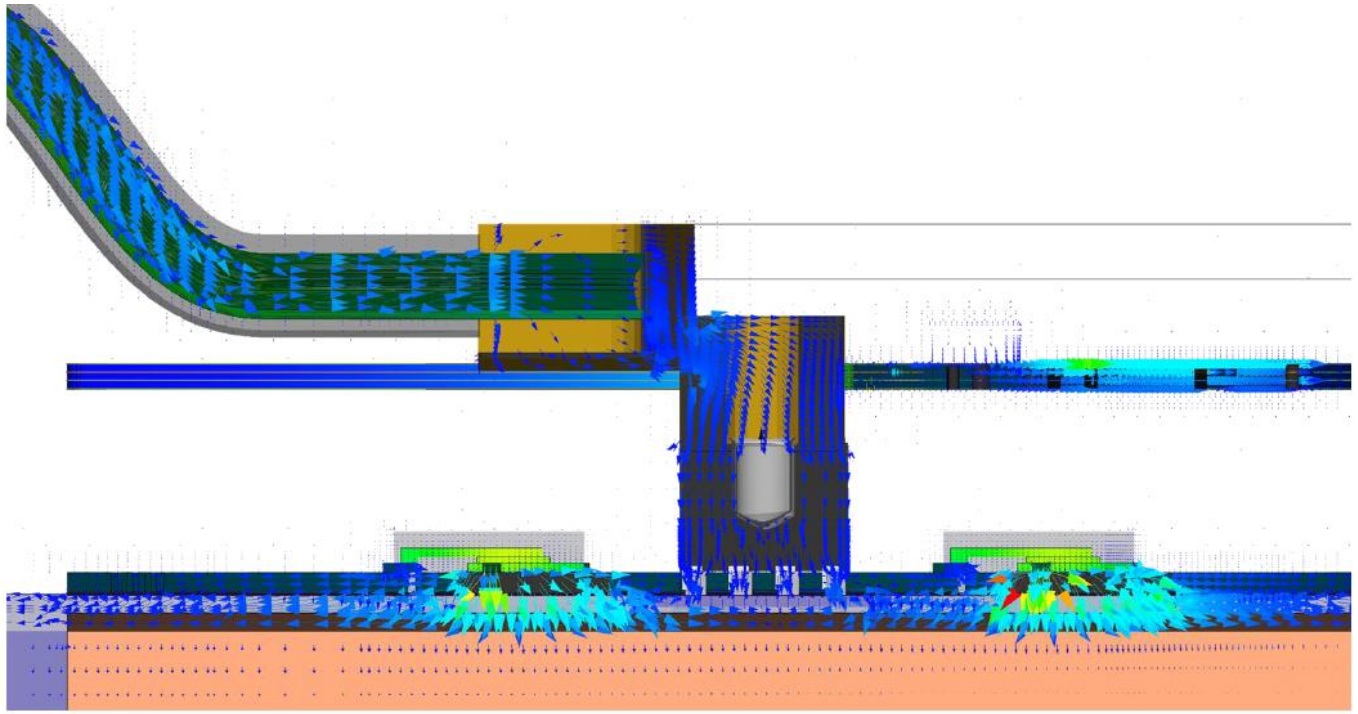
- Simulation results of the final model (example 6SigmaET0)
  - DC/DC converters



Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- Simulation evaluation (example 6SigmaET0)
  - Heat flow transformer coiling, connection, module

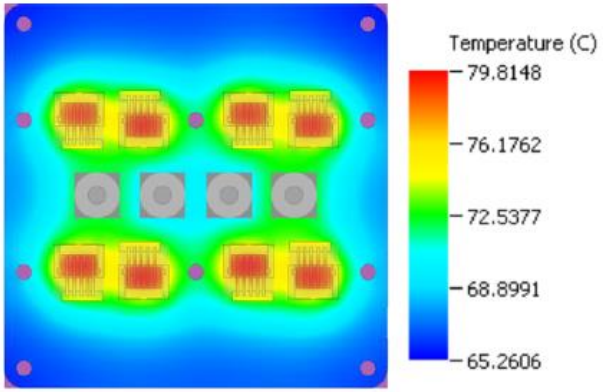


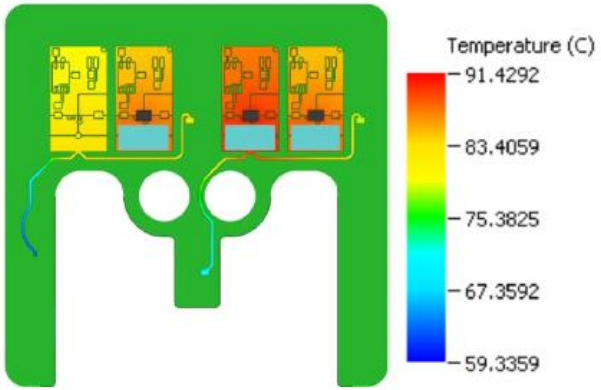
Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- Simulation result (example 6SigmaET)
  - List of the temperature of each component

	Owner PCB	Junction Temperature	Mean Volume Temperature
Gate_switch_1 (Case)	Driver_Board	85.3	85.3
Gate_switch_2 (Case)	Driver_Board	89.47	89.47
Gate_switch_3 (Case)	Driver_Board	91.81	91.81
Gate_switch_4 (Case)	Driver_Board	89.82	89.82
Switch_1 (IPT020)	Module	75.91	75.91
Switch_2 (IPT020)	Module	76.42	76.42
Switch_3 (IPT020)	Module	76.55	76.55
Switch_4 (IPT020)	Module	76.1	76.1
Switch_5 (IPT020)	Module	76.3	76.3
Switch_6 (IPT020)	Module	76.49	76.49
Switch_7 (IPT020)	Module	76.44	76.44
Switch_8 (IPT020)	Module	76.35	76.35
Gate_Resistor_1 (Resistor)	Driver_Board		83.43
Gate_Resistor_2 (Resistor)	Driver_Board		87.71
Gate_Resistor_3 (Resistor)	Driver_Board		89.89
Gate_Resistor_4 (Resistor)	Driver_Board		88.14

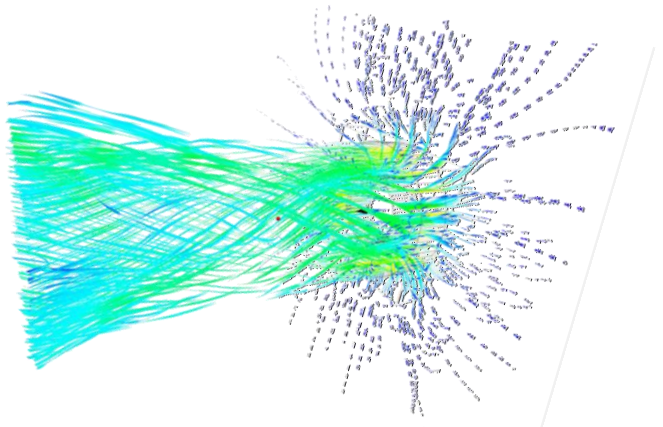


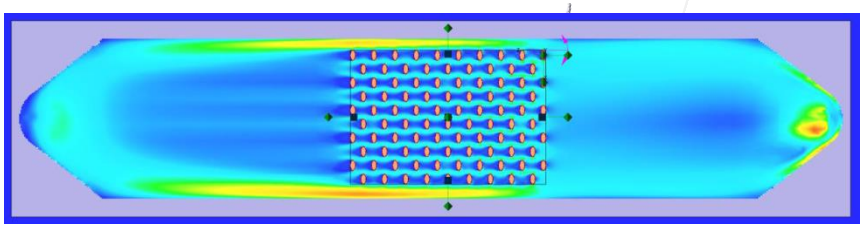


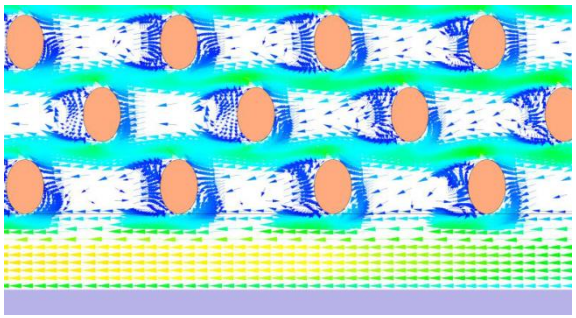
Simulation methods and theoretical consideration

Thermal simulation of electronic systems during design - Conjugate Heat Transfer

- **Further possibilities**
- Radiation
  - Within the system
  - Solar radiation
- Replacement models
  - Fan
  - Peltier element
- Transient
- Hybrid cells
  - Further refinement of the geometry mapping







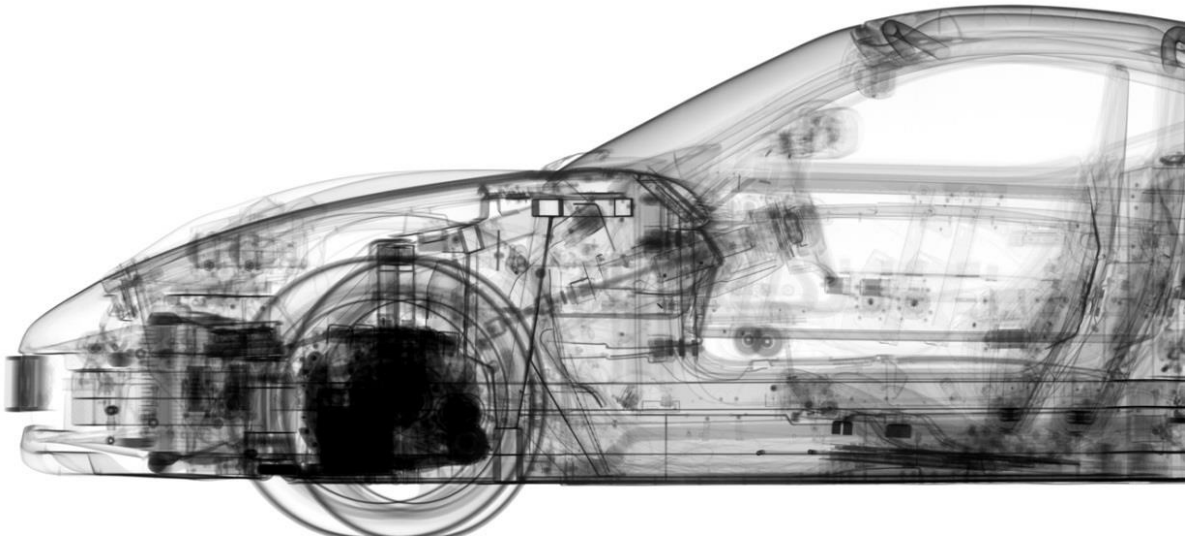
Packaging Technologies in Power Electronic Modules

- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - Packaging concepts
  - Interconnection technologies
  - Packaging at Fraunhofer IISB
  - Thermal design and insulation coordination
- Simulation process and theoretical consideration
- **Test procedure and analysis**
  - General
  - AQG 324 (LV 324)
- Test setups and parameters
- Summary

Test procedure and Analysis

Reliability and requirements

- Reliability is the probability that a product will properly meet its specific requirements for a specified period of time under certain environmental conditions (VDI Guideline 4001)
- Reliability is a function of time and time can be measured in various ways:
  - Operating time
  - Performance
  - Life time
  - Load Cycles



Packaging Technologies in Power Electronic Modules

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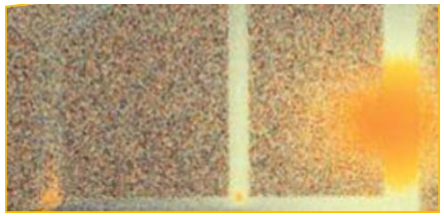
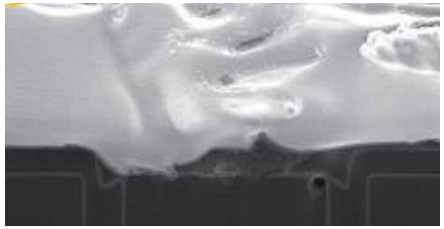
- Simulation process and theoretical consideration
- Test procedure and analysis
  - **General**
  - AQG 324 (LV 324)
- Test setups and parameters
- Summary

Test procedure and Analysis

Overview - Test and reliability

- **Non-destructive examination methods**
  - Optical microscopy
  - 3D laser scanning (laser profilometer)
  - Ultrasonic microscopy
  - Measurement of electrical quantities/ parameters
  - Lock-in thermography
- **Destructive examination methods**
  - Metallographic preparation / grinding technique
  - Shear and pull test
  - Partial discharge measurement
  - Nano-Indentation
  - FIB preparation (Focused Ion Beam)

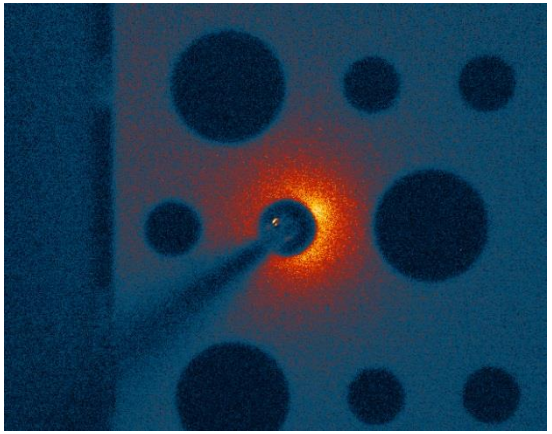




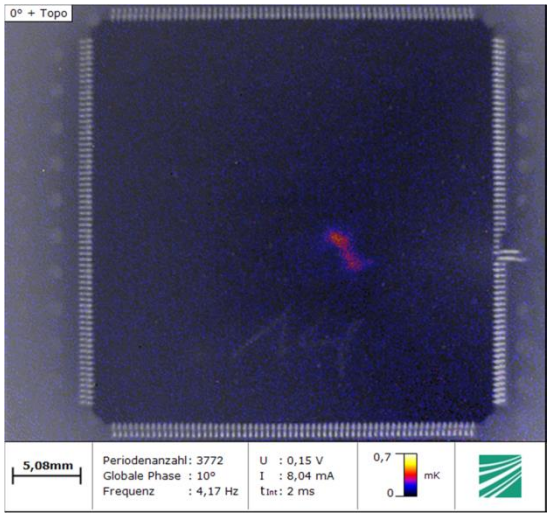
Test procedure and Analysis

Lock-In Thermography - Hotspot Troubleshooting

- **Non-destructive examination method**
  - Electrical defects in test item



- Principle/ process steps
  - Stimulation of the test object with electrical pulses
  - Localization of the hotspots (power loss) in the test object by means of infrared camera

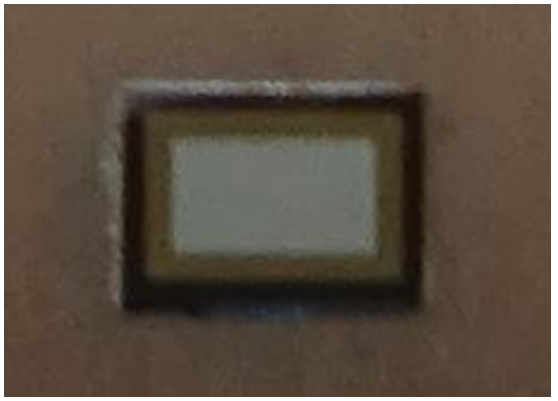


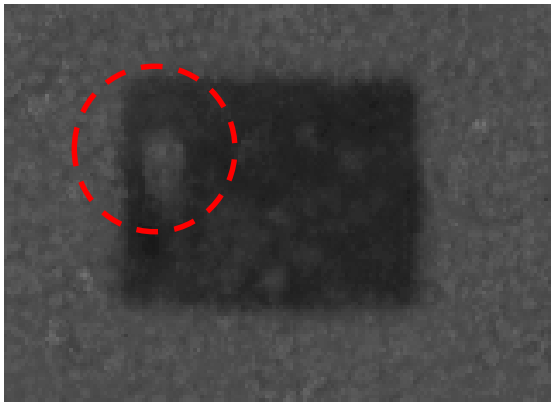
Fraunhofer IMWS

Test procedure and Analysis

Ultrasonic microscopy/ acoustic microscopy

- **Non-destructive examination method**
  - Defects, material properties and material changes
  - Blowholes, cracks, etc. in solder and sintered layers
  - Wetting behaviour between semiconductor and substrate
- Principle/ process steps
  - Generation of images from the interior of an object by means of ultrasonic pulses



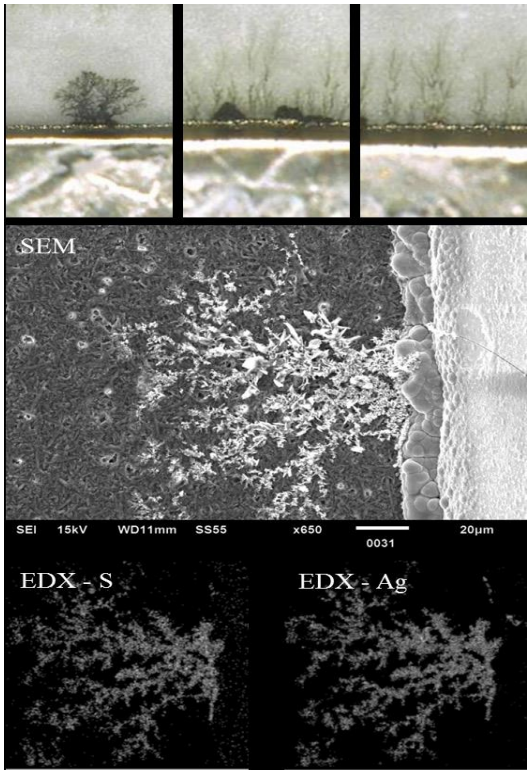


Test procedure and Analysis

Partial discharge measurement/ investigation of the insulation strength

- **Destructive examination method**
  - Insulation strength or defects in the insulation system
  - Exceeding the limit of the material typical breakdown field strength
  - Sliding discharges, internal and external partial discharges (corona)

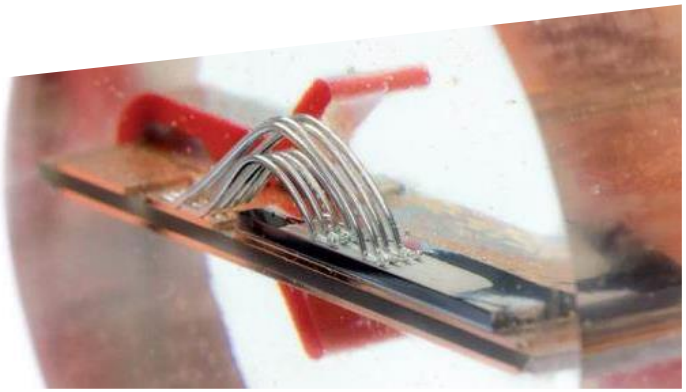
- Principle/ process steps
  - Partial discharge measuring device/plant
  - Determination of the application-related partial discharge interruption voltage
  - Measure and evaluate PD pulses from the test object



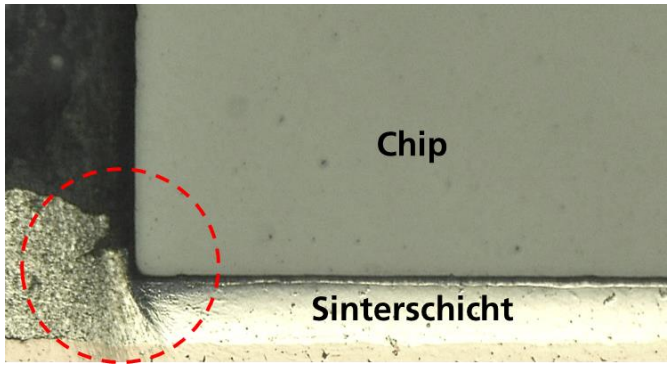
Test procedure and Analysis

Metallographic preparation / microsection analysis

- **Destructive examination method**
  - Quality of the interconnection layers (e.g. solder and sinter layer between chip and substrate)
  - Material grain boundaries/structure



- Principle/ process steps
  - Disconnect
  - Embedding (warm, cold)
  - Grinding
  - Polishing

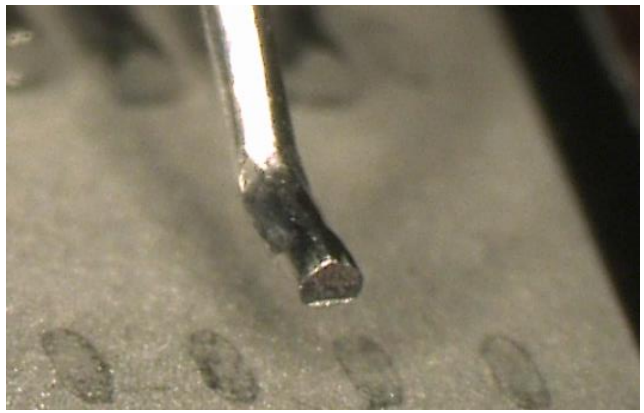


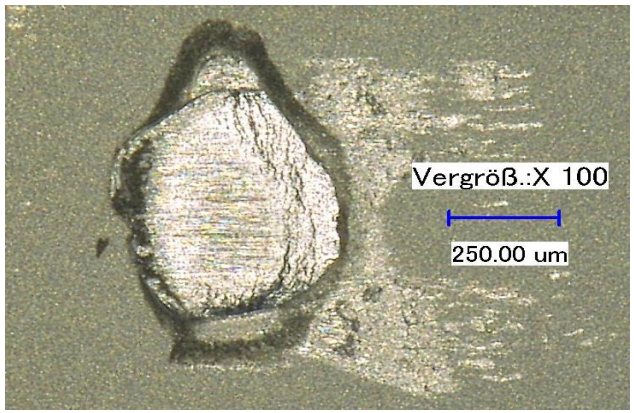
Test procedure and Analysis

Shear strength analysis/ investigation of mechanical adhesion

- **Destructive examination method**
  - Quality and reliability of bonding wires, soldered and sintered semiconductor devices

- Principle/ process steps
  - Measurement of contact strength in force per area
  - Shear tester with shear blade

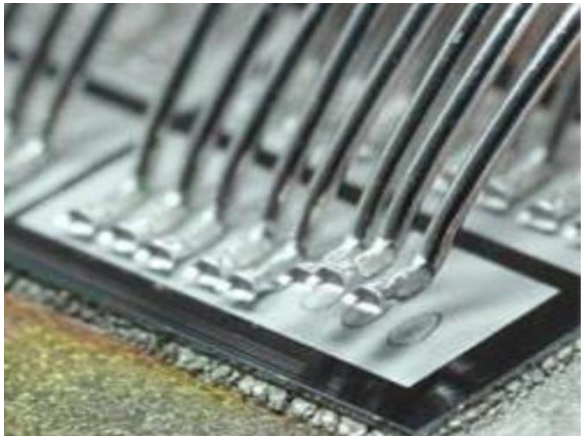




Test procedure and Analysis

Overview - Service life and reliability

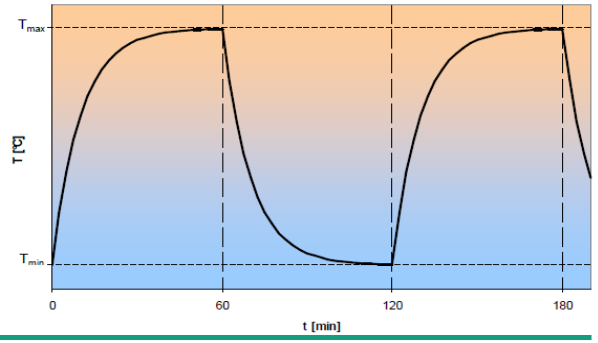
- Active Power Cycling
- Passive Power Cycling / Thermal Shock Test
- Storage Tests (HTRB, HTGB, H3TRB)
- Statistical analysis
- Lifetime modelling



Test procedure and Analysis

Temperature shock test or passive load cycle test

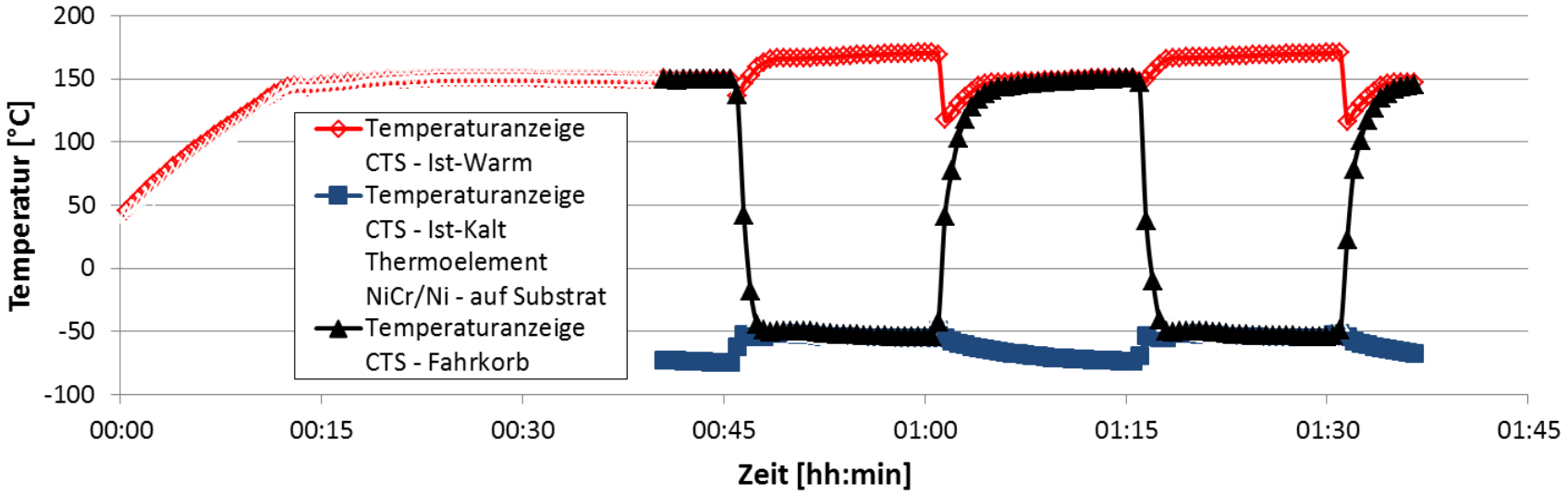
- **Destructive examination method**
  - Thermal shock resistance of materials, joints and superstructures
  - Failure prediction (first bond? solder point? potting? etc.)
- Principle/ process steps
  - Thermal chamber with hot and cold sections
  - Temperatures from -50 °C to +150 °C
  - With and without holding time
  - Typical number of load cycles: 100 to 1000 cycles
  - Failure criteria such as delamination (e.g. solder), crack length, electrical damage



Test procedure and Analysis

Temperature shock test or passive load cycle test

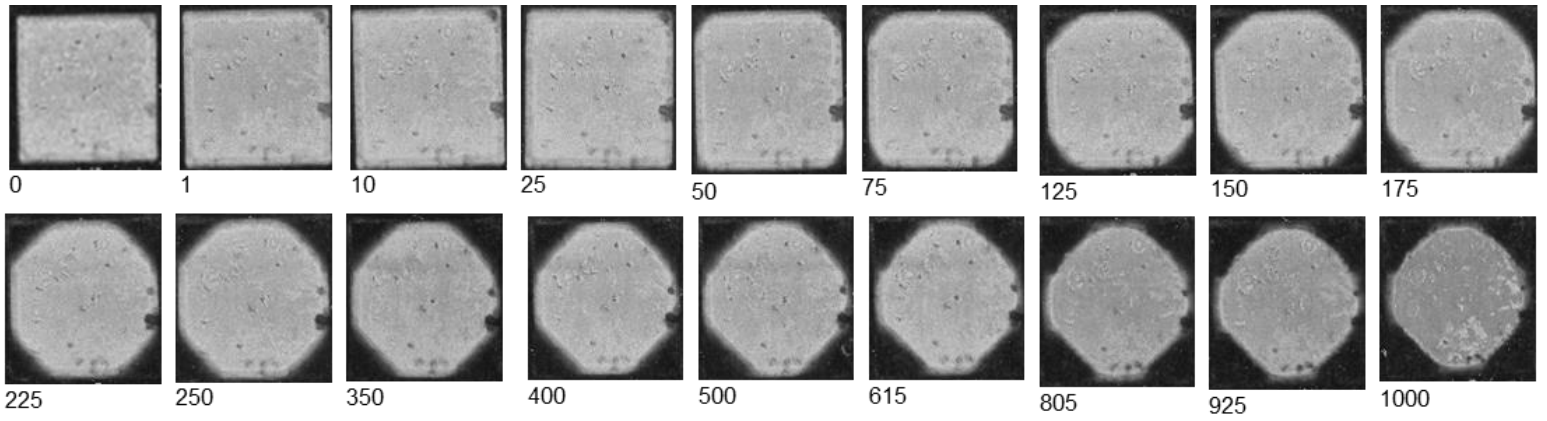
- Problems and effects on the test result
  - Concept of the inspection equipment
  - "not directly visible" setting parameters (maintenance, etc.)
  - Thermal mass of the test specimen
  - Filling level of the test chamber (thermal resistance)

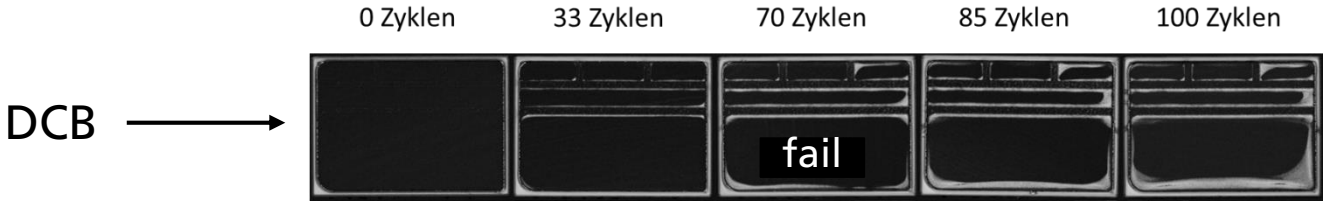


Test procedure and Analysis

Temperature shock test or passive load cycle test

- Problems and effects on the test result
  - Evaluation is difficult → Limits of the failure criterion can only be interpreted subjectively

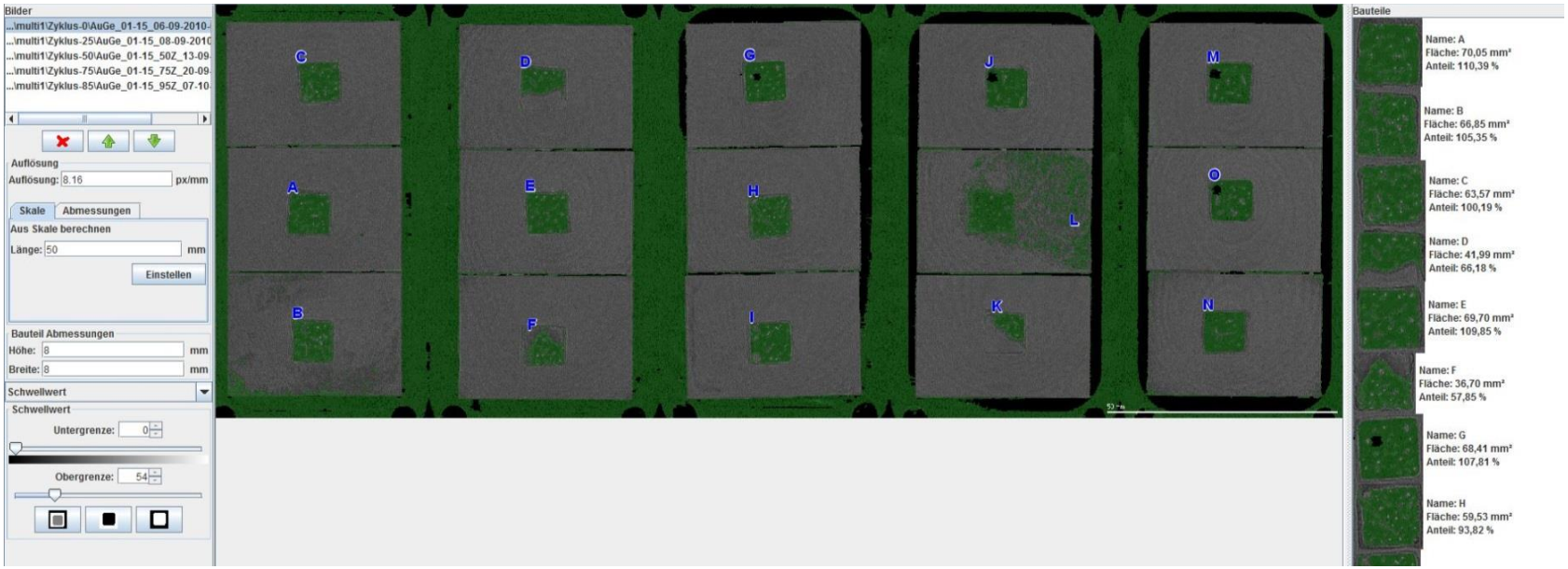




Test procedure and Analysis

Temperature shock test or passive load cycle test

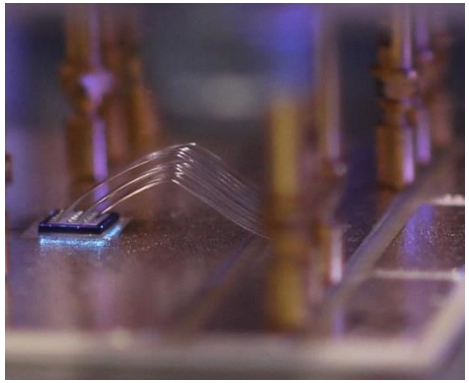
- Evaluation with software support
  - Detection of delamination via grey values or via edge search
  - Automatic recognition of several components on one SAM image
  - Failure detection according to defined criteria (e.g. 20% area reduction)



Test procedure and Analysis

Active Power Cycling

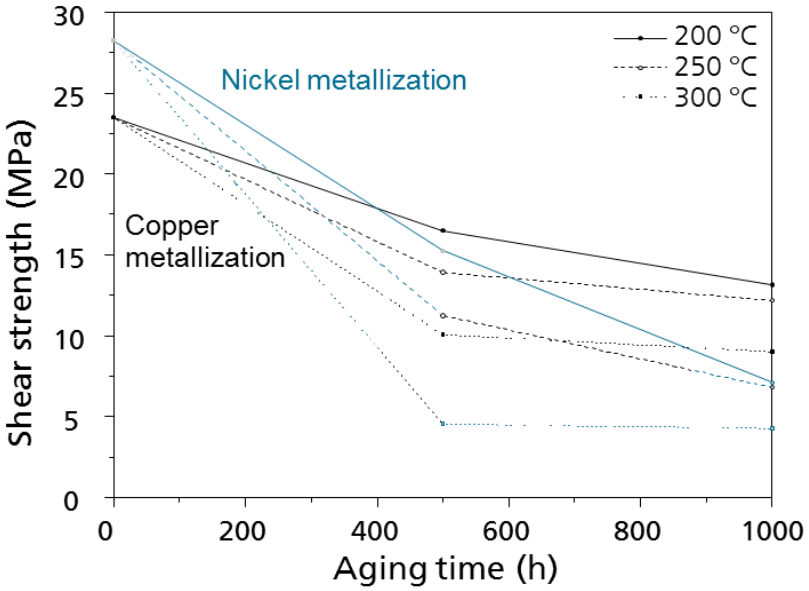
- **Destructive examination method**
  - Quality of the interconnection layers (e.g. solder and sinter layer between chip and substrate)
- Thermal impedance measurement Z_{th} at each cycle
- Principle/ process steps
  - Individual setting of the gate voltage for each test object
  - Automatic End-of-Life Detection
  - Heating current from 0.1 A to 2 kA
  - Heating voltage up to 35 V
  - Heating and cooling capacity up to 20 kW
  - Cooling temperature from -60 °C to +350 °C



Test procedure and Analysis

High temperature and cold storage

- **Destructive examination method**
  - Change of solder materials, adhesives, packaging and interconnection technology and semiconductor properties
- Principle/ process steps
  - Uninterrupted bearing stress
  - Standard test time 1000h
  - Constant temperature 85...150 °C
  - Standard cold storage at -40 °C
  - Measurements during and after the test
- Example:
  - Chip on substrate
  - PbSn5 Solder material
  - shear strength over time



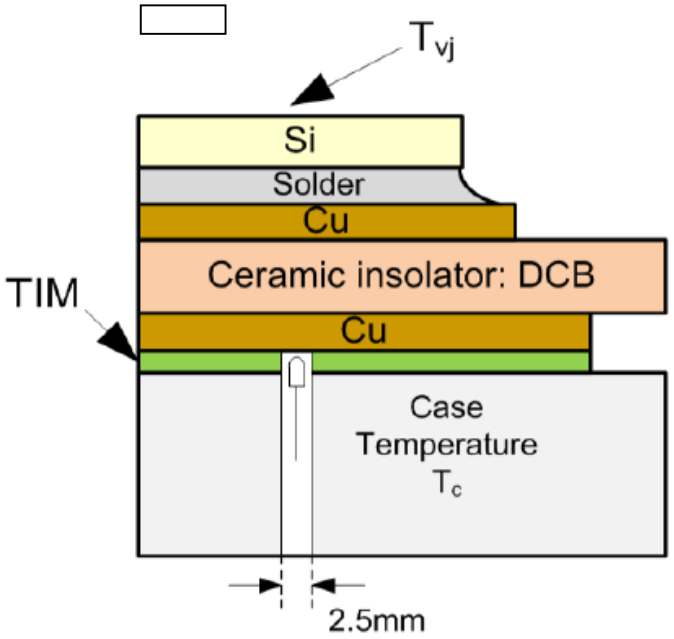
Packaging Technologies in Power Electronic Modules

- Packaging and interconnection technologies for power electronics
  - Comparison and evaluation of packaging methods
  - Packaging concepts
  - Interconnection technologies
  - Packaging at Fraunhofer IISB
  - Thermal design and insulation coordination
- Simulation process and theoretical consideration
- Test procedure and analysis
  - General
  - **AQG 324 (LV 324)**
- Test setups and parameters
- Summary

Test procedure and Analysis

Characterization of modules according to AQG 324 (LV 324)

- Determination of the **thermal resistance** of individual components in the power module
- DIN EN 60747-15:2012, clause 5.3.6.1: **R_{th}, j-c**
- Important:
  - The position and distance of the temperature sensor that determines the reference point for defining the **reference temperature T_c** must be documented
  - The temperature sensor must be located as close as possible to the power module
  - When measuring T_c, a hole (Ø 2.5 mm) must be made centrally under the DUT (device under test)
  - Information on the TIM material must be given (manufacturer, designation, thickness, thermal conductivity)



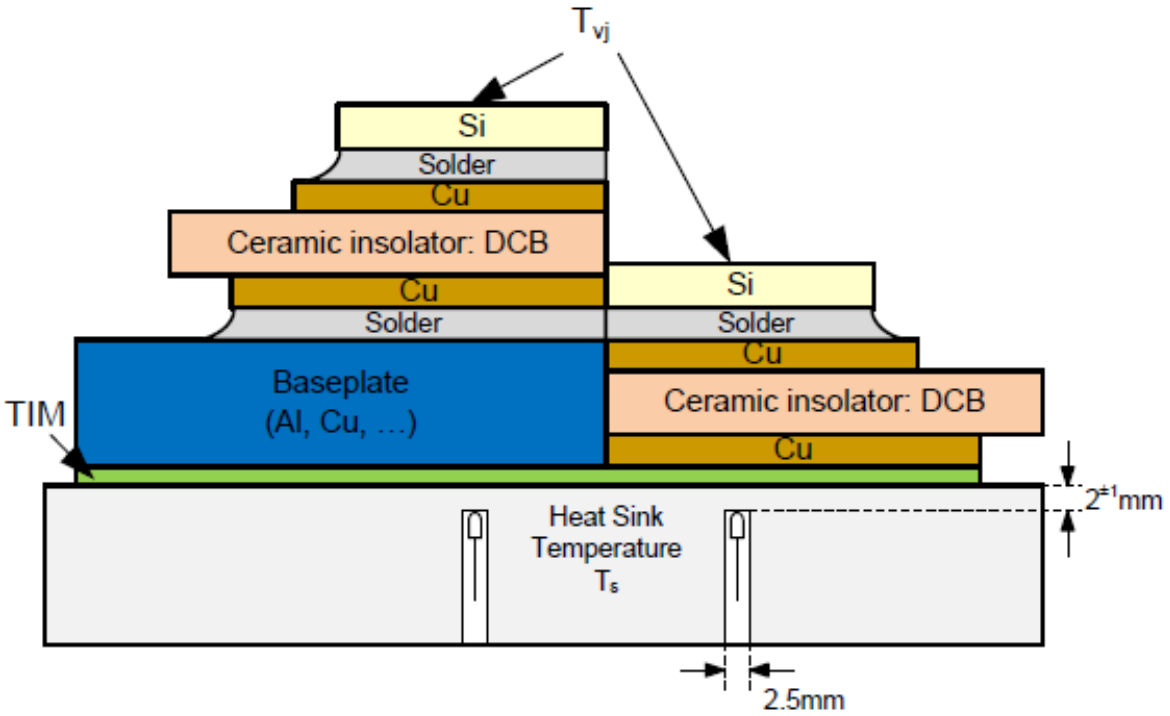
$$R_{th,j-c} = \frac{T_{vj} - T_c}{P_v}$$

Test procedure and Analysis

Characterization of modules according to AQG 324 (LV 324)

- Determination of **the thermal resistance** of individual components in the power module
- DIN EN 60747-15:2012, clause 5.3.6.4: Rth, j-s
- Reference point, **reference temperature T_s** → Heat sink

$$R_{th,j-s} = \frac{T_{vj} - T_s}{P_v}$$

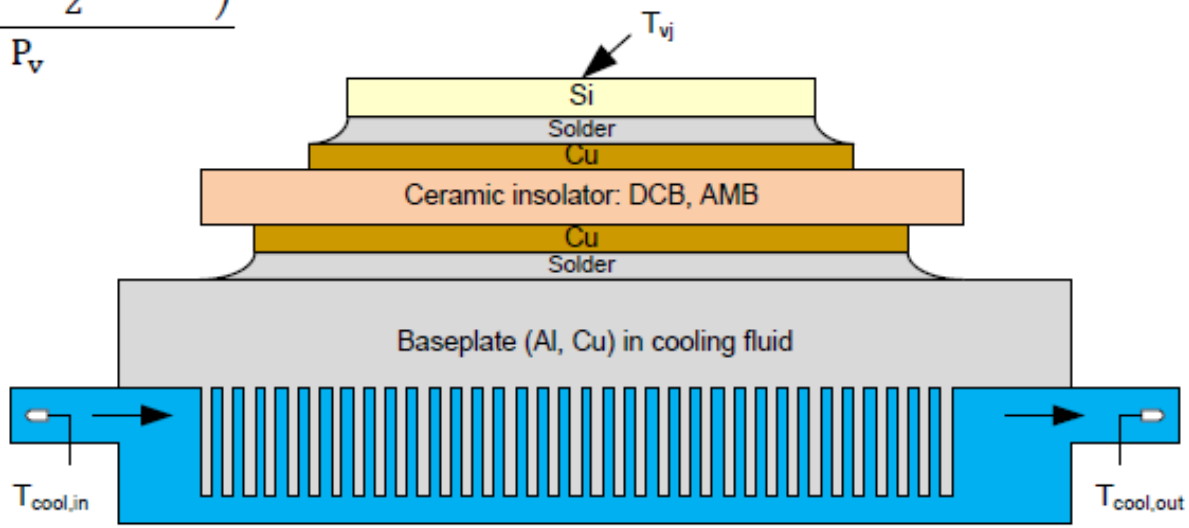


Test procedure and Analysis

Characterization of modules according to AQG 324 (LV 324)

- Determination of the **thermal resistance** of individual components in the power module
- Supplementary test to DIN EN 60747-15:2012
- Reference point, **reference temperature $T_{cool,in}$ / $T_{cool,out}$** → Liquid cooling systems
- Documentation → Coolant, pressure of the coolant circuit and coolant flow

$$R_{th,j-a} = R_{th,j-f} = \frac{T_{vj} - \left(\frac{T_{cool,in} + T_{cool,out}}{2}\right)}{P_v}$$



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Packaging Technologies in Power Electronic Modules

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- Test procedure and analysis
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  - AQG 324 (LV 324)
- **Test setups and parameters**
- Summary

Test procedure and Analysis

Characterization of modules according to AQG 324 (LV 324)

- Determination of the **resistance** to **mechanical stress** due to **passive temperature changes**

- IEC 60749-25:2003
  - Testing only in a two-chamber system (air/air), single-chamber or three-chamber system not permitted
  - Focus on cycle frequency for solder joints (1 - 2 cycles per hour)
  - T_{dwell} > 15 min (dwell time) for the highest / lowest temperature
  - Testing of power modules → $T_{stg,min}$ = -40 °C / $T_{stg,max}$ = +125 °C
  - t_{change} < 30 s (transfer time)
  - Minimum number of cycles without failures/errors → N_C > 1000

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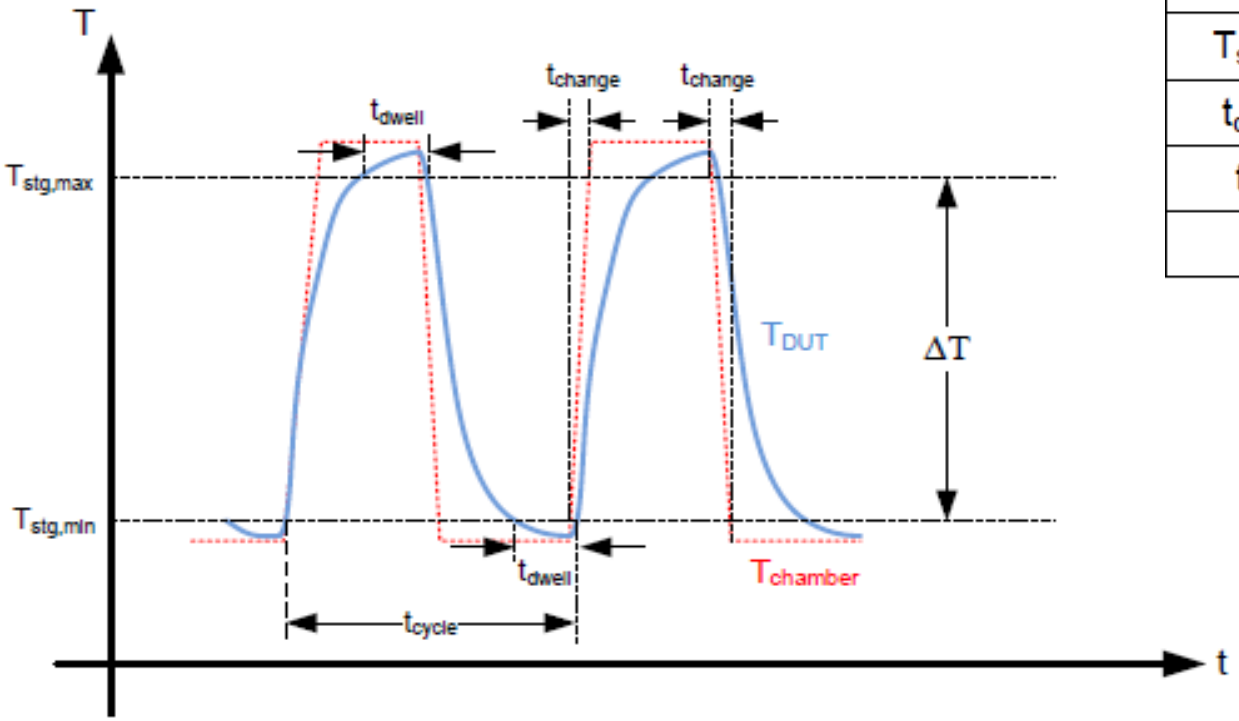
Test procedure and Analysis

Temperature shock test (TST) according to AQG 324 (LV 324)

- Determination of the **resistance** to **mechanical stress** due to **passive temperature changes**
- IEC 60749-25:2003



$T_{stg,min}$	$-40°C^{0}_{-10}$
$T_{stg,max}$	$+125°C^{+15}_{0}$
t_{change}	< 30 s
t_{dwell}	> 15 min
N_C	> 1000

Test procedure and Analysis

Power Cycling (PC_{sec}) Test according to AQG 324 (LV 324)

- Targeted generation of stress situations in power modules under highly accelerated conditions → causing wear and tear
- **QL-01 Power Cycling (PC_{sec}):** Stress formation in the near area of the chip connection (die-attach and top side contact) by limiting the parameter **t_{on} < 5 s (on-time of the load current)**
- IEC 60749-34:2011

Parameter		Value
On-time of the load current	t_{on}	< 5 s
Value of load current	I_L	> 0.85·I_{CN} [a, b]
Gate voltage	V_{gate}	typically 15 V [c]

[a] The value of the load current > 0.85·I_{CN} must only be used for one node.

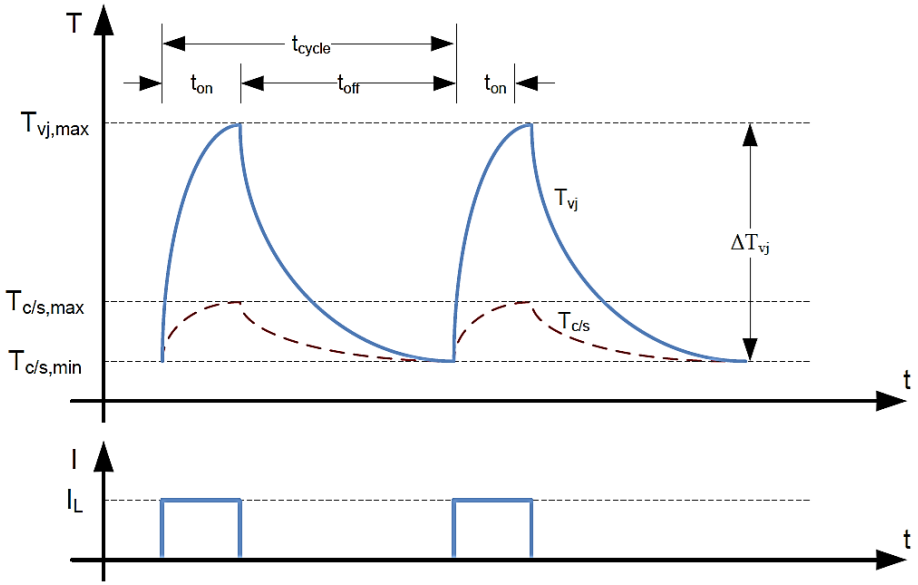
[b] A value < 0.85·I_{CN} can be selected for the second node in order to allow a suitable difference of the temperature rises to be set.

[c] The gate voltage for testing IGBT and MOSFET can fall below the 15 V (e.g., when contact currents become too high), if – due to the thermal properties of the module – the desired temperature rise cannot be achieved with on-times of t_{on} < 5 s. For this, however, it must always be ensured that the switch is permanently operated in the saturated range. In these cases, the gate voltage used must only be set once at the start of the tests and documented in each case.

Test procedure and Analysis

Power Cycling (PC_{sec}) Test according to AQG 324 (LV 324)

- **QL-01 Power Cycling (PC_{sec})**
- Test conditions:
- The DUTs must be energized at least until the first EOL criterion occurs
- However, it is strongly recommended that the DUTs continue to be loaded after the first EOL criterion is reached to improve the evaluation of the results



Parameter	
Temperature rise of virtual junction temperature (starting value for test after settling process)	$\Delta T_{vj,start}$
Duration of settling process (in cycles)	N_{start}
Load current	I_L
On-time of the load current (heating period)	t_{on}
Off-time of the load current (cooling period)	t_{off}
Minimum virtual junction temperature at the start of the test	$T_{vj,min}$
Maximum virtual junction temperature at the start of the test	$T_{vj,max}$
Coolant feed temperature	T_{cool}
Gate voltage	V_{gate}

Test procedure and Analysis

Power Cycling (PC_{sec}) Test according to AQG 324 (LV 324)

- **QL-02 Power Cycling (PC_{min}):** Stress formation both in the chip-remote connection (system soldering) and in the near area of the chip connection (die attach, top-side contacting)
- **t_{on} > 15 s (on-time of the load current**)
- Test conditions:

Parameter		Value
On-time of the load current	t_{on}	> 15 s
Value of load current	I_L	> 0.85·I_{CN} [a]
Gate voltage	V_{gate}	typically 15 V [b]

[a] A value < 0.85·I_{CN} can be selected for the second sampling point and additional test conditions in order to allow a suitable difference of the temperature rises to be set.

[b] The gate voltage for testing IGBT and MOSFET can fall below the 15 V (e.g. when contact currents become too high), if – due to the thermal properties of the module – the desired temperature rise cannot be achieved with on-times of t_{on} > 15 s. For this, however, it must always be ensured that the switch is permanently operated in the saturated range. In these cases, the gate voltage used must only be set once at the start of the tests and documented in each case.

Test procedure and Analysis

Power Cycling (PC_{sec}) Test according to AQG 324 (LV 324)

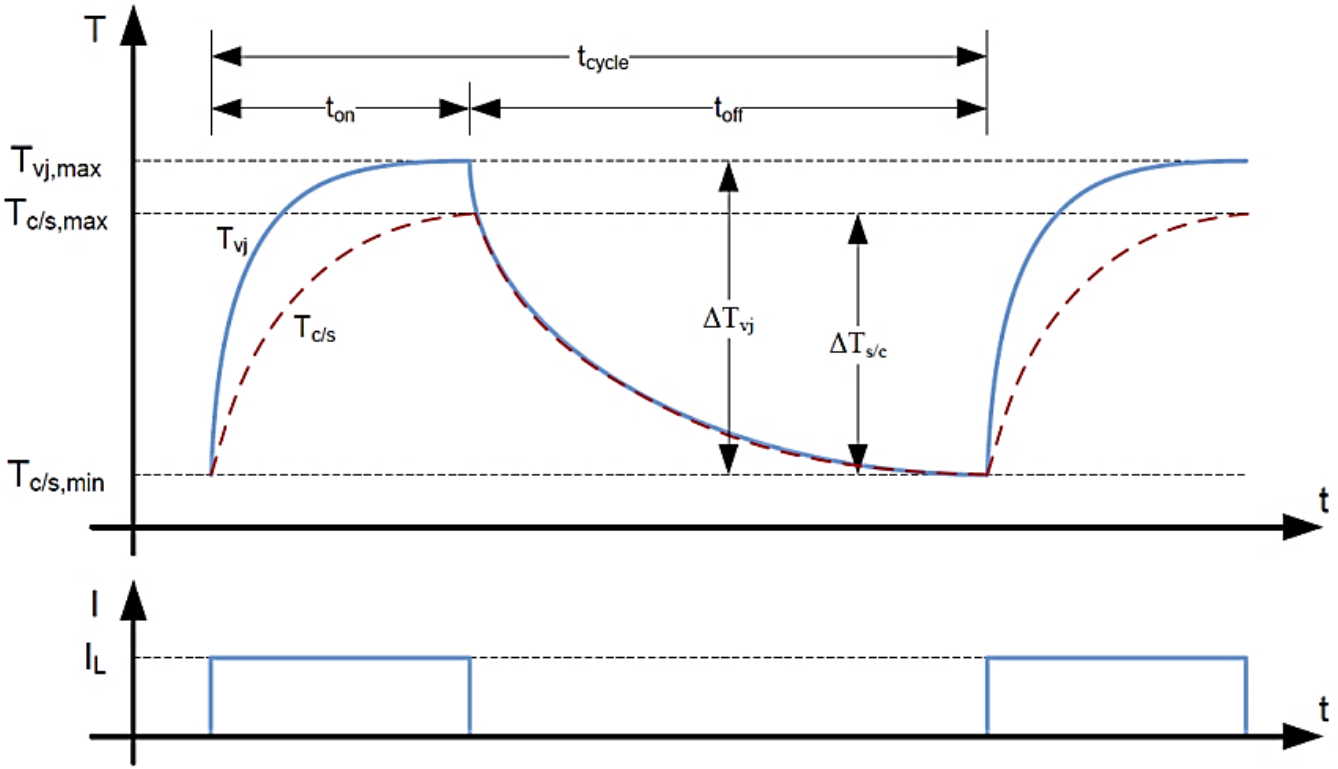
- **QL-02 Power Cycling (PC_{min})**
- Test conditions:

Parameter	
Temperature rise for virtual junction temperature (starting value for test after settling process)	$\Delta T_{vj,start}$
Duration of settling process (in cycles)	N_{start}
Load current	I_L
On-time of the load current (heating period)	t_{on}
Off-time of the load current (cooling period)	t_{off}
Average junction temperature	$T_{vj,avg}$
Maximum junction temperature at the start of the test	$T_{vj,max}$
Heat sink temperature (indirect cooled modules)	T_S
Base plate temperature (modules with base plate)	T_C
Coolant inlet temperature	T_{cool}
Gate voltage	V_{gate}
Thermal resistance (determined in the module test)	R_{th}

Test procedure and Analysis

Power Cycling (PC_{sec}) Test according to AQG 324 (LV 324)

- **QL-02 Power Cycling (PC_{min})**
- Test conditions:



Test procedure and Analysis

Power Cycling (PC_{sec}) Test according to AQG 324 (LV 324)

- **Failure and evaluation criteria**
- QL-01 Power Cycling (PC_{sec}) and QL-02 Power Cycle (PC_{min})
- It is recommended to inspect the test specimens for cracks in the solder joints, substrates, tool parts and housings after the end of the test using ultrasonic microscopy. Other relevant thermal and mechanical connections with effects on the EOL criteria should be checked.

Parameter		Change from standard value
Forward voltage	IGBT: $V_{CE,sat}$ MOSFET: V_{DS} Diode: V_F, V_{FSD}	+5% [a]
Increase of thermal resistance	$R_{th,j-c}$, $R_{th,j-s}$, $R_{th,j-f}$ [b]	+20%

[a] Note: See also the notes on the settling process under test conditions

[b] Note: It has to be ensured that the duration of temperature rise is sufficient for the calculation of static R_{th}, or an additional online R_{th} measurement should be performed without removing the power modules from the test bench, when TIM or a baseplate is part of the DUT.

Test procedure and Analysis

High Temperature Storage (HTS) Test according to AQG 324 (LV 324)

- **Storage** of power modules at **elevated temperatures**
- IEC 60749-6:2002
  - If the specimens to be tested are classified for a temperature above 125 °C, this higher temperature must be used for the test
  - In the case of intermediate measurements (if agreed with the purchaser), the test specimens must be removed from the test chamber at TRT and replaced at TRT
  - It is recommended that the DUT be examined by SAM analysis at the above defined times during this test and the degree of delamination at the connection points be documented

Parameter	Value
Test duration	1000 h
Ambient temperature $T_a = T_{stg,max}$	≥ 125 °C

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Test procedure and Analysis

Low Temperature Storage (LTS) Test according to AQG 324 (LV 324)

- **Storage** of power modules **at very low temperatures**
- Investigation of ageing effects such as embrittlement and crack formation in the power module
- JEDEC JESD-22 A119:2009
  - Test must be performed at -40 °C
  - If the specimens to be tested are classified for a temperature below -40 °C, this lower temperature must be used for the test
  - In the case of intermediate measurements (if agreed with the purchaser), the test specimens must be removed from the test chamber at TRT and replaced at TRT
  - It is recommended that the DUT be examined by SAM analysis at the above defined times during this test and the degree of delamination at the connection points be documented

Parameter	Value
Test duration	1000 h
Ambient temperature $T_a = T_{stg,min}$	≤ -40 °C

Test procedure and Analysis

High Temperature Reserve Bias (HTRB) Test according to AQG 324 (LV 324)

- Determination of weak points in the layer structure of chip passivation and chip edge sealing as a function of time.
- Focus on production-related ionic impurities that are formed under the influence of temperature and electric fields and thus increase the surface charges
- Especially relevant for chips without passivation such as in IGBT and MOSFET power modules
- Test according to IEC 60747-9:2007 (IGBT) and IEC 60747-8:2010 (MOSFET)

Parameter	Value
Test duration	≥ 1000 h
Ambient temperature T_a	$T_{vj,max}$ - $T_{(Pv)}$ *
Collector-emitter voltage Drain-source voltage	$V_{CE} \geq 0.8\ V_{CE,max}$ (IGBT) $V_{DS} \geq 0.8\ V_{DS,max}$ (MOSFET)
Gate voltage	$V_{GE} = 0$ V (IGBT) $V_{GS} = 0$ V (MOSFET)
* *$T_{(Pv)}$ defines the heat input in the semiconductor caused by the leakage losses*	

Test procedure and Analysis

High Temperature Gate Bias (HTGB) Test according to AQG 324 (LV 324)

- Investigation of the combined effect of electrical and thermal loading of semiconductor devices with gate connection (MOSFET and IGBT) as a function of time
  - The integrity of the gate dielectric
  - The state of the semiconductor/dielectric interface
  - The contamination of the semiconductor by mobile ions

Parameter	Value	
	Variant 1	Variant 2
Test duration	For each DUT ≥ 500 h, V_{GE} or V_{GS} > 0 ≥ 500 h, V_{GE} or V_{GS} < 0	50% of the DUTs, each with ≥ 1 000 h, V_{GE} or V_{GS} > 0 ≥ 1 000 h, V_{GE} or V_{GS} < 0
Ambient temperature T_a	$T_{vj,max}$	
Collector-emitter voltage or Drain-source voltage	V_{CE} = 0 V (IGBT) V_{DS} = 0 V (MOSFET)	
Gate voltage	V_{GE} = $V_{GE,max}$ (IGBT), DUT switched off V_{GS} = $V_{GS,max}$ (MOSFET), DUT switched off	

Test procedure and Analysis

High Humidity, High Temperature Reverse Bias (H3TRB) Test according to AQG 324 (LV 324)

- Investigation of the weak points in the entire module structure including the power semiconductor
  - Permeability of moisture in the passivation layer
  - Production-related ionic impurities
  - Thermomechanical stresses on the package and interaction with semiconductor chips
  - ➢ Formation of increased leakage currents
  - ➢ Corrosive substances that are created by the influence of corrosive gas and the interaction of these substances with the packaging technology and the chip

Test procedure and Analysis

High Humidity, High Temperature Reverse Bias (H3TRB) Test according to AQG 324 (LV 324)

- Test according to IEC 60749-5:2003
  - Test must be performed with constant voltage load
  - Test must be performed with permanently locked DUTs

Parameter	Value
Test duration	≥ 1000 h (switched off)
Temperature	85 °C (constant)
Relative humidity	85 %
Collector-emitter voltage* Drain-source voltage	$V_{CE} = 0.8 \cdot V_{CE,max}$ (IGBT), max. 80 V $V_{DS} = 0.8 \cdot V_{DS,max}$ (MOSFET), max. 80 V
Gate voltage	$V_{GE} = 0$ V (IGBT) $V_{GS} = 0$ V (MOSFET)
**To avoid locally reducing the relative humidity influence too strongly through power loss created by leakage currents, the voltage applied to devices must be set to 80% of the specified nominal breakdown voltage*	

Test procedure and Analysis

Mechanical Shock (MS) Test according to AQG 324 (LV 324)

- Investigation of the resistance of the PCU (Power Electronic Converter Unit) to mechanical shocks (error patterns such as cracks, detachment of the component)
- DIN EN 60068-2-27
  - Mechanical stress during handling, transport and field use
  - Half sinus wave with defined amplitude and time (e.g. 30 g/ 18 ms)

Peak acceleration	500 m/s^2
Shock duration	6 ms
Shock form	half-sine
Number of shocks per direction (±X, ±Y, ±Z)	10
Number of DUTs	6

Test procedure and Analysis

Vibration (V) Test according to AQG 324 (LV 324)

- Investigation of the mechanical structure of PCUs for automotive applications
  - Simulation of the vibration load of a module during operation to validate the module resistance against vibrations (error patterns such as material fatigue, component separation)
- DIN EN 60068-2-6
  - Frequency change of 1 octave/ min (total duration approx. 7 min)
  - Frequency from 10 Hz to 2000 Hz
  - Amplitude approx. 5 g
  - Execution 4 times in x, y and z direction (12 times in total)

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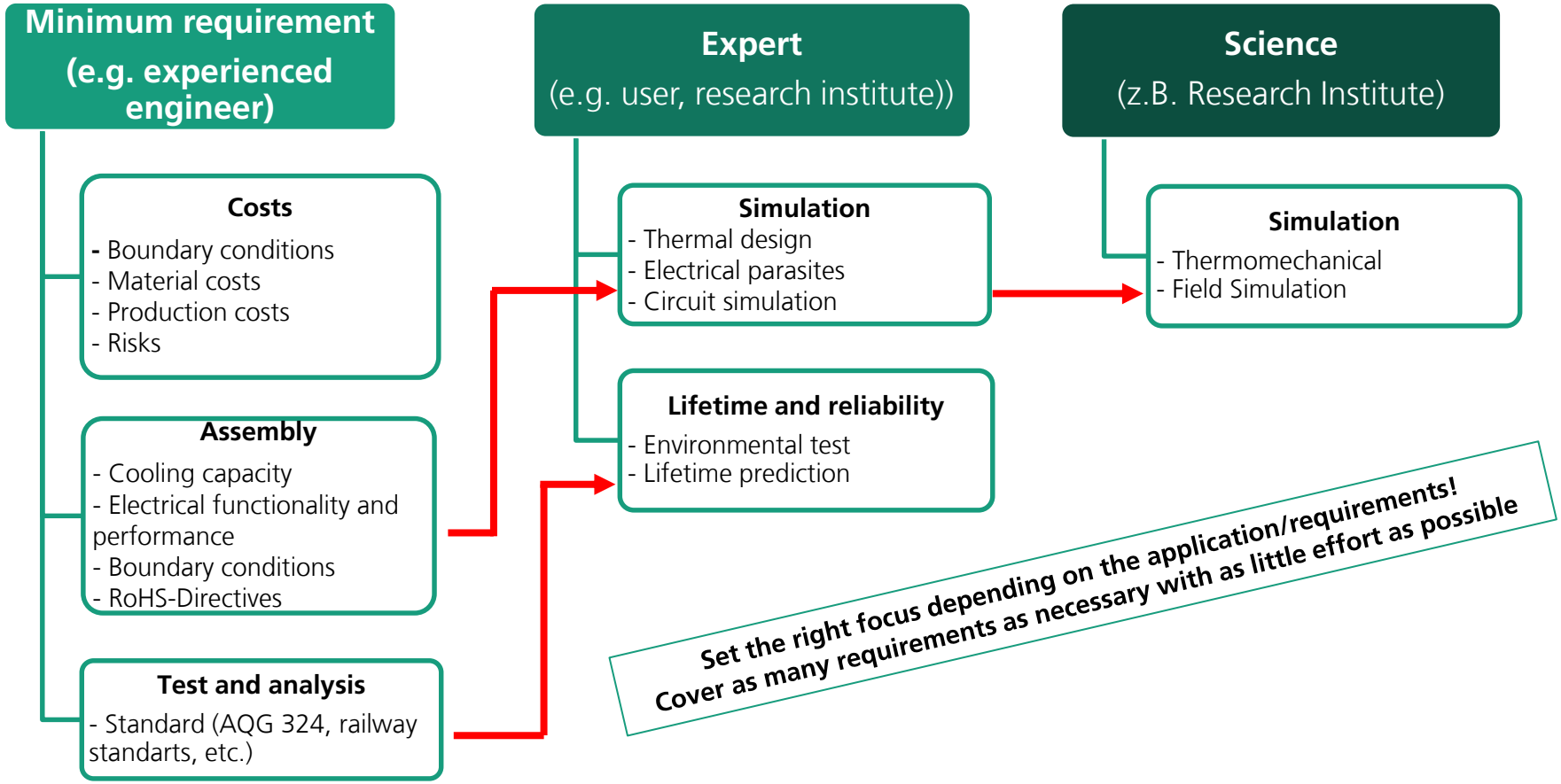
Summary

Aspects to be considered and procedure for module design - What is needed?



Summary

Concept of component comparison

Comparative consideration of the main aspects	A	B	C	D
Expenses				
Functionality				
Production possibilities (internal/external)				
Longevity/ reliability				
1. Thermomechanical Most critical test: temperature shock test (TCT or TST), cold & hot storage, etc. (possibly function test under extreme temperature conditions see above) or also load change test) Here, in case of unavailability, thermal and thermo-mechanical simulations are possible or other AVT options are exhausted until a target test value is reached or the equivalent stresses in the model are reduced, etc.				
2. Vibration, mechanical shock Test according to desired standard, as most critical (vibrometer, possibly HASS/HALT) Here, in case of unavailability, vibrometric simulations (eigenmodes) and partial tests to improve the vibration resistance				
3. chemical, environmental compatibility Single gas test with H_2S or NO_2, as the most critical harmful gas tests for weak point detection Here, in case of unavailability, examination of the weak points shown and the passivating metallization as well as the insulating coating				

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THANK YOU FOR YOUR ATTENTION!

Fraunhofer IISB

Schottkystraße 10
91058 Erlangen
Germany

Dr. Christoph F. Bayer et al.
christoph.bayer@iisb.fraunhofer.de

www.iisb.fraunhofer.de

Contact

K. Chuluunbandi, L. Bach, U. Waltrich, A. Schletz, T. Menrath

Fraunhofer IISB