n-TYPE SILICON SOLAR CELLS WITH AMORPHOUS/CRYSTALLINE SILICON HETEROJUNCTION REAR EMITTER

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ABSTRACT

We present the first silicon solar cells processed at Fraunhofer ISE featuring an amorphous/crystalline silicon heterojunction rear emitter and a diffused front surface field.

In this work, we focus on the optimization of the silicon heterojunction rear emitter of *n*-type silicon solar cells with regards to the intrinsic hydrogenated amorphous silicon a-Si:H(i) and boron-doped hydrogenated amorphous silicon a-Si:H(p) layer thickness and the influence of a transparent conducting oxide layer on the rear emitter surface. Efficiencies up to 19.1 % (V_{oc} = 687 mV, J_{sc} = 34.9 mA/cm^2, FF = 79.9%) have been reached for non-textured solar cells on *n*-type absorbers. Furthermore, we attained an efficiency of 19.8% on textured p-type absorbers featuring an amorphous/crystalline silicon heterojunction rear emitter.

INTRODUCTION

Amorphous/crystalline silicon heterojunction (a-Si:H/c-Si SHJ) solar cells [1-11] featuring a heterojunction at the front and back side of the solar cell allow to achieve open-circuit voltages (V_{oc}) beyond 700 mV for a simple one dimensional cell design. However, the crucial factor in order to reach high efficiencies is the design of the heterojunction at the illuminated front side. The optimisation of this contact is a trade-off between V_{oc}, short-circuit current density (J_{sc}) and fill factor (FF). With increasing thickness of the intrinsic and doped layers, the passivation and the band bending at the a-Si:H/c-Si interface improves, leading to higher V_{oc} [4, 11]. However, to enable a sufficient carrier transport, the thickness of the intrinsic layer is limited to approximately 5 nm [1, 4, 12]. Therefore, V_{oc} can only be enhanced by increasing the thickness of the doped layer, which leads to higher absorption within the front side amorphous layer system. Due to the low minority carrier diffusion lengths within the amorphous layers, photo-generated carriers recombine before reaching the separating junction and, therefore, J_{sc} decreases with increasing layer thickness. This behaviour becomes even more crucial for heterojunctions formed on textured surfaces [4, 7, 10].

To overcome this problem, the silicon hetero-emitter is formed at the rear side and a phosphorus-diffused homo-front surface field (FSF) is used at the front side resulting in a n^+np^+ solar cell structure [13]. This allows the optimization of the hetero-emitter only in respect to its electrical properties. Thus, the thickness of the doped layer can be optimized until either the vertical conductivity or the recombination within the volume of this layer becomes the limiting factor. Another advantage is that the SHJ at the rear is formed at a planar and not textured surface. This leads to a better passivation of the a-Si:H/c-Si interface [4, 7, 10]. Furthermore, for the applied front contact no transparent conducting oxide (TCO) layer is required. This further improves the quantum efficiency for shorter wavelengths and therefore the J_{sc} compared to cells featuring a SHJ at the front.

We have already used a similar n^+np^+ structure for manufacturing simple and high-efficiency *n*-type solar cells featuring a screen-printed aluminium-alloyed rear p^+ emitter. Efficiencies up to 20.1% (V_{oc} = 649 mV, J_{sc} = 39.3 mA/cm^2, FF = 78.9%) have been reached for these cells [14], proving the high potential of this simple cell design. By placing a hetero-emitter at the back of the cell, we aim to increase V_{oc} and thus the efficiency of this type of cell.

EXPERIMENTAL

Figure 1 shows a schematic cross-section of the investigated solar cells. Small (2 x 2 cm^2) solar cells have been fabricated on non-textured, 200 µm thick, 1 Ω cm and 10 Ω cm *n*-type float-zone silicon wafers using a high-efficiency cell process. A shallow 150 Ω/□ phosphorus c-Si(n^+) FSF diffusion [15] forms the majority carrier contact. A stack of a thin thermally grown oxide (SiO$_2$) and a silicon nitride (SiN$_x$) layer deposited by plasma-enhanced chemical vapor deposition (PECVD) serves the purposes of passivation and antireflection [15]. The front side metallization consists of a thermally evaporated Ti/Pd/Ag stack thickened by silver plating. For
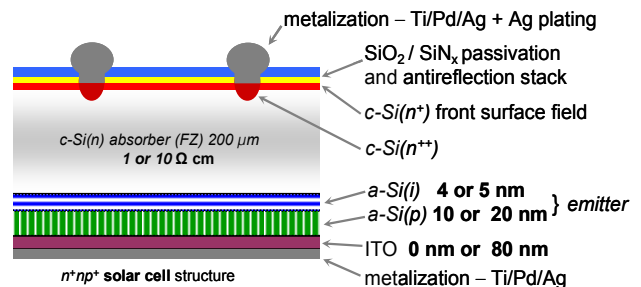

Figure 1: Schematic cross-section of the *n*-type silicon solar cell with amorphous/crystalline silicon heterojunction rear emitter.

process temperatures above 200°C, applied after the deposition of the amorphous layers, a significant degradation of V_{oc} caused by the SHJ emitter is observed [16]. Therefore the conventional contact annealing well above 200°C for the semiconductor/metal contact at the front side can not be applied to this type of cell. To realise a sufficient contact resistance, a deep 20 Ω/□ phosphorus c-Si(n^{++}) diffusion was carried out underneath the front side metallization. In addition two grid finger widths of 30 µm and 5 µm were used to investigate the influence of the contact area on the series resistance. The rear hetero-emitter consists of two layers of hydrogenated amorphous silicon (a-Si:H): a thin intrinsic layer of a-Si:H(*i*) directly on the rear surface of the *n*-type absorber, covered by a boron-doped layer a-Si:H(*p*). The a-Si:H(*i*)/a-Si:H(*p*) stack has been deposited by means of PECVD, using a 13.56 MHz parallel plate reactor (PP). For the optimization of the rear emitter, a-Si:H(*i*) layers of about 4 nm or 5 nm and a-Si:H(*p*) layers of about 10 nm or 20 nm have been used. For some cells, the emitter stack is covered by 80 nm sputtered indium tin oxide (ITO). The back side metallization is realized by thermal evaporation of Ti/Pd/Ag. The influence of the different parameters have been investigated by dark and light current density-voltage (J-V) characteristics, quantum efficiency and Suns-Voc measurements.

RESULTS AND DISCUSSION

Influence of a-Si:H(*i*) and a-Si:H(*p*) thickness and ITO

In Figure 2 the maximum V_{oc} and maximum *FF* for solar cells with 1 Ω cm absorber and 30 µm grid fingers width are shown. A maximum V_{oc} of 704 mV was reached. As expected, an increase of V_{oc} for increasing a-Si:H(*i*) and a-Si:H(*p*) layer thickness can be seen. This holds for cells with and without ITO at the rear. Compared to our full SHJ
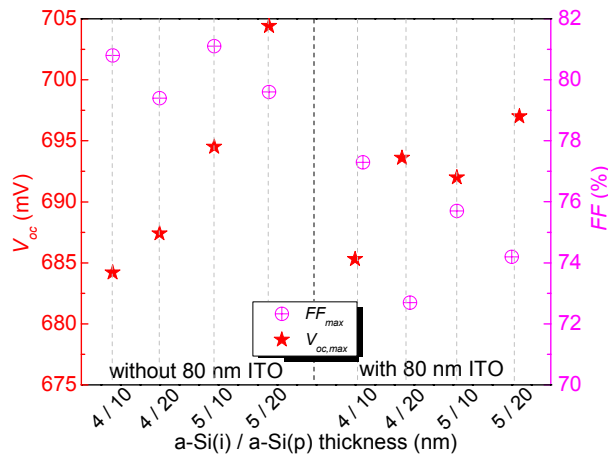

Figure 2: Maximum V_{oc} and fill factor (*FF*) for planar n⁺np⁺ cells with 1 Ω cm absorber. Variation of a-Si:H(i) and a-Si:H(p) thickness, with and without ITO.

a-Si:H(i) (nm)	a-Si:H(p) (nm)	ITO	grid finger width (µm)	R_s (Ω cm²)	PFF – FF (%)
4	10	No	30	0.4	0.3
	20			0.5	1.2
5	10			0.4	0.7
	20			0.8	2.1
4	10	Yes		1.0	3.5
	20			2.1	8.4
5	10			1.5	5.5
	20			2.8	10.9
4	10	No	5	0.5	1.8

Table 1: Series resistance (R_S) and difference between pseudo fill factor (*PFF*) and fill factor (*FF*) for the cells with highest *FF* shown in Figure 2.

solar cells [10], the influence of the a-Si:H(*p*) layer thickness on V_{oc} is substantially lower than expected. Estimations of the V_{oc} potential while considering only the FSF and bulk recombination as limiting factors [15], and taking the applied c-Si(n^{++}) and metallisation fraction into account, resulted in a maximum V_{oc} of about 720 mV for planar surfaces. Summing up it can be stated that the recombination losses of the SHJ rear emitter are the limiting factor.

It can be seen for cells with ITO that a comparable V_{oc} level can be reached. This means that the deposition process of the ITO has no negative influence on V_{oc} and the inversion of the SHJ emitter and the involved limitation of the V_{oc} by the TCO layer as observed elsewhere [17] can be excluded for this contact.

Corresponding to the *FF* shown in Figure 2, the series resistance (R_s) determined from light J-V and Suns-Voc characteristics [18] is summarized in Table 1. For cells without ITO, high *FF*s of up to 81.1% have been reached. For cells with ITO, the *FF* is limited to 77.3%. It can be seen that the drop in *FF* observed for cells with ITO is attributed to an increased series resistance. This finding gives us an opportunity to learn more about a possible *FF* limitation of our full SHJ solar cells. Further investigations are required to identify whether this effect is caused by the a-Si:H(*p*)/ITO or the ITO/Ti contact.

For the a-Si(*p*) layer a clear trend towards lower *FF* for increasing layer thickness can be seen. As shown in Table 1 this effect is related to an increased series resistance. This was unexpected for the investigated layer thicknesses [4] and can most likely be explained by the decreased vertical conductivity of the a-Si:H(*p*) layer with increasing thickness.

Surprisingly, no negative influence of the a-Si:H(*i*) layer thickness on the *FF* is observed. However, taking a closer look on R_s only for cells without ITO and 10 nm a-Si:H(*p*) a similar R_s observed. A very low R_s of 0.4 Ω cm² was reached for this cells. For all other cells, an increase in R_s for increasing a-Si:H(i) thickness is observed.

In summary it can be said that the influence of the a-Si:H(*i*) layer thickness on *FF* and R_S is less pronounced than the one of the a-Si:H(*p*) layer thickness and of the ITO layer. For cells without the limitation of R_S due to the
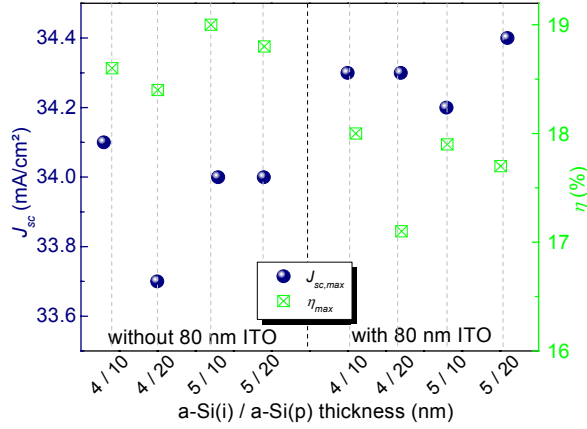
Figure 3: Maximum J_{sc} and efficiency (η) for planar n^+np^+ cells with 1 Ω cm absorber. Variation of a-Si:H(i) and a-Si:H(p) thickness with and without ITO.

ITO and/or 20 nm a-Si:H(p), it can be concluded that a-Si:H(i) layers up to 5 nm do not contribute to FF or R_s and therefore form no relevant transport barrier for these cells.

In Figure 3, the maximum J_{sc} and maximum efficiency (η) values of the planar solar cells with 1 Ω cm absorber and 30 µm grid finger width are shown. Concerning the a-Si:H(i) and a-Si:H(p) layer thickness, no influence on the J_{sc} can be seen. For cells with ITO at the rear, a higher J_{sc} is observed. This is attributed to the fact that the ITO layer acts as a dielectric mirror, which increases the quantum efficiency for wavelengths above 950 nm.

The highest efficiency for 1 Ω cm solar cells with 30 µm grid finger width is 19.0% (V_{oc} = 694 mV, J_{sc} = 33.8 mA/cm², FF = 81.1%). These results have been reached for a cell without ITO, an a-Si:H(i) layer thickness of 5 nm, and an a-Si:H(p) layer thickness of 10 nm. This efficiency is primarily limited by the low J_{sc} due to the non-textured front.

Influence of absorber resistance and grid finger width

For cells with 10 Ω cm absorber, a similar behavior concerning V_{oc} and FF was found compared to cells with 1 Ω cm absorbers. However, for J_{sc} a gain of about 1 mA/cm² was observed. This is mainly attributed to the fact that for increasing absorber resistance, the passivation of the front side is improved. This effect is well known for cells featuring a FSF [19]. For cells with 10 Ω cm absorbers, we achieved a maximum efficiency of 19.0% (V_{oc} = 693 mV, J_{sc} = 34.7 mA/cm², FF = 78.8%). The associated cell features a 5 nm a-Si:H(i) and a 10 nm a-Si:H(p) layer and no ITO.

The highest efficiency has been reached for cells with a 1 Ω cm absorber and decreased grid finger width (η = 19.1%, V_{oc} = 687 mV, J_{sc} = 34.9 mA/cm², FF = 79.9%). This can be explained by the increase in J_{sc} of about 1 mA/cm² due to the decreased shaded area of the front side metallization. This result was reached for a

cell without ITO and with a 4 nm a-Si:H(i) and 10 nm a-Si:H(p) layer.

For annealing temperatures of 150°C, very low series resistances of 0.4 mΩ cm² (Table 1) have been reached for the best cells. This leads to the conclusion that for cells with 30 µm grid finger width the contact resistance of the c-Si(n^{++})/Ti/Pd/Ag is not a limiting factor. For the cells with 5 µm grid finger width, the decreased contact area leads to a slight but tolerable increase in series resistance.

Another observation is the relatively low PFF of below 82% of all solar cells under investigation. For cells with 10 nm a-Si:H(p) and without ITO the small difference between PFF and FF can be attributed to the very low series resistances. Therefore it can be concluded that the FF is at least partly limited by the PFF. This low intrinsic FF is also observed for our full SHJ solar cells. Limiting factors such as junction quality and shunt resistance still have to be investigated.

OVERVIEW OF RESULTS FOR n- AND p-TYPE SOLAR CELLS WITH SHJ REAR EMITTER

In Table 2 an overview of results for solar cells with SHJ rear emitter is given. In the first row the details for the best n-type cell are shown. In the second row the results for a comparable cell with textured front (inverted pyramids) can be seen. As expected, an increase in J_{sc} is observed. Unfortunately, this batch of cells suffers from technological problems with the front side metallization. This limits the FF to 66%, therefore, an efficiency of only 17% was reached. Furthermore, we present results for p-type solar cells featuring a boron-doped FSF, passivated by Al_2O_3 and an a-Si:H(i)/a-Si:HC(n) rear emitter. Efficiencies of 19.8% have been reached for these cells. As known from full SHJ solar cells, we achieved a lower V_{oc} for p-type cells compared to n-type cells [3, 20, 3].

structure	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm²)	η (%)
p^+nn^+ - planar	687	79.9	34.9	19.1
n^+np^+ - textured	681	66.2	37.8	17.0
p^+pn^+ - textured	667	78.6	37.8	19.8

Table 2: Overview of results for solar cells with SHJ rear emitter fabricated at Fraunhofer ISE.

SUMMARY

We have successfully adapted our silicon heterojunction emitter to the n^+np^+ solar cell structure. A significant increase in V_{oc} of 49 mV from 655 mV for the passivated aluminium-alloyed rear emitter [14] to 704 mV for the a-Si:H(i)/a-Si:H(p) rear emitter was reached. Besides the high V_{oc}, we managed to obtain a high FF of 81.1%. It is important to note that this FF is not limited by the series resistance of the a-Si:H(i) layer. Another observation is the

decrease of *FF* for increasing a-Si:H(*p*) layer thickness (10 nm vs. 20 nm). This means that, as is already known for the a-Si:H(*i*) layer, the trade-off between V_{oc} and *FF* with differing layer thickness also applies for the a-Si:H(*p*) layer. Furthermore, we could show that the applied ITO has no negative influence on V_{oc}. We also found that when using an ITO layer between the SHJ rear emitter and the back side metalization, the *FF* is decreased. A maximum efficiency of 19.1% which is restricted by the low J_{sc} due to the non-textured front of these solar cells, has been attained.

ACKNOWLEDGEMENTS

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