

## LARGE-AREA N-TYPE SILICON SOLAR CELLS WITH PRINTED CONTACTS AND ALUMINIUM-ALLOYED REAR EMITTER

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**ABSTRACT:** We have further improved our *n*-type silicon solar cells with full-area screen-printed aluminium-alloyed rear  $p^+$  emitter. For our laboratory-type  $n^+np^+$  back junction solar cells ( $4\text{ cm}^2$ ) featuring a high-efficiency front side with evaporated contacts, we have optimised the rear Al- $p^+$  emitter and the phosphorus-diffused  $n^+$  front surface field including the antireflection coating. Thereby, we have obtained an increase in the open-circuit voltage of around 15 mV, resulting in excellent  $V_{oc}$  values for this cell structure above 640 mV and cell efficiencies of 19.8 %. By applying an industrially feasible front metallisation of aerosol-printed and silver-plated contacts, we have successfully demonstrated the upscaling of our cells to large areas. For our best industrial-type  $n^+np^+$  solar cell with front and rear printed contacts, we have achieved a record-high efficiency of 18.2 % ( $148.5\text{ cm}^2$ ) on *n*-type phosphorus-doped  $10\text{ }\Omega\text{cm}$  monocrystalline silicon material.

**Keywords:** *n*-type Solar Cells, Aluminium-alloyed Emitter, Printed Contacts

### 1 INTRODUCTION

Today, more than 90 % of the industrially produced silicon solar cells are made from *p*-type crystalline silicon wafers. This is mainly due to the fact that the processing sequence, in particular the phosphorus diffusion for the  $p^+$  emitter formation, is well established in industrial solar cell production since many years. Nevertheless, *n*-type silicon has been proven to be a stable high-lifetime material featuring superior electrical properties compared to *p*-type silicon [1] and, therefore, it has become of growing interest for photovoltaic cell research and development during recent years. The large potential of this material for the application to industrial high-efficiency cells is further supported by the fact that the two only companies which produce high-efficiency solar cells today, SunPower and Sanyo, are using *n*-type Si wafers in their lines. Thus, a suitable solar cell fabrication process should yield high efficiencies. However, the high temperature boron diffusion needed for the formation of the  $p^+$  emitter is technologically challenging and can lead to a severe degradation of the electronic bulk properties. Therefore, we use aluminium-alloying from screen-printed Al pastes to form an Al-doped  $p^+$  emitter on the rear surface of the cell. One great advantage of this back junction *n*-type cell structure is the fact that the process step for rear emitter alloying is already well established for the back surface field (BSF) formation in conventional *p*-type cell production lines.

For back junction  $n^+np^+$  solar cells featuring a screen-printed rear Al- $p^+$  emitter, we have already achieved remarkably high efficiencies: 19.0 % for laboratory-type solar cells ( $4\text{ cm}^2$  aperture area) with evaporated front contact grid [2] and 17.0 % for front and rear screen-printed industrial-type cells ( $100\text{ cm}^2$  total area) [3]. For laboratory cells with a surface-passivated Al- $p^+$  emitter, we have recently demonstrated efficiencies exceeding 20 % [2].

In this work, we focus on a further improvement of (i) our high-efficiency laboratory-type solar cells by optimising the rear Al- $p^+$  emitter and the phosphorus-diffused  $n^+$  front surface field (FSF) including the antireflection (AR) coating and (ii) our large-area industrial-type cells by implementing a new industrially feasible metallisation technique for the front contacts into our solar cell process. As the performance of our back junction *n*-type Si cells is strongly dependent on the quality of the FSF and a low surface recombination velocity is essential for high efficiencies [4], we use aerosol printing [5] and subsequent light-induced silver plating [6] to form the front contact grid. Recently it has been shown that this two-layer metallisation concept is superior to the commonly used screen-printing of metallisation pastes for reaching higher aspect ratios of the contact fingers resulting in lower shading and for forming a good contact to a P-diffused  $n^+$  surface with a decreased peak doping concentration [7]. Therefore, a combination of an aerosol-printed and Ag-plated front grid and a full-area screen-printed rear Al- $p^+$  emitter is very promising to fulfil the demands for easy-to-fabricate highly efficient large-area *n*-type silicon solar cells. In this publication, we first of all describe in detail our  $n^+np^+$  solar cell structures and the processing sequences. Subsequently, we present results and characteristics for our laboratory and industrial cells.

### 2 SOLAR CELL FABRICATION

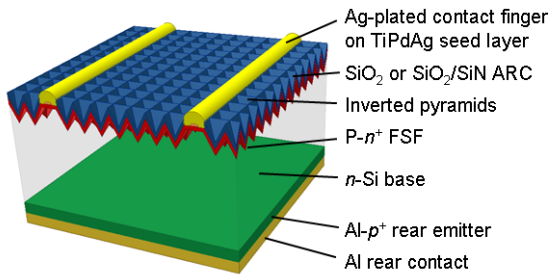
#### 2.1 Cell Structures

In the course of this work, we fabricated two types of  $n^+np^+$  back junction solar cells while both cell types feature a full-area screen-printed Al- $p^+$  emitter on the rear. Figure 1 shows schematic sketches of the realised cell structures:

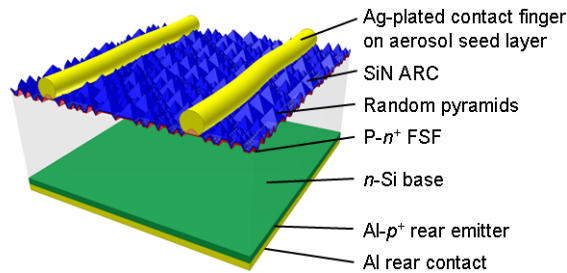
(a) Laboratory-type solar cells ( $4\text{ cm}^2$ ) with a high-efficiency front side consisting of a textured surface with inverted pyramids and a contact grid formed by evaporation of a TiPdAg seed layer followed by silver plating. We fabricated two sets of cells: (i) cells featuring a driven-in phosphorus-diffused  $n^+$  front surface field – with a sheet resistance  $R_{sh}$  of  $120\ \Omega/\text{sq}$  and a peak doping concentration  $N_{peak}$  of  $8 \times 10^{18}\text{ cm}^{-3}$  – and a thermally grown  $105\text{ nm}$  thick silicon oxide layer as surface passivation and antireflection coating and (ii) cells featuring a P-diffused  $n^+$  FSF – with  $R_{sh} = 350\ \Omega/\text{sq}$  and  $N_{peak} = 5 \times 10^{19}\text{ cm}^{-3}$  – and an AR coating stack consisting of a  $10\text{ nm}$  thin thermal  $\text{SiO}_2$  and a plasma-enhanced-chemical-vapour-deposited (PECVD) silicon nitride layer.

(b) Large-area ( $148.5\text{ cm}^2$ ) solar cells with an industrially feasible front side metallisation of an aerosol-printed and Ag-plated contact grid, a textured surface with random pyramids, a P- $n^+$  FSF with  $R_{sh} = 65\ \Omega/\text{sq}$  and  $N_{peak} = 1 \times 10^{20}\text{ cm}^{-3}$  and a PECVD SiN AR coating.

(a) High-efficiency laboratory type



(b) Large-area industrial type



**Figure 1:** Schematic sketches of our  $n^+np^+$  back junction Si solar cells with full-area screen-printed aluminium-alloyed rear  $p^+$  emitter.

## 2.2 Processing Sequences

In this study, we used  $n$ -type phosphorus-doped float-zone (FZ) silicon wafers with a resistivity of  $10\ \Omega\text{cm}$  as base material for our  $n^+np^+$  solar cells.

(a) Laboratory-type solar cells ( $20 \times 20\text{ mm}^2$ ):

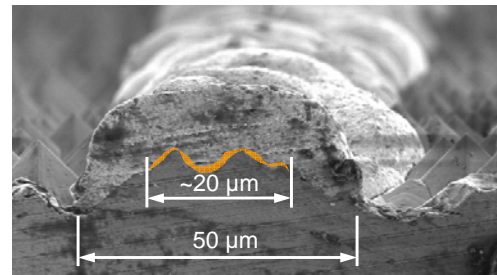
First, a silicon oxide mask is prepared on the rear of the shiny-etched wafers by thermal oxidation and front side etching. Then the front surface is textured with inverted pyramids in KOH solution and, subsequently, the phosphorus-doped  $n^+$  front surface field is formed by  $\text{POCl}_3$  diffusion. In the next step, an antireflection oxide layer is thermally grown and, at the same time, the P-diffusion is driven in. After removal of the  $\text{SiO}_2$  on the

rear, a non-fritted aluminium paste is screen-printed onto the entire surface and, subsequently, the  $\text{Al-p}^+$  emitter is alloyed in a conveyor belt furnace at a peak temperature of  $900\text{ }^\circ\text{C}$ . Now, the front contact grid is formed by evaporating Ti, Pd and Ag and a photolithographic lift-off process. After that, the front contacts are thickened by light-induced Ag plating and, finally, the solar cells are annealed in a forming gas ambient at  $425\text{ }^\circ\text{C}$ .

To further improve the cell performance, in a first step we optimised the rear Al emitter properties (depth and homogeneity) by varying the amount of screen-printed paste and the firing conditions for alloying. For non-surface-passivated emitters, deep profiles have been proven to be advantageous due to an enhanced shielding effect of the highly Al-doped region [8]. In a second step, we improved the solar cell's front by replacing the  $105\text{ nm}$  thick AR oxide layer by a stack of a  $10\text{ nm}$  thin thermally grown  $\text{SiO}_2$  and a PECVD SiN layer.

(b) Industrial-type solar cells ( $125 \times 125\text{ mm}^2$ , pseudo):

After saw damage etching, an oxide mask is prepared on the rear of the wafers to allow single-side texturing with random pyramids and a single-side phosphorus diffusion for the front surface field. Subsequently, the oxide is etched off in HF. Then, a PECVD AR silicon nitride layer is deposited on the front and the seed layer of the contact grid is printed via the aerosol technique. After screen-printing of the aluminium paste on the rear, the contacts are co-fired in a belt furnace and, at the same time, the  $\text{Al-p}^+$  emitter is alloyed. Finally, the fired seed layer is thickened during a light-induced silver plating step. Figure 2 shows an SEM picture of a cross-section of an aerosol-printed and Ag-plated front contact finger. The aerosol-printed seed layer has a height of only  $1\text{--}3\ \mu\text{m}$ . Usually, the finger width amounts to  $20\text{--}60\ \mu\text{m}$  after printing and  $40\text{--}100\ \mu\text{m}$  after plating.



**Figure 2:** SEM picture of a cross-section of an aerosol-printed and silver-plated front contact finger. The seed layer is only  $1\text{--}3\ \mu\text{m}$  thick and about  $20\ \mu\text{m}$  wide. Plating of the conductive layer results in an aspect ratio of 0.4.

## 3 SOLAR CELL CHARACTERISATION

### 3.1 Solar Cell Results

Table I summarises the electrical parameters of our back junction  $n$ -type silicon solar cells featuring full-area aluminium-alloyed  $p^+$  rear emitters, fabricated in the course of this work.

By improving screen-printing and firing conditions for the Al emitter formation, the open-circuit voltage  $V_{oc}$  of the laboratory solar cells is remarkably increased from  $625\text{ mV}$  to  $640\text{ mV}$  which is an excellent  $V_{oc}$  value for this cell type. Similar high values have been reached formerly by our reference process only after application

**Table I:** Electrical parameters measured under standard testing conditions (AM1.5G, 100 mW/cm<sup>2</sup>, 25 °C) of our  $n^+np^+$  solar cells with full-area screen-printed aluminium-alloyed rear emitter fabricated on  $n$ -type phosphorus-doped 10  $\Omega$ cm float-zone Si wafers.

Cell type	Cell area [cm <sup>2</sup> ]	Front contact grid	Further details	$V_{oc}$ [mV]	$J_{sc}$ [mA/cm <sup>2</sup> ]	$FF$ [%]	$\eta$ [%]
Laboratory	4.0 (aperture)	Evaporated TiPdAg seed layer, Ag-plated	Reference process [2], AR SiO <sub>2</sub>	625	38.4	79.1	19.0*
			Improved rear Al- $p^+$ , AR SiO <sub>2</sub>	640	37.9	79.4	19.2*
			Improved rear Al- $p^+$ , AR 10 nm SiO <sub>2</sub> /SiN	642	38.7	79.6	19.8*
Industrial	148.5 (total)	Aerosol-printed seed layer, Ag-plated	AR SiN	632	36.0	80.0	18.2*

\* Confirmed at Fraunhofer ISE CalLab, Freiburg, Germany

of an additional passivation layer of amorphous silicon or aluminium oxide on the rear emitter surface [2]. We observe a light decrease in the short-circuit current density  $J_{sc}$  by 0.5 mA/cm<sup>2</sup> which we relate to a degradation of the AR SiO<sub>2</sub> layer during emitter alloying. After implementation of a firing-stable AR SiO<sub>2</sub>/SiN coating stack,  $J_{sc}$  values of 38.7 mA/cm<sup>2</sup> are obtained, resulting in cell efficiencies up to 19.8 %.

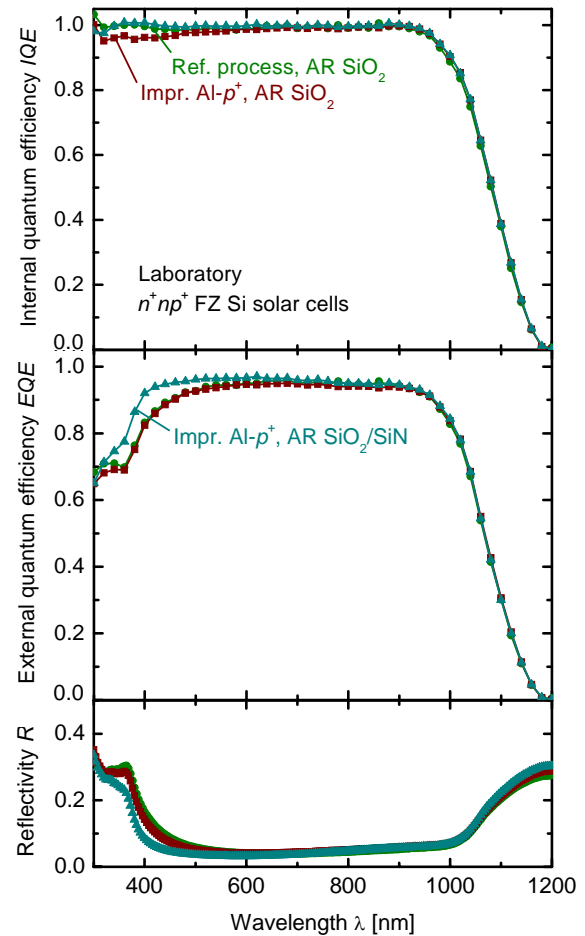
For our large-area solar cells with front aerosol-printed contacts, an efficiency of 18.2 % is reached, demonstrating the industrial feasibility and the successful upscaling of this cell concept. Compared to cells featuring a conventional screen-printed front grid [3], all cell parameters could be significantly increased by applying our two-layer metallisation technique. Open-circuit voltages above 630 mV and fill factors  $FF$  of 80 % show the high potential of these solar cells.

### 3.2 Solar Cell Quantum Efficiency Analysis

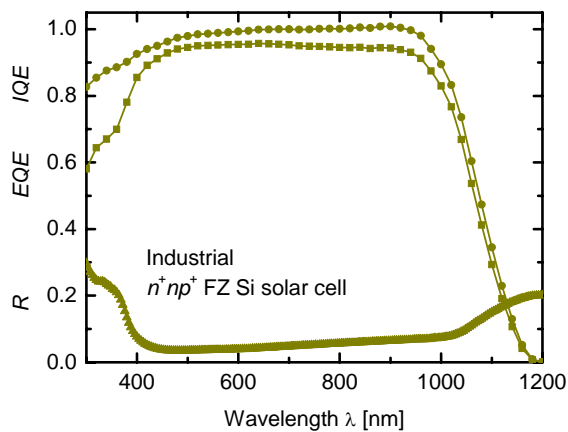
We carried out measurements of the external quantum efficiency  $EQE$  and of the hemispherical reflectance  $R$  to determine the internal quantum efficiency  $IQE$ .  $EQE$  and  $R$  have been measured with spot sizes smaller than 1 cm<sup>2</sup> on cell areas without busbars.

Figure 3 shows the  $IQE$ ,  $EQE$  and  $R$  curves of the three laboratory-type cells of Table I. For the reference cell, high  $IQE$  values near 1 are achieved for a wide wavelength range  $\lambda = 300\text{--}900$  nm, demonstrating the excellent surface passivation quality of the applied front surface field including the SiO<sub>2</sub> layer as well as the high minority carrier bulk lifetime of the base material. After adapting the printing and firing conditions for alloying electrically improved Al emitters, we observe a light decrease of the  $IQE$  curve for short wavelengths which we relate to a degradation of the SiO<sub>2</sub> antireflection coating during the firing process. Replacing the AR SiO<sub>2</sub> layer by an SiO<sub>2</sub>/SiN stack improves the front surface properties to withstand emitter alloying, leading to enhanced  $IQE$  values. Furthermore, the reflectivity on the front is decreased significantly by the SiO<sub>2</sub>/SiN stack.

The  $IQE$  curve of our large-area industrial-type solar cell plotted in Figure 4 shows values near 1 for a wavelength range  $\lambda = 500\text{--}900$  nm, demonstrating the high bulk quality. At the front, only poor  $IQE$  values are

**Figure 3:** Internal, external quantum efficiencies and reflectivities of the laboratory-type  $n^+np^+$  Si solar cells of Table I.

reached, indicating much potential for further improvements, e. g. by application of an SiO<sub>2</sub>/SiN AR stack suitable for a more effective passivation of phosphorus-diffused surfaces with peak doping concentrations  $\leq 1 \times 10^{20}$  cm<sup>-3</sup>. The lower internal reflectance at the rear arises as a consequence of the higher surface roughness of the KOH-etched wafers compared to those of the shiny etched ones used for the lab cells.



**Figure 4:** Internal, external quantum efficiencies and reflectivities of the industrial-type  $n^+np^+$  Si solar cell of Table I.

#### 4 SUMMARY

We have further improved our  $n^+np^+$  back junction silicon solar cells with screen-printed aluminium-alloyed rear  $p^+$  emitter. For our laboratory high-efficiency cells ( $4\text{ cm}^2$ ) we optimised (i) printing and firing conditions for rear emitter alloying and (ii) the phosphorus-diffused  $n^+$  front surface field including the antireflection and passivation layer. Thereby, the open-circuit voltage has been increased by around 15 mV to values above 640 mV which are excellent for this cell type featuring no additional surface passivation of the emitter. This leads to cell efficiencies of 19.8 %.

We have demonstrated the industrial feasibility and the successful upscaling of this cell structure by manufacturing large-area ( $148.5\text{ cm}^2$ ) front and rear printed solar cells. By applying our two-layer metallisation concept for the front contact grid, consisting of an aerosol-printed seed layer and a silver-plated conductive layer, record-high efficiencies of 18.2 % have been obtained. This is, to our knowledge, the highest efficiency for  $n$ -type silicon solar cells with aluminium emitter and printed contacts reported so far.

We are confident that by optimisation of the front surface field of the industrial-type solar cells and, furthermore, by applying an effective surface passivation (e. g. amorphous silicon or aluminium oxide layers) on the rear  $\text{Al-}p^+$  emitters of our  $n^+np^+$  back junction solar cells we will achieve efficiencies towards 21 % for our laboratory and 19 % for our industrial cells, respectively.

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