Thermal On-Board Spectroscopy : Thermal Impedance Simulation Using FEM and Thermal Modelling

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Abstract

Autonomous driving, together with electromobility, is the next major innovation step in future mobility. Not only does it add a gain in comfort but also increases vehicle and road safety. In addition to the more obvious challenges, such as the performance of algorithms (artificial intelligence), there are also major open issues regarding hardware reliability. A computer-controlled vehicle is directly relying on the functionality of its electronic components. In completely autonomous operation, with lack of human supervision, the functional failure of electronic components becomes a central issue. That's why, a safe electronic surveillance system must take over the role of human supervision in the future. To improve the electronics' functional safety, much research has already been done in recent years. On a basic level, the on-board sensor implementation to observe the system temperature and observing the thermal management for electronic devices is a well advanced topic and has been existing for a while in the automotive industry in general. However, an "intuitive" early detection of physical defects was rarely in focus. In this paper, a defect diagnosis and physical damage detection method for electronics packaging and assembly is being presented. This process of thermal on-board spectroscopy uses intelligent temperature sensors to monitor the status of electronic assemblies and ECUs during vehicle use by analyzing the thermal impedance and the time-dependent thermal changes of the electronic packaging system.

1. Research methodology

The aim of this research is first to check if the investigated failure mechanism of the components can influence the heat transfer, secondly if this heat transfer modifications can be detected with the built-in sensors on the board. Lastly it is investigated if different failure mechanisms or damages can be distinguished.

The method used to analyze the thermal behavior for the different possible damages in this research is the finite element method (FEM) followed by thermal compact modelling with an RC-network.

First the electronic components are modelled in CAD and then introduced in the FE simulation program. The program (e.g. ANSYS) computes several transient thermal load cases, each case corresponds to a failure mechanism occurring at different location in the electronic components. The simulation shows the heat transfer behavior of the overall system detected at the sensors' area.

To ensure the delivery of accurate and reliable results, the simulation model must be validated. Therefore, several boards of the same design are experimentally tested, where each board contains one remarkable damage that is incorporated on purpose. The comparison will serve as validation for the simulation results and prove the feasibility of the approach. To ensure nominal design parameter equality between the CAD data and the manufactured boards, optical tests are done to check the dimensions and the deviation from the original design resulting from errors in production or finishing. The test board is also CT-scanned to check and measure the layers and components like solder layer which can't be detected visually. This examination process is necessary to confirm accuracy of the simulation model.

The third step is to proceed with experimental measurements of the test board. In this step the chip will be heated up by a specified current and the on-board sensors will take the measurement to determine the thermal behavior. This process will be repeated simultaneously for each test board variation where different cooling curves and thermal behavior are detected. The experimental measurement data will be used as reference to build and validate the simulation model.

The FE model is a geometric model based on the nominal design with nominal dimensions, but the production and finishing inaccuracies are taken into consideration as well as the results of the CT scan concerning the solder layer. The simulation takes place with the same boundary conditions as the experiment measure. Once the results match, the model is assumed as validated and reliable to simulate further possible failures.

Some typical failure mechanisms occurring in the system are damage in the die attach, solder lot failure characterized by voids, damage in the PCB, damage in the thermal-via e.g. poor electroplating of the copper or material bad quality, voids in conductive paste and wire frame or cracking mold compound caused by fatigue or thermal shock. Figure 1 shows the different components of the assembly where the damage can possibly occurs.

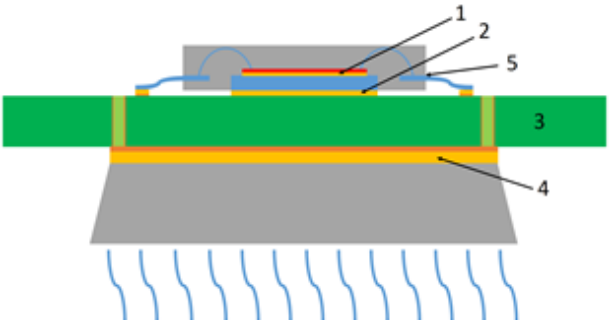

Figure 1: Electronics packaging module components: 1. Die attach, 2. solder layer, 3. PCB, 4. conductive paste, 5. wire frame

The FE simulation will deliver as results the thermal behavior characterized by the cooling curve as a function of time. Once the failure mechanisms are modelled and detected by the sensors, the data will be collected in one database including the thermal behavior of the system for each damage.

Analog thermal simulation:

Second part of the simulation is setting up an analog simulation model based on the thermal impedance curve. Another way to simulate and to visualize the failure is following the method of thermal resistance, junction-to-case determination or the thermal impedance, Z_{th}. Thermal resistance, junction-to-case by definition is the thermal resistance from the active heated layer of a semiconductor device to the outside surface of the package (case). This is limited to the chip mounting area when the heat flow is properly transmitted through the surfaces. There are different ways to determine the Z_{th} such as using the structure functions of one-dimensional heat-flow through a layered structure. This method has limited capacity to determine the thermal resistance since it only applies for one dimensional heat flow path with the same cross section area. This is not the case for the investigated chip package since the heat source (chip) is covered by the mold and in contact with lead frame which applies heat flow in different direction known as lateral heat flow. This lateral heat flow is significant and affects the one direction heat flow path. There is an alternative approach to determining the Z_{th} from transient dual interface measurements, which is not based on structure functions. This method is called numerical deconvolution of the function explained in [3].

The traditional method thus requires the measurement of the thermal impedance, Z_{th}. It is calculated as:

$$Z_{th} = \frac{T_J - T_C}{P} \qquad (1)$$

where T_J is the junction temperature, T_C is the case temperature designated as reference temperature, and P is the power dissipation in Watt, used as one single pulse switched on at t = 0 s till it reaches its steady state. In this paper we are interested in determining the effect of damage on the thermal behavior, therefore a mathematical thermal models known as RC network model will be calculated following the method of Y.C. Gerstenmaier [2] and used to simulate the transient thermal behavior of semiconductor devices based on the thermal step-response data. The thermal step-response, known as "transient response" or "heating curve", measures the junction temperature after a sudden step-change in internal power dissipation till it reaches its steady state. In other method, the step response can also be calculated or be defined as the "cooling curve'' after sudden change in the internal power dissipation (in that case power is switched off) till it reaches the steady state at the ambient temperature. For direct measurement of the thermal impedance, Z_{th}, the power dissipation is set at 1 W and the chip is switched on at t=0 s. The reference temperature is set at T=0°C. The simulation runs till it reaches a steady state and stops after 10000 s, which is sufficient to obtain ''transient response'' heating curve. From equation (1), Z_{th} is designated as the junction temperature per Watt (K/W) and can be obtained by measuring the junction temperature as a function of time. This method is used and explained in previous research as in the method of Siegel [4] and in the presentation by GaN systems "Modeling Thermal Behavior" [1].

Next step is to develop a recognition method and algorithms able to analyze the thermal data detected by the sensors on board. These algorithms are used to classify the measured data as representing a system in good condition or possibility of a damaged component. At the end, the project result will be able to deliver a monitoring system for the electronic components where the sensors are able to measure the thermal impedance as a function of time and check if the data corresponds to a safe functional mode or some parts are damaged and need to be repaired or replaced.

Simulation process steps: actual status

The actual state of the research is to define a validated simulation model that delivers reliable results for each relevant failure mechanism in the packaging. This simulation model has to be validated with real measurement data for the same devices and system with the same boundary conditions. For this purpose, a test board has been designed and produced. The test board has two purposes, first to check if the thermal sensors are effective in measuring the thermal behavior and detecting modifications occurring in the package experimentally. Second, they deliver the reference value in order to validate the FE simulation model and make it reliable for further failure mechanisms.

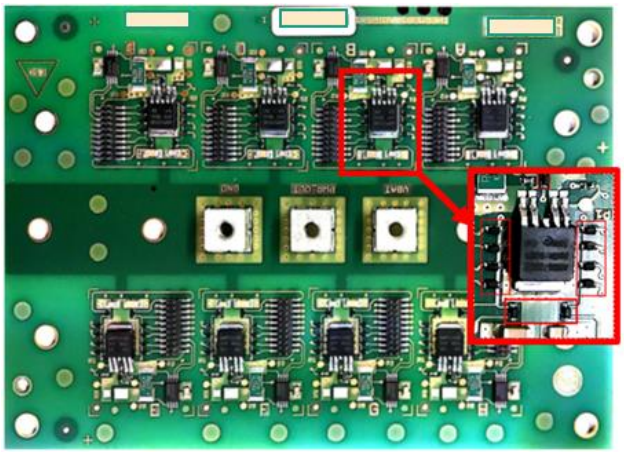

Figure 2: Overview of chip and sensors' locations on test board

This board consists mainly of several chips surrounded by 11 sensors as shown in figure 2. The sensors are surrounding the chip with 8 sensors on the horizontal sides, one on the upper side and 2 on the bottom side. The sensors used on this board are diodes that can measure the voltage at constant current and indicate the temperature by a certain analog factor. The same chip and sensor layout is replicated 8 times. Where each package has a distinct damage that is incorporated on purpose in the solder layer between the lead frame and the PCB. In figure 3, just the solder layer is highlighted where the damage is introduced. In each chip packaging system on the test board different damage sizes and locations are implemented.

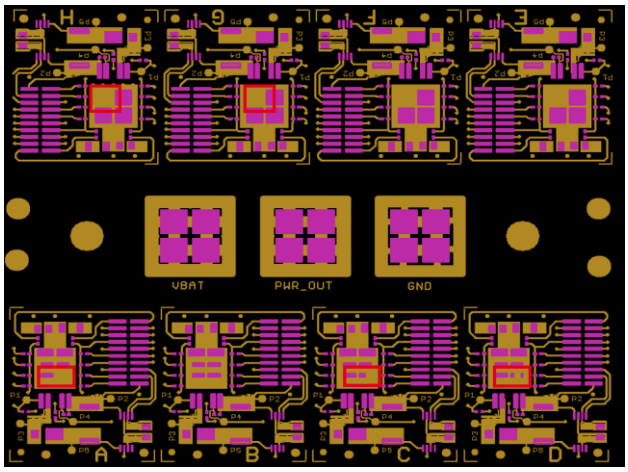

Figure 3: Test board solder layer design with introduced solder voids (highlighted inside the rectangle area)

The variation of the damage in the test board allows the simulation model to be accurately validated. Additionally the limit and the ability of the sensors to detect the possible damage occurring in the solder layer in first place is determine experimentally.

The validation method consists first of an experimental test for the test board. Figure 4 shows the experimental result for one chip as an example. This measurement is repeated for each chip on the board. The module sample used for validation belongs to a package with no introduced damage and the results are shown in figure 4.

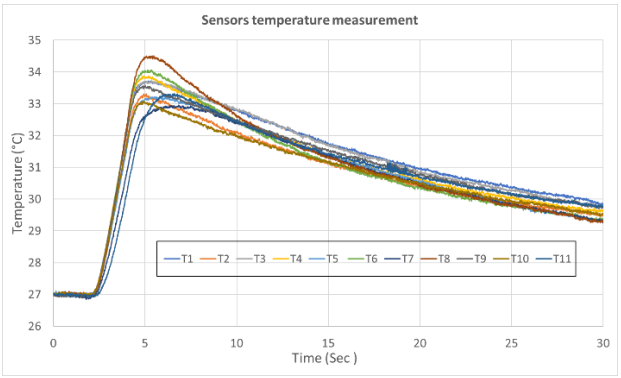

Figure 4 : Temperature curves measured by the sensors

As experimental boundary condition, the input power of the die is set to a pulse of 2.93 W for 2 seconds at room temperature with no cooling device attached. The experimental results show that the current is sufficient to heat up the chip from 27°C to approximately 34°C with some variation from sensor to sensor as shown in figure 4. This variation of the sensor data came from the position of the sensor diodes surrounding the Chip package system. The heat is transmitted by conduction to the rest of the system. It immediately starts to cool down progressively until reaching room temperature again after 3 minutes of time. The system temperature is affected as well by the free convection heat loss to the environmental air in the room. The sensors take measurements every 10 ms for a time interval of 30 s in total. This time is sufficient to obtain the thermal transmission behavior during the cooling phase and notice the thermal changes over time. In total 5 test boards of the same design are measured to take into consideration the tolerance and finishing inaccuracies from production.

To adapt the FE model and obtain similar result as the experiment, two principal factors must be taken into account. First the material characteristics of density, isotropic thermal conductivity and the specific heat capacity for each material of the packaging has to be analyzed. This data should be confirmed and match the material data given by the manufacturing company. Second is the real geometrical measurement of the system components. That's why the test boards are measured after production to check that the nominal design measures match the measures of the product. The real measurement shows a deviation in the dimensions of the solder area, deviation in the diameter of the vias as well as the copper and FR4 material layers thickness in the PCB.

These measurements are taken into consideration in the simulation model for an accurate result. One important aspect for the model is the shape of the solder layer where the damage is introduced. This layer cannot be investigated by visual inspection because it is located beneath the chip. To obtain this measurement we use a computed tomography (CT) scan of each test board to check the

solder layers as it is shown in figure 5.

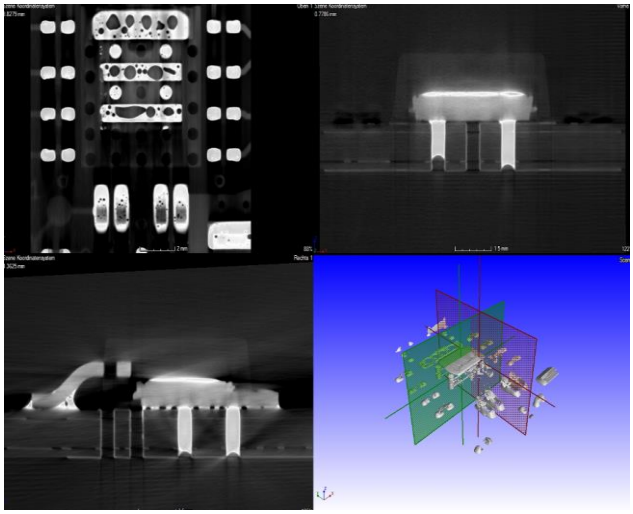

Figure 5: Cross section view in CT photo of the chip package

This cross section top view and side view of the package system allow to detect the production inaccuracies of the test board and a better recognition of the damage size and location in the board which is to be modeled in the FE simulation. Figure 5 shows a top plane view of the solder layer between the chip carrier and the PCB. It is clear in the solder bar that air bubbles are formed in the layer which indicate a production error aspect and might affect the thermal behavior of the system. The right side photo shows a side view cross section image. This photo shows that the vias are filled with solder material that probably slipped out from the solder layer and fills the hole. This damage is resulting from a poor solder coating phase in the production process. This kind of unwanted damage can be critical and presents a significant influence on the thermal impedance, therefore it should be taken in consideration.

From the scanned picture in figure 5, it's clear that the real test board doesn't match the design model exactly, and must be modified in the simulation model in order to obtain accurate or similar results as the experiment.

FE model boundary conditions:

In order to validate the results, the FE simulation model has to be modified. The setup starts in the pre-processing phase. First the geometry model is adapted to the real design board according to the accurate measurement of the components as well as the PCB layers thickness. Second, the solder layer is adapted where the main damage is introduced specially at void formation (bubble shapes) in the solder as shown in the CT pictures in figure 5.

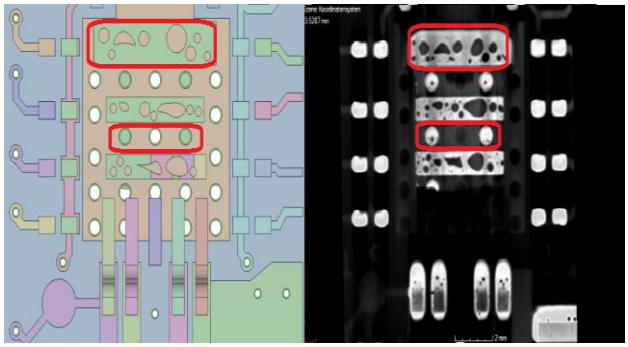

Figure 6: Geometry adaptation for simulation model

In the picture above, the solder layer is adapted geometrically based on the scanned picture of the board, modification is focused on the voids and air bubble formation in the solder bar and on the vias solder filling between the solder bars.

The second phase of model adaption is setting up the boundary conditions for the simulation exactly as in the experiment. The material data are set to the manufacturer reference. The room temperature in the simulation is set to 0°C since we focus only on the temperature difference at the cooling time. Heat flow of 2.93 W for 2 sec is set on the top surface of the chip as measured experimentally. The outer surface of the packaging is exposed to convection heat transfer with the environment air. The PCB layers and the chip package as well as the solder contact layer are exposed to a conduction heat transfer depending on each layer's material density (kg/m^3), isotropic thermal conductivity (W/m·K) and specific heat capacity (J/Kg·K). The simulation time is set to 8 s after the heat pulse which is sufficient to monitor the cooling curve of the system and detect the variation. All components are set to room temperature and convection heat exchange with the environment. Figure 7 and 8 show the curve of the experimental result and the curve of the simulation result respectively for the same sensor "1" and sensor "5". The main validation criterium is the curve shape.

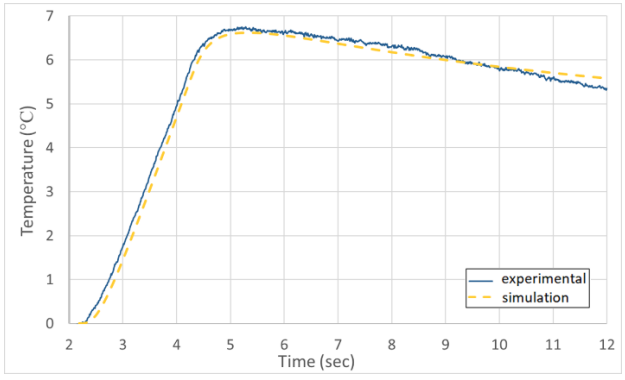

Figure 7: Experimental and simulation results comparison for sensor "1"

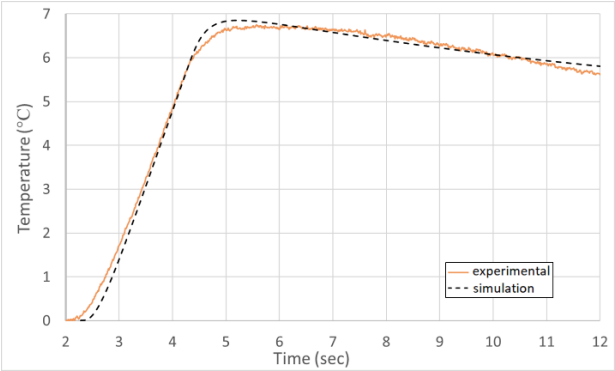

Figure 8: Experimental and simulation results comparison for sensor 5

The graphs in figures 7 and 8 show the temperature curve comparison between the experimental results and the simulation results for two different sensors (sensor "1" and sensor "5" respectively) on the test board of the same module. The temperature curve resulting from the simulation model fits well with the experimental result with deviations of less than 3% and can be considered a good result. To have a reliable simulation model, all chips and their surrounding sensors on the test board must be experimentally measured and compared with the simulation model. Once the simulation model is validated by the experimental measurement by comparing each sensor's simulation result with the experimental measurement the next step in the research is to obtain and create a database containing the specific thermal behavior for each relevant failure mechanism and damage that could be formed and detected. To create this database, several simulations will be performed at different positions in the electronic components.

The following examples show the thermal impedance difference between the original model (no damage) and one models for the same packaging with void formation in the solder layer between the chip carrier and the PCB copper layer. Figure 9 shows the difference at the solder layer between the original model (left) and the model with void.

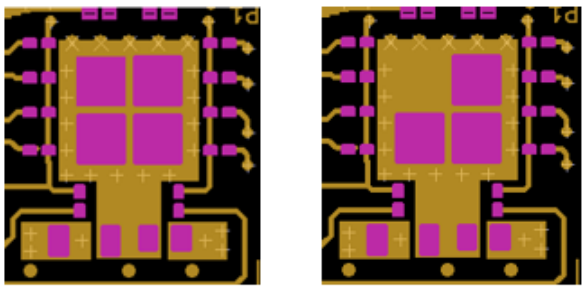

Figure 9: The difference at the solder layer level

Figure 10 shows the temperature difference as a function of time for the same sensor but different models. The load cases in terms of boundary conditions i.e. heat flow and material are the same.

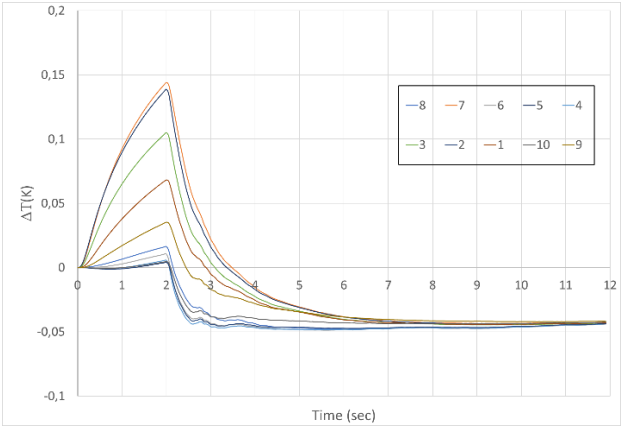

Figure 10: Temperature difference ΔT between model with no damage and model with void damage in the solder layer

The figure 10 shows the temperature difference registered by ten sensors surrounding the chip between 2 simulated models. The difference in models are shown in the figure 9 at the solder level. It is notable that the damage at the die attach layer has significant influence registered by sensors 3, 4, 7, 9 and 10 in heating phase (first 2 seconds). The sensors show that the model with damage is less heated to reach a temperature difference of 0.15 K, whereas in the cooling phase the sensors in the damaged model are cooled down faster the first 4 seconds. Therefore the curves sink down to show a temperature difference of -0.05 K. The temperature difference at the heating and cooling phase confirms that the thermal impedance of the system is influenced by the failure mechanisms and at least for the introduced damage at the die attach level, the sensors are capable of detecting the variations.

These damages or failure mechanisms are among the most likely to occur in the electronic packaging systems and can affect the functionality of the system. Therefore the research will be focused on these damages but also on any other relevant failure mechanism that can be detected by the sensors and can affect the functionality of electronic systems.

Thermal modelling: RC-network simulation

To be useable in an on-board setting the damage detection has to be accomplished with minimal computing power. To regularly do an FEM simulation to determine the location and severity of a possible damage is not feasible. Hence, a compact model is used. This kind of model is commonly used for electrical simulations but works just as well as for thermal modeling by equating the thermal variables to electrical ones i.e. thermal heat flow to electrical current. To perform the equivalent electrical simulations many powerful algorithms are state of the art and can be accessed through specialized programs such as LT Spice or can be implemented on low computing power devices such as a micro controller.

The compact model used in this work is an RC-network i.e. a network consisting of resistances and capacities. There

are two forms of this kind of model that will be discussed here, the Foster model and the Cauer model.
From figure 10, sensor "7" shows significant thermal impedance deviation from the original model (no damage). Therefore, in the following example, the thermal step responses registered by the sensor number "7" will be investigated and the steps for RC-Cauer thermal model will be explained based on the transient heating curve. The method used in this paper is explained well in [6,7]. The model is obtained by linear square fitting function to measured or simulated heating curves. For building the thermal RC model, simulation of the thermal impedance is started by a heat flow of 1W till reaching the steady state. The effective time constants (t) is distributed logarithmically between $t_{min} = 10^{-4}$ s and t_{max}= 1000 s.

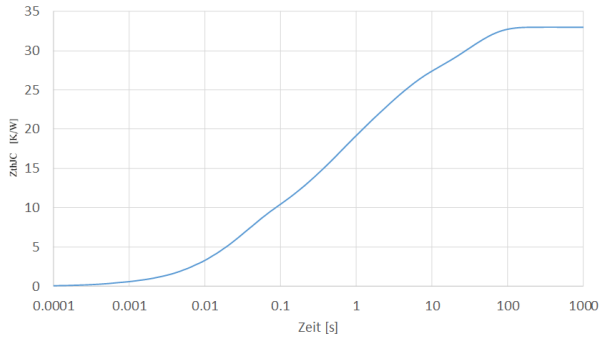

Figure 11: Thermal impedance measured with sensor 7 for a die attach void model

The next step is to fit the simulated thermal curve in figure 11 by the thermal impedance Z_{th}, which represents the Foster thermal circuit and known as:

$$Z_{th1}(x,t) = \sum_{i=1}^{M} R_i(x)(1 - e^{-t/ti}) \qquad (2)$$

With $R_iC_i=t_i$, and $C_i = t_i/R_i$. the thermal curve will be fitted by the corresponding curve for the Cauer model and the number of R and C will be deduced and calculated. The next step is the transformation of the Cauer model to Foster model following a convolution integrals approach. The transformation follows algebraic system by applying the Laplace-transformation. This method is explained in [4].

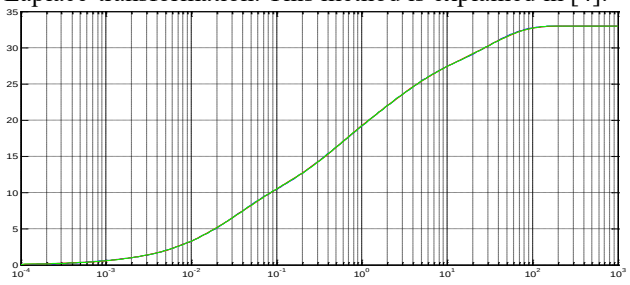

Figure 12: Thermal impedance fitting function curve

Figure 12 shows the fitted function of the thermal impedance in figure 11. Once the model is fitted with the green and red curve (here the green and red curve are not well visible because they are well fitted with the Z_{th} curve), the number of the RC pairs for the Cauer and Foster model as well as their values is determined.
The model can be built and simulated in LTSPICE. It needs to be mentioned here, that the thermal Cauer model is created solely by a mathematical algorithm for fitting the thermal impedance curve and includes no physical description of the real model components. Therefore a structure function analysis (i.e. equating the resistances and capacities to distinct layers or materials of the package) is not possible for this method.

Introducing the last step concerning the circuit simulation in LTSPICE, it has to be noted since the Cauer model is mathematically deduced, some values of the resistance and capacitance can be unrealistic or physically impossible like negative values or extreme high number values of resistance and capacitance. In this case, this resistor and capacitor components should not be simulated in the circuit and could not be built in the electrical circuit in order to obtain a plausible results.

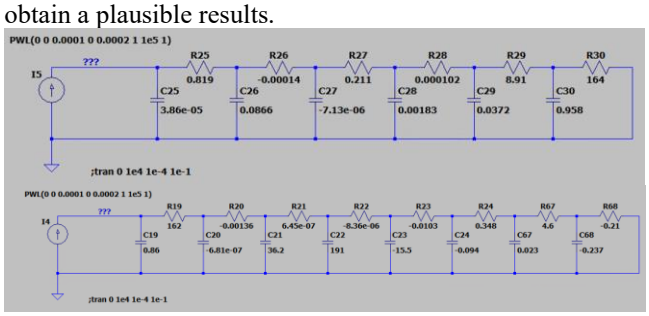

Figure 13: RC Cauer model for sensor 7 with and without simulated damage

Figure 13 shows the Cauer thermal model registered by sensor "7" for the undamaged system and the second for the model with damage in the die attach. The thermal model has to be validated by comparing the FEM simulation with the LT Spice simulation for the thermal curve under the same boundary conditions. It can be confirmed that the Cauer thermal model can deliver reliably repeatable result for the thermal impedance.

Figure 14 shows the thermal impedance curve of the FEM result and the LT Spice temperature curve simulation (same load case and boundary conditions as figure 7) and it can be seen that the two simulations deliver the same result.

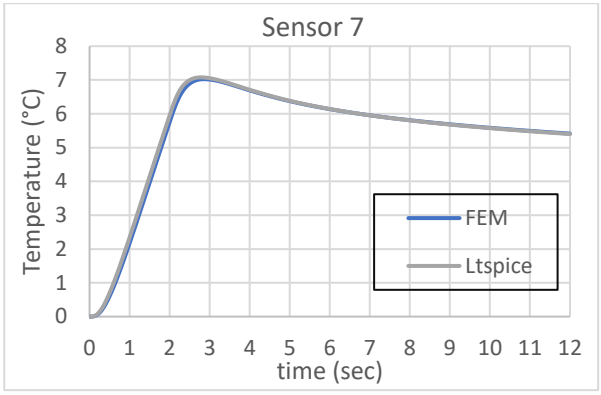

Figure 14: Thermal impedance comparison for sensor 7 for the same model without damage

The same process of validation is done for measurements of other sensors and comparison is made between the FEM simulation and Spice simulation so it's been confirmed that the LT Spice can deliver a consistent results as well as the validated FEM model.

Since the model in LT Spice cannot be used for the structure function analysis, another method should be used here for damage detection analyses. Here two methods of thermal equivalent circuit models will be introduced and developed in order to find the best method to detect the different failure mechanisms. The first method is the one-dimensional heat flow modelling. This method introduced by M. Rencz in [9] can generate a Cauer RC network based on the physical characteristics and a structure-function analysis can be built afterward to detect the variations depending on the material of each layer in the model. However in real semiconductor devices even with practically ideal heat sinks, the heat flow is never a one-dimensional path. Nevertheless modern power packages provide a main heat-flow path through chip, die-attach, and PCB to the outside environment but the heat will always spread in all lateral direction and that can affect the reliability of the RC model and deliver inaccurate result. This method has some limitation and should be compared and validated experimentally with the FEM Simulation before it can be used as detection method to investigate other failure mechanism. The second method to be used is the method introduced by Siegal [4]. This method is based on measuring the thermal impedance of the heating curve until it reaches the steady state as it is shown before in figure 10. Then, the separation point of the Z_{th}-curves where the curves deviate from each other is determined. In order to determine the point of separation, it is recommended to establish the derivatives da/dz of the Z_{th}-curves with z=ln(t). This method can deliver better visualization of the difference between the Z_{th}-curves.

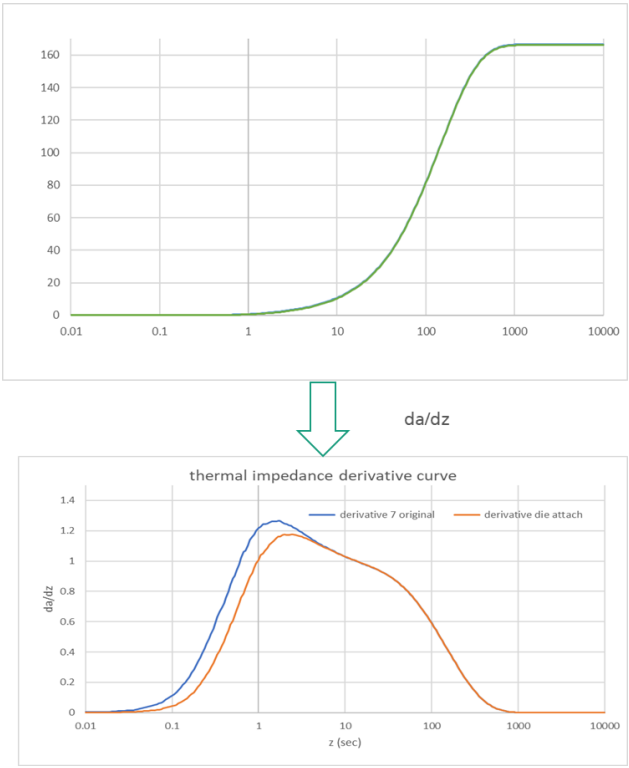

Figure 15: Zth curve derivative transformation

Figure 15 shows an example for the same sensor how the difference between the thermal impedance curve is clearer in the first derivative of the heating curve with respect to time. this method is well described by Schweitzer [5,8]. It can be implemented in our case of study for the given example as well as for further failure mechanism investigations.

3. Future research steps

In this paper we developed a simulation model, validated with experimental data and made it ready to provide results about the thermal impedance as a function of time corresponding to each failure mechanism in the packaging system. The simulations will be continued and expanded to detect all relevant failure mechanisms for this test board. In further work, another test board with different layout design and different electronic components will also be produced and investigated exactly the same way as the test board discussed here previously. The purpose of the second test board is to ensure reliable simulation results and data of the thermal behavior independently from the components tolerances and production inaccuracies and to ensure that the sensors can be applied on different electronic systems with varying design and still be able to detect the damage in the systems using the same method.

4. Conclusions

In this work a new approach to reliability monitoring has been presented. Herby the method of thermal spectroscopy is used and implemented as on-board and in-use monitoring. We have shown a correlation between the thermal impedance of the system and the size and location

of the damage in FEM simulations and validated these simulations experimental. It has been proven in this work that different purposefully added damages can be accurately reproduced in simulations and a thermal impedance curve be derived.

Moreover, a thermal RC compact model is built and validated with the FEM simulation. Once the thermal behavior of every relevant failure mechanism or damage is determined and collected in one database, an algorithm for damage and failure detection will be developed. With this algorithm it will be possible to detect and distinguish these different damages.

The last step is to implement this algorithm and damage detection method in electronic systems like a car's ECU. There a set of sensors will be placed on the PCB, capable of measuring the thermal impedance of the packaging system as a function of time and analyzing the data in order to notify the system if there is possible damage. The developed technology will act as a self-monitoring system for the electronic devices and ensure the reliability of the electronic system. In the future it might also be possible to develop the technology further for use in safety critical applications where functional safety is an essential requirement for the autonomous driving mode in the automotive industry.

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