Path-Based Statistical Gate-Level Analyses Considering Timing and Energy

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***Abstract*—Global and local fluctuations in leading-edge semiconductor manufacturing affect today's integrated circuits. While the former had been known and counteracted for years already, the latter arose when moving device dimensions into the deep submicron regime. In industrial digital circuit design, global and local variations are considered separately by process corners and on-chip variations. Both approaches have been criticized being inaccurate. As an alternative, for instance Statistical Static Timing Analysis applies analytical standard cell models to handle variability on gate level. We think, however, that multivariate statistical models may be an attractive solution as well since they may combine information on timing and power. In this paper, we propose a fully statistical approach for standard cell modeling and its application in statistical gate-level analyses combining propagation delay and energy consumption for timing paths. Using 45-nm predictive technology models, our gate-level results are close to SPICE reference simulations. Nevertheless, further research on statistical standard cell modeling is required on the way towards statistical analyses of complete digital blocks.**

I. Introduction

Random local variations, such as random dopant fluctuation and line edge roughness, have gained importance since device dimensions in leading-edge semiconductor technologies reached the deep submicron regime. In combination with global fluctuations due to reticle-, wafer-, and lot-based manufacturing, they lead to partially correlated device and interconnect variations.

Corner-based design and analysis methods, such as placement, routing, and Static Timing Analysis (STA) considering best-case and worst-case timing, have been state of the art in digital circuit development for years. Although some extensions, for instance on-chip variations (OCV) and advanced OCV (AOCV) were introduced to capture variability, these approaches have become unrealistic [1]. To increase accuracy, a lot of research has dealt with modeling standard cell variability and model application. As the most popular topic, Statistical Static Timing Analysis (SSTA) [2], many methods express standard cell performance characteristics as linear or higher-order polynomial functions of varying process parameters. While some approaches neglect global variability [3] or limit themselves to timing data [4], others use only linear approaches to combine timing and energy consumption [5]. Since analytical models may be too inaccurate or complex, a combined analytical and statistical timing model was developed [6].

We consider multivariate statistical standard cell modeling as a suitable alternative. Conventional gate-level analysis methods, such as STA or static power estimation, describe standard cell performance by a fixed set of characteristics, primarily delay times, dynamic energy consumption, and leakage power. Replacing numbers by statistical variables may dramatically increase accuracy. Propagating joint probability distributions of standard cell performance characteristics through digital designs, as illustrated in Fig. 1, may capture the statistics of timing and energy consumption at once and provide information for further abstraction of variability.

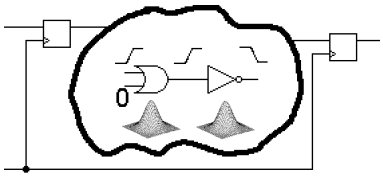

Fig. 1. Principle idea for statistical gate-level analyses

For this purpose, a multivariate model needs to be chosen to approximate

- marginal distributions of performance characteristics, such as delay, leakage power, and dynamic energy consumption;
- correlations of performance measures of a single cell;
- and correlations between different instances.

In general, standard cell performance characteristics follow non-normal distributions. Though, they can be approximated by Generalized Lambda Distributions (GLD) [7]. Intra-cell correlations can be considered using rank correlation coefficients, which has already been applied to multivariate statistical device compact models [8].

In this paper, based on Monte Carlo SPICE simulations, we statistically model timing- and energy-related characteristics of combinational standard cells as well as their correlations using the GLD and rank correlation coefficients. We extend the approach in [8] to preserve correlations between different instances, too. A path-based gate-level analysis considering timing and energy consumption is proposed to apply our multivariate statistical models.

The remainder of this article is organized as follows. Section II provides background information on statistical modeling and model application. A cell characterization method and the implementation of an adapted gate-level analysis are outlined in section III. Example circuitry is analyzed in section IV, before we draw conclusions and give an outlook

in section V.

II. Theory of Multivariate Statistical Modeling

In general, a multivariate random variable $\mathbf{X}$ is determined by marginal distributions of the single components X_i and interdependencies between the components X_i and X_j.

Describing probability distributions of various shapes with only 4 parameters, we use the GLD to approximate marginal distributions. After Freimer et al. [9] and with renamed parameters [10], it is defined by the quantile function

$$x_i = F_i^{-1}(u_i) = \lambda_{i,1} + \frac{\frac{u_i^{\lambda_{i,3}}-1}{\lambda_{i,3}} \frac{(1-u_i)^{\lambda_{i,4}}-1}{\lambda_{i,4}}}{\lambda_{i,2}}, \qquad (1)$$

with the uniformly distributed random variable $U_i \sim U(0,1)$ and the distribution parameters for location ($\lambda_{i,1}$), scale ($\lambda_{i,2}$), and shape ($\lambda_{i,3}, \lambda_{i,4}$). The parametrization in (1) differs from the definition in [7], [8] to better suit data approximation [10].

With the expectation $E[\cdot]$, the mean value $\mu_k = E[X_k]$, and the standard deviation $\sigma_k = E\left[(X_k - \mu_k)^2\right]^{1/2}$, product-moment correlation coefficients

$$c_{Xi,Xj} = \mathrm{corr}[X_i, X_j] = \frac{E\left[(X_i - \mu_i) \cdot (X_j - \mu_j)\right]}{\sigma_i \cdot \sigma_j}, \qquad (2)$$

express interdependencies between random variables X_i and X_j. Replacing raw values X_i and X_j by ranks $\mathrm{rk}(X_i)$ and $\mathrm{rk}(X_j)$, i.e. the positions in the ordered samples, results in rank correlation coefficients

$$r_{Xi,Xj} = \mathrm{corr}\left[\mathrm{rk}(X_i), \mathrm{rk}(X_j)\right], \qquad (3)$$

being invariant under monotone transforms and hence applicable in non-Gaussian multivariate distributions [11]. For simplicity, rank correlation coefficients are often summarized in the $(m \times m)$ correlation matrix $\mathbf{R_X}$ with $\mathbf{R_X}(i,j) = r_{Xi,Xj}$.

Multivariate modeling means that the parameters of marginal distributions and correlation coefficients need to be determined from training data. We generate samples from Monte Carlo SPICE simulations as input for GLD fitting and rank correlation coefficient calculations.

To use the obtained model in gate-level Monte Carlo analyses, a sampling method has to be available. A four-step approach solves this issue [11]:

1) Calculate a correlation matrix $\mathbf{C_Z}$ from the rank correlation matrix $\mathbf{R_X}$ using
$$\mathbf{C_Z}(i,j) = 2 \cdot \sin\left[\frac{\pi}{6} \cdot \mathbf{R_X}(i,j)\right]. \qquad (4)$$
2) Sample from an m-dimensional Gaussian variable $\mathbf{Z}$ with the correlation matrix $\mathbf{C_Z}$.
3) Convert the Gaussian components into uniform components applying the standard Gaussian cumulative distribution function (CDF) $U_i = \Phi(Z_i)$ such that $U_i \sim U(0,1)$.
4) Transform the uniform samples into performance characteristics X_i using marginal quantile functions (1).

In the subsequent section, we implement multivariate statistical standard cell modeling and statistical gate-level analyses.

III. Implementation Details

A. Origin

Our starting point is the Nangate Open Cell Library [12], which we use with 45-nm bulk CMOS Predictive Technology Models (PTM) [13]. In this paper, we focus on transistor variability as interconnect variability is beyond the scope of this paper. To capture device variability, we treat PTM corner models as $\pm 3\sigma$ values of all shifted BSIM4 parameters: lint, vth0, k1, u0, and xj. As in [14], instance parameter distributions are considered Gaussian. We assume a correlation of 0.5 between different devices and uncorrelated parameters of single instances to account for local and global device variability.

To keep the effort reasonable, we focus on combinational timing paths in this paper. For circuit simulations, we define an input signal waveform and the simulation end point t_e.

Extensive SPICE simulations, including the nominal case and Monte Carlo simulations, create a set of reference data. To implement a statistical characterization method and sampling-based gate-level analyses, we use statistics software R [15] because methods to handle the GLD are available [16]. With increasing circuit complexity, a recursive sampling approach as the one in [17] may have to be applied, but this is not necessary in our examples.

B. Logic Gate Characterization Methods

1) Direct Extraction from SPICE Simulation: First, we have to check whether the method of multivariate GLD modeling and sampling-based gate-level analyses is feasible at all. For this purpose, we directly extract cell delay and energy consumption from SPICE reference simulations. Statistical gate models including correlations are built for every instance. Since this approach does not improve efficiency, alternative modeling methods are required.

2) Piecewise Characterization: Piecewise characterization [18] may be an approach to reduce simulation effort. As it is illustrated for a 5-stage inverter chain in Fig. 2, the signal path is split into parts containing three instances each to reduce netlist complexity. While driver and receiver cells model the circuit environment, the cell in between is statistically characterized. The cell model has to contain gate delay, dynamic energy consumption, and state-dependent leakage power.

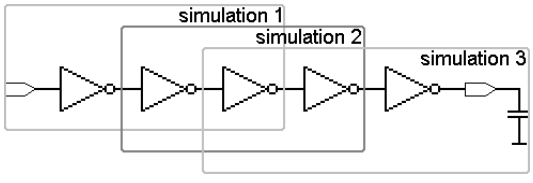

Fig. 2. Piecewise statistical cell characterization; adapted from [18]

Taking input signal transitions from the nominal simulation, SPICE simulations can be parallelized. Since this approach neglects signal transition variability, it may introduce a systematic error affecting especially long timing paths, however. An alternative, which increases accuracy at the cost of efficiency, is to apply output waveforms of previous parts.

C. Implementation of Statistical Gate-Level Analyses

In Fig. 3, terms for the path-based statistical gate-level analysis are defined on the example of an inverter.

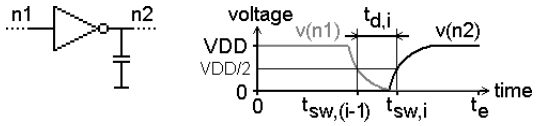

Fig. 3. Definition of terms and principle of statistical gate-level analyses

The first required information is stage delay time $t_{d,i}$, which is a figure of merit in both characterization approaches. Path propagation delay is the sum of stage delays,

$$t_{d,\text{path}} = \sum_{i=1}^{n} t_{d,i}. \tag{5}$$

It is straightforward to determine path energy consumption using the direct extraction method. For piecewise characterization, though, the computation is a bit more complex since state-dependent leakage power before and after switching, $P_{\text{l(bef)},i}$ and $P_{\text{l(aft)},i}$, as well as dynamic energy during switching, $W_{\text{dyn},i}$, need to be combined. Since the time points for signal switching, $t_{\text{sw},(i-1)}$ and $t_{\text{sw},i}$, are known from delay calculations, stage energy consumption can be calculated by

$$W_i = t_{\text{sw},(i-1)} \cdot P_{\text{l(bef)},i} + W_{\text{dyn},i} + (t_e - t_{\text{sw},i}) \cdot P_{\text{l(aft)},i}. \tag{6}$$

Finally, overall energy consumption is the sum of stage energy consumption,

$$W_{\text{path}} = \sum_{i=1}^{n} W_i. \tag{7}$$

The calculations in (5) – (7) have to be repeated for sample values of cell characteristics to provide statistical information on path propagation delay $t_{d,\text{path}}$ and energy consumption W_{path} including marginal distributions and correlation. This may be an input to a further abstraction of variability to be used in system-level examinations.

In the following section, modeling and gate-level analysis will be applied to inverter chains comparing accuracy and efficiency to SPICE reference simulations.

IV. Practical Application

As depicted in Fig. 4, our test vehicles are inverter chains of up to 9 stages. SPICE reference simulations, including a nominal run and a 1000-sample Monte Carlo simulation, are conducted with a fixed input waveform, output load, and end point $t_e = 1.2\ ns$. For piecewise cell characterization, further 1000-sample Monte Carlo SPICE simulations create the data sets for statistical modeling. Statistical gate-level analyses use the sample size $N = 10000$.

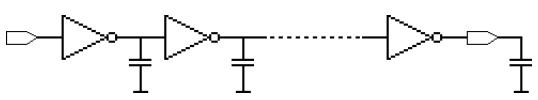

Fig. 4. Inverter chain gate-level schematic

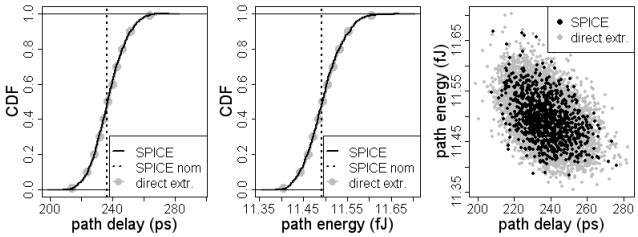

Fig. 5. SPICE results vs. direct extraction

The representative example of the 9-stage chain in Fig. 5 compares SPICE simulation results with the gate-level analysis based on direct extraction of cell characteristics. Marginal distributions of path propagation delay and energy consumption are approximated accurately, and the correlation between the figures of merit, which is moderate in this example, is preserved. As an intermediate result, multivariate statistical standard cell modeling using GLD and rank correlation coefficients as well as its application in gate-level analyses appears feasible, but the computational effort needs to be reduced.

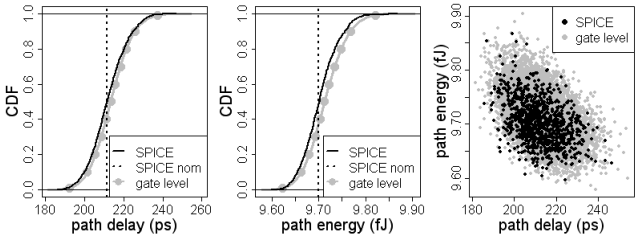

Fig. 6. SPICE results vs. piecewise extraction

Piecewise characterization of involved standard cells is one method to improve efficiency. The application of the resulting cell models to the 8-stage inverter chain is shown in Fig. 6. Both marginal distributions are slightly shifted towards higher values compared to SPICE simulations, overestimating path delay and energy consumption. Furthermore, this implementation of cell characterization and gate-level analysis tends to overestimate negative correlation between path performance measures to some extend.

Since these inaccuracies may be introduced by parallelizing SPICE simulations during characterization and neglecting signal transition variability, they may be systematic. To check this assumption, mean values μ, standard deviations σ, and coefficients of variation $CV = \sigma/\mu$ of the path characteristics are considered in Fig. 7. Mean values of delay and energy

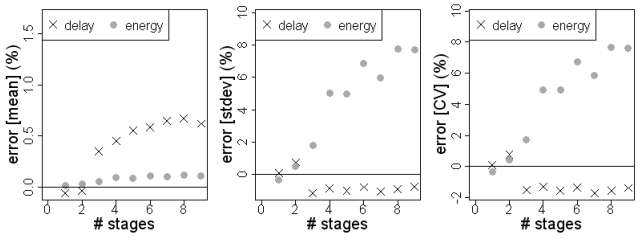

Fig. 7. Accuracy of statistical gate-level analysis

distributions are within 1% compared to SPICE. Nevertheless, a trend towards slightly overestimating both measures for long paths appears. Delay standard deviations are within 2%, while the spread in energy distributions is estimated too high with up to 8% deviations from SPICE. This effect also translates to coefficients of variation. Hence, delay distribution calculation can be considered accurate with only insignificant deviations. Further investigations on modeling and evaluating energy consumption are required to reduce the errors in energy standard deviations.

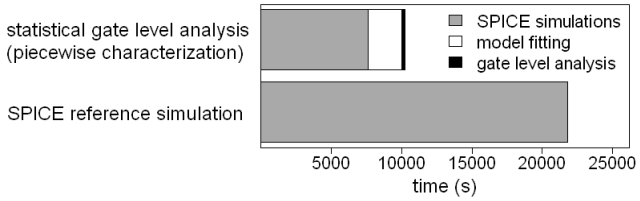

Fig. 8. Comparison of analysis runtimes

Although the 9-stage inverter chain as a single path is not convincing, it provides a rough estimate about analysis efforts. For this purpose, Fig. 8 contrasts analysis runtimes. For our example, the runtime of the gate-level analysis is 50 s and can be neglected while most effort has to be spent on SPICE simulation runs. Overall, analysis effort can be reduced by about 54% to approximately 2 h 45 min by the gate-level analysis applying piecewise characterization.

V. Summary, Conclusions, and Outlook

In this paper, we have presented an approach for multivariate statistical standard cell modeling. The distributions of delay and power characteristics are approximated by Generalized Lambda Distributions (GLD), and correlations are captured by rank correlation coefficients. A sampling-based gate-level examination evaluates these models and enables a path-based statistical analysis combining timing and power. Its results may be an input to statistical digital block modeling using the GLD and rank correlations.

Statistical cell characterization is a major task in this context. We apply piecewise characterization to efficiently generate path-specific standard cell models. However, neglecting signal transition variations introduces inaccuracies that especially affect energy distributions of long paths. To provide more general cell models, introducing statistics into industry-standard non-linear delay and power models or current source models [19] may be subject to future research.

The proposed statistical gate-level analysis is demonstrated using inverter chains of up to 9 stages. Reducing the effort by 54% compared to SPICE Monte Carlo simulations, the distributions of propagation delay and energy consumption as well as their correlation are close to the reference data so that the methodology of statistical modeling and multivariate gate-level analysis is applicable. Mean values of delay and energy distributions are nearly identical to SPICE results. The errors in energy standard deviation of up to 8% depending on cell count shows a trend towards larger deviations for longer paths. Further research is required to identify and counteract the root causes of this effect. Delay standard deviations and coefficients of variation are within 2% to SPICE which offers a near-term industrial application: the more efficient generation of AOCV tables for sign-off STA.

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