Analysis and Design of a 1MHz LLC Resonant Converter with Coreless Transformer Driver

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Abstract

In this paper, the analysis and design of a 1MHz LLC resonant converter is presented. Zero-voltage switching (ZVS) of the primary MOSFETs (Infineon) and zero-current switching (ZCS) of the rectifier diodes are guaranteed over the entire operation range, which dramatically reduce the switching loss and improve EMI performance. In addition, the low voltage stresses of MOSFETs and the rectifier diodes allow the designer to use the devices with better conduction performance. The detailed design method for the LLC resonant tank parameters is presented in this paper, which fully guarantees the ZVS conditions. An integrated driver solution is implemented by a novel half bridge driver IC 2ED020I12-F (Infineon) employing coreless transformer (CLT) technology. Finally, a 1MHz 250W LLC resonant converter prototype is implemented to verify the operational principles and design method of the proposed converter. The developed prototype can operate with a wide input voltage range of 250-400V with maximum 92.7% efficiency at 24V and 250W output. Therefore, the proposed converter is suitable for high efficiency and high power density application such as LCD and PDP TV power module.

Keywords: LLC resonant converter, ZVS, quality factor

1 Introduction

DC/DC converter with high power density and high efficiency is increasingly required, e.g., in LCD and PDP application.

Compared to conventional PWM converters, which suffers from decreased efficiency and deteriorated EMI problem at high switching frequency, resonant converter is a good alternative due to its well known advantages of high efficiency, high switching frequency and high power density [1][2].

In this paper, a 1MHz LLC resonant converter suitable for high efficiency and high power density applications is analysed and implemented. Firstly, in the overall designed operation ranges, the primary MOSFETs are turned-on under ZVS condition, and the secondary rectifier diodes are turned-on and turned-off under ZCS condition. Hence high switching frequency and high power density are reasonable. Secondly, the primary MOSFETs and the secondary rectifier diodes have low voltage stresses clamped by the input and output voltages, respectively. And so the designer can use the devices with better conduction performance, and consequently smaller conduction loss can be achieved. Thirdly, optimal design can be realised at the normal operation point, moreover, operation with a wide input voltage range is achieved. Fourthly, the two resonant inductors of the LLC resonant tank can be easily integrated in one magnetic core without additional inductor, hence the power density can be further increased.

In this paper, a detailed quantitative analysis of the LLC topology is provided, as well as the design method for the LLC resonant tank parameters, which guarantee the ZVS condition and optimised operational efficiency.

To realize an integrated solution, a novel IC 2ED020I12-F employing coreless transformer (CLT) technology is used to drive the half bridge. The basic principle of CLT is the implementation of a microplanar transformer embedded within the semiconductor process. High insulation capability, no ageing, small package size, easy integration of additional logic functions, and cost effectiveness are provided by 2ED020I12-F[6]. Also, The transformer core selection and the controller implementation are briefly presented in this paper.

2 Operation Principle

The schematic of a half-bridge LLC resonant converter is shown in Fig.1. The elements that make the resonant tank are the leakage inductance L_r, the magnetizing inductance L_m of the transformer and the resonant capacitor C_r.

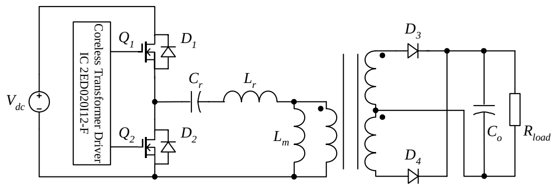

Fig.1 LLC resonant converter

The DC characteristic of LLC resonant inverter is shown in Fig.2. There are two critical resonant frequencies f_0 and f_1 ($f_0 < f_1$). The bigger one f_1 is determined by the resonant capacitor C_r and leakage inductance L_r. The other smaller one f_0 is determined by C_r, L_r and L_m.

At normal operation condition, i.e. 400V dc input, the operation point should be placed near the resonant frequency f_1 as shown in Fig.2, where the voltage gain is unity and its load independent characteristic is obtained.

During hold up time, input voltage drops, switching frequency is reduced to regulate the output voltage [2][3].

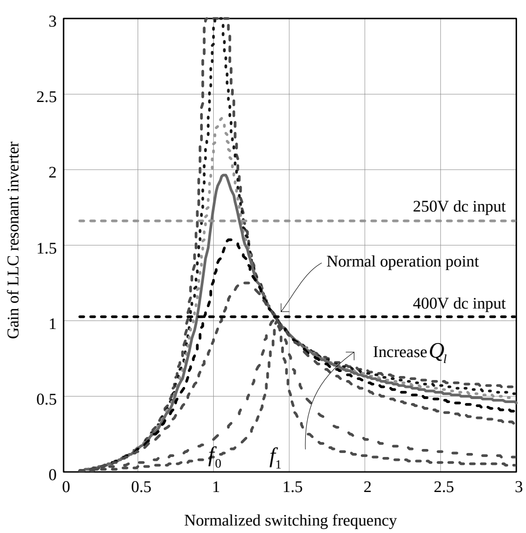

Fig.2 DC gain of LLC resonant inverter

From Fig.2, in order to guarantee the output voltage regulation over the entire range of input dc voltage, the loaded quality factor Q_l at full load is required to be bigger than a critical value $Q_{l\_\min}$, which guarantee the required voltage gain and ZVS condition within the variation range of load and input voltage.

3 Design Consideration and Practical Implementation

LLC resonant converter is to be used as one stage of front end AC/DC converter. In order to provide the hold up time capability and decrease the input capacitor volume, the input voltage range of the converter is to be designed widely from 250V to 400V.

3.1 Resonant Parameters Design

The voltage gain of the resonant tank can be described as equation (1) using the first harmonic approximation approach.

$$M = \frac{1}{\sqrt{(1+A)^2 \cdot (1-(\frac{f_0}{f_{switch}})^2)^2 + \frac{1}{Q_L{}^2}(\frac{f_{switch}}{f_0} \cdot \frac{A}{A+1} - \frac{f_0}{f_{switch}})^2}} \quad (1)$$

With the following parameters definition:

The ratio of the inductance:

$$A = L_r / L_m \quad (2)$$

The corner frequency:

$$\omega_0 = \frac{1}{\sqrt{(L_r + L_m)C_r}} = 2\pi f_0 \quad (3)$$

The characteristic impedance:

$$Z_0 = \omega_0 (L_r + L_m) = \frac{1}{\omega_0 C_r} = \sqrt{\frac{L_r + L_m}{C_r}} \quad (4)$$

The equivalent input resistance of the transformer center-tapped rectifier:

$$R_i = \frac{8N^2}{\pi^2} R_{load} \quad (5)$$

The loaded quality factor at the corner frequency f_0:

$$Q_L = \frac{R_i}{Z_0} = R_i \Big/ \sqrt{\frac{L_r + L_m}{C_r}} \quad (6)$$

Due to the load independent characteristic at the maximum resonant frequency f_1, the switching frequency at normal operation point is specified as f_1:

$$f_{normal\_switch} = f_1 = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (7)$$

Using (1), the maximum switching frequency f_2 can be calculated as (8), which occurs at maximum input voltage and zero load:

$$M_{zeroload} = \frac{1}{\sqrt{(1+A)^2 \cdot (1 - \frac{\frac{f_{normal\_switch}^2}{1+1/A}}{f_2^2})^2}} \qquad (8)$$

The minimal voltage gain is required at maximum input DC link voltage:

$$M_{\min} = 2N \frac{V_{out}}{V_{dclink\_\max}} \qquad (9)$$

Let $M_{zeroload} = M_{\min}$, and assume the maximum switching frequency f_2 is specified as a certain value bigger than f_{normal_switch}, for example 1.4MHz, and the maximum possible input voltage as 415V, and then the inductance ratio A can be calculated from equation (8)(9):

$$A = \left(\frac{1}{M_{\min}} - 1\right) \Bigg/ \left(1 - \frac{f_{normal\_switch}^2}{f_2^2}\right) \qquad (10)$$

The next important step is to check what is the minimal required quality factor, which guarantee the ZVS condition is still available at all the allowed operational conditions.

The input impedance of the resonant circuit is given by:

$$Z = \frac{1}{j\omega c} + j\omega L_r + \frac{j\omega L_m R_i}{j\omega L_m + R_i} \qquad (11)$$

The resonant frequency $f_{resonant}$ is defined as the frequency at which the phase shift angle ψ of Z is zero, which constitutes the boundary conditions between capacitive and inductive load. For $f_{switch} > f_{resonant}$, $\psi > 0$ and the resonant circuit represents an inductive load, which is recommended for the ZVS conditions for MOSFETs [1-3].

From equation (11), assuming the imaginary part of Z is zero, the normalized resonant frequency is found to be:

$$\frac{f_{resonant}}{f_0} = \sqrt{\frac{(1+A)\cdot\left\{1 - Q_l^2(1+A)^2 + \sqrt{\left[1 - Q_l^2(1+A)^2\right]^2 + 4Q_l^2(1+A)A}\right\}}{2A}} \qquad (12)$$

As $Q_l \to 0$, $f_{resonant} / f_0 \to \sqrt{(1+A)\cdot A}$. For a fixed value of A given by (10) and loaded quality factor Q_l, the actual normalized switching frequency f_{switch} / f_0 should be higher than $f_{resonant} / f_0$, which guarantee the inductive load and consequently the ZVS condition.

From equation (1), the plots of f_{switch} / f_0 against Q_l at specified values of $M_{resonant\_\tan k}$ are obtained as shown in Fig.3.

The boundary condition given by (12) is also plotted in Fig.3, and the area beyond the boundary condition is desired for ZVS condition.

The maximum required voltage gain, assuming minimal input dc link voltage 250V during the holdup time, is obtained referring to (9):

$$M = 1.55 \qquad (13)$$

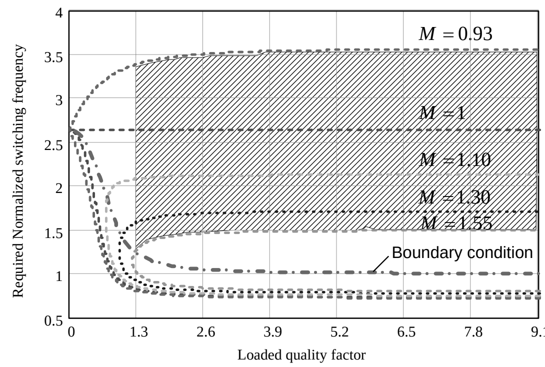

Fig.3 Selection of loaded quality factor

From Fig.3, the minimal required loaded quality factor can be directly and approximately obtained:

$$Q_{l\_\min\_required1} = 1.3 \qquad (14)$$

The shadow area shown by Fig.3 is the designed operation range, which guarantee both the ZVS condition and the required voltage gain within the variation range of load and input dc link voltage.

Another important conditions for ZVS is that the turn off current should be big enough to discharge junction capacitors within the dead time.

$$\sqrt{2} \cdot I_{resonant} \cdot \sin\psi \geq \frac{2 \cdot C_{oss\_effective} \cdot V_{dc\_link}}{t_{dead}} \qquad (15)$$

Consider the rms resonant tank current equals to:

$$I_{resonant} = \frac{P_{in}}{\cos\psi \cdot \frac{\sqrt{2} V_{dc\_link}}{\pi}} \qquad (16)$$

Thus the following expression can be derived by (15) and (16):

$$tg\psi \geq \frac{2 \cdot C_{oss\_effective} \cdot V_{dc\_link}^2}{\pi \cdot t_{dead} \cdot P_{in}} \qquad (17)$$

Where $C_{oss\_effective}$ is a fixed effective output capacitance that gives the same charging time as the output capacitance of a MOSFET while V_{DS} is rising from 0 to 400V.

From the input impedance equation (11), $tg\psi$ can be given as functions of f_{switch} / f_0 at fixed values of Q_l:

$$tg\psi = \frac{1}{Q_l}\left(\frac{f_{switch}}{f_0}\cdot\frac{A}{A+1}-\frac{f_0}{f_{switch}}\right) + Q_l\cdot\frac{f_0}{f_{switch}}\cdot(1+A)^2\cdot\left[1-(\frac{f_0}{f_{switch}})^2\right] \quad (18)$$

At normal operation condition, the relationship between actual $tg\psi$ and Q_l is

$$tg\psi = \sqrt{A\cdot(1+A)}\cdot Q_l \quad (19)$$

Using (18) and (19), and assuming $C_{oss\_effective} = 124\text{pF}$ (CoolMos_SPP16N50C3), $t_{dead} = 100\text{ns}$, $P_{in} = 270\text{W}$ and $V_{dc\_link} = V_{dc\_link\_normal} = 400\text{V}$, then, leaving some margin, the minimal required loaded quality factor is obtained as $Q_{l\_\min\_required2} = 2.0$, which insures $tg\psi$ fully meets the requirement given by (17).

In the actual experiment, the requirement given by (17) can also be met by adjusting the dead time t_{dead}.

The efficiency of the LLC inverter can be approximately obtained as:

$$\eta = \frac{1}{1+\frac{r}{R_i}\cdot\left\{1+\left[Q_l\cdot\frac{f_0}{f_{switch}}\cdot(1+A)\right]^2\right\}} \quad (20)$$

Assuming the equivalent conduction loss resistance r is constant, the maximum efficiency occurs at

$$Q_l = \frac{\frac{f_{switch}}{f_0}}{1+A} \quad (21)$$

The efficiency optimisation is focused on normal operation point, 400V DC link input, where the switching frequency is load independent and equals to $f_{resonant}$.

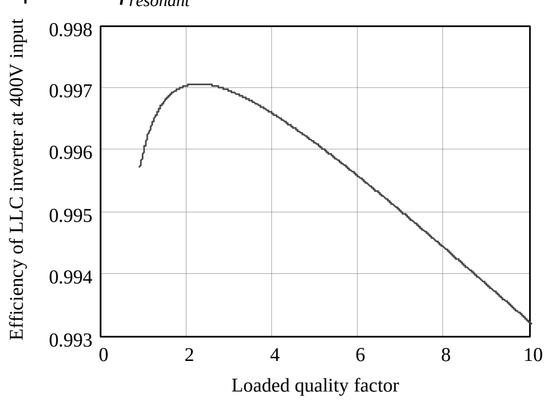

Fig.4 LLC inverter efficiency

From Fig.4, if the loaded quality factor from 2 to 3 for full load condition is realized, then the maximum efficiency for LLC inverter at full load and 400V input conditions can be obtained.

The final conclusion can be given, taking some margin, $Q_{l\_\min\_required} = 2$ is selected.

The component values of the resonant circuit can be given as:

$$C_r = \frac{Q_l}{2\pi f_0\cdot R_{i\_\min}}$$

$$L = \frac{R_{i\_\min}}{2\pi f_0 Q_l} \quad L_r = \frac{L}{1+\frac{1}{A}} \quad L_m = \frac{L}{1+A} \quad (22)$$

3.2 Transformer Core Selection

The resonant converter can significantly reduce the switching losses, thus improve the power conversion efficiency. However, at higher switching frequency, the transformer core exhibits increased magnetic loss, which could offset the reduced switching losses. Accordingly, many attempts have been made by core manufacturers to advance the state-of-the-art in the power ferrite technology.

The type of ferrite material chosen will influence the core losses at given operating conditions. N49 ferrite core produced by EPCOS has been selected for its low magnetic power losses, and its high frequency range varies from 300kHz to 1MHz, and core temperature up to 100°C.

Finite element analysis (FEA) is used to define the transformer winding strategy, and consequently the expected leakage inductance and magnetizing inductance can be realised. At the same time, the ac resistance also can be optimised.

3.3 Half Bridge Driver

To reduce the volume of the converter, integrated driver solution is implemented, IC 2ED020I12-F (Infineon) employing coreless transformer (CLT) technology is used to drive the half bridge. The basic principle of CLT is the implementation of a microplanar transformer embedded within the semiconductor process. Compared to other conventional level shifting technologies based on optocouplers, discrete transformers or level shifters, 2ED020I12-F with CLT technology simultaneously features high and safe isolation, low cost and no degradation over time [6].

The 2ED020I12-F contains two drivers for an IGBT or MOSFET half-bridge, and the high side is galvanicly isolated from the low side part through a coreless transformer system.

The integrated operational amplifier and comparator are suitable to detect over current and/or short circuit current.
External push-pull circuit is used to enhance its drive capability at 1MHz switching frequency.

3.4 Controller IC

Controller IC-MC34067 is used to implement the output voltage regulation against variations of the load and input voltage. MC34067 is a high performance resonant mode controller designed for zero voltage switching DC/DC converter applications that utilize frequency modulated constant deadtime control.

4 Experiment Results

To verify the operational principles of the proposed converter, a 250W prototype is implemented as shown in Fig.5.

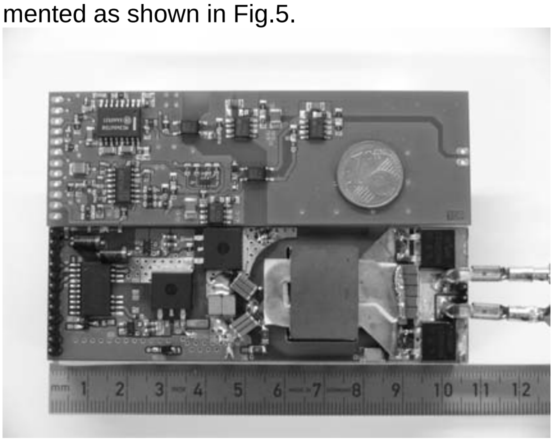

Fig.5 LLC resonant converter prototype

Fig.6 and Fig.7 show the key waveforms at full-load and 5%full load with an input voltage of 400V. Ch3 waveform is the drive signal for MOSFET (CoolMos), Ch2 waveform is the voltage across MOSFET. It's clear that MOSFET is turned-on under ZVS condition over the entire range of load.

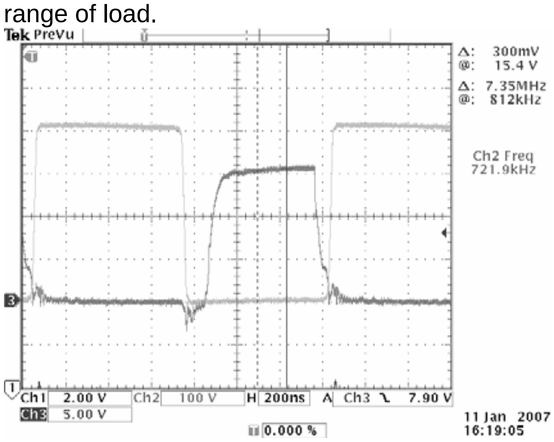

Fig.6 MOSFET ZVS conditions @400V Full load

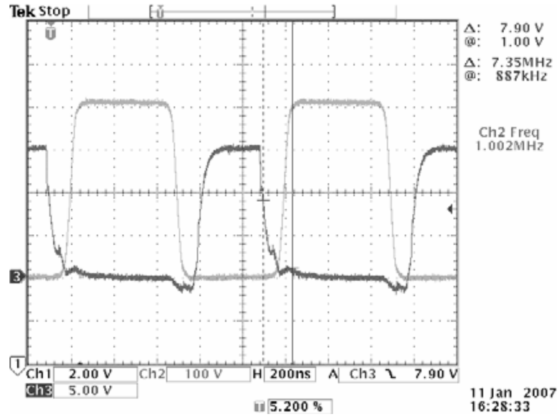

Fig.7 MOSFET ZVS conditions @400V 5% Full load

To evaluate the performance of the feedback control, the load step response of the LLC resonant converter has been analysed. Fig.8 shows the response of the converter to a positive step of the load current. And current step slew rate = 0.4A/us.Fig.9 shows the response of the converter to a negative step of the load current.

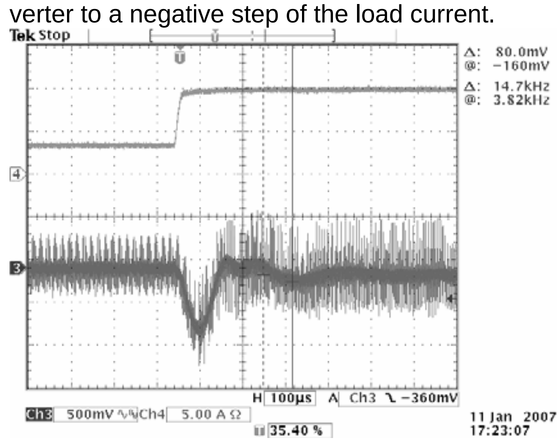

Fig.8 Load jump @ Vin=400V from 30%full load to full load

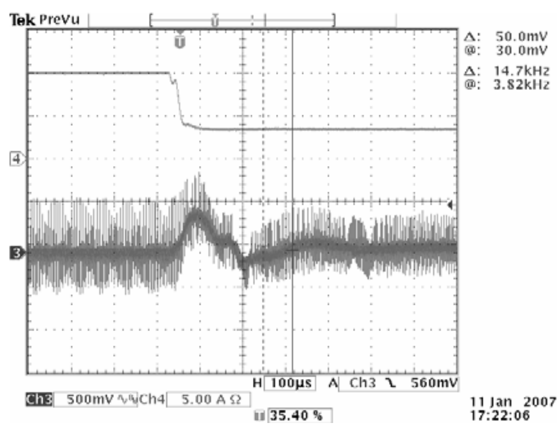

Fig.9 Load jump @ Vin=400V from full load to 30%full load

Normally, LLC converter operates between 350V to 400V input voltage. In Fig.10, efficiency measurements have been performed at these different operation points; the developed LLC resonant converter prototype exhibits high-efficiency in the normal 400V operation point.

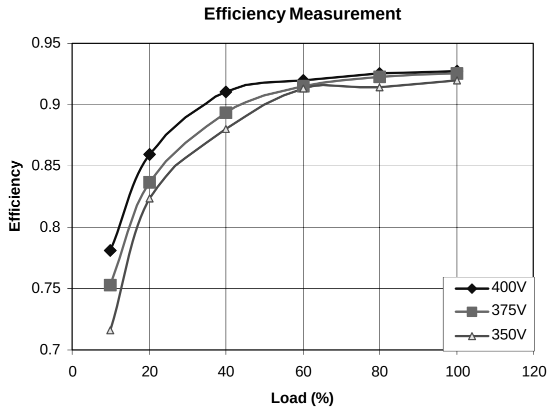

Fig.10 Efficiency measurement results

During the hold up time, the input dc voltage is allowed to drop to 250V, output voltage of LLC resonant converter can still be regulated, however, it operates far away from the resonant point, which means the converter is less efficient, nevertheless it only lasts for about 20ms and will not cause extra thermal problem.

5 Conclusion

In this paper, a 1MHz LLC resonant converter is proposed for high efficiency and high power density application. The operational principle of the proposed converter is analysed, and corresponding calculation result is given. The design method for the resonant tank parameters is also detailed. The half bridge drive IC and the transformer core selection for 1MHz switching frequency have also been discussed, too. The ZVS of MOSFETs is guaranteed over the entire operation range. To further confirm its operation and developed design method, a 24V/250W prototype is implemented, ZVS is realised and high efficiency up to 92.7% is also achieved. The LLC resonant converter is an excellent alternative in high efficiency and high power density application.

6 Acknowledgment

The authors wish to acknowledge the funding of the German Ministry of Education and Research (BMBF) and all partners from Infineon Technologies Company and Fraunhofer Institute of Integrated Systems and Device Technology.

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