

PLASMA ETCHING FOR INDUSTRIAL IN-LINE PROCESSING OF c-Si SOLAR CELLS

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ABSTRACT

Thinner wafers and the reduction of breakage losses make it attractive for solar cell manufacturers to use in-line production systems. Closing the gap between diffusion and in-line silicon nitride deposition systems a plasma etching system has been designed suitable for a throughput of 1000 wafer/h with an automated transport system. Different plasma sources appropriate for etching large areas were tested and etch rates of around 13 $\mu\text{m}/\text{min}$ for saw damage removal could be reached with sufficient homogeneity. For phosphorous glass (PSG) removal selectivities between PSG and silicon above 10 could be achieved with a $\text{CF}_4/\text{C}_2\text{H}_4$ etch gas mixture with sufficient PSG etch rates of around 80 nm/min. Solar cells processed with the plasma PSG removal step show slightly decreased efficiencies attributed to the plasma induced damage to the emitter layer and the silicon bulk. Further process optimization is needed to reduce this damage.

1. INTRODUCTION

Although in semiconductor industry plasma etching has been a well established technology for more than 15 years it is not widely used in solar cell production. Only edge isolation is performed by plasma etching using barrel type reactors in some fabrication lines. Recently though, because of increasing water and chemical waste disposal costs as well as the demand for integrated solutions for process equipment, the PV industry has been showing an increasing interest in other dry etching processes as well, like saw damage removal, surface texturing and cleaning, or phosphorous silicate glass (PSG) removal [1] [2]. One advantage of dry processing is the full control of all process parameters allowing good reliability and reproducibility, that is necessary for industrial production. An in-line capable plasma etching system is feasible to close the gap especially between diffusion and deposition furnaces to enable a totally in-line solar cell fabrication process.

The aim of this work is the development and implementation of plasma etching processes for in-line production in solar cell fabrication. To achieve the goal of high throughput different types of plasma sources, excitations and etch gases (SF_6 , $\text{CF}_4/\text{C}_2\text{H}_4$) are used suitable for scalability to larger areas. Other boundary conditions in designing a large plasma etching system like temperature and bias control were considered in terms of etch rates and plasma-induced damage.

2. PLASMA SOURCE TYPES

Two different commercially available plasma source types have been investigated concerning high silicon etch rates and scalability towards larger areas. The working principle of the HCD plasma source (Fig. 1, left) is the hollow cathode effect. Cylindrical hollow cathodes are arranged in a hexagonal matrix building the basic plasma. The cathodes are coupled with a high frequency (HF) generator. At the bottom side (anode) openings in the same hexagonal matrix order provide the extraction of intensive plasma jets out of the cathode cylinders. In between, additional openings provide the supply of monomer gases.

A microwave linear antenna (Fig. 1, right) consists of conducting rods into which (either from one end or) from both ends the MW power is coupled. The plasma builds up around the rod and along its entire length. Several of these antennas can be used simultaneously in order to obtain etch homogeneity over large areas as well as to increase the wafer throughput.

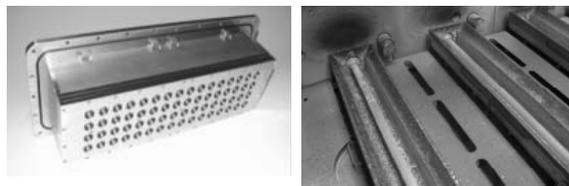


Fig. 1 Plasma sources suitable for large area plasma etching: HCD hollow cathode (left) and two microwave linear antennas (right).

Experiments concerning temperature variations as well as PSG removal were carried out on a so called ECR-RIE system (see Fig. 2). A microwave powered electron cyclotron resonance (ECR) plasma source on top of the reaction chamber provides a high density plasma.

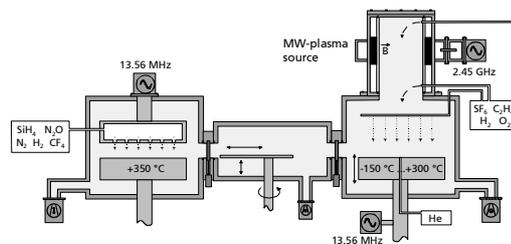


Fig. 2 Plasma cluster consisting of a PECVD and an ECR-RIE module, linked by a transfer system with load lock.

Additionally or alternatively, the sample electrode can be powered by radio frequency to accelerate (reactive) ions onto the sample (RIE / MWRIE mode).

3. EXPERIMENTAL

3.1 High rate silicon etching

In order to reach a wafer throughput of more than 1000 Wafer/h in a large area etching system (at least 25 10x10cm² wafer per run) high silicon etch rates (above 10 μm/min) are needed for saw damage removal. Overall etch rates for saw damage removal were tested on standard boron-doped Cz-silicon material. Wafers were weighted before and after the plasma etch cycle. In addition polished float zone silicon samples were added inside the reaction chamber determining the etch rate. Combined with a small amount of oxygen (10 %) etch rates above 10 μm/min could be reached, using sulphurhexafluoride (SF₆) as etching gas.

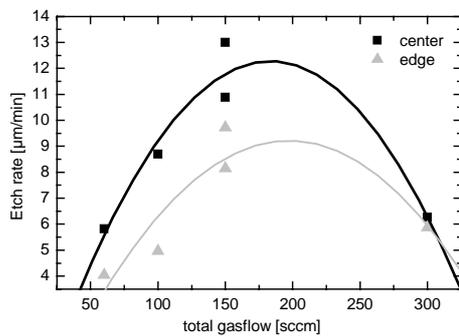


Fig. 3 Total etch rates of the HCD source against the gasflow. Other plasma parameters are: HF-power 700 W, pressure 50 Pa, O₂ and Ar 10% (fitted lines are guides to the eye).

Both plasma source types, the microwave linear antenna and the hollow cathode could reach such high etch rates. In case of the HCD source, a RIE based process with a pressure of 50 Pa in the reaction chamber and a bias voltage of approximately 300 V reached a silicon etch rate of 13 μm/min in the center of the reaction chamber. Near the edges etch rates still remain high with nearly 10 μm/min (Fig. 3). Homogeneity over the full length of the carrier is assured in case of the microwave linear antenna plasma source (Fig. 4). It can be observed, that the etch

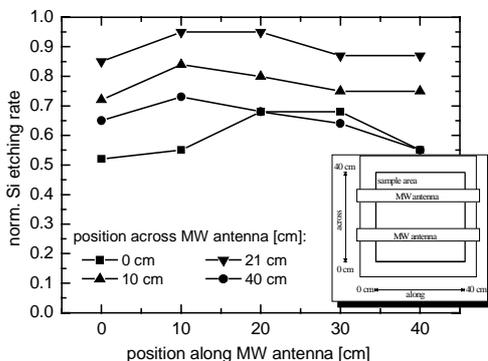


Fig. 4 Etch homogeneity along and across the length of a microwave linear antenna.

rate is varying just slightly along the length of a linear antenna. Across the antennas the etch rate reaches a maximum directly underneath the rods and decreases

slightly moving aside at each side, which becomes unimportant in case of an in-line etching system. Increasing temperature, a further increase in etch rate is observed. This can be explained by a higher ion mobility and therefore a higher degree of ionization in the plasma. To analyze the plasma-induced damage provoked by the higher temperature, small FZ Si wafers were etched in the ECR-RIE system (SF₆ RIE) and covered by a protecting SiN_x layer. Lifetime measurements were carried out using the microwave photoconductance decay (MWPCD) method. Results are shown in Fig. 5.

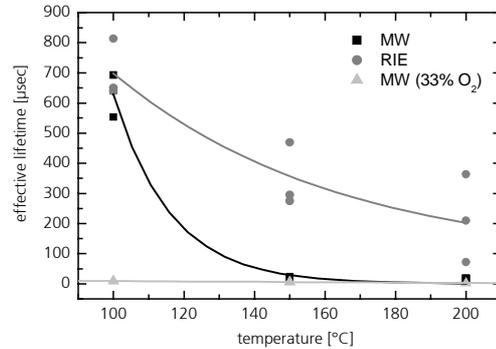


Fig. 5 Fitted lifetime of charge carriers for different plasma treatments against the process temperature.

At 100°C carrier lifetimes comparable to standard process conditions (20°C) are reached with pure microwave as well as RIE processes. Adding oxygen increases dramatically the plasma-induced damage, i.e. decreases the carrier lifetime.

3.2 Phosphor silicate glass removal

Phosphor silicate glass (PSG) is formed during emitter diffusion and has to be removed for further solar cell processing. The etching process has to meet three critical requirements: first it has to be highly damage-free, since no further high temperature step is following, second an etch stop at the underlying silicon is needed (to avoid etching of the emitter), and finally it has to be residue-free (for good adhesion of metallisation and ARC).

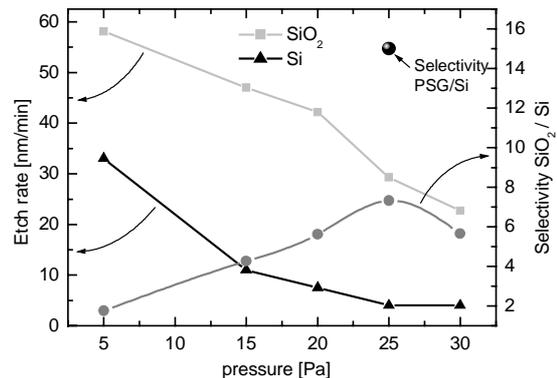


Fig. 6 Etch rates of SiO₂ and Si and the corresponding selectivity against pressure for a MWRIE PSG etch process.

As etch gas a mixture of CF₄ with small amounts of ethylene (C₂H₄) is used [3]. SiO₂ served as substitute for PSG during process development since it has very similar properties (unless the etch rate which is about a factor of 2

smaller). Process optimization has been carried out in the ECR-RIE plasma reactor at Fraunhofer ISE leading to maximum selectivities between SiO_2 and Si of 7.5 (Fig. 6) with etch rates sufficient for short process times (< 1 min). Due to the carbon and fluorine containing chemistry a polymer-like surface layer of several nanometers is formed during etching. Selectivity between SiO_2 or PSG and Si can be mainly attributed to this thin polymer layer, because its growth on silicon surfaces is much faster preventing further etching [4][5][6]. Such layers mainly consist of $\text{C}_x\text{H}_y\text{F}_z$ polymers, their constitution can be suppressed by a certain degree of physical etching, controlled by the DC-bias [7].

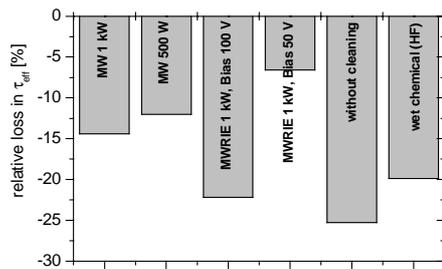


Fig. 7 Percentage loss in lifetime compared to wet chemical PSG etching for different dry etching post-treatments.

Below a bias voltage of 100 V etch rates drop to negligible values and the forming of polymers accelerates again. For the process with the highest selectivity a bias voltage of nearly 300 V is needed resulting also in a certain degree of damage to the underlying emitter layer [1][8]. Nevertheless remaining polymer layers of a few nanometers could not be prevented after the etching process. Avoiding significant modifications to the SiN_x antireflection coating, a further cleaning step before SiN_x deposition had to be applied. Favourable is a short post-treatment of the wafers in an oxygen plasma (ashing) in the same plasma reactor. Different plasma processes (MWRIE, MW) with large amounts of oxygen and varying microwave power as well as wet chemical cleaning steps have been applied. Relative losses in effective lifetime for different polymer ashing procedures compared to wet chemical PSG removal are shown in Fig. 7. The presence of a harmful polymer layer can be seen on the right, without cleaning step or with wet chemical HF etching (should not remove polymers), the losses in lifetime are significantly higher.

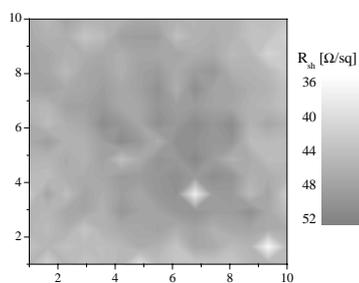


Fig. 8 Lateral sheet resistance distribution proving the etch homogeneity on a $10 \times 10 \text{ cm}^2$ wafer (measured at the Fraunhofer ISE Laboratory & Servicecenter Gelsenkirchen).

For the pure plasma processes, the most favourable post-treatment turned out to be a MWRIE process with moderate bias voltage and gas pressure with a minimum loss of around 7 %. The etch homogeneity on a $10 \times 10 \text{ cm}^2$ silicon wafer was investigated after PSG removal with an emitter sheet resistance of $46.3 \text{ } \Omega/\text{sq}$. and a standard deviation of just $2.1 \text{ } \Omega/\text{sq}$. throughout the whole wafer (Fig. 8).

3.3 Solar cell results

Multicrystalline (mc) silicon wafers have been used for solar cell manufacturing. The process sequence is shown in Fig. 9, conventional wet chemical removal of PSG has been replaced by a plasma process using $\text{CF}_4/\text{C}_2\text{H}_4$ described above. Emitter formation was carried out in a tube furnace using POCl_3 as phosphorous source. After complete PSG removal a PECVD SiN_x antireflection coating has been deposited in a conventional parallel plate direct plasma reactor [9]. For solar cell metallisation commercially available silver and aluminium pastes have been screen printed onto the front and back, respectively. The solar cells contacts have been fired using Rapid Thermal Firing technique in a single-wafer RTP furnace [10]. In the end edge isolation has been carried out using a Nd:YAG laser system.

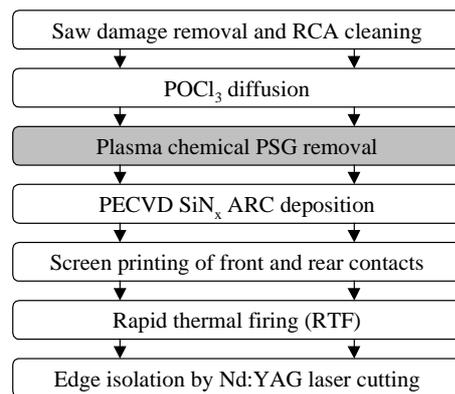


Fig. 9 Process sequence for plasma PSG etched solar cells.

The results of the processed solar cells are displayed in Table 1.

Table 1. Results of untextured solar cells on Cz- and mc-Si material. (total cell area 96.8 cm^2).

Material	V_{oc} [mV]	j_{sc} [mA/cm^2]	FF [%]	η [%]
Cz (Ref.)	612	31.9	78.7	15.4
Cz (PE)	613	31.2	78.5	15.0
mc (Ref.)	606	30.9	77.8	14.6
mc (PE)	601	30.0	78.4	14.1

PE: PSG removal with plasma etching

Plasma PSG etched solar cells reach efficiencies of 15 % on Cz-Si and 14.1 % on mc-Si material with excellent fill factors. The difference of 0.4 % in efficiency to wet chemical PSG etched solar cells can be mainly explained by the reduced short circuit current on Cz-Si material. Still existing polymer residues on the surface may be a possible source for the discrepancy. On mc-Si material, a reduced short circuit current as well as a reduction of the open

circuit voltage is observed. The polymer ashing process after PSG etching, a short microwave based oxygen-rich post-treatment, might be an explanation for this reduced V_{oc} value on mc-Si. Analysis of the dark characteristics show similar values of the saturation current of the second diode j_{02} indicating no significant damage induced by the PSG plasma etching step. Further prove of the nearly damage free etching gives the internal quantum efficiency of the plasma processed solar cells (Fig. 10).

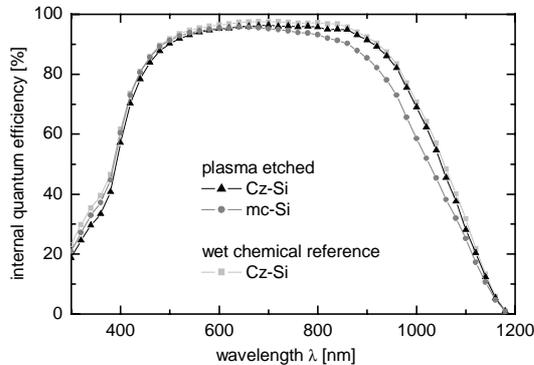


Fig. 10 Internal quantum efficiency of PSG plasma etched solar cells (reference: wet chemical PSG removal).

Although not noticeable in open circuit voltage, lower IQE values of the plasma etched cells for small wavelength compared to the wet chemical reference can be attributed either to still existing polymer residues influencing the antireflection properties of the applied Si_x ARC layer as well as a certain degree of plasma induced damage to a thin surface layer.

4. IN-LINE PLASMA ETCHING SYSTEM

A completely in-line capable plasma etching system is designed (see Fig. 11). The demonstrator will be equipped with a microwave linear antenna as well as a HCD plasma source. All processes developed on the smaller test systems will be transferred to this new system.

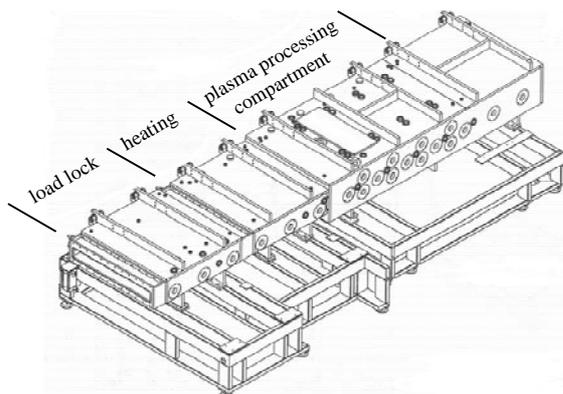


Fig. 11 Lay-out of a Roth&Rau plasma etching reactor equipped with two different plasma sources.

5. CONCLUSION

Plasma etching processes for saw damage and phosphorous glass removal are developed reaching high

etch rates and high selectivities fulfilling the requirements for high throughput fabrication in solar cell production lines. Processed solar cells on multicrystalline Si material achieve efficiencies nearly comparable to wet chemical etched references. Slightly reduced open circuit voltages and short circuit currents in case of plasma etched solar cells on mc silicon can be attributed to a polymer ashing post-treatment as well as still existing polymer residues.

6. ACKNOWLEDGEMENTS

The authors would like to thank E. Schaeffer, T. Zerres and H. Lautenschlager for technical assistance and measurements. Financial support by the German Federal Ministry for economics and technology (BMWi) under contract No. 329879E is gratefully acknowledged.

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