A TCAD Process Model with Monte Carlo Ion Implantation for 4H-SiC JBS Diode Analysis and Design

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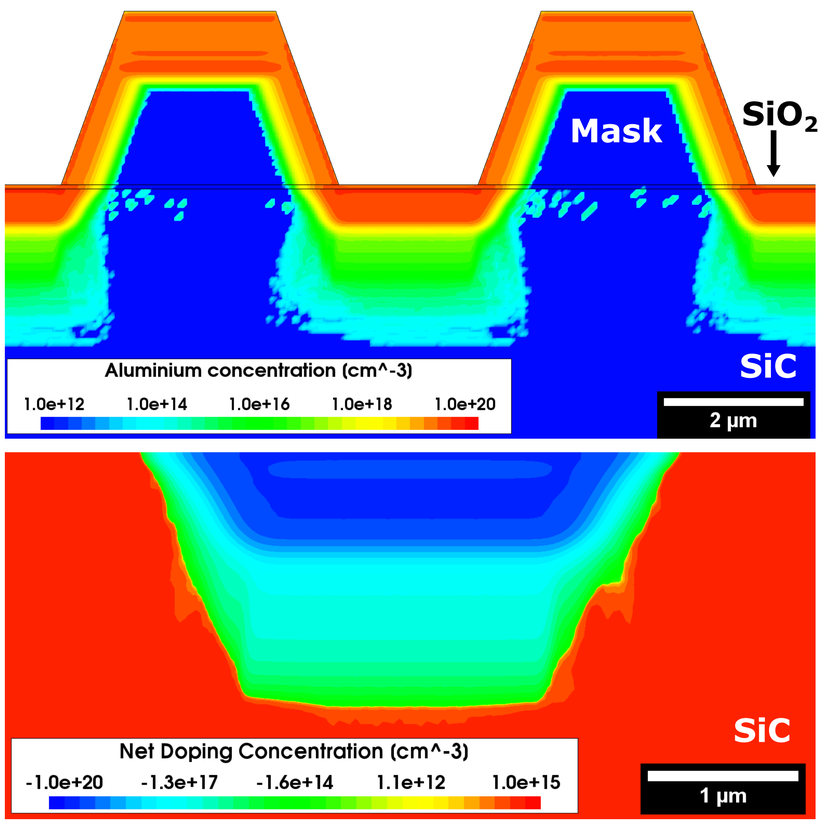
Introduction

The electrical characteristics of Junction Barrier Schottky (JBS) diodes are primarily determined by the geometry and dimensions of the junction barrier which is formed by ion implantation. The final doping profile is affected by the implantation parameters and process conditions. Channeling, lateral straggling, as well as flank angle and resolution of the implantation mask have an influence on the profile shape [1].

A TCAD process model was developed to reproduce the parameters and conditions of the ion implantation and to analyze the electrical characteristics of devices depending on the design of the junction barrier.

TCAD 2D Doping Profiles



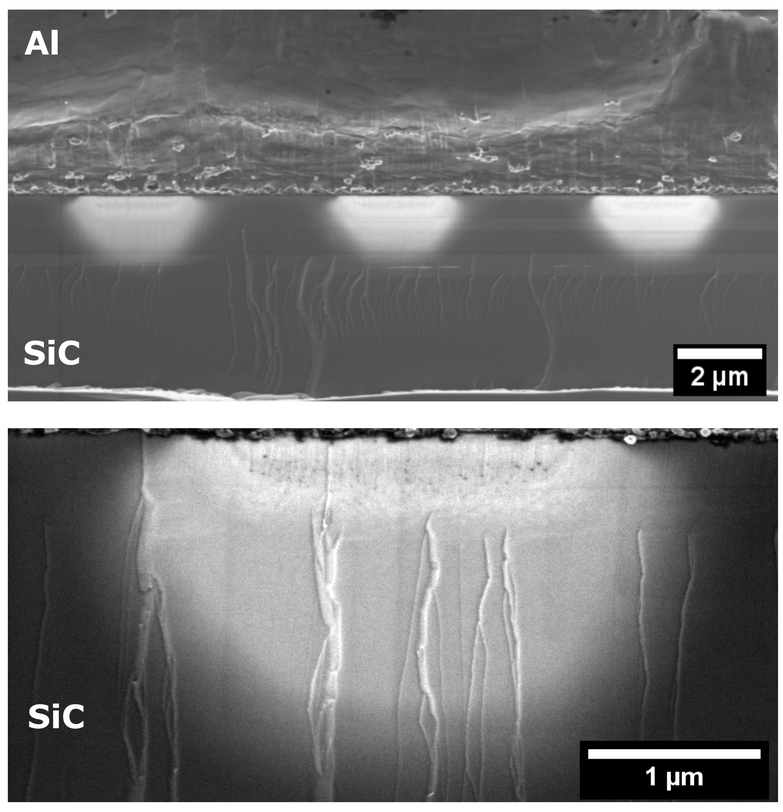
TCAD Process Model

Process Simulation

The TCAD model was implemented in Synopsis Sentaurus. The process simulation included deposition of a scattering oxide, aluminium ion implantation, high temperature annealing, thermal oxidation and metal deposition. The simulation parameters were taken and adapted from a standard diode process. Special focus was given to the Monte Carlo (MC) ion implantation.

The 4H-SiC n-type substrate and epitaxial layer were cut 4° off the [0001] direction. The aluminium implantation was performed under a 7° tilt with a dose of 2.6 x 10^{15} cm^{-3}. The resist mask was implemented with a flank angle of 70° which was extracted from electron images of resist cross-sections.

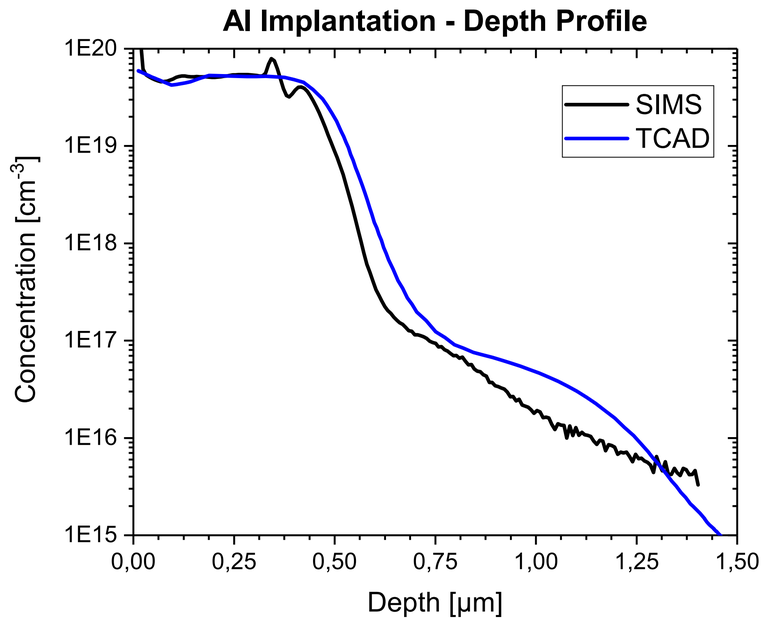
Doping Contrast Images



MC Ion Implantation

A simulated 1D doping profile and corresponding SIMS measurement are shown below. The simulation fits well to the data in the plateau region. Diffusion during the activation anneal which is not considered accurately in the process model might cause the differences visible at lower concentrations. Ion channeling below 1 x 10^{17} cm^{-3} is evident in both profiles.

TCAD 2D doping profiles of nominally 2 µm wide p^+ stripes implanted with aluminium to form a 500 nm deep box profile are depicted next to doping contrast cross-section images of a diode. The general shape of the implantation profile is trapezoidal which is due to the low mask flank angle. A higher flank angle leads to a more rectangular shape. The box profile plateau of about 5 x 10^{19} cm^{-3} is surrounded by a larger halo region where channeling and lateral straggling dominate. This increases the width of the junction barrier stripes by about 800 nm compared to the nominal width in the layout.



Model Verification

Diode Fabrication

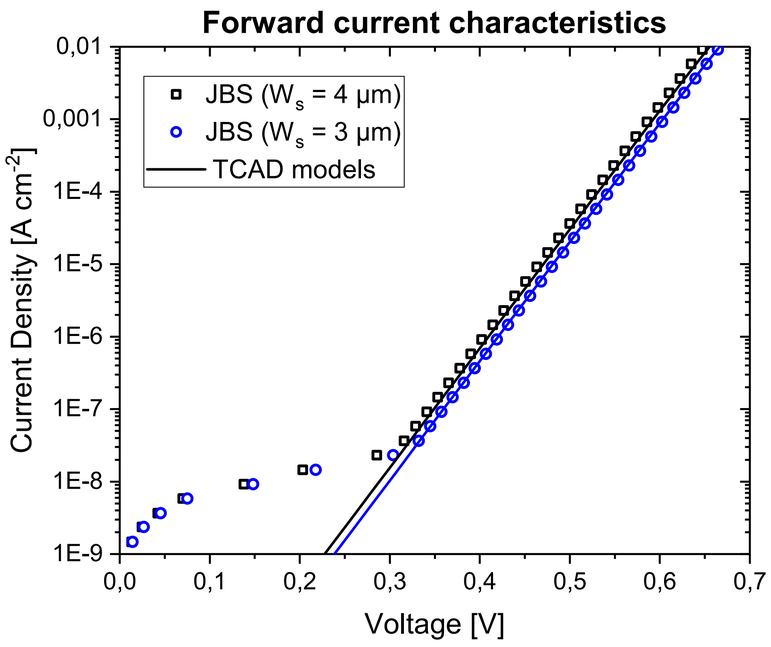
For verification of the model JBS diodes with a striped junction barrier design were fabricated on 100 mm 4H-SiC wafers with a 11 µm wide, 7.0 × 10^{15} cm^{-3} n^- doped epitaxial layer. The implantation parameters were chosen to yield a 5.0 × 10^{19} cm^{-3} box profile as shown in the figures above. The implantation was annealed at 1700°C for 30 minutes. 100 nm titanium, annealed at 450°C for 30 minutes, was used for the Schottky contact and 4 µm aluminium for the electrode. Two diode variants with 2 µm nominal p^+ width and spacing of 3 µm and 4 µm, respectively, were investigated.

Electrical Simulation

The device simulation using the developed process model took into account image force barrier lowering and tunneling across the Schottky barrier. The same parameters were used for forward and reverse bias simulations. The work function of the contact metal was calibrated using data from a Schottky Barrier Diode. A Schottky barrier height of about 1.2 V was extracted from the simulation which agrees well with published data.

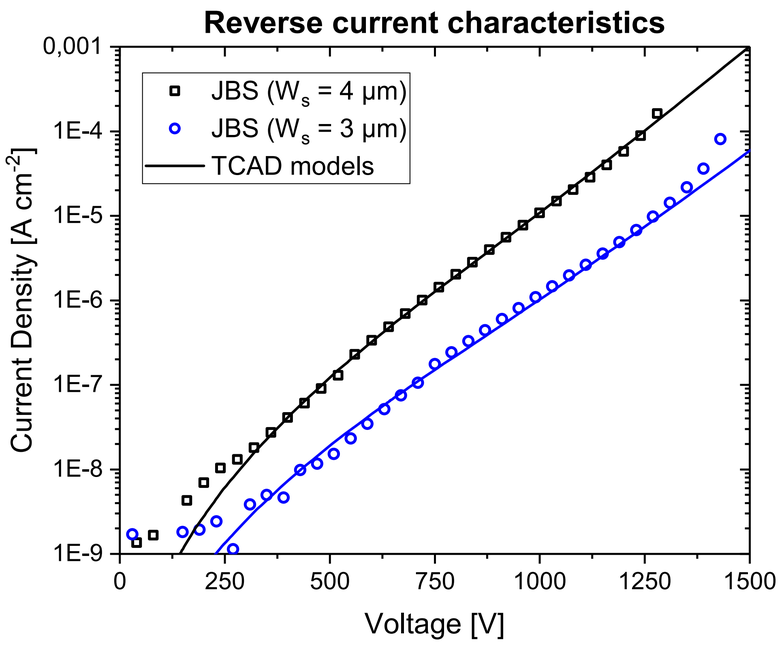
Forward Bias

Electrical measurements of two nearly ideal JBS diodes with different spacing W_s are plotted against data from the TCAD simulation. The measurement data confirms the validity of the model. Above the measurement resolution the model data fits well to the diodes in the low current regime. The difference in spacing results in a change of only a few tens of millivolts.



Reverse Bias

The model accurately reflects the differences in leakage current between the diode variants. The leakage at 1200 V is below 10 µA cm^{-2} with 3 µm and 100 µA cm^{-2} with 4 µm spacing. The reduced leakage current for the narrow spacing comes with little penalty under forward bias. The avalanche onset at 1300 V is not seen in the simulation due the breakdown being in the edge termination region.



References

[1] J. Buettner, T. Erlbacher, et al., Technological Advances Towards 4H-SiC JBS Diodes for Wind Power Applications, Applications in Electronics Pervading Industry, Environment and Society (2018) 83.