Integration of multi physics modeling of 3D stacks into modern 3D data structures

Peter Schneider[1], Andy Heinig[1], Robert Fischbach[2], Jens Lienig[2],
Sven Reitz[1], Jörn Stolle[1], Andreas Wilde[1]
[1]Fraunhofer IIS, Design Automation Division, Dresden
[2]Dresden University of Technology, Institute of Electromechanical and Electronic Design
Email: peter.schneider@eas.iis.fraunhofer.de, Tel: +49 (351) 4640 710

Abstract— This paper deals with the concept of how to integrate results of multi physics investigation of 3D stacks into modern comprehensive 3D data structures. Beside a description of modern 3D data structures and methods for floorplanning and Place&Route, approaches for multi physics modeling are introduced. The extension of the layout optimization process by multi physics modeling is investigated. Finally, we conclude with a summary of the future needs for an improved interoperability.

***Index Terms*— 3D IC, 3D data structures, multi physics modeling, Floorplanning, Place&Route**

I. Introduction

Currently, 3D integration is still characterized by stacking similar dies (e.g. memories or CPUs) or few tiers (imager and signal processing IC) which are mostly connected to each other trough their outer boundaries. Nevertheless, first steps are made towards 3D products combining different functional units (sensors, micro controller, memory, power supply) that are usually not designed for 3D integration [1]. Interposers which contain rewiring as well as through silicon vias (TSVs) are often used to connect these dies in order to realize the system functionality. However, it is expected that the potential of 3D integration will change this situation rapidly in the near future [2].

In order to enable a systematic 3D design, modern 3D data structures are needed that are able to represent the vertical relationship between the tiers in a 3D system. There has been a rapid development in this field over the last couple of years [3]. These data structures are an abstract model of the corresponding layout problem. They must enable the consideration of 3D-specific layout constraints. In 3D systems, those constraints are strongly influenced by the interaction of different physical effects within the 3D stack. The influence of these physical effects on the electrical behavior plays the most important role in system design, but also reliability aspects have to be considered simultaneously. Therefore, the impact of both the stack geometries and the interconnect structures on signal propagation and power distribution as well as electro-thermal and thermo-mechanical effects have to be considered in order to find an optimal 3D layout.

Within this 3D layout optimization process, the evaluation of the cost function is a crucial point. Straightforward approaches are solely considering the length of transmission lines or the violation of timing constraints to obtain a performance estimation. For complex 3D applications, the integration technology and the related thermal effects as well as power and signal integrity within the stack have to be considered. Furthermore, reliability aspects might also be included into the cost function. Therefore, interfaces between multi physics simulation and 3D data structures are urgently needed and are the main topic of this paper. Aiming at a fast evaluation of the cost function, a hierarchical modeling approach [4] can subsequently be combined with advanced methods for model abstraction and derivation of design guidelines.

II. 3D Data Structures

Data structures are mathematical objects used for the storage of information. Their logical structure determines how the data is organized internally. Operations realize data access and management functions. Typical basic data structures are arrays, lists and graphs (Figure 1).

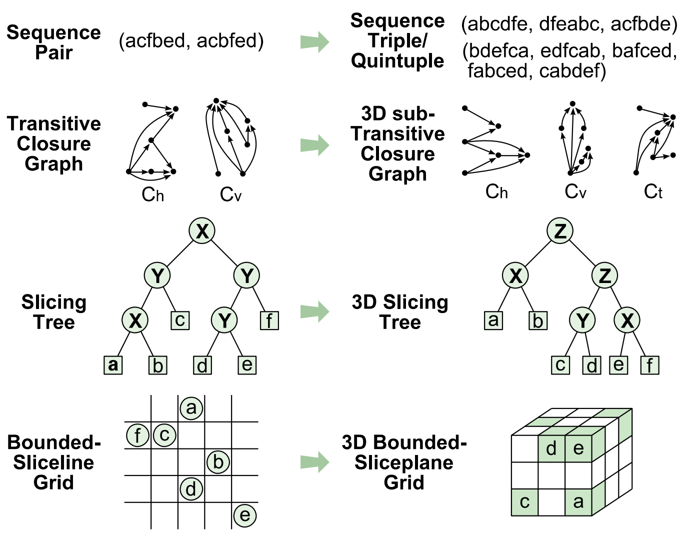

Figure 1. Well-known 2D data structures (left) and their 3D counterparts (right)

Design and design optimization require highly specialized data structures. In the area of physical design, many efficient data structures are available to handle classical two dimensional (2D) integrated circuits. Some well-known representatives are Sequence Pair, Transitive Closure Graph, Slicing Tree, and Bounded Sliceline Grid (Figure 1 left). Yao et al. [5] give a detailed overview of classical 2D data structures.

However, to handle 3D stacks, data structures capable of considering vertical constraints, such as inter-layer geometric relationships, are required [6]. The adoption of the classical 2D data structures into the third dimension allows the modeling of 3D stacks. Examples are Sequence Triple/Quintuple [7], 3D sub-Transitive Closure Graph [8], 3D Slicing Tree [9], and 3D Bounded-Sliceplane Grid [10] (Figure 1 right). These 3D data structures are able to represent functional blocks in all three dimensions.

Besides the vertical dependencies and the multitude of new constraints, 3D data structures need to meet further requirements. Adjacency information should be efficiently available to allow fast simulations of interactions between different functional blocks. The solution space and runtime complexity increases compared to 2D data structures. Thus, highly efficient implementations and solution limiting restrictions are needed (e.g. the possibility of pruning during solution finding). During optimization, cost evaluation typically takes place separate from the data structure (i.e., the solution is transformed into its real geometry which in turn is evaluated). Data structures with inherent cost correlating properties significantly fasten the time-consuming cost evaluation process. The relationship between problem formulation, optimization strategy and data representation is shown in Figure 2.

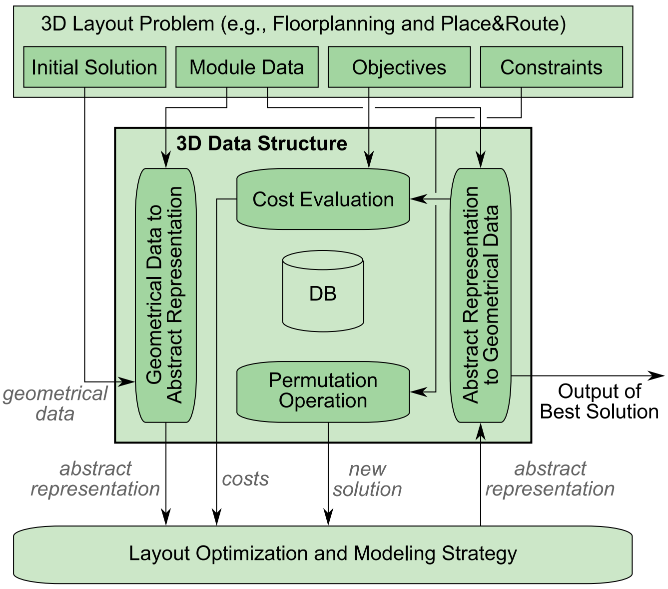

Figure 2. Interaction of a data structure with the layout problem (top) and the optimization and modeling strategy (bottom).

The data structure uses layout information, such as physical data of modules, constraints, and objectives, to evaluate concrete layout solutions as well as to transform between abstract and geometrical solution. Successful 3D physical design requires an efficient interaction between these components.

Data structures are important for many design steps, for instance the subsequently described Floorplanning and Place&Route. They enable the application of problem unspecific metaheuristics, like Simulated Annealing, for optimization. As depicted in Figure 2, data structures offer an abstract interface to the optimization and modeling strategy, for example, to modify and evaluate solutions.

III. Floorplaning and Place&Route

There are two different basic approaches to floorplanning of 3D systems. On one hand, there are stochastic methods like simulated annealing [11, 12], genetic algorithms [13] or threshold accepting. On the other hand, analytical approaches are used which apply, for example, a force model [14]. In this model, contracting forces are assumed at the edges between the cells. If this system is optimized, all cells might have the same position. Additional repulsive forces are usually inserted to avoid such a solution. The strength of the repulse is calculated from the congestion of the area including the cell information related to this force.

In analytical approaches, TSVs are usually included into to cost function in order to keep their number small. A simple optimization function, which considers the die area and the number of TSVs is given by:

$$F() = a\text{*area} + b\text{*Number(TSV)}$$

a and *b* are weighting factors (cost factors). However, the finding of balanced weighting factors is an important issue. In most chip designs, the congestion for the cells (sum of cell area divided by the total chip area) is lower than one. Thus, a number of TSVs can be inserted without consuming extra chip area. Only TSVs above this maximum number enlarge the chip area. However, while the size of the area usable for TSVs is actually needed for determining the weighting factors, it is only known after the floorplanning. That is a major disadvantage of analytical approaches for floorplanning.

Stochastic approaches aim at placing macro blocks of the design to the different dies in the 3D system in order to minimize the overall area occupied. Timing properties, thermal or mechanical effects are considered as constrains. If a 2.5D data structure is used, i.e. a 2D data structure for every die of the system, the TSVs must be inserted after every optimization step. In contrast, in a 3D data structure this can be done directly in the data structure and, hence, no extra effort is needed. Thus, the extra area consumed by the TSVs is known after each optimization step and can therefore be considered in the next step. So the total area (area of cells and area of TSVs) is optimized.

Another optimization goal for stochastic approaches is the cost of the entire 3D system. In this approach, the total cost of a 3D stack is calculated by a sum of the costs of die manufacturing, processing costs for TSVs, costs for assembly as well as testing costs. Detailed considerations on such a cost model are described in [15].

The floorplan for a microprocessor design is depicted in Figure 3. The design is divided into a four layer stack. The microprocessor consists of about 45000 cells in 45nm technology. These cells are at first partitioned into 128 macro blocks and then the floorplanning is performed by a threshold accepting algorithm. Minimizing the overall cost of the 3D system is the optimization goal. Please note that the chip area of the four dies might differ. This is because more macro blocks in the fourth die require more TSVs and thus, more area. However, such a solution is not cost-optimal according to the used cost model.

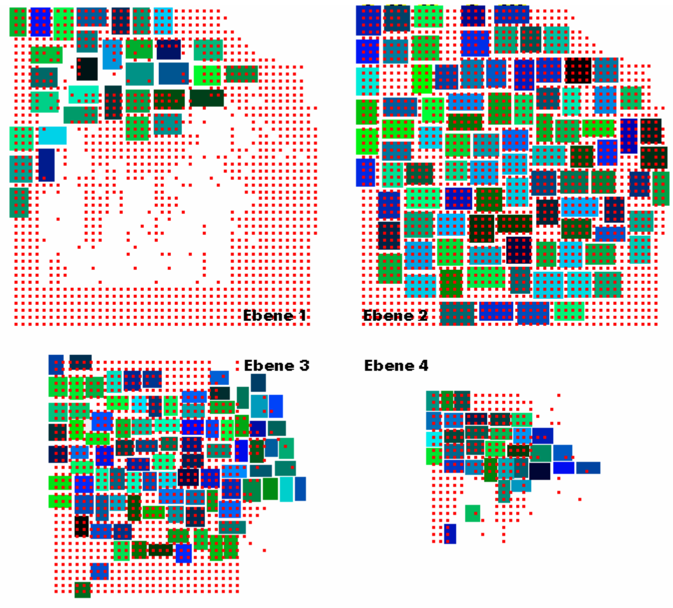

Figure 3. Floorplan of a four die stack of a microprocessor design. Blue and green squares point to macro blocks and the red dots to TSVs

Considering 3D Place&Route, the usage of TSVs positions and the positions of the macro blocks as input data for a standard 2D P&R tool is one option. Subsequently, every die can be placed. The cells in the macro blocks can be moved by the P&R tools while the TSVs are fixed. Performing Place&Route in 3D requires the modification of the TSV positions as well as the consideration of additional information about the interactions between the layers in order to achieve a better result. To this day, this is not efficiently supported by available tools. An important prerequisite for 3D place and route is the availability of appropriate data structures supplemented by techniques to gain the above mentioned information.

IV. Multi Physics Modeling of 3D Systems

The main goal of multi physics modeling is to capture the influence of the integration technology on the system behavior. This influence is dominated by complex interactions of the thermal, electrical and mechanical domain, e.g., thermal induced stress, electro thermal interactions, electromigration (see Figure 4).

In general, these different domains are coupled and cannot usually be considered independently within the design process. In order to build up a 3D system, the particular tier layouts and different technology options have to be combined. Based on measurements of test structures and multi physics simulations, first approaches for detailed investigations of 3D stacks are available. They include derivations of network and behavioral models. Based on this analysis, design constraints or guidelines can be elaborated.

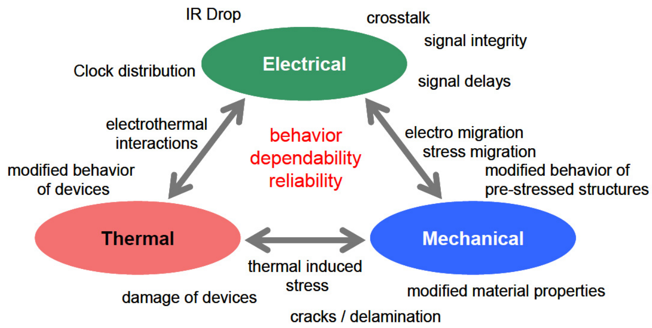

Figure 4. Multi physics modeling and cross domain coupling in 3D systems

However, there is no established flow to consider the influence of packaging and integration technology on system behavior and reliability for multi physics modeling in 3D systems. Therefore, a commonly accepted generic hierarchical modeling approach for multi physics problems in 3D systems is necessary in the long term. This approach should contain different abstraction levels:

- Detailed models of single via structures, e.g. for technology development and optimization,
- Coarse grain models for local interconnect structures in order to derive design guidelines or behavioral models,
- More abstract models for the analysis of entire stacks [16].

Usually the influence of the inter-chip interconnects (TSVs, balls etc.) on the *electrical behavior* of the system is of the main interest. Above all, decreasing geometrical dimensions and increasing operating frequencies require the detailed investigation of power and signal integrity, cross talk, and interconnect delays. Moreover, the small dimensions locally lead to very high current densities which results in electromigration that may cause reliability problems. Due to the dense interconnections between the stacked layers, parasitic effects play an increasing role. Electrical interconnects and TSVs which are crossing dies may elevate the risk of substrate coupling to active regions within the die. In addition, special processing steps will lead to changed device characteristics, e.g. after thinning of wafers, especially for ultra thin silicon.

The close location of functional blocks in a 3D structure and the mostly limited surface available for heat transport to the environment result in higher temperatures or hot spots within the stack. This may affect function and lifetime of the system. Therefore, an appropriate *thermal management* considering specific constraints is essential. There are different fundamental issues related to thermal effects:

- Semiconductor devices can reach a high level of temperature which leads to accelerated aging or immediate damage of these devices,

- Nonuniform temperature distributions may influence the operation of circuit blocks and sensing elements significantly,
- Different processing temperatures during the 3D integration process and/or heating of the stack in operation may cause additional mechanical stress in the system.

The *thermo-mechanical behavior* of the stack strongly influences its reliability. Sometimes the switching speed of transistors is affected as well. Furthermore, for 3D integration of sensor elements like pressure sensors or vibrating micro mechanical structures, intrinsic stress may result in a significant change of the behavior of the sensor, e.g. shift of eigenfrequencies or modified conductivity in piezoresistors.

An efficient treatment of the variety of the mentioned problems by simulation in different physical domains requires a systematic modeling. Hence, the hierarchical modeling approach, an appropriate methodology for multi level and multi physics analysis, proposed in [4], is used for a multitude of simulation tasks (Figure 5).

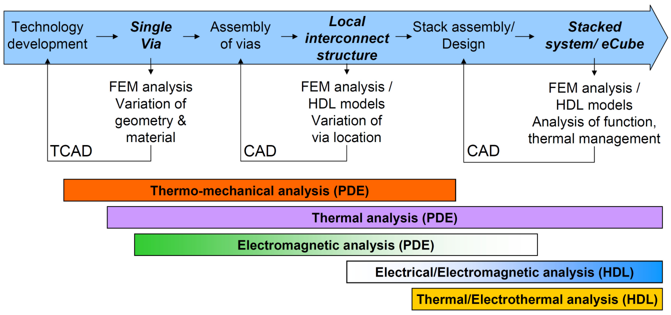

Figure 5. Hierarchical modeling approach for multi physics simulation ranging from technology development to entire stacked systems

One essential element of this approach is to generate parametric models of single or local structures (basic modules). Since a lot of different simulations tools are relevant for the 3D field, one important step in the modeling flow is a tool-independent structural representation. Based on an XML-description of fundamental structures of a 3D stack (layers, TSVs, interconnects), parametric models can be generated.

The models can be modified concerning geometrical and material properties as well as the represented physical effects (thermal, electrical, mechanical, …). These parametric models, which are provided for the finite element domain as well as for behavioral modeling, are stored in libraries and can be used to build up a model of the complex stacked system. Within this approach, the results of the analysis on one level of abstraction can be used for optimizing on the same level as well as input for modeling on the next level.

In Figure 6, variants for a TSV as well as for a structure of two dies and a PCB connected with micro balls are shown. Electrical and thermal characterization can be carried out using such models considering geometrical parameters for the different integration technologies [17].

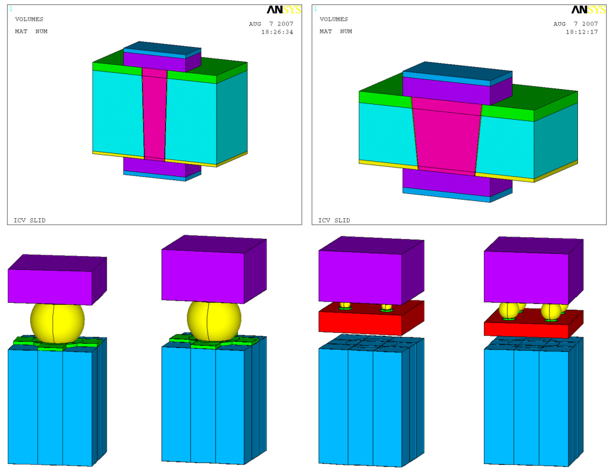

Figure 6. Parametric basic models of TSVs, as well as dies and PCB connected using balls

Beside the modification of geometry, which may cover a wide range of variations (see Figure 6), the change of material properties is also possible. In Figure 7, results of an analysis of a TSV structure in a substrate are shown. Assuming different conductivities of the substrate, the S parameter S21 (transmission) is depicted depending on the operating frequency and the permittivity of the substrate.

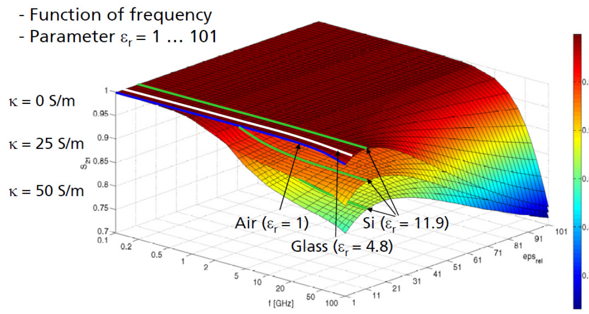

Figure 7. Results from parametric analysis of a TSV structure – magnitude of the S parameter S21 depending on operation frequency and permittivity of substrate

In addition, multi physics modeling tasks are also covered by our approach. A structure with TSVs crossing a lossy substrate is shown in Figure 8. For a single TSV, the influence of substrate temperature on the S parameters has been investigated in a temperature range of 20 to 100°C.

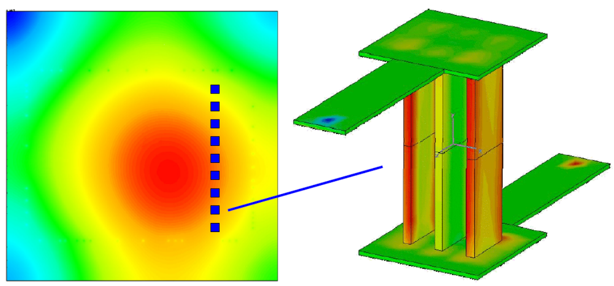

Figure 8. Setup of TSVs crossing a lossy substrate and exposed to different temperatures

The results are depicted in Figure 9 for the transmission parameter S21. Above a frequency of 2.5 GHz, a significant change of the transmission can be observed. Due to the higher temperature, the losses in the substrate increase and therefore, a decrease of S21 from 0.928 at 20°C to 0.889 at 100°C occurs.

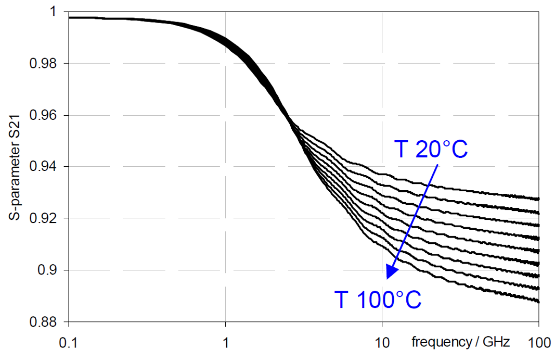

Figure 9. Transmission parameter S21 as function of temperature dependent substrate losses

To enable a more comprehensive investigation of the interactions within a 3D system, these models of basic structures must be combined to more complex models, e.g. for local interconnect structures. An example for electrical models suitable for RF investigations is shown in Figure 10.

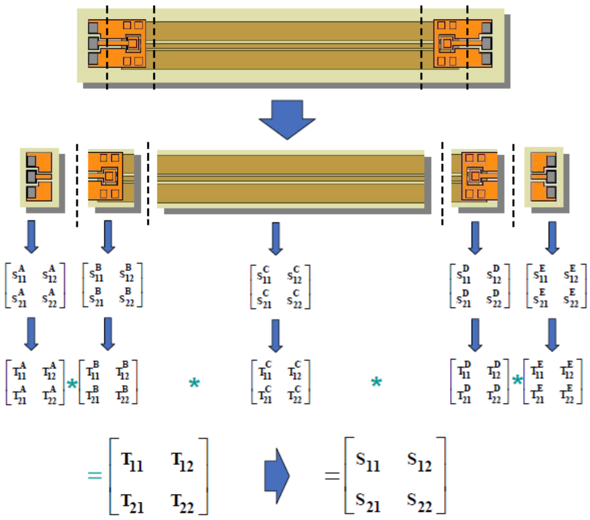

Figure 10. Combination of S-Parameter models of TSVs and transmission line structures

Based on a partitioning of an interconnect structure into transmission lines and TSVs, a simulation with a PDE solver is carried out for each partial structure. The results are matrices of scattering parameters of the partial structures. These S parameter matrices can be easily transformed into scattering transfer parameters (T parameter matrices). By a simple matrix multiplication the T matrices for the particular structures can be combined to the T parameter matrix of the entire interconnect structure. It is transformed back to the corresponding S Matrix, which can be used in electrical simulation.

Another possibility suitable for electrical as well as thermal simulation is the application of model order reduction (MOR) methods. Based on generic models (see Figure 6), the model for an entire stack can be built up. Using the meshing algorithms of PDE solvers, the matrices, e.g. for thermal resistances and capacitances, can be generated. Those large matrices with about 100,000 .. 1,000,000 degrees of freedom can be simplified by the above mentioned MOR algorithms. The result is a system description with a significant lower number of system variables, usually in range of 10 .. 1,000. From these smaller matrices, behavioral models can be derived, that can be calculated much more efficiently in circuit simulators. This MOR-based approach for model simplification is described in more details in [18].

Although there are several methods for automated model generation and simplification, it is still a big challenge to bridge the gap between the detailed knowledge of processing technology and a fast evaluation of the cost function within the layout optimization process.

V. Concept for Integration of Models/Simulation Results into Data Structures

In order to include results of multi physics simulation into data structures, an optimization cycle has to be established, which includes the following fundamental steps:

- Analysis of stack layout,
- Automatic derivation of coarse grain models for relevant physical effects including model simplification, if needed,
- Calculation of quality measures,
- Evaluation of cost function,
- Adaptation of stack layout.

There are different possibilities to implement this cycle depending on the layout optimization algorithms and 3D data structures used. If the floorplanning is carried out using a statistical approach (see Section II), multi physics modeling might be included as an additional branch in which supplemental input for cost evaluation is generated. One possibility is shown in Figure 11.

Normally, if a new solution is constructed it is evaluated using a cost function like:

$$C_{total} = w_1 * c_1 + w_2 * c_2 + \ldots + w_n * c_n$$

C_{total} is the total cost to evaluate and c_i are the considered cost terms weighted by the factors w_i. For an efficient optimization process, the evaluation has to be carried out very fast. Therefore, simple analytical formulas provided by the data structure are needed.

However, there is a risk that this analytical approach neglects some important details of the current solution. Therefore, more detailed simulation models must be included (Figure 11, right). The geometrical structure of the current solution has to be transferred into models for appropriate simulation tools covering the different physical domains. From the results of multi physics simulation, additional terms for the cost function are derived.

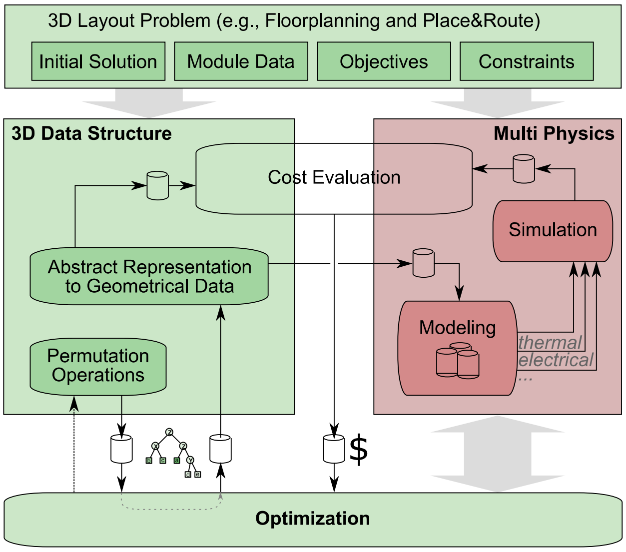

Figure 11. Extension of layout optimization by multi physics modeling

One important issue is an appropriate level of accuracy. On one side, it is possible to represent interconnects by signal delay, damping coefficient or a maximum power budget for different stack regions. This information is gained by parametric detail simulation and is provided as behavioral models based on lookup tables. These tables enable a rapid evaluation of the cost function. On the other side, more detailed models are available which are able to represent more complex interactions within the 3D stack. However, their use will slow down the optimization process significantly.

Another crucial point is the transformation of the geometrical structure into a suitable simulation model. Due to the complex structure within 3D stacks, powerful algorithms for structural analysis are needed. Based on the results of this analysis, models can be generated using the approaches describe in Section IV.

VI. Conclusions

Several design methodologies are available for the support of 3D design. However, current approaches are fairly isolated and a lot of manual work has to be carried out by the designer.

Modern 3D data structures are able to represent the relations of subsystems in a layered integrated circuit. With a modular hierarchical modeling approach, multi physics effects in 3D systems can be analyzed. To take advantage of this information, we suggest to establish a link between layout optimization and multi physics simulation. A first concept is introduced in the paper.

The most important issue in this context is to find a trade-off between the limitations of simple lookup table models and the high computing time of detailed models of the 3D stack. Furthermore, techniques for automatic modeling and model simplifications are urgently needed. In addition, the increase of simulation speed by advanced solution algorithms will have a significant impact on the quality and efficiency of 3D layout tools.

References

[1] Flatscher, M.; Dielacher, M.; Herndl, T.; Lentsch, T.; Matischek, R.; Prainsack, J.; Theuss, H.; Weber, W.: A bulk acoustic wave(BAW)-based sensor node for automotive wireless sensor networks", e & I Elektrotechnik und Informationstechnik, Springer, Volume 125, Number 4, April 2008

[2] Garrou, P.; Bower, C.; Ramm, P.: Handbook of 3D Integration. 2 vols. Technology and Applications of 3D Integrated Circuits. Wiley, August 2008

[3] Y. Kohira, C. Kodama, K. Fujiyoshi, and A. Takahashi: Evaluation of 3D-packing representations for scheduling of dynamically reconfigurable systems. In Proc. IEEE International Symposium on Circuits and Systems ISCAS 2006, pp. 4487–4490, 2006

[4] Schneider, P.; Reitz, S.; Wilde, A.; Elst, G.; Schwarz, P.: Towards a Methodology for Analysis of Interconnect Structures for 3D-Integration of Micro Systems. Proc. DTIP2007, 25.-27. April 2007, Stresa, pp. 162-168

[5] Yao, B., Chen, H., Cheng, C.-K. & Graham, R.: Revisiting floorplan representations. ISPD '01: Proceedings of the 2001 international symposium on Physical design, ACM, 2001, pp. 138-143

[6] Fischbach, R.; Lienig, J. & and T. Meister, T.: From 3D circuit technologies, and data structures to interconnect prediction. in SLIP '09: Proceedings of the 11th international workshop on System level interconnect prediction. ACM, 2009, pp. 77–84.

[7] Yamazaki, H., Sakanushi, K., Nakatake, S. & Kajitani, Y.: The 3D-Packing by Meta Data Structure and Packing Heuristics. Fundamentals of Electronics, Communications and Computer, IEICE Transactions on, 2000, Vol. E83-A(4), pp. 639-645

[8] Yuh, P.-H., Yang, C.-L., Chang, Y.-W. & Chen, H.-L.: Temporal floorplanning using 3D-subTCG. Proc. Asia and South Pacific Design Automation Conference the ASP-DAC 2004, 2004, pp. 725-730

[9] Cheng, L., Deng, L. & Wong, M.D.F.: Floorplanning for 3-D VLSI design. ASP-DAC '05: Proceedings of the 2005 Conference on Asia South Pacific Design Automation. ACM, 2005, pp. 405-411

[10] Yamagishi, H., Ninomiya, H. & Asai, H.: Three dimensional module packing by simulated annealing. Evolutionary Computation, IEEE Congress on, 2005, Vol. 2, pp. 1069-1074

[11] Tan Yan, Qing Dong, Yasuhiro Takashima, Yoji Kajitani: How does partitioning matter for 3D floorplanning ACM GLS-VLSI, 2006

[12] Zhuoyuan Li, Xianlong Hong, Qiang Zhou, Yici Cai, Jinian Bian, Hannal Yang, Prashant Saxena, Vijay Pitchumani: A divide-and-conquer 2.5-D floorplanning algorithm based on statistical wirelength estimation. ISCAS (6) 2005: 6230-6233

[13] S. Salewski, E. Barke: An Upper Bound for 3D Slicing Floorplans, Proceedings of 7th ASPDAC and 15th Int'l Conf. on VLSI Design (2002), January 2002

[14] J. Cong and G. Luo: A Multilevel Analytical Placement for. 3D ICs, Proceedings of the 2009 Conference on Asia and South Pacific Design Automation

[15] Xiangyu Dong and Yuan Xie: System-level Cost Analysis and Design Exploration for 3D Architectures, ASP-DAC 2009

[16] Schneider, P.; Reitz, S.; Stolle, J.; Martin, R.: Design Aspects of 3D Integration of MEMS-based Systems. DTIP 2009, Rome, Italy, 1.-3. April 2009

[17] Schneider, P.; Reitz, S.; Stolle, J.; Martin, R.; Wilde, A.; Ramm, P.; Weber, J.: Design Support for 3D System Integration by Multi Physics Simulation. Mater. Res. Soc. Symp. Vol. 1112, Materials and Technologies for 3-D Integration, MRS Fall Meeting 2008, pp. 235-246

[18] Köhler, A.; Clauß, Ch.; Reitz, S.; Haase, J.; Schneider, P.: Snapshot-Based Parametric Model Order Reduction. MATHMOD 2009, Vienna, February 11 - 13, 2009