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EMITTER FORMATION AND PASSIVATION DEPENDENCE ON CRYSTAL GRAIN ORIENTATIONS AFTER ATMOSPHERIC PRESSURE DRY NANOTEXTURING

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ABSTRACT: In this work, we investigate the emitter performance of a multicrystalline silicon solar cell as a function of the grains crystallographic orientation and associated texturing level, after using a nanotexturing process by plasma-less atmospheric pressure dry etching that enables low reflectivity, followed by a short anisotropic alkaline etch. It was seen in our investigation that darker grains exhibit lower emitter sheet resistance ($R_{sh} \approx 72$ Ω/sq.) than that of lighter grains ($R_{sh} \approx 79$ Ω/sq.). We show that with our current etching process flow, there is a linear correlation between charge carrier lifetime and weighted surface reflection in different grains.
Keywords: Atmospheric pressure dry etching, nanotexturing, multicrystalline silicon, crystal grain orientations, emitter performance

1 INTRODUCTION

Alternatives to the incumbent wet-chemical texturing method have been sought after by the photovoltaic community for quite some time [1, 2]. More recently, nanotexturing processes (also often referred to as "black silicon") have generated renewed interest due to their ability to reach low reflectivities and higher solar cell efficiencies using slurry-sawn multicrystalline silicon (mc-Si) wafers [3, 4]. The plasma-less atmospheric pressure dry etching (ADE) process recently demonstrated efficiencies above 20% using mc-Si wafers [5]. ADE is also suitable for monocrystalline silicon (c-Si) wafers [6]. For mc-Si wafers, the texture varies depending on the crystallographic orientation of the grains and the degree of anisotropy of the etching/texturing steps that are used. Anisotropic etching causes reflection variations among the mc-Si grains, due to the formation of structures different in morphology. It is observed that, this difference in morphology of the crystal grains cause variations in emitter diffusion affecting the carrier concentration and the emitter sheet resistance.

As a continuous improvement in the ADE technique, in this work, we investigate the various crystal orientations within mc-Si wafer and their effects on specific cell processes, such as surface reflection, surface passivation, emitter diffusion, carrier concentration and lifetime. The purpose of this work is to understand these variations in a quantitative way and to analyze the distribution of results of the ADE-nanotextured mc-Si solar cells which will allow further optimization of the surface texture and the subsequent cell manufacturing process steps to achieve higher conversion efficiencies.

2 APPROACH

2.1 Experiment design

The process workflow is presented in Figure 1. 156x156 mm^2 boron-doped *p*-type mc-Si wafers (base resistivity (ρ_B) ≈ 1.6 Ωcm) were pre-treated by saw-damage etching using wet-chemical process (alkaline), subsequently the ADE texturing was performed in order to form black silicon structures on wafer front sides [5–9]. The wafers then went through a post-treatment process in order to lower the surface roughness to allow better integration of this texture into common solar cell processing steps, most notably emitter diffusion and surface passivation [7]. During this post-treatment process the wafers were subjected to a short anisotropic wet-chemical treatment (alkaline) adjusted to reach an average value of surface reflection at 600 nm, $R \approx 15\%$. Some wafers were characterized for surface morphology, weighted surface reflectivity (R_w) [9] and scanning electron microscopy (SEM). Emitter was formed on the textured surface by industry-type $POCl_3$-based tube diffusion furnace, followed by chemical edge isolation including phosphosilicate glass (PSG) etching. Some wafers were characterized for emitter diffusion properties by using electrochemical-capacitance-voltage (ECV) and four-point-probe (4pp) measurement techniques. The wafers were first passivated by applying conformal layer of AlO_x both on front side (2 nm) and rear side (6 nm) by using fast atomic layer deposition (ALD) technique [8], followed by a low-temperature annealing, so called "outgassing" process [10] and were finally passivated by applying SiN_x depositions using plasma-enhanced chemical vapor deposition (PECVD) both on front side (75 nm) as anti-reflection coating (ARC) and on rear side (150 nm) for capping following passivated emitter and rear cell (PERC) structure and then fired at a set temperature of 850 °C, and finally were characterized for surface reflection and photoluminescence (PL).

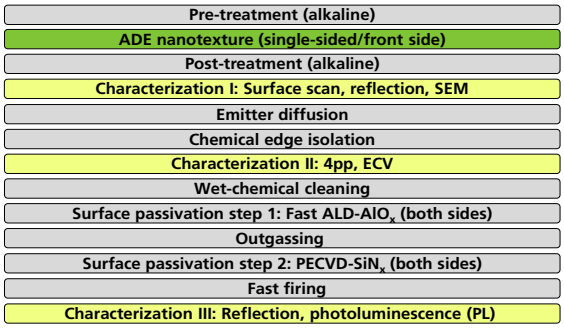


Figure 1: Schematic process workflow.

2.2 Characterization

In order to investigate the influence of the etching steps on mc-Si grains, at first scanned image of an ADE-

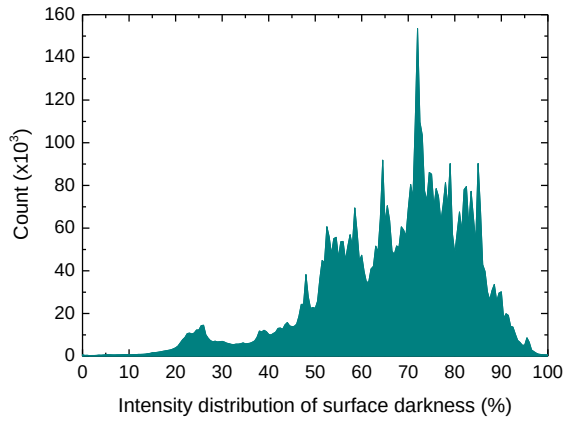
textured surface was characterized for its intensity distribution of the surface darkness. One dark grain (a) and one light grain (b) were selected for further characterizations, such as R_w and SEM.

Following emitter diffusion process, emitter sheet resistance (R_{sh}) of the dark grain (a) and the light grain (b) for identical emitter diffusion process was then characterized before surface passivation by using four-point-probe (4pp) technique. Furthermore, electrochemical-capacitance-voltage (ECV) method as per [11] was performed in order to obtain various emitter profile characterization values by characterizing the dark grain (a), the light grain (b) along with the flat surface for identical emitter. As the surface roughness influences the ECV measurement (the surface enlargement factor (f) correlates with the charge carrier concentration (N) and the depth (d)), we corrected the measured carrier concentration profile, that the R_{sh} determined from the profile matches the local R_{sh} determined by 4pp technique [12–14]. After surface passivation and firing, the samples were characterized with PL method for lifetime-calibrated PL-imaging.

3 RESULTS AND DISCUSSION

3.1 Reflection distribution over ADE-textured mc-Si

Figure 2(i) presents correlation between counts over surface darkness distribution for a scanned surface of an ADE-textured wafer. Such distribution of surface darkness can be translated as a distribution function of surface reflection over the textured surface. The SEM images of the lowest reflective grain of the wafer, namely the dark grain (a) ($R_w \approx 8.8\%$) and the highest reflective grain of the wafer, namely the light grain (b) ($R_w \approx 16.5\%$) are presented respectively in Figure 2(ii) for the dark grain (a) with densely situated porous structures, and in Figure 2(iii) for the light grain (b) with comparatively less porous structures than the dark one.



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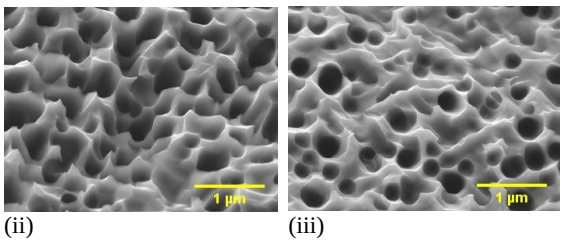
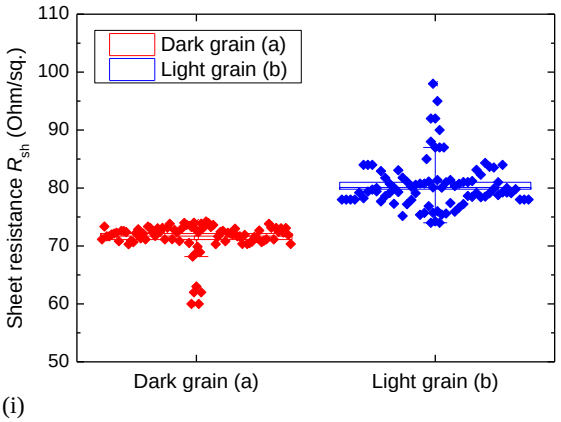


(ii) (iii)

Figure 2: (i) Histogram of an ADE-textured wafer after surface scanning representing counts over intensity distribution of the surface darkness. (ii) and (iii) Inclined top-view of scanning electron microscopy (SEM) images of dark grain (a) and light grain (b) of the selected ADE-textured wafer respectively.

3.2 Emitter diffusion

Figure 3(i) presents the corresponding R_{sh} distributions for dark grain (a) and light grain (b) measured by 4pp technique. The emitter diffusion characterized by ECV method and fitted for R_{sh} measurement by 4pp technique is presented in Figure 3(ii) exhibiting a possible trend with highest carrier concentration (N) for lower reflection grains to lower N for higher reflection grains. Surface enlargement is found to be higher for the dark grain (a) (factor of 2.2) due to higher texturing than for the light grain (b) (factor of 1.6), which is the reason behind higher N for dark grain (a) and comparatively lower N for light grain (b). In comparison, pertaining to a low surface enlargement, N is lower for the flat surface for the diffusion of the identical emitter.



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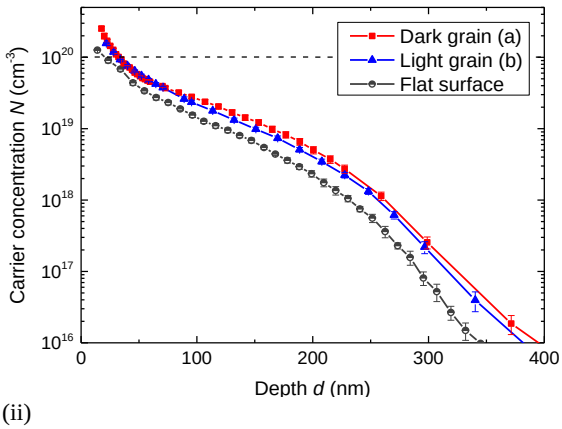


(ii)

Figure 3: (i) Emitter sheet resistances (R_{sh}) for dark grain (a) and light grain (b) measured by four-point-probe (4pp) technique. (ii) Carrier concentration (N) in comparison between ADE-textured dark grain (a) and light grain (b) to flat surface for carrier concentration (N) measured by electrochemical-capacitance-voltage (ECV) method and fitted for R_{sh} from Figure 3(i).

Different emitter profile characterizations are, namely maximum carrier concentration at the surface (N_s), depth of the highly doped region (d_{high} at $N = 10^{20}$ cm^{-3}), depth of the lowly doped region (d_{low} at $N = 10^{16}$ cm^{-3}), emitter sheet resistance (R_{sh}) (see table I).

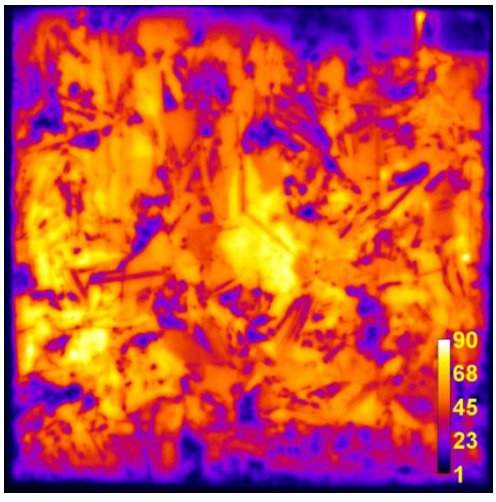
Table I: Characteristics of the emitter diffusion profile measured with ECV method and adjusted with 4pp technique for the dark grain (a), the light grain (b) and the flat surface after emitter diffusion and PSG etching.

Grains/ Properties	Dark grain (a)	Light grain (b)	Flat surface
N_s (x10^{20} cm^{-3})	(2.5±0.2)	(1.6±0.0)	(1.3±0.0)
d_{high} (nm)	35	30	20
d_{low} (nm)	400	390	350
R_{sh} (Ω/sq.)	72	79	88
R_w (%)	8.8	16.5	30.0

Nonetheless, ECV method does not preserve the surface roughness inherently obtained from texture itself, hence the surface enlargement is argumentative over two factors: mostly the texture and to some extent the ECV method itself. Moreover, ECV method only provides a mean value of N for the whole measurement area as it does not consider diffusion profile/emitter performance separately at the tip of the nanostructures or inside the nanostructures. Although during the adjustment of the measured values from ECV method (by using R_{sh} from 4pp technique) we assume that the emitter is evenly distributed over the whole texture. Therefore, it can be concluded that although the ECV method provides insight to the emitter diffusion profile to good extent, yet the data obtained needs to be considered with caution.

3.3 Comparison of charge carrier lifetime and weighted surface reflection

Figure 4(i) shows lifetime-calibrated PL image of ADE-textured surface passivated with fast ALD-AlO_x/PECVD-SiN_x stacks on front and rear sides after firing showing a variation of minority charge carrier lifetimes along the wafer surface area. Figure 4(ii) shows the distribution of the charge carrier lifetime over the entire surface. We can see from 4(i) and 4(ii) that the carrier lifetime varies throughout the surface. Although the carrier lifetimes in various mc-Si grains are known to be influenced by their inherent bulk lifetimes (due to grain boundaries, defect/dislocations, etc.), we expect that a variation in surface morphology in different grains also significantly affects the effective lifetime due to a difference in emitter formation and surface passivation.



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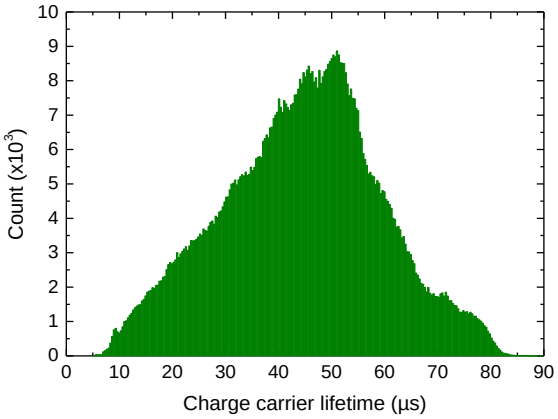
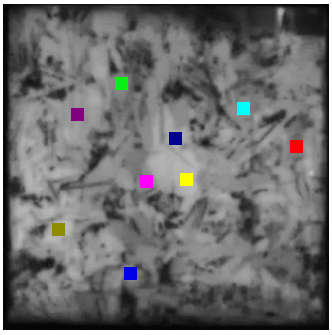


(ii)

Figure 4: (i) Lifetime-calibrated PL image of passivated ADE-textured surface. (ii) Histogram of the charge carrier lifetime representing counts over lifetime for an entire ADE-textured surface.

From the lifetime-calibrated PL image nine arbitrary points were identified for measuring their corresponding R_w by avoiding areas with bulk-inherited surface defects, dislocations and impurities for this measurement. The correlation between carrier lifetime and weighted reflection is linear (Figure 5(ii)) within the investigated parameter range; with increasing R_w the lifetime also increases.



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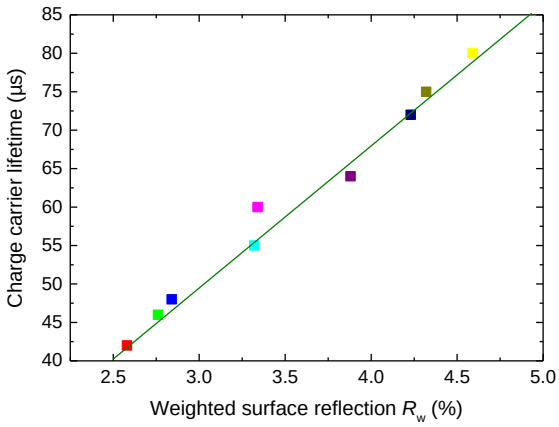

(ii)

Figure 5: (i) PL image of ADE surface presented in Figure 4(i) with arbitrary points for measuring their weighted surface reflections in order to correlate to their corresponding lifetime values obtained from Figure 4(i). (ii) Correlation between weighted surface reflection (R_w) and the corresponding charge carrier lifetime of the arbitrary points.

4 CONCLUSION

We investigated how the electrical properties relevant for the solar cell performance may vary over the surface due to difference in surface morphologies in different grains, after using ADE-textured mc-Si wafers followed by a short anisotropic alkaline wet etch.

We find that the grains with lower surface reflection, pertaining to a higher surface enlargement, show higher carrier concentration and consequently a lower emitter sheet resistance in comparison to the grains with higher surface reflection. We also highlighted a linear relationship between weighted surface reflection and charge carrier lifetime.

This study provides an insight on methods through which the influence of a large distribution of surface reflection on electrical properties of a nanotextured solar cell can be studied. We expect that with further investigations, this approach could also facilitate the optimization of the emitter formation process on diamond-wire sawn mc-Si solar cells textured by various nanotexturing methods.

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6 REFERENCES

[1] J. Rentsch, N. Kohn, F. Bamberg, K. Roth, S. Peters, R. Lüdemann, R. Preu, “Isotropic plasma texturing of mc-Si for industrial solar cell fabrication,” Proceedings of the 31st IEEE Photovoltaic Specialists Conference, pp. 1316–1319, 2005.

[2] K.-s. Lee, M.-H. Ha, J. H. Kim, J.-W. Jeong, “Damage-free reactive ion etch for high-efficiency large-area multi-crystalline silicon solar cells,” Solar Energy Materials and Solar Cells, vol. 95, no. 1, pp. 66–68, 2011.

[3] J. Oh, H.-C. Yuan, H. M. Branz, “An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures,” Nature nanotechnology, vol. 7, no. 11, pp. 743–748, 2012.

[4] X. X. Lin, Y. Zeng, S. H. Zhong, Z. G. Huang, H. Q. Qian, J. Ling, J. B. Zhu, W. Z. Shen, “Realization of improved efficiency on nanostructured multicrystalline silicon solar cells for mass production,” Nanotechnology, vol. 26, no. 12, p. 125401, 2015.

[5] B. Kafle, A. I. Ridoy, P. Saint-Cast, L. Clochard, E. Duffy, M. Hofmann, J. Rentsch, “Atmospheric pressure dry texturing enabling > 20% conversion efficiency on multicrystalline silicon PERC solar cells,” AIP Conference Proceedings 1999, pp. 50003 (1–7), 2018.

[6] B. Kafle, J. Seiffe, M. Hofmann, L. Clochard, E. Duffy, J. Rentsch, “Nanostructuring of c-Si surface by F_2-based atmospheric pressure dry texturing process,” Phys. Status Solidi A, vol. 212, no. 2, pp. 307–311, 2015.

[7] B. Kafle, T. Freund, A. Mannan, L. Clochard, E. Duffy, S. Werner, P. Saint-Cast, M. Hofmann, J. Rentsch, R. Preu, “Plasma-free dry-chemical texturing process for high-efficiency multicrystalline silicon solar cells,” Energy Procedia, vol. 92, pp. 359–368, 2016.

[8] P. Saint-Cast, B. Kafle, R. Pandey, A. I. Ridoy, M. Hofmann, L. Clochard, T. Schwarze, M. Pittroff, J. Rentsch, R. Preu, “Rear passivated mc-Si solar cells textured by atmospheric pressure dry etching,” Energy Procedia, vol. 124, pp. 260–266, 2017.

[9] B. Kafle, “Mask-less dry texturing of crystalline silicon solar cells in atmospheric pressure conditions,” Dissertation, Albert-Ludwigs University of Freiburg, Freiburg, Germany, pp. 272, 2016.

[10] S. Werner, E. Lohmüller, P. Saint-Cast, J.M. Greulich, J. Weber, S. Schmidt, A. Moldovan, A.A. Brand, T. Dannenberg, S. Mack, S. Wasmer, M. Demant, M. Linse, R. Ackermann, A. Wolf, R. Preu, “Key aspects for fabrication of p-type Cz-Si PERC cells exceeding 22% conversion efficiency,” 33rd European Photovoltaic Solar Energy Conference, Amsterdam, The Netherlands, 2017.

[11] B. Kafle, T. Freund, S. Werner, J. Schön, A. Lorenz, A. Wolf, L. Clochard, E. Duffy, P. Saint-Cast, M. Hofmann, J. Rentsch, “On the nature of emitter diffusion and screen-printing contact formation on nanostructured silicon surfaces,” IEEE J. Photovoltaics, vol. 7, no. 1, pp. 136–143, 2017.

[12] R. Bock, P. P. Altermatt, J. Schmidt, “Accurate extraction of doping profiles from electrochemical capacitance voltage measurements,” 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, 2008.

[13] A. Kimmerle, “Diffused surfaces for crystalline silicon solar cells – process development, characterization and modelling,” Dissertation, Albert-Ludwigs University of Freiburg, Freiburg, Germany, 2015.

[14] S. Werner, E. Lohmüller, S. Maier, S. Mourad, A. Wolf, “Challenges for lowly-doped phosphorus emitters in silicon solar cells with screen-printed silver contacts,” Energy Procedia, vol. 124, pp. 936–946, 2017.