Fraunhofer IPMS

HF-Release of sacrificial layers in CMOS-integrated MOEMS structures

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Introduction

- IPMS fabricates various types of Spatial Light Modulators (SLM) a kind of MOEMS [1],[2]
- MOEMS-part is integrated on customizes CMOS-backplanes
- In CMOS various oxides (PE-USG, BPSG, thermal) are used as interlayer dielectric material
- In MOEMS-part PE-USG is used as sacrificial layer to obtain smooth surface for several metal layer depositions and to provide full movability of the mirror during the operation.
- Sacrificial layers are released by hydrogen fluoride gas phase etching [3]
- Oxides in CMOS-part have to be protected against HF attack
- Release should be done fast to avoid fluorine corrosion of metal parts
- Residues from the PECVD precursor can lower device performance
- Knowing the release kinetics for a specific device gives the opportunity to optimize the release process to reduce the number and the negative influence of residues, leading to a better device performance

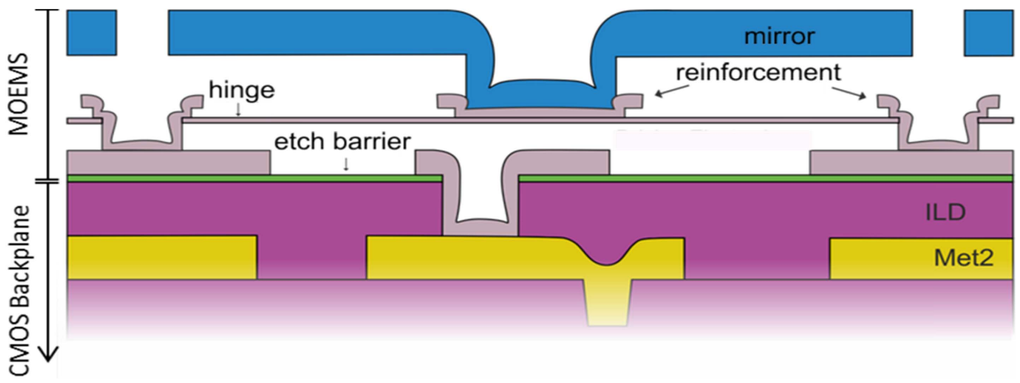

Figure 1. Schematic cross-section image of three-level MOEMS structure after the HF-release.

Release kinetics

Residues

- Residues remain after release process
- String- or canvas-like shape as shown in figure 2
- Often contain carbon, probably from the TEOS precursor, together with fluorine, oxygen and maybe boron and small amounts of other elements as shown in figure 3
- Not solved in HF or later plasma treatments, they may stay in the device even for later operation
- Can affect general performance or functionality in terms of restriction of single mirrors
- We assume, that they agglomerate at the border, at which two etching fronts meet in the later release process
  - Changing the shape of the structure under the mirror can influence the velocity and shape as well as possible numbers and direction of movement for etching fronts at a certain point.
  - Arrangement and number of etch holes in the mirror can be changed to push positions of residues and thus decrease their number and influence of device performance
- Layout offers several possibilities for optimization (additional to technological processes)

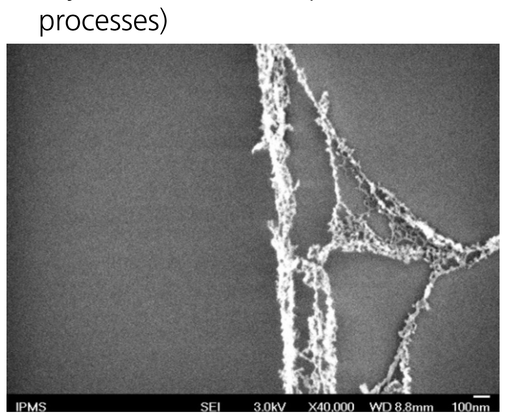

Figure 2. SEM-image of a typical Residue on the mirror backside taken after the HF release.

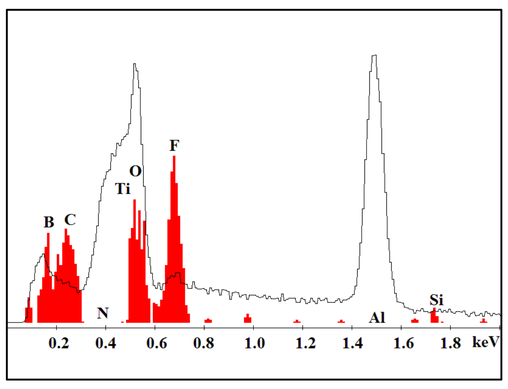

Figure 3. Analysis of a mirror backside affected by residues by energy dispersive X-ray spectroscopy. The full spectrum is shown as black line, while the red bars are calculated as the difference between an effected and an unaffected area.

Release mechanisms

- Three different mechanisms were observed:
  1. Isotropic etching (A)
  2. Topology based anisotropic etching (B)
  3. Interface layer anisotropic etching (C)
- Isotropic etching at begin of release process
- Topology based etching
  - increases etching velocity in vertical direction on top of filled vias and structural edges (figure 5)
  - Growing zones during via filling
  - Probably caused by differences in density, porosity and stoichiometry
  - Effect is effective even few micron above and outside the structure
- Interface based etch
  - increases etching velocity in horizontal direction
  - Takes place on top of surfaces acting as stop for metal etching
  - Probably physical/chemical modification of the surface by RIE chemicals (Cl_2/BCl_3) [4]
  - Reaction of HF with reactants like Si, $SiCl_4$, vinylic polymers (BOCl) leads to change in release velocity

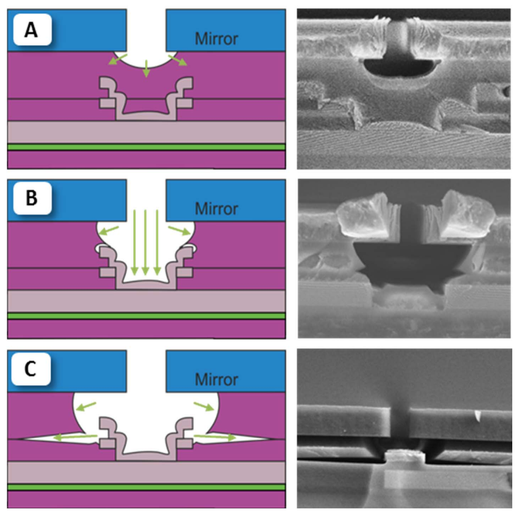

Figure 4. Schematic (left) and representative SEM images (right) of the release processes. (A) Isotropic Etch, (B) topology based etch, (C) interface etch.

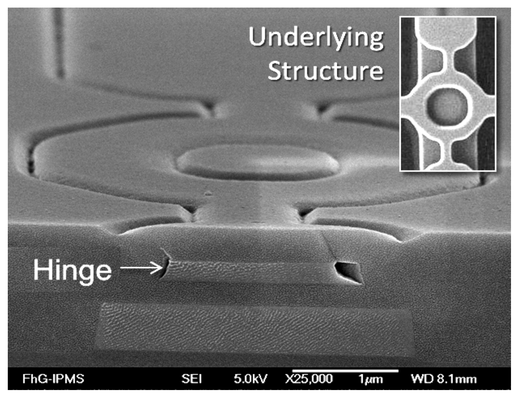

Figure 5. SEM image taken in oblique view showing the topology based etch on top of the hinge layers structures without deposited mirrors (inset).

CMOS-protection

- Effective barrier layer between the top electrode layer and the inter-layer dielectrics is necessary.
- Different possible materials, which are HF inert and electrical insulating [5], [6]
  - Al_2O_3 was best suited
  - ALD-Al2O3 was superior to sputtered Al_2O_3 since it showed less defects and better coverage
- Devices prepared with an etch stop from ALD-Al_2O_3 did not show any hint of etching attack to the CMOS from MOEMS side (see figure 6)

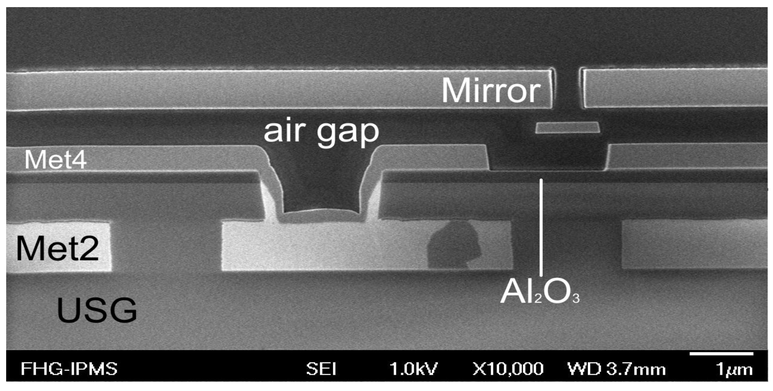

Figure 6. Cross-section of a MOEMS device prepared by ion polishing. For improvement of the mechanical stability the air gap, the mirror slits and the space above the mirrors is filled by epoxy glue. To increase contrast between USG and Al_2O_3 the original image was slightly recoloured.

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