## Model Abstraction of 3D-Integrated/Interposer-Based High Performance Systems for Faster (Thermal) Simulation

Andy Heinig<sup>1</sup>, Dimitrios Papaioannou<sup>1</sup>, Robert Fischbach<sup>1</sup>,

<sup>1</sup> Fraunhofer Institute for Integrated Circuits, Design Automation Division, Zeunerstrasse 38, 01069, Dresden, Germany Email: firstname.lastname@eas.iis.fraunhofer.de

### ABSTRACT

Complex, high-integrated and high-performance microelectronic systems that include an interposer-solution become more and more dominant in the field of advanced 2.5/3D system integration. In such systems, for example required in network and image processing applications, the different ICs (e.g. processors and memories) are placed on a silicon interposer, which allow shorter interconnect lines between the elements, improving the signal transmission. The example system used throughout this paper combines an ASIC for signal processing with a high-performance memory. These two chips are placed as bare dies side-by-side on a silicon interposer using copper pillars. The interposer itself is located on a PCB. The good thermal conductivity of the copper structures within the interposer (i.e., top and bottom metal layers and the through-silicon-vias), in combination with the copper pillars underneath the dies, enable a high-performance and effective thermal behavior of the system; the heat produced by the processor and memory dies is dissipated through these elements to the PCB substrate that supports the system. However, in complex microelectronic systems that include arrays of different metal layers, TSVs, copper pillars, solder balls etc., their modeling and simulation can be an expensive procedure. This is especially a problem in early design phases where many different technologies options (e.g., packaging variants) have to be evaluated. Moreover, a real design exploration can be time consuming in many cases. In order to simplify the modeling procedure and speed up simulation, we present an alternative approach to derive simulation models from system descriptions, reduce the simulation time, and ensure the reliability of the obtained results. The array of copper pillars of the system is substituted with simplified blocks with the same volume and material properties. In terms of simulation, the meshing of cuboids and rectangular blocks is easier than meshing cylinders or spheres. The simulation time of the simplified model can be significantly reduced. First simplifications already result in 10-15% shorter simulation time (down to 2 mins reduction). The obtained numerical results are similar to the ones extracted prior to the aforementioned simplifications; the value deviation ranged between 1.5-3% for simulation cases up to 10 W applied power. However, the possible degree of simplification is strongly dependent on the application specific boundary conditions. As an example, for high-power applications; by further increasing the applied power, larger deviations can be observed (up to 7.8% for 25 W power, according to our simulation). Additionally, we propose an efficient solution in order to simulate the hot-spots inside the dies; they are performing complex and high-speed functions that result in heat concentration at specific points of the IC. Finally, another important parameter examined is the

influence of the thermal interface material (TIM) in the behavior of the system with respect to the heat dissipated through the system if a heat-sink is included in the model.

**KEY WORDS:** high-speed dies, interposer, heat-sink, thermal behavior, heat distribution, power dissipation, thermal interface materials, copper pillars, thermal conductivity

### NOMENCLATURE

T/ T <sub>max</sub>	Temperature/ maximum temperature
TSV	through-silicon via
FR-4	flame retardant
BGA	ball grid array
C4	controlled collapse chip connection bumps
PCB	printed circuit board
TIM	thermal interface material
ASIC	application-specific integrated circuit
IC	integrated circuit
MEMS	micro-electro-mechanical systems
CTE	coefficient of thermal expansion
SiP	system-in-package
Pb	lead
Si/SiO <sub>2</sub>	Silicon/silicon dioxide
Cu	copper
Sn	tin
Al	aluminum
Ag	silver
h <sub>c</sub>	convective heat transfer coefficient $(W/m^2*K)$
K	thermal conductivity (W/m*K)
Q	rate of heat transfer $(W/m^3)$
q	conductive heat-flux (W/m <sup>2</sup> )
$C_p$	heat capacity (J/kg*K)

#### **Greek symbols**

 $\rho$  mass density (kg/m<sup>3</sup>)

#### **INTRODUCTION**

The use of silicon interposers for the interconnection between of heterogeneous modules, based on the System-in-Package (SiP) technology, will play a dominant role in the integration of advanced microelectronic systems in the following decade. The performance of devices, such as smartphones and tablets consisting of processors, memories, sensors and RF elements, is increasing generation by generation. The demand of smaller and shorter interconnect paths between the different sub-elements of the system is one crucial aspect for their improved behavior and performance, and especially between the memory and the processor. In older configurations used, they were fabricated separately and subsequently mounted side by side on a substrate (e.g. PCB board). However, due to the demand of higher data rates, smaller dimensions, less noise, optimal thermal, electrical and mechanical performance of the system, the interposer configuration has been applied and widely implemented, based on advanced packaging solutions. The thermal aspects of the system are crucial and must be taken into consideration in early design steps. Additionally, the high-performance components and interconnects applied within the package are temperature dependent. In the current paper we focus on the thermal behavior of such architectures, on the effects and the temperatures that are present and we propose simplification methods in order to reduce the design and simulation time.

As an example we use an advanced SiP system that includes a memory die placed next to a processor, placed on a silicon interposer. The latter is used as an intermediate interconnect layer between the incorporated dies and the PCB board. We give here a brief description of what a die stands for, saying that they are basically integrated circuits that perform complex logic operations, such as field programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs), microprocessors, etc. Our system also includes a memory that is directly connected to the logic unit; via interconnect routes through the bulk of the silicon interposer. Such routed offer high-speed data acquisition and their storage in the memory. Finally, additional components such as e.g., micro-electro-mechanical systems (MEMS) may also be included in an advanced integrated system [1-7].

In systems where the dies are packed side-by-side on an interposer (2.5D architecture) or stacked on top of each other (3D architecture) through TSVs (through silicon vias), the amount of thermal and mechanical effects caused by heat dissipation is increasing; the reason is that the number of active devices is increased while the volume of the SiP is decreased. The thermal investigation in the design of such components is a crucial part where the various thermal issues can be discovered and solved prior to the fabrication of the end device. In this work we will explore the thermal constraints of a system containing a high-speed memory and a processor; furthermore we will suggest ideas and solutions to reduce the modeling and simulation time of the aforementioned system. Such simplifications concert the arrangement of the copper tracks of the interposer, the shape and the arrangement of the copper pillars found underneath the substrate of the dies and used to mount the memory and the processor on the copper tracks of the board [1-7].

An additional enhancement in the system for further heat reduction (caused by the ICs and the memories) is a heat-sink. It is an aluminum (in most cases) structure with pins of fins arranged in matrix which significantly reduces the heat dissipated through the interposer and the board, by leading it to follow the path of the lower thermal resistance: the path that includes the heat-sink. That leads to lower thermal stresses and temperature mismatches of the board, the interconnect tracks and bumps due to different thermal coefficient of expansion (CTE) of the involved materials of these elements. In systems and applications that dissipate high power the presence of a heat-sink is strongly recommended; otherwise due to this CTE-mismatch possible cracks, rupture areas and failure points may occur in the components of the system and especially in the interface where two of them interconnect (e.g. in the copper tracks where the microbumps are soldered). Finally, due to the surface roughness of the heat-sink base and the dies, a thermal interface material (TIM) is placed between them [1-8].

In this paper, we describe and examine a highly-integrated 2.5D microelectronics system. Figure 1 depicts a 2dimensional configuration that includes the interposer, an ASIC and a memory arranged side-by-side on this silicon interposer; this set-up leads to higher and shorter interconnection paths between the dies improving the routing of their signals. The aforementioned assembly is mounted on a PCB substrate. Furthermore, for optimal dissipation of the heat produced by the dies, a heat-sink with an attached TIM epoxy material is placed on top of them. The heat is produced by hotspots found inside the ICs; the transistors in the dies perform and execute complex functions, leading to higher concentration of the heat. Depending on the degree of complexity and the speed of execution, this heat can range between several watts, up to several tens of watts in some cases. As mentioned above, a big part of the heat is dissipated through the heat-sink; this minimizes the heat that is transferred through the interposer, copper pillars, microbumps and PCB of the assembly, reducing also the resulted temperature of these parts. Furthermore, the risk to have critical thermal stresses due to CTE-mismatch between these different components of the system is decreased; the risk of having possible cracks and failure in these features is almost eliminated [7].



Fig. 1 We demonstrate a high-performance 2.5D electronics system with a processor (ASIC) and memory die, mounted on a silicon interposer, found on a PCB substrate. Finally, for optimal heat dissipation, a heatsink is placed on top of the dies.

## **DESCRIPTION OF THE MODEL**

The following subchapter will give a detailed description of the aforementioned model, of the parameters that should be taken into account, the materials involved, and the different boundary conditions set. Figure 2 demonstrated the model with the aid of COMSOL Multiphysics ver. 5.1 software program.

The designed system incorporates the following features:

• The processor (ASIC) and memory **dies** placed on their substrates. An important point to investigate the thermal behavior of the model is to represent the various hotspots in the ICs; we divided their volume into 100 sub-blocks. Furthermore, for the substrates of the dies we modeled several layers of silicon dioxide mixed with copper; vias were also modeled between these layers offering interconnect routes between them.



- Fig. 2 The designed model of the 2.5D system is depicted by using the COMSOL Multiphysics ver. 5.1 simulation program.
  - For the mounting of the dies on the interposer, **copper pillars** with top and bottom metal pads underneath the substrates of the dies are also implemented. They are modeled as cylinders with a hemispherical tip. The first array of pads can be found between the substrate of the die and the copper pillars and the other array is found between the latter and the interposer.
  - Subsequently, a silicon interposer with TSVs through its volume is modeled. For its placement, an array of C4 solder bumps is implemented. Two copper layers are found in the top and bottom surface of the interposer. Finally, copper vias are designed through the bulk of the interposer; they offer interconnect routes between the two metal layers making the dies capable of communicating with each other.
  - A **substrate** where the interposer is mounted; it is a printed circuit board with **copper tracks** and **FR-4 body**. The former is used to route the signals and the latter is an insulating layer.
  - **Ball-grid array (BGA) solder balls** can be found underneath the FR4 part of the substrate board for possible mounting of the model on another substrate.
  - Finally, in order to reduce possible high temperatures in the system, a heat-sink with an attached **thermal interface material** (TIM) on the dies are used; the dissipated heat is directed towards the pins of the **heat-sink**. For our model, an array of 12x12 pins was designed.

The machine specs of the server used for the simulation are: Intel (R) Xeon (R) CPU @ 2.90 GHz (2 Processors), 256 GB RAM, running on Windows server 2008 R2 Enterprise (64-bit).

Figures 3, 4 and 5 demonstrate the different aforementioned components of the system.



Fig. 3 For better heat dissipation produced by the two dies, a heat-sink with the attached thermal interface material was incorporated in the system.



Fig. 4 We divided the two ICs in 10x10 sub-blocks that can be used as hot-spots inside the dies. They are responsible for the heat produced and dissipated in the system.



Fig. 5 Closer view at the sub-elements that serve as hot-spots in the simulated system. We assume that purple regions indicate the highest activity areas of the chip. Two different cases of produced heat are applied: 5 and 25 W overall power produced by the processor and memory dies.

#### System parameters

A first important parameter that affects the thermal behavior of the system is the over power (heat) that is dissipated through the two dies in the system. Processors (such as ASICs) are components of the system that perform numerous and complex logic functions; there are several parts of their volume where these commands are performed and they exhibit a concentration of dissipated power. In that case we talk about the hot-spots found inside the ICs. On the contrary, memories typically have a steadier thermal behavior. However, the overall system power consumption depends on the specific applications performed by the processor and its communication with the memory. For our simulation purposes, we assume an overall power consumption up to 25 W for the two dies; we wanted to take the maximum possible power values into considerations and examine how the system behaves under the worst case scenario [9].

A second important parameter affecting the thermal behavior of the system is the distance between processor and memory; in one hand, this distance should be minimized in order to have the shortest possible interconnect routes and the smallest possible volume; in that case we also minimize the losses in the signal transmission. On the other hand, if the distance between the dies is really small, this will lead to higher overall dissipated heat. In our model the selected distance is set to 1 cm. The selection is a good compromise based on the two aforementioned criteria, because further simulations with shorter distance between the dies (0.9 cm for example) exhibited a ~4.5% increase in the maximum temperature of the system.

#### Materials and dimensions of the components

Concerning the materials of the different components of the system and their dimensions, the following table sums up all the related information. All the components are modeled as blocks, apart from the vias and the body of the copper pillars that are modeled as cylinders and the various bumps that are modeled as spheres. The copper pillars, including the top and bottom metal pad layers, the various TSVs, the C4 and BGA solder bumps are arranged in arrays. More specifically, the vias of the dies substrate, the copper pillars and their pads are arranged in 10x10 arrays, the C4 bumps in a 26x12 array and finally, the BGA bumps in a 26x16 array. The vias of the interposer are arranged in a 35x18 array. Finally, the pins of the heat-sink were designed in a 12x12 array, with 144 overall pins used. The dimensions of the various components are given in length x width x height:

Table 1 Information about the various features of the design with respect to the materials used and the dimensions applied.

		Tip: 40 [µm] radius
Copper pillar pads	Al	3x3x0.05[mm]
		(height/pad)
Interposer: bulk	Si	18x8x0.1 [mm]
Interposer: metal	Cu	18x8x0.005 [mm]
layers		
C4 bumps	Solder	0.105 [mm]
	(60Sn/40Pb	radius
PCB substrate	Cu (tracks)	Each component has 5
	FR-4	[cm] length and 3 [cm]
	(insulation)	width. The copper block
		has 30 [µm] height and
		the FR-4 block has 300
		[µm] height
BGA bumps	Sn/Pb	0.5 [mm] radius
Heat-sink	Al	Base: 50x50x2.8 [mm]
		Pins: 1.2 [cm] height,
		1.5 [mm] diameter
TIM	Gel [8-11]	3x3x0.1 [mm]

#### **Boundary conditions**

As mentioned above, the hotspots (parts of the dies that perform complex functions) inside the dies are responsible for the heat that is produced and dissipated through the components of the system. For modeling and simulation purposes, 4-5 spots (sub-blocks) inside each die were selected to function as hotspots. Figure 5 depicts the selected hotspots for each die (colored in purple). We chose the 'heat transfer in solids' module of COMSOL Multiphysics. As heat transfer mechanism, the natural convection has been chosen, for our compact model. The convective heat transfer coefficient  $h_c$  given was set to 25 W/m<sup>2</sup>\*K. the rate of heat transfer Q for the system, stated in the 'boundary conditions' section of COMSOL Multiphysics is given by the following equation:  $Q=h_c*(T_{ext}-T)$  [12]. The ambient (external) temperature in our simulations was set to 20 °C.

Concerning this dissipated power, different values up to 25 W (overall power) are implemented and the temperature and heat distribution of the system is observed. The material properties of primary importance here are the density, thermal conductivity, and heat capacity. Their numerical values are given by the COMSOL Multiphysics library. We modified only the values for the SiO<sub>2</sub>/Cu substrate layers and Sn/Ag tips of the copper pillars. Concerning the TIM properties we added the information given by the manufacturers for the various TIM material used for each case [8-11]. Table 2 sums all the material properties used based on the material library of COMSOL [13]:

Table 2 Density, thermal conductivity, and heat capacity values for the different materials used during simulation of the 2.5D model.

Components	Materials	Dimensions				
Dies	Si	3x3x0.2 [mm]	Material	Density	Thermal	Heat
Die-substrates	SiO <sub>2</sub> /Cu	3x3x0.06 [mm] (height/layer)	used	[kg/m <sup>3</sup> ]	conductivity	capacity
Vias	Cu	40 [µm] height,				
		40 [um] radius	Si	2329	130	700
Conner nillars	Cu (body)	Body: 30 [um] height	$SiO_2$	2200	1.4	730
copper pinuis	Sn/Ag (tip)	40 [um] radius	Cu	8700	400	385
		- Lfr. J				

Ag Solder	10500 9000	429 50	235 150
(60Sn/40Pb)			
FR-4	1900	0.3	1369
Al	2700	238	900

Another issue taken into consideration is the thermal conductivity of the thermal interface materials in the x-y and z axis; it describes the capacity of the material to spread the dissipated heat through its bulk into the attached heat-sink. Several TIM manufacturers provide with different numerical values for several types of materials and also give the thermal conductivity in the x-y and z plane. In our simulations, three types of TIM were used with respect to their thermal conductivity: 1.7, 6 and 12 W/m\*K, based on the material properties given by the manufacturers; normal materials have their conductivity ranging between 0.5-2 W/m\*K. However, there are materials with improved dissipation capacity that exhibit thermal conductivity up to 12 W/m\*K [8-11].

Concerning the influence of the copper pillars, their cylindrical body and hemispherical tip is substituted by two cuboids of the same material and volume; we wanted to propose a simplification model that reduces the simulation time and provides with similar numerical results of the temperature.

#### SIMULATIONS AND RESULTS

This section collects the results obtained during the simulation of the described 2.5D system. The design and simulation of the system was performed with the COMSOL Multiphysics ver. 5.1 software tool. The simulations were based on the boundary conditions described in the corresponding sub-chapter and they focus on 4 main points: first, to investigate how the addition of a heat-sink reduced the heat dissipation and distribution in the designed model. Second, how does the TIM and its thermal conductivity k affect this distribution. Third, another important aspect is the influence of k in the x-y and z planes. Finally, we dedicated a part of our simulations to the shape of the copper pillars and especially to their degree of influence in the thermal behavior of the system and the simulation time.

Concerning the numerical equations solved by the software program, a very important one is already given in the 'boundary conditions' section; it defines the rate of heat transfer Q under the natural convection mechanism. Another important equation included is the Q=P/V equation that relates the rate of heat transfer Q with the total power P dissipated (given in W) divided by the overall volume V of the system (given in cubic meters). The latter is calculated based on the dimensions that we give for each component of the system and the former is given by the user; as selected power values, we have given 5 and 25 W for low-power and high-power applications respectively, as explained in previous section.

For the 'heat transfer in solids' module of the software, the Fourier's law of heat conduction equation is also solved:  $q=-k\nabla T$ , which shows that the conductive heat flux q (given in W/m<sup>2</sup>) is proportional to the temperature gradient calculated at each point of the system [14].

Concerning the mesh option and its parameter applied during the simulation of the model, a 'fine mesh' has been chosen for all cases; the maximum element size has been set to 4 mm and minimum element size to 0.5 mm respectively.

# Temperature distribution and maximum temperature prior to and after the incorporation of a heat-sink

The numerical values of the maximum temperature of the system, as well as the heat and temperature distribution in the different components are compared. We simulated the cases where the system functions under 5 and 25 W (overall power) produced by the processor and memory dies. Elevated temperatures have been observed inside the system; if a heat-sink is added the maximum temperature of the system exhibits a significant reduction. Further temperature decrease is observed for better thermal conductivity of the TIM.

Figure 6 demonstrates the temperature distribution of the system under 5 W of produced power without the heat-sink. The regions colored in yellow, undergo the maximum temperature, since they are closer to the hotspots of the dies. On the other hands the areas with red have lower temperature values. The maximum temperature of the system is approximately 130 degrees Celsius and it is found in the dies and their substrates. It is a logical outcome considering that the hot-spots are the sources of heat. The corners of the PCB board and the BGA solder balls exhibit the lowest temperature of the system (approx. 35-40 degrees). If we increase the power produced by the dies, the system shows extremely high temperatures that are unrealistic under the present boundary conditions.



Fig. 6 In the case where no heat-sink is attached in the model, 5 W of produced heat leads to a maximum temperature of 130 °C in the system.

Our following sets of simulation takes into consideration the heat-sink of the system; we investigate how much the temperature of the system and the various components changes with this addition. The same boundary conditions, as before, were applied and we will present the cases where 5W (the average conductive heat-flux is approximately  $6.95 \times 10^5$ W/m<sup>2</sup> through its bulk) and 25 W (with an average conductive heat-flux of  $3.47 \times 10^5$  W/m<sup>2</sup> average system heat flux in the volume of the model) overall power is produced by the dies. Figure 7 shows the temperature distribution and its maximum value in the simulated model; we can observe that by adding the heat-sink the maximum temperature sunk from 130  $^{\circ}\mathrm{C}$  down to 50.8  $^{\circ}\mathrm{C}.$ 



Fig. 7 If we add a heat-sink in our previous model, the produced heat is better distributed and dissipated through the direction of the sink; this leads to significant reduction of the system temperature.

## The influence of the heat conductivity of the thermal interface material in the thermal behavior of the system

In both aforementioned cases (with and without heat-sink) the thermal conductivity k of the TIM was set to 1.7 W/m\*K. We conducted further simulations with 5 and 25 W power produced by the dies. We also changed the thermal conductivity of the TIM material; it was set to 6 and 12 W/m\*K. Table 3 sums all the resulted values of the maximum temperature if the thermal conductivity is altered under 5 and 25 W:

Table 3 Numerical values of the maximum temperature of the simulated system if different power values are applied and dissipated through TIM materials with thermal conductivity of 1.7, 6 and 12 w/m\*K respectively.

Applied k	5 [W] applied	25 [W] applied
[w/m*K]	power	power
1.7	50.8 [°C]	174 [°C]
6	42.3 [°C]	131 [°C]
12	39.8 [°C]	129 [°C]

We can observe that by applying 5 W power in the system and adding heat-sink, the maximum temperature of the model is significantly decreased from 130 °C down to 50.8 °C, with k=1.7 w/m\*K., for example. For 25 W dissipated power, it is strongly recommended to use a TIM with thermal conductivity higher that 3-4 w/m\*K; a material with poor k exhibits a maximum T of approximately 174 °C which may destroy the incorporated electronic components.

In cases where the manufacturer of the TIM material provides with information about the x-y- and z plane thermal conductivity of the material, we can apply these numerical values in our simulations and see how the results differ with the previous cases. For ,Tgon<sup>TM</sup> 800' thermal interface material fabricated by 'Laird Technologies' company, ,...a

high thermal conductivity of 240 W/m\*K in the XY plane and 5 W/m\*K through the z-axis...' is referred in the company's Tgon<sup>TM</sup> 800 Series datasheet [11].

If we apply these specific values in our simulations we have an improvement of the thermal behavior of the system; the high in-plane thermal conductivity in the xy-axis improves the heat dissipation, leading to smaller  $T_{max}$  of the system. It was reduced by approximately 2% and 3% for 5 W and 25 W applied power respectively. The high k in the x and y direction means that the material is better able to dissipate the heat through the length and width of its bulk where its dimension are much higher than its height that is only a few micrometers.

#### A proposed simplified model to reduce the simulation time by reforming the copper pillars found underneath the dies

Another issue examined was the influence of the shape of the copper pillars that can be found underneath the dies and connect them to the interposer. The cylindrical body and the hemispherical tip of the pillars were substituted with two cuboids of the same volume and same material properties. First we wanted to investigate whether their shape affected the temperature distribution/maximum temperature of the system and second if the simulation/computation time was reduced.

Figure 8 shows this exact transformation. The body of the pillars is colored in red and its tip in orange. The blue rectangles represent the aluminum pads of the copper pillars. For 5 W dissipated power the maximum temperature differs by 1.5%. However, for 25 W this difference rises up to 7.8%. Furthermore, for both cases the simulation time was reduced by 1 and 1.5 minutes respectively, down to 13 and 15 minutes respectively for the total simulation time of the model. In that case we can propose the substitution of the copper pillars model with cuboids if the dissipated power is relatively low.



Fig. 8 We redesigned the shape of the copper pillars in order to investigate if and how this substitution influenced the simulation results and if it reduced the simulation and calculation time of our model.

#### **Summary & Conclusions**

In the current paper, we presented, modeled and simulated the thermal behavior of an advanced microelectronics system based on the 2.5D technology with silicon interposer. Its main components are the two ICs (the processor and memory dies). With such an interposer configuration high data-rates between the components can be achieved; they communicate with short interconnect routes that pass through the metal layers and the TSVs of the interposer.

With the aid of the COMSOL Multiphysics software program a complex and precise model of the aforementioned system was designed and simulated in order to investigate its thermal behavior. Different produced power values were applied, under the absence or presence of a heat-sink. For the first case, the system exhibited a maximum temperature of 130 degrees Celsius (for 5 W power); in the area inside the dies and their substrates. For high-power and high-speed application the use of a good heat-sink is strongly recommended. By incorporating a heat-sink in the system, the overall temperature of the model was reduced, with a maximum value of approximately 51 °C for a thermal interface material with average thermal conductivity. If such conductivity is used under 25 W power the system exceeds the region of allowed temperatures for the microelectronics; it reaches temperatures up to 180 °C which may damage and destroy the electronic components.

For that purpose, we simulated and investigated the influence of commercial TIM materials with better conductivity k (6 and 12 W/m\*K respectively) and also the case where different values of k are used for the x-y and z planes. In all aforementioned cases, we observed a reduction of temperature, meaning that the higher the k of the TIM, the better able is the material to dissipate the produced heat through the heat-sink that is attached with it. For example for 25 W power, a thermal conductivity of 1.7 K/W\*K would not be able to sufficiently dissipate the heat and could destroy the electronics. However, if a TIM with 6 or 12 W/m\*K k is used the system exhibits a maximum temperature of approx. 130 °C meaning that the electronics are capable of functioning without any issue. It is obvious that by using a TIM with excellent thermal conductivity, the system will exhibit a better thermal performance. However, the final selection of the material depends on the cost offered by each manufacturer, the budget for the intended product, the kind of application where it is meant to be used, and of course, if this application will be a high-power or a lower-power one. The purpose of our simulation sets under different k-values was to show how it influences the general thermal performance of the system under low and high applied power values; the final decision for the specific thermal material used depends on the research group or industrial department that intent to use it. For lowpower application it makes more sense to use a cheaper, wellknow and wide-used TIM.

Additionally, we proposed an efficient and simplified way to model and simulate the hot-spots inside the dies that are responsible for the produced heat due to the transistors that are concentrated on the active areas of the die. With such a simplified approach the design and simulation time can be further reduced.

One last parameter examined was the influence of the shape of the copper pillars where the dies are mounted. By reforming their shape we achieved similar resulted temperatures for lower power applications (up to 8-10 W) and we achieved a decreased simulation time down to approximately 2 minutes. In simulations with total run time of 15-20 minutes, a reduction of the simulation time by 1 or 2 minutes is not a significant improvement. However, if the proposed simplifications are applied on more accurate and complex microelectronic models derived by layout and design

tools (with expected simulation times up to several days), such a shape adaptation are reasonable.

#### Acknowledgments

This work has been funded within the project ESiMED under label 16M3201B by the German Ministry of Education and Research (BMBF = Bundesministerium für Bildung und Foschung). Furthermore, it was supported by the Fraunhofer Internal Program SmartTicket under Grant No. MAVO 828 440.

#### References

- Tu, K.N. (2011) Reliability challenges in 3D IC packaging technology. Microelectronics Reliability, 51 (3), 517–523.
- [2] Bayer, C. et al. (2012) Enabling system level simulation of 3d integrated systems. ECCOMAS.
- [3] Heinig, A. et al. (2014) Thermal analysis and optimization of 2.5D and 3D integrated systems with wide I/O memory. Springer.
- [4] Tan, S.C. et al. (2008) Wafer Level 3-D ICs Process Technology, Springer.
- [5] Bellenger, S. et al. (2014) Silicon interposers with integrated passive devices: Ultra-miniaturized solution using 2.5D packaging platform. Ipdia.
- [6] J. J. Park, M. Taya, ASME, pages 46-52, Vol. 128, March 2006, Design of Thermal Interface Material With High Thermal Conductivity and Measurement Apparatus, Center for Intelligent Materials and Systems, Department of Mechanical Engineering, University of Washington.
- [7] A. Heinig, D. Papaioannou, R. Fischbach, 'Thermal Considerations for Systems with High Speed Memories', to be published at the proceedings of the '20th European Microelectronics and Packaging Conference (EMPC)', Friedrichshafen, Germany, 2015
- [8] Thermal Interface Materials For Electronics Cooling Products & Custom Solutions Catalog, Parker Chomerics, p. 15, T635 THERM-A-GAP Gel http://vendor.parker.com/852568C80043FA7A/468ea5 de5ac341d385257d39005641c7/C118FE3366B55BA6 85256BD7004F6F0A/\$FILE/THERMALMP.pdf
- [9] Parker Chomerics, https://www.chomerics.com/products/thermal/thermal Gels/legacy/index.html
- [10] T-GLOBAL TECHNOLOGY CO., LTD, http://www.tglobalthermal.com/tg-x-ultra-soft-thermalconductive-pad.php
- [11] Laird Technologies, Tgon<sup>™</sup> 800 Series datasheet http://b7c114b8ac32968eb0a5-0034a95ea8a03cf459b9e4f7b28746f2.r86.cf3.rackcdn. com/home/brandworld/files/THR-DS-TGON-800%201109.pdf

- [12] COMSOL Multiphysics ver 5.1 'Free Convection in a Water Glass' example http://www.comsol.com/model/download/227291/mod els.heat.cold\_water\_glass.pdf
- [13] COMSOL Multiphysics ver 5.1 material library https://www.comsol.com/material-library
- [14] COMSOL Multiphysics Heat Transfer Module http://hpc.mtech.edu/comsol/pdf/Heat\_Transfer\_Modul e/HeatTransferModuleUsersGuide.pdf