INFLUENCE OF PARASITIC PLASMA WRAP-AROUND DURING ANTI-REFLECTIVE COATING DEPOSITION ON THE FORMATION OF AN ALUMINIUM BACK SURFACE FIELD

Karin Krauß, Fabian Fertig, Norbert Kohn, Michael Rauer, Robert Woehl and Stefan Rein
Fraunhofer Institute for Solar Energy Systems (ISE)
Heidenhofstrasse 2, 79110 Freiburg, Germany
Phone: +49 761 4588 5272, Fax: +49 761 4588 9250, Email: karin.krauss@ise.fraunhofer.de

ABSTRACT: In industrial screen-printed aluminium-back-surface-field (Al-BSF) silicon solar cells the standard process for passivating the front surface and optimising its optical properties is the plasma-enhanced chemical vapour deposition (PECVD) of a silicon nitride anti-reflective coating (SiN-ARC). During PECVD of the front side SiN-ARC in an inline, tray-based reactor, the process plasma can wrap-around to the rear side causing a parasitic SiN deposition. We found, that the thickness of this parasitic SiN layer is in the order of 10 to 30 % of the thickness of the front side SiN-ARC. A corresponding SiN layer is investigated concerning its impact on the saturation current density of the aluminium-doped p^+-region formed by two commercially available aluminium pastes. The SiN layer caused a significant decrease in thickness of the p^+-region while its saturation current density increased. This implies a loss in open circuit voltage, which is calculated on the basis of a solar cell model and demonstrated experimentally.
Keywords: Back Surface Field, Antireflection Coating, PECVD, Silicon solar cells

1 INTRODUCTION

Despite the development of numerous high efficiency solar cell concepts, the Al-BSF solar cell is still the most common solar cell concept in industrial production. One reason for the persistence of this solar cell concept compared to advanced solar cell concepts, such as the passivated emitter and rear cell (PERC) [1] and other approaches is the ongoing improvement of the back surface field enabled by the development of advanced aluminium pastes.

However, dielectric layers between the silicon surface and the screen-printed Al paste can detrimentally affect the formation of the highly Al-doped p^+-region of the back surface field which is formed by alloying of the interface between the Al paste and the silicon wafer during the contact firing process. A minor thickness of the p^+-region due to dielectric layers has already been reported in Ref. [2, 3].

In the production process of Al-BSF solar cells a silicon nitride (SiN) is deposited at the front side of the solar cell to passivate the surface and optimize its optical properties. The most commonly used technique for deposition of this anti-reflective coating (ARC) is the plasma-enhanced chemical vapour deposition (PECVD). In an inline, tray-based reactor the process plasma can wrap-around to the rear side causing a parasitic SiN deposition. Especially for reactors coating the wafers from below, a plasma wrap-around can be inevitable without additional covering of the upward facing rear side. If a plasma wrap-around occurs, an unintended parasitic SiN layer is deposited on the rear side during deposition of the front side ARC.

In this work, the impact of such parasitic dielectric layers on solar cell performance is investigated by depositing different SiN layers intentionally and unintentionally (by plasma wrap-around). As a model system, a homogeneous thin SiN layer on the rear side with a layer thickness corresponding to the parasitic layer deposited by plasma wrap-around during deposition of the front side ARC is examined with respect to its influence on the formation of the Al-BSF. The basic properties of the Al-BSF like thickness, sheet resistance and saturation current of the resulting highly Al-doped p^+-region are investigated for different surface conditions and two different commercially available, glass frit containing aluminium pastes. The loss in open circuit voltage, which is induced by this thin SiN layer at the rear silicon surface, is calculated from the results on the basis of a standard solar cell model and demonstrated experimentally on solar cell level.

2 CHARACTERISATION OF PLASMA WRAP-AROUND

2.1 Plasma wrap-around in the PECVD reactor

The PECVD tool used is an inline tray-based reactor; the wafers are transported in trays through the process chambers with the process plasma burning below the tray, see Fig. 1a.

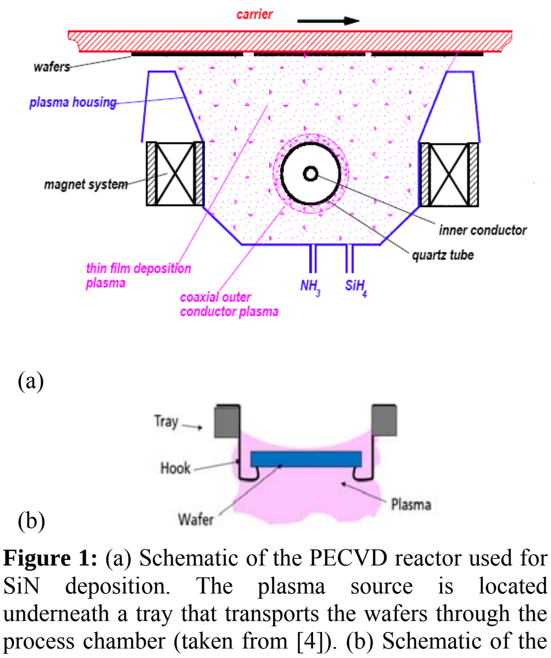


Figure 1: (a) Schematic of the PECVD reactor used for SiN deposition. The plasma source is located underneath a tray that transports the wafers through the process chamber (taken from [4]). (b) Schematic of the tray. The plasma can wrap-around all 4 edges of the wafer to the uncovered rear side of the wafer.

The wafer is placed on four hooks in the apertures of the tray, with its rear side facing upwards during the deposition of the ARC-SiN onto the front side. Fig. 1b shows schematically the plasma passing through the gap between the edge of the wafer and the edge of the aperture. This plasma wrap-around at all four wafer edges causes parasitic deposition at the rear side facing upwards which cannot be avoided without additional measures.

2.2 Sample preparation

In order to evaluate the lateral thickness profile of the parasitic layer at the wafers rear surface, wafers with front side ARC-SiN layers of varying thicknesses d_{ARC} were processed. After a standard-clean, the shiny-etched, pseudosquare float-zone (FZ) Si wafers (edge length 125 mm, diameter 150 mm) were processed in a PECVD reactor as described above. By varying the tray velocity the thickness of the ARC-SiN layer has been varied systematically in three steps with d_{ARC} = 75 nm, 135 nm and 230 nm. The parasitic layers deposited by the plasma wrap-around on the rear surface were measured via ellipsometry along a straight line rectangular to the wafer edges.

2.3 Results

The profile of the parasitic layer's thickness $d_{parasitic}$ at the rear side was found to decrease with increasing distance from the wafer edge, as shown in Fig. 2.

The thickness at the edge of the wafer is about 30 % of the thickness of the front side layer. After a steep decline within the first 20 mm from the edge of the wafer, the parasitic SiN layers for each deposition asymptotically converge towards about 10 % of the front side thickness, for all three depositions. For a front side layer with the standard thickness of d_{ARC} = 75 nm the plasma wrap-around leads to a parasitic SiN layer with a thickness of about $d_{parasitic}$ = 8-25 nm.

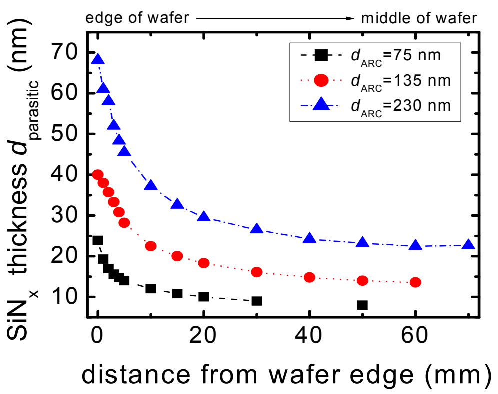


Figure 2: Thickness profile of the parasitic layer at the rear side determined by means of ellipsometry.

3 IMPACT OF THE PLASMA WRAP-AROUND ON THE Al-BSF QUALITY

To quantify the impact of a parasitic SiN layer on the formation of the Al-BSF on different surface morphologies, model stacks with and without homogeneous SiN layer at the interface between Al paste and silicon surface have been studied with respect to the alloying process for two different Al pastes.

3.1 Sample preparation

For the test samples 10 Ωcm p-type FZ-Si wafers with high bulk lifetimes have been used to ensure that the test structure is only limited by the Al-BSF in the end. The shiny-etched wafers have been prepared according the processing sequence shown in Fig. 3. While processing the rear surface of the samples, the front side is masked with a thermal oxide grown at the front side in the first step.

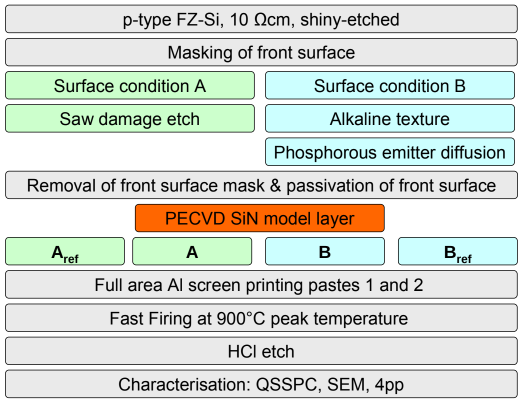


Figure 3: Process flow for the Al-BSF test samples, with two different surface morphologies and dopings at the rear side and with (surface conditions A and B) and without (surface conditions A_{ref} and B_{ref}) SiN model layer at the interface between Al paste and silicon surface.

To represent the rear side of high-efficiency cells, samples with planarised and emitter-free rear silicon surface (surface condition A) have been prepared using a saw damage etching process in KOH for 10 minutes. To represent the rear side of a standard Al-BSF solar cell, samples with a rear surface with alkaline texture and phosphorous n^+-emitter (surface condition B) have been prepared by an alkaline texturing and subsequent tube furnace diffusion with $POCl_3$. Afterwards the oxide mask at the front has been removed in HF solution and the front side has been coated with a passivating SiN layer.

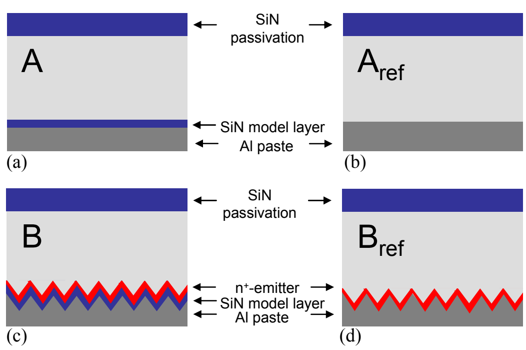


Figure 4: Test sample structure with (a) surface condition A, (b) A_{ref}, (c) B and (d) B_{ref} before alloying.

On half of the wafers from both surface conditions a 15 nm thick SiN layer is intentionally deposited onto the tear side via PECVD which models the parasitic SiN layer caused by plasma wrap-around. The other half of the wafers from both surface conditions was processed identically but without the intermediate SiN layer at the rear and thus reflects the undisturbed reference case. Finally, the rear side of all samples has been fully screen-printed using two different commercially available Al pastes, which led in total to an eight-fold process variation. The resulting sample structures for the two surface conditions are depicted in Fig. 4.

The formation of the Al-BSF is induced by alloying the samples in an industrial conveyor belt furnace at a peak temperature of 900 °C. After alloying, paste residuals and the eutectic Al/Si-layer are removed in hydrochlorid acid (HCl) to enable the characterisation of the p$^+$-surfaces.

In the next three subsections (i) the depth, (ii) the sheet resistance and (iii) the saturation current density of the Al-doped p$^+$-region is analysed for the eight different layer stacks under investigation.

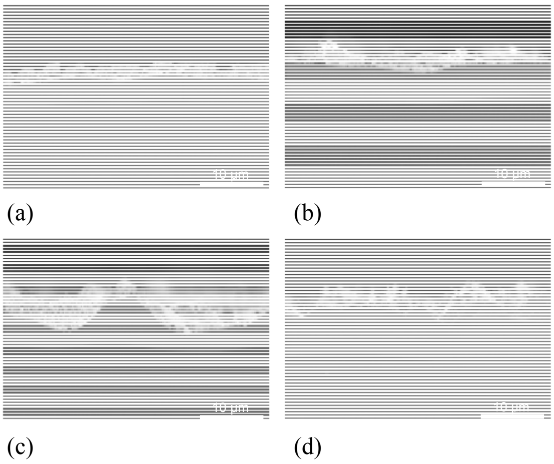


Figure 5: SEM-images of cross sections from samples with surface condition (a) A, (b) A_{ref}, (c) B and (d) B_{ref} for Al paste 1. Al-doped p$^+$-region can be distinguished from Si bulk by the contrast in brightness.

3.2 Impact on the thickness of the p$^+$-region

In order to determine the thicknesses of the p$^+$-region, images of cross sections of the samples were taken by scanning electron microscopy (SEM).

The p$^+$-region shown in the cross section of Fig. 5a has been formed by alloying through the SiN model layer on a planarised surface (surface condition A) which resulted in an average BSF thickness of d_{p+} = 3.3 µm. Fig. 5b shows the cross-section of the corresponding p$^+$-region

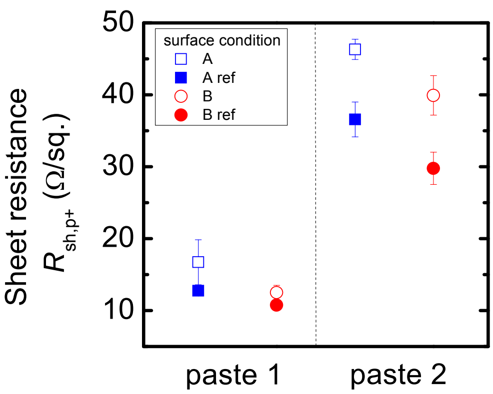


Figure 6: Measured sheet resistance of the highly Al-doped p$^+$-region for surface condition A (blue squares) and B (red circles) with/without intermediate SiN layer (open/solid symbols) for both pastes. Shown are average values of nine measured points on one sample with standard deviation.

formed by the same Al paste which has been screen-printed on the bare silicon rear surface which led to an average BSF thickness of d_{p+} = 5.4 µm. Hence, the intermediate 15 nm thick SiN model layer reduces the thickness of the p$^+$-region on average by 2 µm for paste 1. The p$^+$-region shown in Fig. 5c has been formed by alloying through the SiN model layer on a textured surface with residual emitter (surface condition B). The p$^+$-region is less thick and less homogeneously formed in comparison to the p$^+$-region for samples without SiN model layer (surface condition B_{ref}), shown in Fig 5d.

3.3 Impact on the sheet resistance of the p$^+$-region

The sheet resistance of the highly Al-doped p$^+$-region is characterised by four point-probe (4pp) measurements. The results for the two evaluated Al pastes vary significantly, as can be seen in Fig. 6. Paste 1 yields lower sheet resistances than paste 2. However, the surface condition has only little impact on the sheet resistance of the p$^+$-region formed by paste 1. The presence of an intermediate SiN layer affects the homogeneity of the p$^+$-region's thickness resulting in higher deviations of the $R_{sh,p+}$. For paste 2 the sheet resistance of the p$^+$-region increases significantly by about 10 Ω/sq for both surface conditions if an intermediate SiN layer is present. Furthermore, a trend towards lower sheet resistances for samples with textured surfaces (surface condition B) is observed for the p$^+$-regions formed by paste 2. One reason is a thicker p$^+$-region for samples with surface condition B and second possible reason could be an enhanced solution of silicon into the Al/Si-phase during alloying due to the texture-induced enlargement of the interface.

3.4 Impact on the saturation current density

The saturation current densities $J_{0,bsf}$ of the p$^+$-regions shown in Fig. 7 are extracted from quasi-steady state photoconductance (QSSPC) measurements according to a procedure described in Refs. [5-7]. The results show a significant difference in the Al-BSF quality achieved with the two evaluated Al pastes, paste 1 being better than paste 2. Apart from the differences between the Al pastes, the presence of an intermediate SiN layer has a deteriorating impact on the Al-BSF quality for both pastes. The saturation current density $J_{0,bsf}$ of the

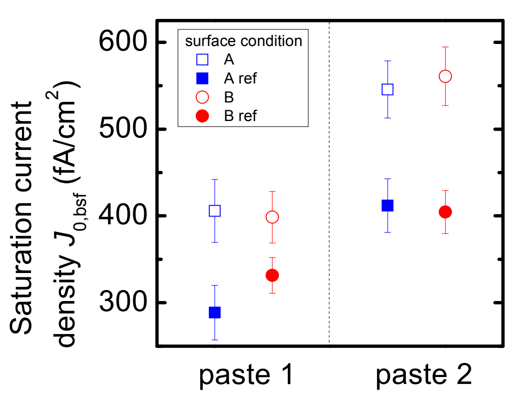


Figure 7: Results for the arithmetic means of the saturation current density $J_{0,\mathrm{bsf}}$ of the Al-doped p^+-region shown for the same variations as in Fig. 6. Shown are average values of three samples with standard deviation.

p^+-region increases from 332 to 398 fA/cm^2 for paste 1 and from 400 to 560 fA/cm^2 for paste 2, respectively, on a textured rear silicon surface with a residual n^+-emitter, as can be seen in Fig. 7.

It can be seen that the increase in $J_{0,\mathrm{bsf}}$ due to the SiN layer is in the same order of magnitude, or even slightly higher than the $J_{0,\mathrm{bsf}}$ difference induced by the choice of the paste. As expected from Ref. [8], the influence of the surface morphology or the presence of an n^+-emitter before alloying is low.

4 LOSS IN OPEN CIRCUIT VOLTAGE

4.1 Modeling of the open circuit voltage

To assess the impact of the differences in $J_{0,\mathrm{bsf}}$ on cell performance, a standard Cz-silicon solar cell is modelled. To determine the bulk diffusion length L, the bulk lifetime is calculated considering Auger-recombination [9] and SRH-recombination caused by the well-known boron oxygen complex [9]. Both effects depend on the bulk resistivity. The effective diffusion length L_{eff} is influenced by the bulk diffusion length L and the rear surface recombination velocity S_{rear}. With the saturation current density $J_{0,\mathrm{bsf}}$ determined in the previous section the surface recombination velocity

$$S_{\mathrm{rear}} = J_{0,\mathrm{bsf}} \frac{N_\mathrm{A}}{q n_\mathrm{i}^2} \quad (1)$$

can be calculated with the doping concentration N_A corresponding to the base resistivity ρ_b in question. Note that S_{rear} is proportional to N_A. The effective diffusion length is given by the following expression [10]

$$L_{\mathrm{eff}} = L_\mathrm{n} \cdot \frac{1 + \frac{L_\mathrm{n} S_{\mathrm{rear}}}{D_\mathrm{n}} \tanh\left(\frac{W}{L_\mathrm{n}}\right)}{\frac{L_\mathrm{n} S_{\mathrm{rear}}}{D_\mathrm{n}} + \tanh\left(\frac{W}{L_\mathrm{n}}\right)} \quad (2)$$

with the device thickness W and the minority carrier diffusion constant D. The base dark saturation current density $J_{0\mathrm{b}}$ is determined via

$$J_{0\mathrm{b}} = \frac{q n_\mathrm{i}^2 D_\mathrm{n}}{N_\mathrm{A} L_{\mathrm{eff}}}, \quad (3)$$

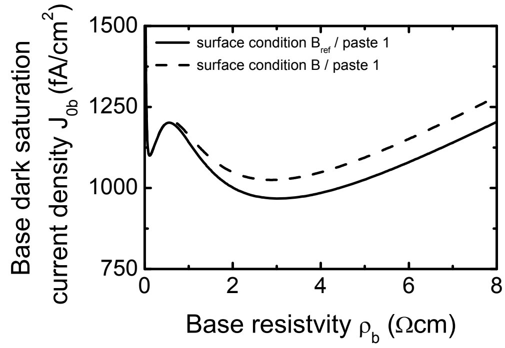
as described in [10]. Since an increase of surface recombination velocity S_{rear} leads to lower effective bulk diffusion lengths L_{eff}, the base dark saturation current density $J_{0\mathrm{b}}$ increases.

A constant emitter saturation current density of $J_{0\mathrm{e}} = 360$ fA/cm^2 is assumed for an industrial front side emitter including higher recombinative areas under the front side metallisation [11] with a typical metallisation fraction of 7.5 %. Assuming a short circuit current density of $J_{\mathrm{sc}} = 35$ mA/cm^2 as well, the one-diode model leads to the following expression

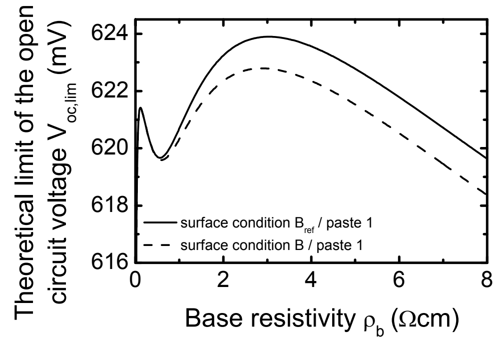
$$V_{\mathrm{oc,lim}} = \frac{kT}{q} \ln\left(\frac{J_{\mathrm{sc}}}{J_{0\mathrm{b}} + J_{0\mathrm{e}}} + 1\right) \quad (4)$$

for the upper limit of the open circuit voltage of an Al-BSF solar cell. The difference $\Delta V_{\mathrm{oc,lim}}$ between $V_{\mathrm{oc,lim}}$ curves for a modelled cell with and without intermediate SiN layer between Al paste and silicon surface reflects the possible loss in open circuit voltage due to a parasitic SiN layer on the rear side from plasma wrap-around.

For a textured rear surface with residual emitter and paste 1, the results for $J_{0\mathrm{b}}$ and $V_{\mathrm{oc,lim}}$ are depicted in Fig. 8a and b. In the process of calculating J_{ob} higher recombinative areas of the solar cells rear side under the soldering pads were considered as well. The previously determined increase of about $\Delta J_{0,\mathrm{bsf}} = 66$ fA/cm^2 in the saturation current density of the Al-BSF due to a intermediate SiN layer, for a textured rear surface with residual n^+-emitter and paste 1 results in a higher base dark saturation current density. Since the dark saturation current density from the base is proportional to $1/N_\mathrm{A}$ and furthermore the recombination velocity S_{rear} at the solar cells rear and the bulk diffusion length L depend on the base resistivity, $J_{0\mathrm{b}}$ depends on the base resistivity as well. For low base resistivity the bulk diffusion length dominates, whereas for increasing base resistivity the surface recombination velocity S_{rear} becomes more important and the progression of the curves splits. A loss in open circuit voltage up to 1 mV due to an intermediate SiN layer can predicted using the one diode model with an assumed short circuit current density $J_{\mathrm{sc}} = 35$ mA/cm^2. For Al paste 2, which formed an inferior Al-BSF with and without intermediate SiN layer compared to paste 1, the calculation of the voltage loss has been conducted analogous and lead to a difference of about 2.2 mV in $V_{\mathrm{oc,lim}}$.



(a)



(b)

Figure 8: (a) Base dark saturation current density $J_{0\mathrm{b}}$ for base resistivities up to $\rho_\mathrm{b} = 8$ Ωcm for a cell without (solid lines) and with intermediate SiN layer (dashed lines) (b) Corresponding $V_{\mathrm{oc,lim}}$ for $J_{\mathrm{sc}} = 35$ mA/cm^2.

4.2 Solar cells

In order to verify the model predictions for the loss in open circuit voltage experimentally, standard Al-BSF solar cells have been processed using paste 1 for the rear side metallisation.

In order to validate if the homogeneous 15 nm thick SiN layer represents the parasitic SiN layer deposited by plasma wrap-around sufficiently well, one Al-BSF solar cell, each with and without a parasitic SiN layer as well as with an intentionally deposited homogeneous 15 nm thick SiN layer on the rear, have been processed. For these solar cells FZ-Si wafers with a base resistivity $\rho_b = 1\ \Omega$cm have been used, eliminating influences of distributed material qualities. Table I shows the results for the IV-parameters of these cells. It can be seen that the open circuit voltage $V_{oc} = 627.3$ mV of the solar cell without intermediate SiN layer exceeds the open circuit voltage for cells with the homogeneous 15 nm thick SiN layer as well as the parasitic layer. Since the open circuit voltage $V_{oc} = 625.8$ mV of the cells with homogeneous layer and parasitic layer match, the homogeneous 15 nm thick SiN layer represents the parasitic SiN layer well.

Table I: Results for solar cells with and without parasitic SiN deposition on the rear side during the deposition of the ARC. A FZ-Si solar cell with an intentionally deposited SiN layer on the rear was processed as well.

		V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)
FZ-Si cell without SiN layer		627.3	36.64	77.7	17.86
FZ-Si cell with 15 nm SiN layer		625.8	36.45	77.9	17.77
FZ-Si cell with parasitic SiN layer		625.8	36.36	78.0	17.75
Cz-Si cells with parasitic SiN layer	**Average (21 cells)**	618.2 ± 1.0	35.69 ± 0.11	78.2 ± 0.3	17.24 ± 0.07
	Best cell	617.1	35.67	79.0	17.37
Cz -Si cells without SiN layer	**Average (6 cells)**	619.4 ± 0.6	35.71 ± 0.05	78.0 ± 0.2	17.25 ± 0.06
	Best cell	619.2	35.78	78.2	17.32

To enhance the statistical significance of these results on cell level, solar cells from Cz silicon with a base resistivity $\rho_b \approx 1.3\ \Omega$cm have been processed as well. The results for the IV-parameters are listed in Table I as well. With an open circuit voltage $V_{oc} = 618.2$ mV the loss in open circuit voltage for cells with parasitic SiN layer is about $\Delta V_{oc} = 1.2$ mV compared to the open circuit voltage $V_{oc} = 619.4$ mV of cells without a SiN layer. For the best cells with and without SiN layer, the difference in open circuit voltage is $\Delta V_{oc} = 1.9$ mV and thus slightly higher as expected from the theoretical determination of the open circuit voltage. Therefore a significant difference in the open circuit voltage due to a parasitic SiN layer is observed. However, since short circuit density and the fill factor of the solar cells vary statistically, the systematic loss in open circuit voltage has no systematic impact on the average solar cell efficiencies.

5 SUMMARY

The parasitic SiN layer deposited by plasma wrap-around in an inline tray-based PECVD reactor depositing bottom-up was examined via ellipsometry measurements. Its thickness on the edge of the wafers' rear side was found to exhibit about 30 % of the deposited front side ARC thickness and about 10 % in the middle of the wafer. According to this thickness, a 15 nm thick SiN layer between the silicon surface and the Al paste was examined on its influence on the Al-BSF quality. We have shown that this thin dielectric layer reduces the average thickness of the formed Al-doped p^+-region by 2 µm for a planarised surface and further detrimentally affects the homogeneity of the p^+-regions thickness, especially for textured surfaces.

The saturation current density of the Al-BSF increased by 20 % for Al paste 1 and 40 % for Al paste 2, respectively on a textured rear surface with residual emitter. Based on the one-diode model, the V_{oc} loss due to this $J_{0,bsf}$ increase is calculated to 1-2 mV for two different Al pastes in a standard Al-BSF solar cell.

The two evaluated Al pastes showed a significant difference in quality of the formed Al-BSF whether there is an intermediate SiN layer between the silicon surface and the Al paste or not. The impact of the SiN layer on cell performance in consequence of an inferior Al-BSF however is in the same order as the difference between the two Al pastes.

Since solar cells with an intentionally deposited homogeneous SiN layer and a parasitic SiN layer, deposited by plasma wrap-around, reached equal open circuit voltages, the assumption, that the 15 nm thick SiN layer is suitable to simulate the parasitic SiN layer, holds. A loss of $\Delta V_{oc} = 1.2$ mV in open circuit voltage due to a parasitic layer deposited by plasma wrap-around was experimentally observed on Cz-Si solar cell level for paste 1.

Considering these results, the choice of the aluminium paste is crucial to decide whether a plasma wrap-around during the deposition of the front side ARC in the course of the production of Al-BSF cells is acceptable or not.

ACKNOWLEDGMENTS

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