# SILICON NITRIDE - SILICON OXIDE STACKS FOR SOLAR CELL REAR SIDE PASSIVATION

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ABSTRACT: Plasma-enhanced chemical vapour deposited (PECVD) amorphous silicon nitride films (SiN<sub>x</sub>) are well known in the photovoltaic community for their good optical and electrical properties when being deposited as antireflection film on the solar cell's front and their low- temperature deposition process. The development of highefficiency solar cells brings up the need for passivating films for the solar cells' rear side when being contacted only pointwise (e.g. the passivated emitter and rear cell concept (PERC)). Compared to a thermally oxidised solar cell's rear side, silicon nitride already showed good but lower results in passivation and optical (reflection) quality in the past but it offers benefits in depositi on costs, process time and heat load for the s olar cells. In this work, a new surface passivating stack system consisting of a PECVD-silicon nitride and a PECVD-silicon oxide layer is presented that offers optical and electrical properties very close to those of therm al silicon dioxide without the drawback of heat load and with the benefit of using a quick and ch eap process at a low temperature (~350°C). By sintering lifetime evaluation samples with the new stack sy stem, the dependence of the thermal stability of the passivation on the thickness of the silicon oxide is shown. Furtherm ore, solar cells featuring this new stack system on their rear side are fabricated that show the expected optical and electrical benefits with a maximum solar cell efficiency of 19.3 %. Keywords: passivation, silicon nitride, PECVD.

### 1 INTRODUCTION

The major goal of research in crystalline silicon solar cell technology is to reduce the price per wattpeak. Therefore, new cell designs and new production processes have been developed in the past. Widely used in laboratories around the world is the high-efficiency PERC (passivated emitter and rear cell) concept [1]. Due to its relatively high production costs, this cell concept has not made the step into solar cell mass production. By the use of the Las er-Fired Contacts (LFC) approach [2], an economically feasible technology for mass production of the rear contacts of PERC cells has been introduced. Therefore, rear s ide surface passivation schemes need to be adapted to the LF C process. Furthermore, another possibility to reduce the cost per wattpeak is to lower the wafer thickness. This leads to an increased surface-to-bulk-ratio and to an even stronger interest in passivating both solar cell surfaces. In other words, the solar cell's rear side becomes more and more important

As thermally grown silicon dioxide (SiO  $_2$ ) layers are manufactured by a long-time energy -intensive high temperature process (~1000 °C) [3], [4], they are not the first choice for mass production, although they provide a very good and thermally stable passivation.

Plasma-enhanced chemical vapour deposited (PECVD) hydrogenated amorphous silicon nitride (a-SiN x:H; referred to as SiN x in the text) film s are fabricated by a low temperature processing step (~300-400 °C). They

also provide a very good passivation quality [5], [6] but are not as thermally stable as the SiO<sub>2</sub> layers [7]. As the nitrogen in SiN<sub>x</sub> layers is suspected to be im portant for the formation of fixed positive charges in the SiN<sub>x</sub> film [8], [9] which leads to an inversion lay er at the silicon surface [10], we used very silicon-rich SiN<sub>x</sub> films to reduce the ris k of a current los s while contacting the inversion layer and the p-Si bulk with LFCs. To our knowledge, no PECVD-silicon oxide  $(SiO_x)$  films have been developed so far that achieve good surface passivating qualities.

In this work, SiN  $_x$  films and SiN  $_x$ -SiO $_x$  stacks, all PECVD deposited, are inves tigated as a rear side passivation layer of LFC contacted solar cells.

# 2 SAMPLE PREPARATION

### 2.1 Carrier lifetime evaluation samples

In this work, sy mmetrical carrier lifetime evaluation samples, consisting of boron-doped float-zone (FZ) wafers with a resistivity of 1  $\Omega$  cm and a thickness of 250 µm have been used to investigate a novel surface passivation stack system. Starting with a surface cleaning procedure using a dry plasma etch process, a PECVD-a-SiN<sub>x</sub>:H layer was deposited followed by a PECVD-a-SiO<sub>x</sub> deposition. The SiO x deposition took place immediately after the S iN<sub>x</sub> deposition by only changing the process gases and electrical param eters. Next, the second side of the wafer was treated the same way.

The plasma etch s tep was performed using a microwave  $SF_6$  bias-free plasma in a reactor of S entech (SI). The  $SiN_x$  and  $SiO_x$  layers were deposited in a direct PECVD reactor of Surface Technology Systems (STS). To create the S  $iN_x$  layer, a gas mixture consisting of silane (SiH<sub>4</sub>), nitrogen (N<sub>2</sub>) and hy drogen (H<sub>2</sub>), for the formation of the SiO<sub>x</sub> film a gas mixture of nitrous oxide (N<sub>2</sub>O) and hydrogen (H<sub>2</sub>) was used.

The silicon nitride used was very Si-rich (n > 2,9), which is quite close to amorphous silicon but still silicon nitride.

The plasma etch step and the  $SiN_x$  deposition always have been the same process. The  $SiO_x$  deposition process was varied only in the deposition time (in the range of 15s to 1m in). In this way , the oxide thickness was changed. As the silicon oxi de deposition took only very little time and its deposition can take place in the sam e reactor as the S  $iN_x$  deposition, the cost impact can be assumed to be small.

To characterise the as-deposited surface passivation quality, quasi steady state carrier lifetim e was measured by use of a WCT-100 lifetime tester [11]. Sintering trials in a quartz tube furnace at 425 °C in forming gas ambience for 15 min each including the ramping up time which leads to assumed 5 min at 425 °C were performed with a measurement of the carrier lifetim e after each sintering step. See Table I for a quick overview of the rundown of the processing and Fig. 1 for the scheme of the carrier lifetime evaluation samples.

**Table I:** Process sequence lifetime samples.





Fig. 1: Carrier lifetime evaluation sample structure.

### 2.2 Solar cells

To show the potential of the new surface passivation scheme for photovoltaic energy conversion, solar cells of  $3.85 \text{ cm}^2$  were produced using boron-doped  $1\Omega$  cm floatzone (FZ) wafers with a thickness of 250  $\mu$ m.

The solar cells' front features a high efficiency RP-PERC structure with therm al SiO<sub>2</sub>-passivated emitter, photolithographically defined front contacts and random-pyramid front surface. The solar cells' rear side has been cleaned by the same plasma etch step and the same SiN<sub>x</sub>-SiO<sub>x</sub> stack system was deposited as on the lifetime samples. Cells without SiO<sub>x</sub> or with a SiO<sub>x</sub> thickness of 100 nm were produced and a slight variation of the SiN<sub>x</sub> deposition parameters was carried out.



**Fig. 2:** Random pyramid passivated emitter and rear cell (RP-PERC) with rear side stack passivation system (p-Si/SiN<sub>x</sub>/SiO<sub>x</sub>/Al) and laser-fired rear contacts (LFC).

As reference sam ples, solar cells with rear side passivation layers of thermal silicon dioxide (SiO<sub>2</sub>) were manufactured. Next, the  $SiO_x$  respectively the  $SiO_2$  layer was covered with a 2  $\mu$ m aluminium film by electron beam evaporation. In the following step, laser-fired contacts processing (LFC) was applied [2] to create rear side point and line contacts. Finally , the front contacts were electroplated. After measuring current-voltage (I-V) and internal quantum efficiency (IQE) (including reflection), annealing of the solar cells was performed at 425°C in forming gas for 25 min. Afterwards a second measurement was done.

Table II: Process sequence solar cells.

Solar cell's front side creation					
Plasma etch surface cleaning of rear side					
$SiN_x$ -SiO <sub>x</sub> stack deposition on rear side					
r					
Al deposition on rear side					
Laser-fired contact formation rear side					
Electroplating front contacts					
I-V/ IQE/ reflection measurement					
	1.				
Annealing					
I-V/ IQE/ reflection measurement					



Fig. 3: Carrier lifetime evaluation sample results.

## 3 RESULTS AND DISCUSSION

3.1 Carrier lifetime evaluation samples

The as-deposited carrier lifetim es of all lifetim e evaluation samples showed a very high range of about 1100  $\mu$ s to 1300  $\mu$ s, independently of the thickness of the silicon oxide lay er; see Fig. 3. For the performed incremental sintering the results can be split into two phases and two groups of samples.

Phase no. 1 includes the first 5min of the sintering procedure; phase no. 2 is made up of the following sintering steps. In phase no. 1, the sintering shows a slightly positive effect on the lifetime of the samples with an oxide thickness of 100 nm and 200 nm; the samples with lower thickness almost did not vary.

In phase no. 2 (after the next sintering step (accumulated 10 min)) the samples with silicon oxides of a thickness of 50 nm and without any oxide showed a strong decrease in carrier lifetime. Only about half of the lifetime of the previously measured value could be reached (1250  $\mu s \rightarrow 550 \mu s$ ; 1100  $\mu s$ → 400 µs). Furthermore, these samples showed a continued decrease in lifetime with the sint ering time to around 100 µs. Phase no. 2 of the samples with 100 nm oxide (starting at a sintering time of 5 m in) is characterised by a steady decrease in lifetime that does not show the heavy drop between 5 min and 10 min like the samples with a lower oxide thickness. This steady decrease led to around 800 µs after 25 min of sintering.

Phase no. 1 of the samples with 200 nm of plasma silicon oxide is set to 0 m in to 10 min sintering time – in contrast to the other s amples – because of the measured rising of the carrier lifetime. After the lifetime peak, the lifetime is as well decreasing but on a much lower level than the other samples. This yields a lifetime after 25 min of sintering of 1200  $\mu$ s.

The measurement results lead to the conclusion that a plasma silicon oxide lay er of sufficient thickness on top of a surface passivating plasm a silicon nitride film is very beneficial for the therm al stability of the carrier lifetime. A SiO<sub>x</sub> thickness of 100 nm or 200 nm can be called sufficient. This depends on the subsequent production steps and their heat load on the wafer.

As a reason for the decrease in carrier lifetime that all samples showed can be assumed that significant parts of the - for the s urface passivation very beneficial -

hydrogen of the hydrogenated silicon nitride layer is lost as the sintering time is rising. Also Lauinger et al. [12] have found a strong negative influence of an annealing step on the passivating quality of single layer  $SiN_x$  films.

### 3.2 Solar cells

Solar cells (250  $\mu$ m, p-type, FZ, 1  $\Omega$  cm) with a highefficiency front (RP-PERC) were fabricated with different rear side passivation systems to compare the new passivation stack system to the single lay er passivation films of PECVD-SiN<sub>x</sub> and thermal SiO<sub>2</sub>. In order to give rise to the energy conversion efficiency, the rear side (non-Si) absorption should be low (therefore, the reflection should be high). In wavele ngth dependent reflection measurements the optical rear s ide behaviour can be seen in the range starting from ~1000 nm. Fig. 4 shows that the rear side reflection of the therm al SiO<sub>2</sub> reference and the SiN<sub>x</sub>-SiO<sub>x</sub> stack system are almost identical and on a high level whereas the single layer SiN<sub>x</sub> passivation film shows a significantly lower reflection. Looking at the internal quantum efficiency (IQE) plots in F ig. 4, thermal SiO<sub>2</sub> shows the best behaviour with the  $SiN_x$ -SiO<sub>x</sub> stack system being very close. This leads to the conclusion that not only the reflective but also the passivating properties of both passivation systems are of a quite com parable quality. In contrast, the SiN x layer cell shows a much lower highwavelength IQE. This fact can be explained with a lower passivation quality of the SiN<sub>x</sub> layer.



**Fig. 4:** Wavelength dependency of the internal quantum efficiency (IQE) and reflection (R) m easurement values of solar cells with different rear side passivation schemes. The optical influence of the rear s ide can be seen at wavelengths above 1000nm with a strongly increasing reflection. An increas ed rear side reflection is beneficial for the energy conversion efficiency because the potential light path through the silicon is doubled and therefore the likelihood of photon absorption is increased. The IQE at higher wavelengths (starting from ~800 nm) is an indicator for the passivation quality of the rear surface.

Taking a look at the solar cell parameter results (see Table III) shows that the surface passivation has a significant influence on the open circuit voltage (V  $_{OC}$ ) [4]. Consequently, the thermal SiO<sub>2</sub> solar cells show the best rear side passivation. Th is is consistent with the conclusion of Fig. 4. In cons istency with Fig. 3 are the ranges of V  $_{OC}$  of the single lay er SiN<sub>x</sub> and the s tack

system SiN<sub>x</sub>-SiO<sub>x</sub>.

The sintering step (425 °C) did not show a uniform result when looking at the SiN $_x$  solar cells: Sam ple 7.3 (*very* Si-rich SiN<sub>x</sub>) shows a decreas e in  $V_{OC}$  but an increase in fill factor (FF). This leads to the interpretation that the aluminium on top of the SiN $_x$  destroyed parts of the passivation effect by improving the Al contact to the silicon. The short circuit current  $(J_{SC})$  did not change significantly. On the other hand, Sample 10.3 (Si-rich SiN\_x) showed almost the opposite behaviour: increase in  $V_{OC}$ , decrease in  $J_{SC}$  and FF

Comparison of the two s tack systems with SiN<sub>x</sub> and SiO<sub>x</sub> (samples 6.4 and 10.4) shows the same behaviour for both samples: increase in V<sub>OC</sub>, J<sub>SC</sub> and decrease in FF leading to an increased energy conversion efficiency.

Looking at Fig. 3, the samples with 100 nm SiO  $_x$  show an increase in carrier lifetim e when being sintered for 5 min. This might be the same effect here with the solar cells. Therefore, V<sub>OC</sub> increased after the annealing step as well. Als o, J<sub>SC</sub> is dependent on the rear s urface passivation [4]. If the rear s urface passivation increases through annealing, the short circuit current can increase as well. The reason why J<sub>SC</sub> at sample 10.4 does not grow in that amount like at sample 6.4 might be that the silicon nitride used at sample 6.4 had a lower nitrogen content.

As Dauwe et al. have shown in [10] , a parasitic shunting can take place at the s olar cell's back if a high amount of fixed positive charges is located in the SiN film. This induces an invers ion layer within the silicon bulk (surface). The occurrence of the invers ion layer depends on the density of charges in the passivating layer. Mäckel et al. demons trated that the amount of nitrogen in the SiN<sub>x</sub> layer is correlated to the density of K<sup>+</sup> centres and therefore correlated to the fixed positive charge density [9]. This leads to the estimation that more current is lost in sample 10.4 because more fixed charges in its SiN<sub>x</sub> layer produce a more intense inversion lay er and therefore more current loss through shunting processes. A stronger energy conversion efficiency decrease is the consequence.

Sam-	SiN <sub>x</sub>	SiO <sub>x</sub>	Anneal	Voc	$\mathbf{J}_{\mathbf{SC}}$	FF	η
ple no.			after LFC				
		[nm]	425°C, forming gas	[mV]	[mA/ cm <sup>2</sup> ]	[%]	[%]
7.3	SiN <sub>x</sub> 4 (very Si-rich)	0	before	621	35,6	77,7	17,2
7.3	SiN <sub>x</sub> 4 (very Si-rich)	0	after	615	35,7	79,4	17,4
6.4	SiN <sub>x</sub> 3 (very Si-rich)	100	before	637	37,2	78,2	18,5
6.4	SiN <sub>x</sub> 3 (very Si-rich)	100	after	658	37,8	77,7	19,3
10.3	Si-rich	0	before	622	38,3	75,5	18,0
10.3	Si-rich	0	after	639	35,5	74,3	16,8
10.4	Si-rich	100	before	637	37,2	77,6	18,4
10.4	Si-rich	100	after	652	37,3	76,3	18,5
2.1	thermal Si	O <sub>2</sub>	before	664	38,7	77,9	20,0
2.1	thermal SiO <sub>2</sub>		after	673	39,1	78,2	20,6

### Table III: Best solar cell results.

#### 4 CONCLUSIONS

A new surface passivation stack system has been presented. It consists of two layers, both deposited by PECVD: First, a silicon nitride  $(SiN_x)$  and then a silicon oxide  $(SiO_x)$  layer is deposited. If the  $SiO_x$  layer has a sufficient thickness (~100 nm) a good thermal stability of the passivating effect could be shown.

The special applicability of the SiN  $_x$ -SiO $_x$  stack system for locally contacted solar cell rear sides has been demonstrated. Good solar cell results have been presented that were in the range of the thermally oxidised solar cell references (SiN  $_x$ -SiO $_x$ : 19,3 %, th. SiO  $_2$ : 20,6 %). IQE diagrams showed the potential of the new stack system.

The stack system has three m ajor benefits when compared to single layer  $SiN_x$  passivation films:

- 1. Improved rear side reflectance, therefore higher  $J_{SC}$ .
- 2. Protection of the  $SiN_x$  film from the Al layer,
- 3. High thermal stability,

moreover, compared to therm al  $SiO_2$ , the stack system has the advantage of a quick low-tem perature PECVD process and therefore should be well suited for the solar cell mass production.

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